A New Methodology for Concurrent Technology Development and Cell Library Optimization

Marko Chew, Sharad Saxena, Thomas F. Cobourn, P.K. Mozumder and Andrzej J. Strojwas
PDF Solutions, Inc., San Jose, CA 95110

Abstract

To minimize the time to market and cost of new sub 0.25um process technologies and products, PDF Solutions, Inc., has developed a new comprehensive approach based on the use of predictive simulation tools combined with highly efficient experimental design techniques and special test structures. This paper focuses on our approach for concurrent development of new technologies and optimization of cell libraries for these technologies. We present a software system called *Circuit Surfer* which performs this library optimization in a highly automated fashion and with guaranteed correctness in silicon. We demonstrate several examples of *Circuit Surfer* applications to cell library design to optimize such objective functions as performance, cell area or yield.

1. Introduction

With each new generation of technology and products, semiconductor manufacturing becomes more complex. The increase in IC functionality has been made possible by a continuous drive towards smaller feature sizes. This decrease in dimensions of semiconductor structures has given rise to a new set of problems as manufacturing sensitivity to critical design and processing parameters has risen dramatically. While IC manufacturing becomes more complex, market windows for new products are shrinking. Success in today's marketplace requires effective technology integration as dictated by consumer demand. Against the backdrop of changing market conditions, the overall design cycle time and yield ramp have become the key drivers for product profitability. Technology independent design methodology, popularized by Mead and Conway[14] and used ever since to address the growing complexity problem, no longer applies to deep submicron designs. Unfortunately, this failure is happening at a time when it is more crucial than ever to design products concurrently with new technology development and its transfer to high volume manufacturing

These changes require a redefinition of the interfaces between design, test and manufacturing. In the following section, we present a comprehensive view of the yield problem and a "holistic" yield improvement methodology specifically designed to overcome yield detractors in state-of-the-art technologies. While elimination of systematic and design/process matching issues is critical to yield ramp, and hence profitability, there exist organizational barriers that reinforce traditional approaches. One barrier present in virtually all companies, even vertically integrated manufacturers (IDMs), exists between the design and manufacturing groups. Hence, it is typically difficult to quantify the balance between performance and manufacturing yield. Moreover, it is difficult to know which in-line measurements affect performance and yield the most. Finally, discerning between the signatures of random and systematic problems is complex. Hence, it is often difficult to know where to focus yield improvement efforts. These traditional barriers slow the rate at which manufacturers can achieve economically acceptable yields for leading edge products.

2. Holistic Yield Improvement Methodology

To resolve these problems, PDF Solutions, Inc., has developed a holistic yield ramp methodology that leverages simulation and hypothesis-driven statistical analysis to overcome the barriers between traditional engineering groups. This approach uses a combination of yield and performance prediction as well as statistically based data analysis to isolate gaps where actual and predicted yields are inconsistent, thereby identifying a potential systematic yield loss mechanism. After isolating that mechanism, solutions are proposed and evaluated via simulation until an optimal engineering solution is found that maximizes yield while achieving performance targets.

Predicting defect limited yield is an indispensable capability during the yield learning phase, especially when multiple diverse yield loss mechanisms may be present such as random defects, pattern-dependent effects, within-die process variations and parametric process mis-centering. To help isolate the effects of individual root causes on final product yield, we have developed a methodology and a software system called *pdEx*, in which *limited-yield prediction* [1] is used to provide microscopic observability of physical failure mechanisms. Furthermore, we have demonstrated in a number of joint projects with our industrial partners, several successful applications of this methodology during technology or product development which allowed designers to anticipate certain types of yield loss and employ appropriate design and even test (in-line and sort) optimizations.

Another key component of our yield/performance improvement methodology is the employment of statistical device and process simulation (TCAD) to predict the distributions of electrical test values and SPICE parameters based on the distributions in the manufacturing equipment parameters. PDF Solutions has developed a new comprehensive approach based

on the use of predictive simulation tools combined with highly efficient experimental design techniques and special test structures. The predictive simulation is achieved via statistical calibration of state-of-the-art process and device simulation tools which allows for correct process integration decisions to be made. These calibrated models serve as a virtual fabrication line and, in conjunction with short flow and test structure experiments, reduce the development cycle by several months. This paper will describe a software system, called *pdFab*, which can be applied for process integration and transfer to volume manufacturing. This holistic approach is quite unique and has already been successfully applied to shorten the development cycle in several leading edge semiconductor companies.

The development of cell libraries for these advanced technologies presents an equally challenging problem. Typically, these libraries are characterized and optimized only after the technology is frozen. With the proven predictive capabilities of the statistically calibrated *pdFab* tool suite, it is possible to change this scenario to a concurrent development of technology and cell libraries. We will present a comprehensive device model creation kit based on *pdFab*, and a cell library optimization kit called *Circuit Surfer*. We will demonstrate practical examples of cell library design to optimize such objective functions as performance, cell area and yield.

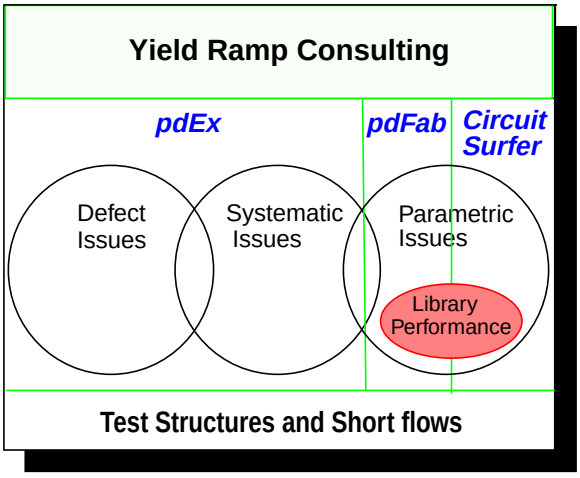


Figure 1: Holistic Yield Improvement™

Components that make up the Holistic Yield Improvement methodology are shown in Figure 1. Our methodology for limited-yield prediction and the *pdEx* tool suite have been described previously[1][2] and therefore, will not be presented here. Instead, this paper will focus on the use of *pdFab* for predictive statistical process and device simulation and *Circuit Surfer* for optimization of cell libraries. Section 3 describes our overall approach to statistical circuit design. Section 4 presents the *pdFab* system and Section 5 describes *Circuit Surfer*. Section 6 outlines the application of these tools for concurrent technology and library development. Section 7 presents several examples of applying *Circuit Surfer* for optimizing digital and analog cell libraries.

3. Statistical Design and Optimization

Manufacturing variations result in a distribution of circuit performances. Since state-of-the-art circuits are often designed very aggressively, statistical variations in performances can result in violations of specification limits, i.e., parametric yield loss. The goal of statistical design is to maximize parametric yield by making a circuit robust to random variations inherent in VLSI fabrication processes.

A common approach to robust design is to ensure that the circuit performances are acceptable under "worst case" conditions. These worst case conditions are derived by analyzing the model parameter values that would result in maximum deviation of each circuit performance from its nominal value. The process corner SPICE models are then generated by combining the worst case model parameters. There are at least two problems with this approach:

1. Unrealistic worst case conditions. Combining the worst case value of each model parameter does not capture the correlations between the SPICE model parameter values necessary to accurately reflect the manufacturing variations. Thus, designers simulate worst case corners that have a very low probability of occurring in a real fab.

2. Different worst case conditions for different circuit types. Typically, worst case SPICE models are developed once for a technology using a subset of circuits. Often these worst case models do not accurately reflect the worst case process variation for the entire family of circuits that will be designed for this technology. This is especially true for analog and mixed-signal designs where the worst case condition could be product specific.

In order to alleviate these problems a number of techniques for statistical design have been proposed[3][4][5][8]. These approaches estimate the complete distribution of circuit performances based on statistical SPICE models. Use of statistical SPICE models instead of the worst case models has two advantages:

1. Identification of realistic worst cases. Since the use of statistical SPICE models allows the estimation of complete circuit performance distributions, the worst case conditions can be circuit specific and are not overly pessimistic.

2. Optimization of statistical criteria. In addition to allowing realistic worst case conditions for performance optimization, statistical SPICE models allow the optimization of statistical criteria like variance and parametric yield.

The next two sections describe how we implement the statistical design methodology outlined in this section. The statistical TCAD framework implemented in *pdFab* results in statistical SPICE models that are used by *Circuit Surfer* for statistical circuit design.

4. *pdFab* Device Modeling Kit

An important part of concurrent technology and library optimization is the need to predict the device and interconnect behavior before the technology development is completed in the actual fabrication line. This necessitates a framework for predictive TCAD simulation that can generate statistical SPICE models based on process and layout changes. The simulation environment must have three properties: the ability to be calibrated to existing technologies, the ability to map process and layout variabilities into parameters and correlations of the SPICE models, and the ability to predict technology changes accurately based on prior calibrations. These changes are caused by technology fine-tuning or the development of technology derivatives.

The *pdFab* framework is such an environment for predictive statistical process and device simulation[10].

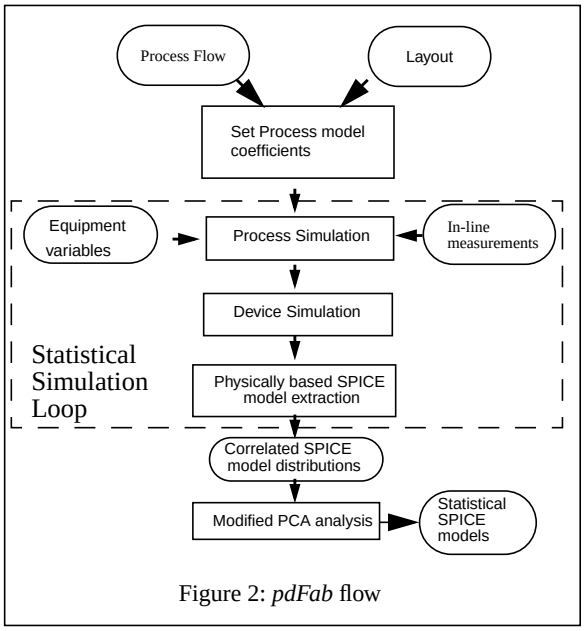


Figure 2: *pdFab* flow

pdFab takes as inputs process flow, device layout, and statistical variations associated with the process and equipment. Using this information, *pdFab* generates the physical wafer state (e.g., layer thicknesses and doping profiles), device performance parameters, and physically extracted SPICE model parameters.

For cell library optimization, the key requirement is a set of statistical SPICE models for all the device types in a given technology. For this purpose, a modified Principal Component Analysis (PCA) algorithm is used to create statistical BSIM3v3 SPICE models that can be used in *Circuit Surfer.* The algorithm identifies statistically independent "factors", thus determining the minimum number of basis vectors that can be used to describe the statistical SPICE model.

To assure the accurate prediction of the effects of process and layout changes on the SPICE models, we use commercial, two-dimensional process and device simulators backed by a robust in-house calibration methodology. *pdFab* can incorporate process and device simulators from multiple vendors, thus permitting best-of-breed application of simulators to suit the nuances of the particular technology to be modeled. *pdFab* can incorporate analytic and semi-empirical models as well. A unified "Chip Database" allows multiple simulators to input, update, and store simulation results in the database. The use of physically based models, coupled with a robust calibration methodology, allows for high confidence in predicting SPICE parameters for a technology under development.

The robust calibration methodology comprises two parts: a nominal calibration, preferably for multiple process splits, and a statistical calibration[11][12][13]. The nominal calibration is carried out with the statistical variations in the simulator set to zero. Ideally, multiple process splits (e.g., varying temperatures, doses, energies, etc.) and device splits (e.g., Lpoly, Tox, etc.) are used to constrain the tuning parameters to values that ensure accurate prediction. The calibration is decoupled into two parts: profile and layer thickness tuning, using process simulation; and device parameter tuning, such as V_t and entire I-V characteristics, using device simulation. Dopant profiles and in-line measurements, such as layer thicknesses and sheet resistances, are used to calibrate the wafer state. The calibration procedure is also decoupled by tuning progressively for transistors of different channel lengths, both in the saturation and linear regimes. The procedure starts by tuning the longest channel length where the transistor behavior is dominated by channel characteristics, and is not as affected by the LDD and halo implants (e.g., a 20 μm long device). Once the channel characteristics are determined, the calibration is performed for progressively shorter gate length devices. Sensitivity analysis is used to determine the effect of model coefficients on long and short channel physical and performance parameters to determine the order in which coefficients need to be manipulated for calibration. Capacitance-Voltage (CV) analysis, in conjunction with I-V's, are used to determine parameters relating to device simulation such as

poly-depletion, interface charge, polysilicon work function, etc. Once the desired nominal calibration is achieved, sensitivity analysis, together with measured data, is used to calibrate the variability associated with the process and equipment.

5. *Circuit Surfer* Cell Library Optimization Kit

Concurrent technology and cell library development requires that the cell library optimization procedure be fully automated. This is because market driven schedule pressures do not allow designers the luxury of manually resizing the cell library for every significant process change. The situation is further complicated due to the larger number of circuit simulation runs necessary to explore the statistical design space. Rather than running simulations for the typical, worst case and best case corner process conditions, the optimization loop must run many more simulations in order to generate statistically valid samples from the statistical model cards.

To address the issues of statistical cell library optimization, we developed *Circuit Surfer*, a software system that quantifies the effect of process variations on cell performances and automates the selection of cell transistor sizes to maximize yield and performance within product constraints. *Circuit Surfer* performs this task by applying design of experiment (DOE)[6] techniques to explore the interplay of transistor sizing with the fabrication process variations, and by providing an efficient response surface methodology (RSM) based method of evaluating the effects of transistor size changes on the performance statistics[3][4][5]. *Circuit Surfer* utilizes these RSM models for its multi-objective optimization algorithms which allow for the fully automatic sizing of the cell transistors. The optimization objectives include such metrics as propagation delay, dynamic maximum current, and setup time requirements.

Circuit Surfer accepts statistical SPICE model cards, the cell library netlist along with layout parasitics, and design specifications such as cell area and cell performance specifications (see Figure 3). In turn, *Circuit Surfer* automatically generates optimal device sizes which can then be sent to a layout compaction system to adjust the cell areas. This entire process can occur in batch mode without any user intervention. The internal *Circuit Surfer* flow is shown in Figure 4.

In addition to the set of new device sizes, *Circuit Surfer* can generate information about the sensitivities of cell performances to the process inputs. With this capability, it become straightforward to identify which cell performances will be affected by process changes. Further information about this capability will be discussed in Section 6.

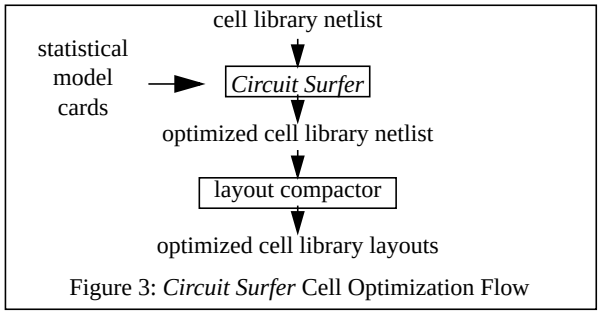


Figure 3: *Circuit Surfer* Cell Optimization Flow

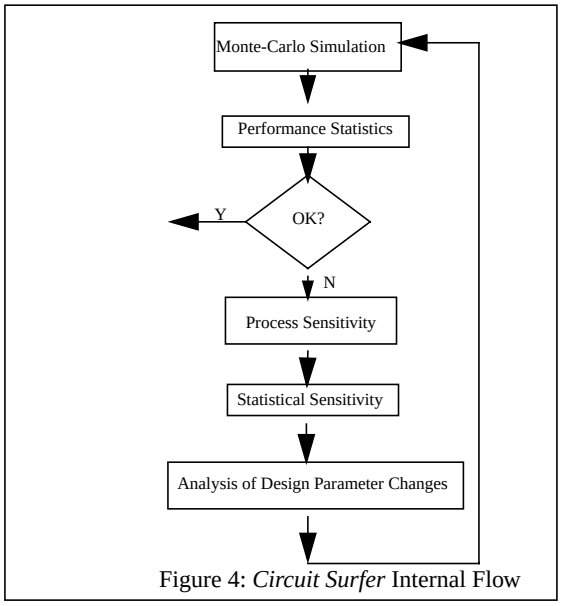


Figure 4: *Circuit Surfer* Internal Flow

5.1 Statistical Model Cards

Circuit Surfer requires access to statistical SPICE model cards which are different from the usual SPICE model cards in that some of the model parameters appear as functions of process factors. It is through these process factors that the SPICE model parameters maintain their correct correlations with each other. Figure 5 shows an example where K1 and TOX for a BSIM3v3 model track each other, and thus changing these model parameters independently is not correct. Typically, the number of process factors is much smaller than the number of model card parameters. For example, we have found that 7-10 process factors account for more than 90% of the variations in each of the approximately 60 BSIM3v3 model parameters.

5.2 Process Sensitivity

Circuit Surfer automatically performs all the operations required to generate the simulation data such as writing out the simulation files, running the circuit simulation, and collating the simulation results. The process sensitivity step generates information about the sensitivity of cell performances to the process factors. Figure 6 shows the Process Sensitivity information where the line graphs contain the sensitivity of performance values to changes in the process factor values.

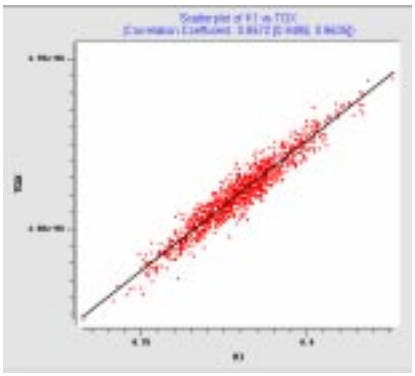


Figure 5: BSIM3v3 TOX vs. K1

The process sensitivity information can be used to reduce the number of process parameters which have to be considered in *Performance Statistical Sensitivity Analysis.* This is because the number of circuit simulation runs is directly proportional to the number of process factors. Another use for the process sensitivity information is to identify the cells that need to be re-optimized when a process factor changes.

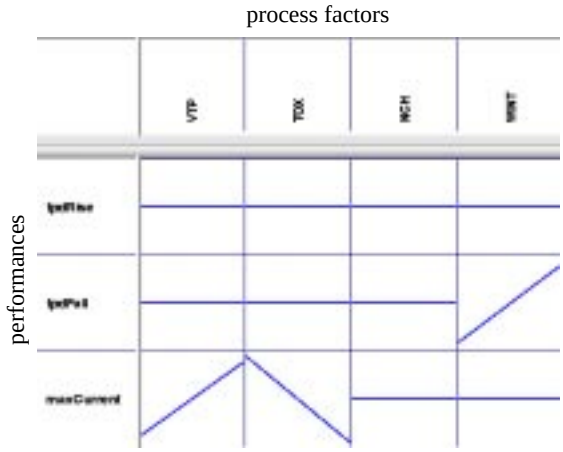


Figure 6: Process Sensitivity

5.3 Performance Statistical Sensitivity Analysis

In this step, simulation data for the sensitivities of the performance statistics to the changes in the design parameters is automatically generated and analyzed by *Circuit Surfer.* The simulation data generation algorithm uses the Taguchi approach[7]. This implementation bypasses the necessity of running the Monte Carlo simulation experiments at each unique setting of design values.

Associated with each performance are the sensitivities of the mean and variance to changes in cell transistor sizes (see Figure 7). This information can be used to identify the set of design parameters with the most significant impact on the performance statistics. The identification of these design parameters is especially difficult for designers to find manually due to the complex interaction of process variations and transistor sizings.

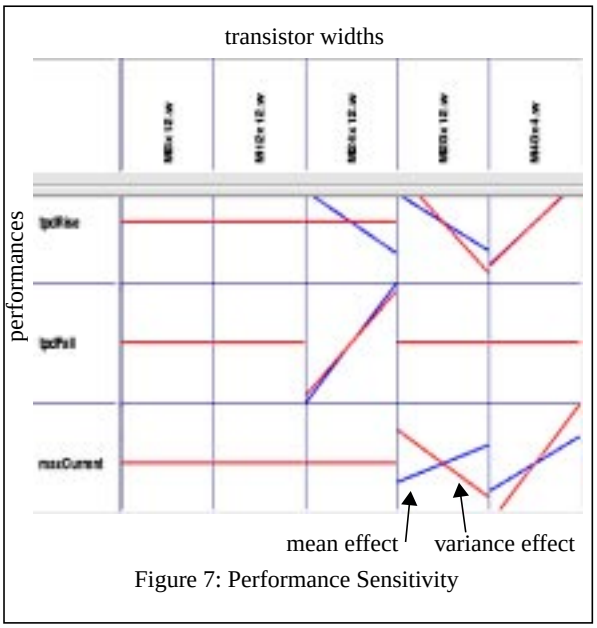


Figure 7: Performance Sensitivity

5.4 Exploration

During the exploration phase, RSM models of the various performances are generated and used within an optimization loop. The RSM models are used to evaluate the effects of different transistor sizes on the performance statistics. The straightforward approach of running Monte Carlo circuit simulation experiments to gauge the change in performance statistics is too computationally intensive to be practical.

The cost function for the optimization algorithm considers all the circuit performances in addition to other considerations such as the cell area and power consumption. Each circuit performance can be assigned a weight to reflect its relative importance. In addition, each performance can have low, high, or both limits, as well as target values, in order to influence the optimization algorithm.

6. Concurrent Technology and Library Development

A methodology for concurrent technology and cell library development should support two classes of changes in technology: (1) the development of technology derivatives like front-end and back-end shrinks, and (2) technology fine-tuning in the later stages of development and transfer to volume manufacturing.

Robust calibration of TCAD simulators and the *pdFab* framework allows for the prediction of the performance of technology derivatives and the generation of SPICE models to update cell-libraries in response to these changes. The impact of technology fine-tuning on the library optimization is minimized by developing a number of indicators that monitor the state of the tech-

nology and its impact on the cell performances. Ideally, these indicators are associated with the in-line and E-test data, as it is not possible to directly measure the SPICE model parameters via electrical test. Moreover, the SPICE parameters are often strongly correlated, making it difficult to relate the SPICE model parameters to the performance objectives for the cells. To alleviate these problems, a principal component analysis (PCA) and pattern recognition is performed on the simulated distributions of the SPICE model parameters, E-tests, and in-lines to determine the following[13]:

- The E-test and in-lines that can be used to track the statistical SPICE parameters, and hence be the indicator of the changes in technology, and
- Nonlinear, empirical relationships from the E-tests and in-lines to the SPICE parameters and performance parameters of different cells.

This enhanced PCA algorithm has two advantages. First, it allows a simple E-test and in-line based tracking of the technology changes and their effects on the SPICE models. The E-tests and in-lines identified in the PCA analysis serve as technology monitors indicating the "vectors" along which the technology has significantly changed. Second, the nonlinear relationships to the cell objectives provide a method for determining if a technology iteration along a given vector affects the objective functions for a given cell. Only those technology changes that result in large changes in performance of the library cells would require re-characterization and re-optimization of the library cells. Moreover, only those cells for which the impact is significant would need to be updated.

7. Examples

Our cell optimization methodology allows optimization of both cell performance and yield. In addition, cells can be rapidly optimized for different applications by choosing application specific objectives and specification limits for the optimization. This section illustrates these capabilities via three examples. The first two examples are a NOR gate and a AND-OR multiplexer from a digital library, the third example is a simple operational transconductance amplifier, which represents a cell in an analog/mixed-signal library.

Table 1 shows the results of using *Circuit Surfer* to optimize the performance of a NOR gate. The use of realistic worst case conditions provided by the statistical SPICE models results in a 10% smaller area, while meeting the 100 psec rise and fall time specifications.

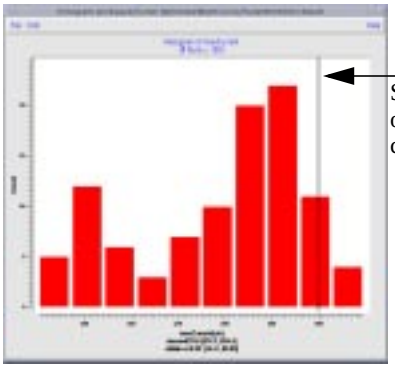
TABLE 1. NOR gate Optimization

	Traditional worst case	*Circuit Surfer*
Objective: Area	Ln,p = 0.25 µm Wn= 0.6 µm, Wp= 2.7 µm	Ln,p = 0.25µm Wn = 0.54 µm, Wp = 2.4 µm
Performance Constraints	< 100 psec rise and fall	< 100 psec rise and fall

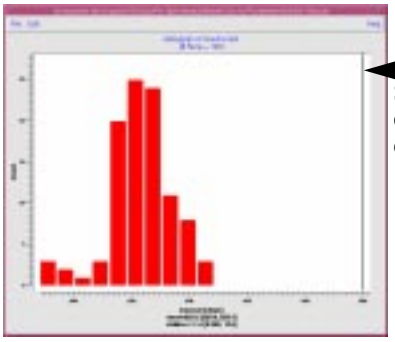
Table 2 compares the result of optimization using worst case corner SPICE models and the statistical optimization using *Circuit Surfer* for an AND-OR multiplexer. Figure 5 illustrates the use of *Circuit Surfer* to optimize statistical criteria: minimization of the standard deviation of maximum current and centering the design to be below the 300 µA spec.

TABLE 2. AND-OR Optimization

	Yield	Wn,p	Max Curr (avg)
Traditional worst case	96%	11.4 µm, 15.6 µm	279.5 µA
Circuit Surf. Optimized	100%	9.13 µm, 15.13 µm	223.5 µA



a) traditional worst case optimization



b) statistical optimization using *Circuit Surfer*

Figure 8: Variance Minimization

Figure 9 shows the schematic of an analog cell: an operational transconductance amplifier. Figure 10 shows

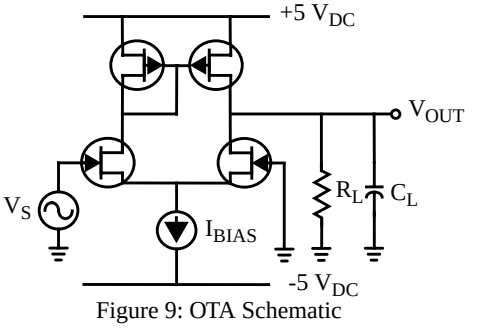
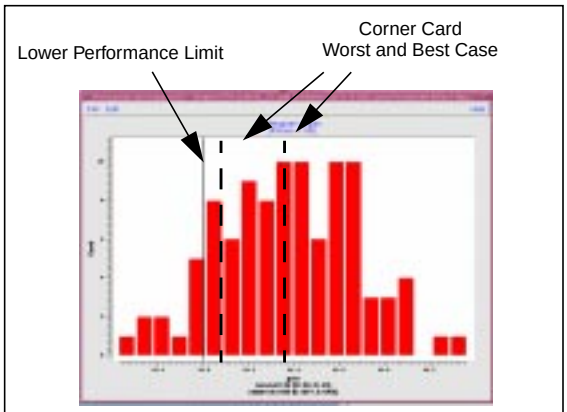


Figure 9: OTA Schematic

that the worst case SPICE models derived for digital circuits are inappropriate for analog designs and that the ability of *Circuit Surfer* to use statistical SPICE models to optimize yield.



A. Traditional Worst Case

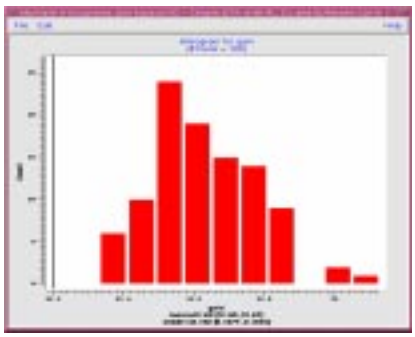

B. Optimized by *Circuit Surfer*

Figure 10: *Circuit Surfer* Optimization of OTA

8. Conclusions

Given the continuous increase in IC design and manufacturing complexity, and shrinking market windows, the overall design cycle time and yield ramp for new generations of technology and products have become the key drivers for profitability. In such an environment, the IP core and cell-library based approaches are indispensable. This paper presented a new and comprehensive approach to simultaneous development of new technologies and products. This approach enables the efficient re-use of the existing libraries, by optimizing them for a given technology even before the technology development is frozen.

We have demonstrated the feasibility of our approach by developing a highly automated library optimization system called *Circuit Surfer*. This system employs a comprehensive set of calibrated statistical process/device simulation models which serve as a virtual fabrication line. Thus, the *Circuit Surfer* statistically optimized cells maximize the utilization of technology capabilities. We have presented several examples of automatic cell optimization for multiple objectives such as performance, area or yield. We believe that this tightly coupled process-design methodology developed by PDF Solutions is absolutely necessary for high performance, low cost system-on-a-chip designs

9. References

[1] D. Ciplickas, A. J. Strojwas, X. Li, R. Vallishayee, W. Maly, “Advanced yield learning through predictive macro-yield modeling”, Proc. Seventh IEEE International Symposium on Semiconductor Manufacturing (ISSM), Oct. 1998.

[2] D. Ciplickas, et al., “Predictive yield modeling of reconfigureable memory circuits”, Proc. Ninth IEEE/SEMI Advanced Semiconductor Manufacturing Conference. 1998

[3] K.K. Low, S.W. Director, “An efficient methodology for the design centering of IC fabrication process”, IEEE Trans on Computer-aided Design”, vol10, pp.895-903,1991.

[4] M.A. Styblinski, J.C. Zhang, “Circuit performance variability reduction: Principles, problems, and practical solutions,” in IEEE ICCAD, Nov 1991, pp.170-173.

[5] P. Feldman and S. Director, “Improved methods for IC yield and quality and optimization using surface integrals,” IEEE ICCAD, 1991, pp.158-161.

[6] G. Box, N. Draper, “Empirical Model Building and Response Surfaces,” John Wiley and Sons, 1987.

[7] R. Roy, “A Primer on Taguchi Methods,”, Nostrand Reinhold, 1990.

[8] P. Cox el al., “Statistical Modeling for Efficient Parametric Yield Estimation of MOS VLSI Circuits”. IEEE Trans. on Electron Devices, vol ED-32, num 2, pp 471-478, Feb 1985

[9] A. Nardi et al. “Impact of unrealistic worst-case modeling on the performance of VLSI circuits in deep sub-micron CMOS technologies”, Third International Workshop on Statistical Metrology, IEEE, pp. 42-45, 1998.

[10] D.M.H Walker, J.K. Kibarian, C. S. Kellen and A.J. Strojwas, “A TCAD Framework for Development and Manufacturing”, Technology CAD Systems (proceedings of Workshop on Technology CAD Systems), Springer-Verlag, Vienna, 1993.

[11] D. A. Hanson, H. S. Chen, D.-B. Kao and J. K. Kibarian, “The use of Technology CAD in M2CMOS Process Development - Manufacturability and SPICE Model Prediction”, Third Statistical Metrology Workshop, Austin, TX, August, 1995.

[12] D. A. Hanson, H. S. Chen, D. B. Kao, J. K. Kibarian, and K. W. Michaels, “Analysis of the Controllability of a Sub-Micron CMOS Process Using TCAD”, pp.85-92, International Symposium on Semiconductor Manufacturing (ISSM), Tokyo, Japan, IEEE EDS / SEMI / UCS, June, 1994.

[13] D. A. Hanson, R. J. G. Goosens, M. Redford, J. McGinty, J. K. Kibarian, and K. W. Michaels, “Analysis of Mixed-Signal Manufacturability with Statistical Technology CAD (TCAD)”, IEEE Transactions on Semiconductor Manufacturing, pp477-488, Vol. 9, No. 4, Nov. 1996.

[14] C. Mead and L. Conway, “Introduction to VLSI Systems”, Addison-Wesley Publishing;,1979.