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Invited Paper

Recent Advances in Analog, Mixed-Signal, and RF Testing

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Due to the lack of widely applicable fault models, testing for analog, mixed-signal (AMS), and radio frequency (RF) circuits has been, and will continue to be, primarily based on checking their conformance to the specifications. However, with the higher level of integration and increased diversity of specifications for measurement, specification-based testing is becoming increasingly difficult and costly. As a result, design for testability (DfT), combined with automatic test stimuli generation, has gradually become a necessity to ensure test quality at an affordable cost. This paper provides an overview of cost-effective test techniques that either enhance circuit testability, or enable built-in self-test (BIST) for integrated AMS/RF frontends. In addition, we introduce several low-cost testing paradigms including the loopback testing, alternate testing, and digitally-assisted testing that offer the promise of significant test cost reduction with little or even no compromise in test quality. Moving forward, in addition to screening the defective parts, testing will play an increasingly important role in supporting other post-silicon quality assurance functions such as post-silicon validation, tuning, and in-field reliability of system chips.

1. Introduction

Advances in silicon technology have enabled the high-level integration of digital, analog and mixed-signal (AMS), and radio-frequency (RF) circuits into a single system-on-a-chip (SoC). In contrast to digital design that has been heavily assisted by a full spectrum of design automation tools from high-level synthesis to layout extraction, synthesis, verification, and analysis tools for supporting AMS/RF circuit design remain limited. In addition, due to the lack of widely acceptable fault models, to date, the final testing of AMS/RF circuits is still primarily based on explicit measurement of circuit performances to determine their

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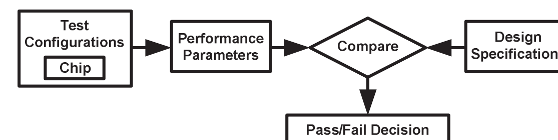

Fig. 1 Specification-based test strategy.

conformance to the specifications. This testing paradigm has been referred to as the *specification-based testing*, which is illustrated in **Fig. 1**. This is in contrast to the *structural testing* paradigm that is based on structural fault models and has been widely adopted for digital testing. Direct measurements for static and dynamic parameters of AMS and RF circuitry are usually very costly owing to the requirements of sophisticated test equipment and long test time. As a result, the design and test cost of AMS/RF circuitry often accounts for a significant portion of that for a mixed-signal SoC.

To address the test cost issue, researchers and engineers have long been searching for cheaper and more effective ways to measure circuit performances. For example, by utilizing signal processing techniques, in principle, one can test higher precision circuitry using a lower resolution/performance tester, which helps reduce the test cost. For data converters and RF transceivers, various techniques for effective and efficient measurement of linearity and error vector magnitude (EVM) have been developed. In Section 2, we will summarize recent advances in cost-effective techniques for specification-based testing.

One key challenge to testing highly integrated AMS/RF designs is the degraded accessibility of individual building blocks. The ability to control the inputs and to observe the outputs of each building block is necessary for thorough characterization and validation, as well as for minimizing test escapes. Potential solutions to enhancing the observability include the addition of simple on-chip measurement circuitry or sensors at internal nodes, whose outputs can be further processed and compressed by on-chip signature generation circuitry. The resulting compressed signatures can then be used for validation and test decisions. On the other hand, inserting on-chip test stimulus generators can improve the controllability of the circuit. The combination of test stimuli generation and response analysis/compression facilitates built-in self-test (BIST). Section 3

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provides an overview of various Design-for-Testability (DfT) techniques for integrated AMS/RF frontends.

The *loopback testing* is among the most popular test strategy for devices that incorporate both transmitters and receivers, or both digital-to-analog converters (DACs) and analog-to-digital converters (ADCs). This low-cost testing strategy incurs no or minor hardware overhead and alleviates the requirement of high-end AMS/RF testers. However, as the entire transceiver/converter-pair is tested as a single, end-to-end unit, the test quality might be compromised due to fault masking among interacting blocks. Section 4.1 reviews recent developments that aim at enhancing the capabilities of loopback testing.

The *alternate testing* is an emerging testing paradigm for AMS/RF circuits that has the potential to significantly reduce the test time and cost. Under this testing paradigm, the device under test's (DUT's) performance is *predicted* based on the DUT's signatures and pre-trained correlation functions, without direct measurement by test equipments. The DUT's signatures used for performance prediction are produced by on-chip signature generation circuitry in response to carefully crafted test stimuli. This signature-based testing approach, which does not require explicit measurement of the DUT's performances, significantly relaxes the test equipment requirements and shortens the test time while achieving the same quality goal of specification-based testing. The alternate testing has been successfully applied to several types of AMS/RF circuits and has also been extended for BIST and performance tuning. Section 4.2 summarizes the alternate testing approaches and their applications.

Leveraging the powerful computing capability offered by the digital circuitry, some modern AMS/RF designs incorporate a digital adaptation or calibration unit into the design to combat process, voltage, and temperature (PVT) variations. We have also seen some phase locked loop (PLL) designs becoming *digital intensive* —— with more digital building blocks replacing the analog ones [1]. These new design trends enable a new testing paradigm, called *digitally-assisted testing*. With minor DfT modifications to designs that follow such a design style, the digital adaptation or calibration unit can be reused for characterizing and testing AMS/RF circuitry. The idea and specific techniques of this digitally-assisted testing methodology will be described in Section 4.3.

Manufacturing testing is just one of several post-silicon quality assurance tasks for producing working chips. In addition to manufacturing defects, PVT variations under different operational conditions, random noise, interferences, and even design bugs could all add uncertainty and cause chip failures. Therefore, manufacturing testing can no longer be viewed as an isolated task solely for the purpose of identifying chips with manufacturing defects. Instead, we must take a broader view to ensure the *viability* of the chips, i.e., manufactured chips indeed working correctly in the face of the enormous complexity, parametric variations, environmental variations, and aging, in addition to manufacturing defects. Manufacturing testing must be part of a total post-silicon quality assurance solution and be jointly considered with other tasks such as post-silicon validation, characterization, debugging, adaptation, and even post-deployment resiliency. The test circuitry and the test solution must support, and be reused for, other quality-assurance functions and vice versa. In Section 5, we provide a synopsis of the recent activities aimed at enhancing the viability of system chips.

2. Effective Specification Testing Techniques

To date, for AMS/RF circuits, specification-based testing remains the most prevalent testing practices in the industry [2,3]. To facilitate the measurement of various circuit specifications, specification-based testing often requires multiple test configurations on the load board and incorporation of minor DfT modifications to the DUT. Because direct measurement of performance specifications often incurs long test time and requires expensive test equipment, research in this area has been primarily focused on shortening test time, minimizing test sets, or enabling the use of cheaper test equipment.

2.1 Specification Testing of Data Converters

The linearity of an ADC is usually tested using the histogram (i.e., code density) testing method [4,5], which records the frequency of each code appearance of a DUT, known as the *code frequency* or the *code density*, in response to an applied test stimulus. This code frequency is compared to a reference (i.e., golden) code frequency to derive the static performances of the ADC such as the gain, offset, differential non-linearity (DNL), and integral non-linearity (INL). Typically, a ramp or a sine-wave signal is used as the test stimulus. Three factors

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determine the quality of histogram testing: the clock timing precision, the data capture speed, and the test stimulus linearity [6]. The first factor is critical for testing high-speed ADCs and the latter two factors are important for testing high-resolution ADCs.

To achieve a sufficient resolution in the histogram-testing method, the source of the test stimulus must have greater linearity than that of the DUT. A general practice for testing an n-bit ADC is that the DAC producing the test stimuli should have a resolution of at least $(n+2)$ bits. As a result, high-precision ADCs demand a high-end tester that can generate stimuli of great precision. To alleviate the test generator's linearity requirement, Jin, et al. propose a stimulus error identification and removal (SEIR) algorithm for supporting the use of nonlinear input signals for testing high-resolution ADCs [7]. In addition, a method for eliminating the environmental non-stationary effects on the test results is described in Ref. 8). These two methods can be combined to enable the use of low-linearity test stimuli for testing high-precision ADCs. In essence, these methods separate the test stimulus' nonlinearity and the ADC's nonlinearity by capturing two sets of ADC outputs for further processing: one from the test stimulus, the other from a shifted-version of the test stimulus – with a constant voltage shift to the waveform. An improved SEIR algorithm that yields a smaller measurement error than that of Ref. 7) is proposed in Ref. 9). A similar algorithm that can handle test stimuli with pronounced nonlinearity is proposed in Ref. 10). It should be noted that the SEIR algorithm can be simplified and optimized if the ADC architecture is known [11].

Another approach to alleviating the linearity requirement is to use dynamic element matching (DEM) to produce a finer-resolution test stimulus. First described in Ref. 12), DEM is a technique to tolerate mismatch by dynamically reconfiguring the interconnections among a group of mismatched elements so as to shape or randomized mismatch errors. The DEM technique is usually used to improve the effective linearity of DACs. The application of DEM for testing ADCs was reported in Ref. 13) and its extension to BIST in Ref. 14). The application of DEM for testing DACs was reported in Ref. 15).

To gain sufficient resolution and accuracy, the histogram method demands for a large number of samples to filter out the effects caused by noise. The efficiency and noise sensitivity of the histogram method are analyzed in Refs. 16)–18). To enhance measurement accuracy, Jin, et al. propose to use Kalman filters, in combination with ramp [19] and sine-wave [20] stimuli. These approaches enhance the efficiency of histogram testing and reduce the test time required to achieve a given accuracy level.

By testing only a subset of the codes or analog voltage ranges, the test time and cost can be further reduced. This strategy requires the architecture knowledge of the data converter under test. Test solutions employing this strategy can be found in Refs. 21), 22) for successive approximation register (SAR) ADCs and in Refs. 22)–25) for pipelined ADCs.

In addition to linearity testing, the dynamic performance of an ADC, usually characterized by the effective number of bits (ENOB), is another critical specification for testing. The ENOB is usually tested by applying an AC input stimulus and performing fast Fourier transformation (FFT) on the output codes of the ADC-under-test. The spectrum information from the FFT reveals the fundamental tone of the applied test stimulus, as well as the noise and distortion due to the ADC's non-idealities. There is a strong correlation between an ADC's INL and ENOB. It has been shown that the INL can be estimated from the FFT spectrum [26,27], and the ENOB can be predicted based on histogram testing [28,29]. Another important ADC specification is the aperture jitter, which characterizes the random variation in time of the sampled instances caused by the variations in the sampling clock or the sampling circuitry itself. This specification is important for high-speed ADCs and its efficient test methods were reported in Refs. 30), 31).

Overviews on measurement issues and techniques for mixed-signal systems can be found in Refs. 32), 33), 193).

2.2 Efficient RF Testing Strategies

Most RF circuit performances are specified in the frequency and power domains [2], and RF measurement includes both scalar and vector tests [34]. Scalar tests incur measurements for only a numerical quantity such as the gain, attenuation, output power, linearity, etc. Vector tests, involving both magnitude and direction, are mostly characterized by a device's scattering parameters (s-parameters). Extensive explanations on how to measure these parameters for RF

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devices can be found in Refs. 35), 36).

RF circuits such as low noise amplifiers (LNAs), mixers, and power amplifiers (PAs) have now been integrated into a single-chip wireless SoC as a part of a transmitter, receiver, transceiver, or RF frontend. As a result, modern RF test strategies need to target some system-level specifications for the entire transmitter or receiver. The bit error rate (BER), symbol error rate (SER), and error vector magnitude (EVM) are among the most important system-level specifications-of-interest. In communication systems, the BER/SER is the ratio of the erroneous bit/symbol count to the total count of the received bits/symbols, in which a symbol could consist of multiple bits. An *error vector*, as illustrated in **Fig. 2**, is defined as the distance between the received symbol and the ideal symbol on the complex I-Q plane. The EVM is the magnitude of this error vector. EVM is an effective metric for screening defective devices because the location of the received symbol (and thus the EVM) is affected by the circuit non-idealities, gain/phase imbalance, and phase noise. It was pointed out in Ref. 37) that the root mean square (RMS) of the EVM is independent of the transmitted signals while the SER is sensitive to the data transmitted —— making the EVM a better test metric.

Several techniques have been developed to enhance the efficiency of EVM testing. The techniques proposed in Ref. 38) attempt to reduce the test data length by setting a better boundary for distinguishing passing and failing chips. However, a shorter test sequence will inevitably result in a larger error in EVM measurement and thus make the pass/fail decision less reliable. A more reliable method for test length reduction was proposed in Ref. 39) in which optimization of the test signals is achieved by choosing only those that would more likely exercise circuit impairments.

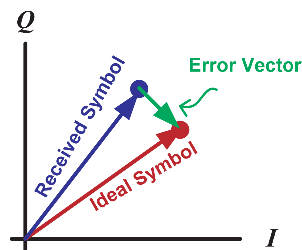

Fig. 2 Definition of error vector.

3. Test Solutions for Integrated Frontends

Several DfT techniques target to add internal access or self-testing capability to the integrated AMS/RF frontends. These techniques either directly measure the circuit performance on-chip or produce a signature that has strong correlation to the "health" of the circuit. To offer self-test capability, the BIST circuitry, which comprises a signal generator and a response analyzer (see **Fig. 3**), should be more robust than the DUT. In the following, we summarize recent developments of DfT and BIST techniques for data converters, PLLs, equalizers in high-speed serial links (HSSL), and RF transceivers. Interested readers could refer to Refs. 40)–44) for additional information on various AMS/RF DfT and BIST techniques.

3.1 DfT and BIST Techniques for Data Converters

A major focus of the DfT research efforts for ADCs is on providing an accurate, on-chip analog test stimulus. On-chip measurement of ADC's static performances is another subject of wide interest. For DACs, facilitating digitization of the analog output for digital response analysis is a main focus.

A straightforward method for generating ramp signals for ADC BIST is to charge a capacitor with a stable voltage-controlled source. The linearity of the generated ramp signal depends on the ability to provide a constant current. Because the current source is implemented using MOS transistors, its current varies with the voltage-dependent resistance of the transistors and, thus, the linearity of the ramp signal is questionable. To deliver ramp signals with a precise slope and great linearity, several analog precision techniques have been proposed. For example, the authors in Ref. 45) proposed to use a differential amplifier feedback to provide a relatively stable current source. Their post-layout simulation results show that the ramp generator can achieve a 15-bit linearity over a 1 V full-scale range. Furthermore, the author in Ref. 46) uses a cascode

Fig. 3 Conceptual diagram of BIST.

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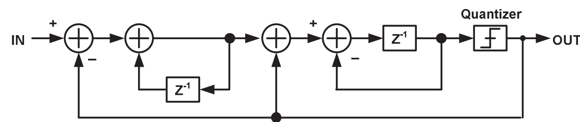

Fig. 4 Block diagram of a second-order SDM.

current mirror to provide a steady current and achieves a 15-bit INL over a 3 V full-scale range.

Calibration methods can also be employed for generating high-linearity ramp signals. The authors in Ref. 47) propose a discrete-time calibration scheme to calibrate the basic ramp generator. They demonstrated an 11-bit INL ramp generator over a 0.5 V full-scale range. The authors in Ref. 48) developed a triangular-wave generator that can test ADCs of 12 bits or fewer by combining two linear ramp generators and a feedback control circuit. The two linear ramp generators are calibrated with respect to a reference voltage using an analog calibration loop.

Another approach for analog stimulus generation involves the use of sigma-delta modulators (SDM). An SDM is often employed for generating high-precision signals from lower resolution devices based on a noise shaping principle – shifting the low-frequency noise to higher frequencies using the oversampling techniques. The sampling frequency of the SDM with respect to the bandwidth of the input signal, defined as the oversampling ratio (OSR), is typically greater than 100. The high-frequency noises appeared at the SDM output can be filtered out using a low-pass filter (LPF), resulting in a signal of great precision. **Figure 4** illustrates the block diagram of a second-order SDM. It involves several loops that estimate the signal values, compute the errors between the signal values and the reference values, and then integrate and compensate for those errors. Higher order SDMs achieve a greater signal-to-noise ratio (SNR) at the cost of a reduced dynamic range. An SDM can be implemented in the analog, mixed-mode, or digital domain. It can even be implemented in software.

A stimulus generator based on the SDM scheme, proposed in Ref. 49), is illustrated in **Fig. 5**. The desired stimulus waveform is converted into a single-bit modulation bit stream by a *software* sigma-delta modulator. This bit stream is then stored in on-chip memory. During testing, the bit stream is retrieved from

Fig. 5 SDM-based stimulus generator scheme [49].

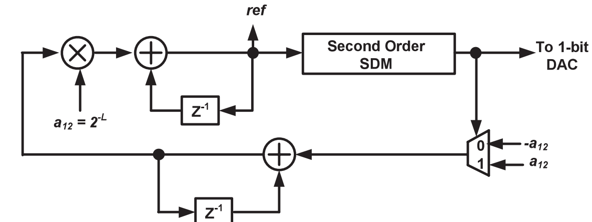

Fig. 6 SDM-based sinusoidal signal generator [57].

this pattern memory and iteratively applied to a one-bit DAC, followed by a LPF, to produce the desired waveform. The application of this stimulus generator to test an analog filter was successfully validated in silicon [50]. A major advantage of this stimulus generation scheme is that different test stimuli can be generated by simply changing the content in the pattern memory without any hardware modification. In addition, the accuracy requirement for the one-bit DAC and the analog filter is relatively low. However, the LPF may incur a non-trivial area overhead.

Instead of using a pattern memory, the author in Ref. 57) combines a digital resonator with an SDM to produce modulation bit streams to the DAC. As shown in **Fig. 6**, the digital resonator contains two cascaded discrete-time integrators that generate a sine-wave signal whose frequency can be adjusted by setting a_{12} and a_{21} to proper values. A major advantage of this generator is that, since the reference signal (*ref* in Fig. 6) is practically the digital version of the produced analog signal, it is readily available for use in on-chip histogram-based response analysis.

This SDM-based stimulus generator can generate accurate test signals fall within the LPF's pass-band. The quality of the generated stimulus depends on the LPF's ability to suppress the high-frequency noise. Another possibility is to increase the bit-width of the bit streams to produce test stimuli of higher

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quality. Each extra bit in the DAC increases the output SNR by approximately 6 dB [51]. However, the DAC's transfer function needs to be characterized as well in order to produce test stimuli with a desired level of quality. The authors in Ref. 52) measure the multi-bit DAC's transfer function using an external instrument. The digital bit stream is then pre-distorted based on the transfer function information to compensate for the DAC's nonlinearity. The authors in Ref. 51) propose an on-chip calibration scheme that measures the transfer function of the multi-bit DAC. Because external references are no longer required, this on-chip calibration scheme is suitable for BIST applications.

An ADC's test response can be analyzed either using an external tester or by on-chip resources such as a built-in DSP. The histogram-testing method has been implemented on-chip for BIST applications. A histogram-testing-based response analyzer records the number of occurrences of each code, called *code frequency*, which is then compared with a reference code frequency to compute the ADC's static performances such as the gain error, offset error, DNL, and INL. However, such an on-chip implementation is considered costly because the histogram data require a large storage area and the analysis demands non-trivial computation resources. In addition, its test time is long – it must accumulate sufficient data in order to achieve a satisfactory level of accuracy. As an example, to achieve a 0.05LSB resolution, it must accumulate at least 1/0.05LSB = 20 hits per code. For an n-bit ADC to store this amount of data on-chip, it would require at least 20×2^n n-bit word memory. Gathering such a huge amount of data and processing them to derive circuit performances would take an enormous amount of time too.

To reduce hardware requirements for on-chip response analyzer, the authors in Refs. 53), 54) derive equations to approximate the static performances based on the histogram-testing theory. Based on these equations, the ADC parameters can be sequentially calculated by sharing the hardware and computation resources, resulting in a reduced hardware overhead. Results of hardware validation and test time analysis of this approach [55] show that the test time is approximately 2^N times longer than that required for the histogram method for an N-bit ADC. On the other hand, the authors in Ref. 56) aim at reducing the test time of histogram testing by parallelizing the performance computation procedure. It was reported that a more than 100X speedup, in comparison with the results in Ref. 55), can be achieved at the cost of quadrupling the size of the DfT circuit.

These on-chip histogram-based methods require the information of a reference code frequency. The stimulus generator can be characterized to obtain the information about the number of hits on each code, which can then be used to compute the reference code frequency. Alternatively, the stimulus generator can be calibrated to have great linearity so as to guarantee the same number of hits for each code. The reference code frequency can then be easily derived. However, characterizing or calibrating stimulus generators either increases test time or costs extra overheads. A solution is to use an SDM-based sinusoidal signal generator [57] (mentioned earlier in Fig. 6) as the stimulus generator in which a reference signal is readily available.

Code width analysis has also been investigated as an alternative to histogram testing. For example, the authors in Ref. 58) analyze the code width information for detecting various static errors such as the missing code, monotonicity, and INL errors. In this method, a code width is measured using a counter, which indicates the cycle count between each code transition. The ADC codes at the current and previous counting cycles are compared to detect a code transition. The comparison result also indicates any non-monotonic code transitions at the ADC output. Furthermore, the authors in Ref. 45) use a bit-flip detector to detect code transitions. They also developed two BIST schemes based on code-width detection – one uses the on-chip DSP and the other uses the scan function to access test data for analysis. The code width information can be accumulated within a single pass of linear ramp and its accuracy is determined by number of hits per code of the ramp signal. The author in Ref. 45) concluded that, given the same amount of test time, the accuracy of the code-width test scheme is similar to that of the histogram methods. However, since code transition noise cannot be properly controlled, its accuracy is still limited.

Several response analysis techniques have been developed for testing DACs. The authors in Ref. 51) propose an SDM-based response analyzer that converts the DAC's analog output waveforms into digital sequences. As shown in **Fig. 7**, the response analyze consists of a single-bit sigma-delta encoder followed by a digital filter. The average of $x(t)$ in every window of D cycles is converted into a digital signal $y(n)$, where D is chosen based on the desired measurement accuracy.

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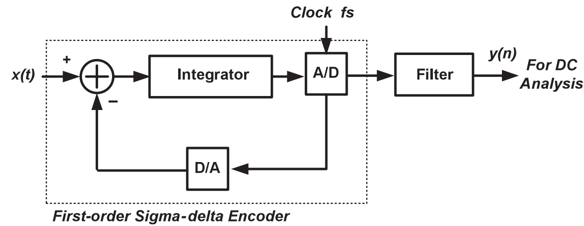

Fig. 7 First-order sigma-delta response analyzer for DAC testing [51].

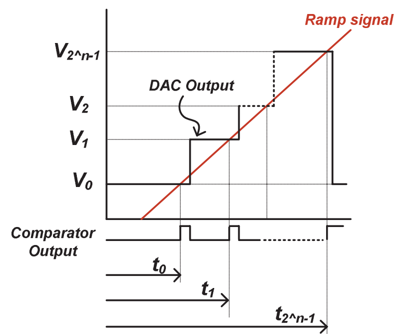

Fig. 8 Illustration of the DAC testing method in Ref. 59).

The sequence of $y(n)$ is then processed using the discrete Fourier transform to derive the AC characteristics of signal $x(t)$.

In Ref. 59), the DAC's output waveform is encoded into time-domain information by comparing the output of a DAC-under-test with a ramp signal. As shown in **Fig. 8**, a comparator is used to compare a ramp signal, which continuously increases in voltage, with the DAC output, whose voltage level is altered when its input digital code changes. During testing, the update to the DAC input code is controlled by a controller. The DAC's input is initially set to the all-zero code and the output voltage corresponding to this code is v_0. The comparator output would be set to 1 when the ramp signal becomes greater than v_0. The time period from initiation of the test procedure to the point that the comparator output is set is recorded as t_0. In addition, immediately after the comparator's output is set, the controller increments the digital code to the DAC's input by one. By repeating this procedure, the DAC's output waveform can be converted to a sequence of time-domain parameters $t_0, t_1, \ldots, t_{2^n-1}$. It is shown in Ref. 59) that the DAC's DNL and INL can be easily calculated based on this time-domain information.

The above-mentioned DfT techniques consider the entire data converter as a DUT without reconfiguring any internal signals of the DUT during testing. Some researchers suggested reconfiguring the DUT to alleviate the requirement of precise signal generation and response analysis. For example, the authors in Ref. 60) suggested adding additional feedback components to the ADC-under-test so that the resulting circuit oscillates. As most catastrophic faults or parametric variations in the DUT would cause deviations in its oscillation frequency and/or amplitude, which can be easily measured using pure digital circuitry, this method can detect faults autonomously in the oscillation mode. This method, called oscillation-based BIST (OBIST), has been successfully applied to test the operational amplifiers [61], analog filters [62], and micro-electro-mechanical systems (MEMS) [63]. In Ref. 64), the authors use regression analysis to build the correlations between the oscillation frequency and the analog circuit performances under various parametric variations. With these correlation models, the analog circuit performances can be predicted based on the measured oscillation frequency.

The test stimulus of OBIST is internally generated and, thus, it does not require a high-precision on-chip test generator. In addition, its test access is pure digital. Despite these advantages, few circuit types can be configured into oscillators, which is the main limitation of this method. Interested reader could refer to Ref. 65) for in-depth discussion on the oscillation test methods.

3.2 DfT and BIST Techniques for PLLs

The phase-locked loop (PLL) is a critical component for a number of applications including clock distribution, timing recovery, and frequency synthesis. As shown in **Fig. 9**, the basic elements in a PLL include a phase frequency detector (PFD), charge pumps (CHP), a loop filter, a voltage-controlled oscillator (VCO), and an optional divider (DIV). The key performance parameters for a PLL includes the output frequency, lock time, lock range, jitter, etc. Several BIST strategies and DfT techniques have been developed to facilitate catastrophic fault

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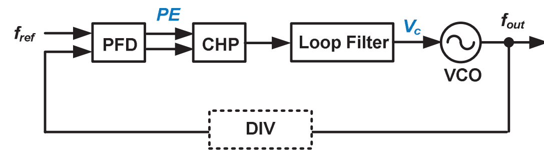

Fig. 9 A typical phase locked loop.

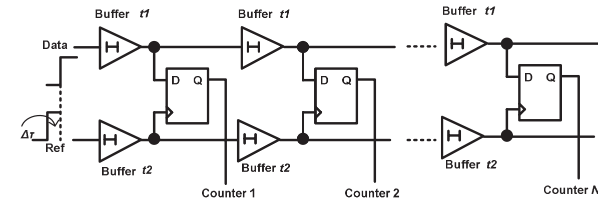

Fig. 10 Vernier delay line.

detection, key performance measurement, and jitter measurement.

A PLL can be tested by reconfiguring its circuit structure. Kim and Soma propose to break the feedback loop at the PLL's PFD output so that the existing charge pump can be used as a test stimulus generator and the VCO/DIV as a response analyzer for testing the PLL[66]. An all-digital DfT technique for detecting catastrophic faults in a PLL was proposed in Ref. 67). The VCO in their targeted PLL is a ring oscillator constructed from inverters.

As such reconfiguration-based approaches need to break the feedback loop during testing, they are not suitable for testing locking characteristics that are of most concerns for PLLs. To address this problem, the authors in Ref. 68) propose adding an extra delay at the PFD inputs so as to introduce an additional phase error to the loop. The PLL's output frequencies with and without this additional phase error are measured by recording the resulting value in the divider. Since defects in the PLL will result in frequency shift and, in turn, incorrect values in the divider, this method can successfully detect defective parts. The advantage of this method is that the PLL is tested as a whole system without breaking the feedback loop while maintaining the advantage that all test accesses are in the digital domain.

When a PLL is used as a clock generator, its timing accuracy affects the overall system performance. The uncertainty of a signal's transition edge, known as *jitter*, may result in intermittent delay faults and cause logic failures. Therefore, characterizing the jitter performance of a PLL is crucial for assuring the clock quality. Several dedicated jitter measurement schemes have been developed recently. Sunter and Roy propose to measure the RMS jitter using a self-calibrated delay line that can be synthesized using a standard digital design flow[69),70]. The reported results show that the jitter measurement resolution is limited to one-eighth of the delay of a logic gate, plus the jitter in the delay line that is technology- and layout-dependent. Since the delay line is fully synthesizable from an HDL following the digital design methodology, its speed and area scale with the technology. In addition, the measurement accuracy does not depend on the matching of the elements in the delay line. The authors in Ref. 71) propose modifications to the Sunter and Roy's method for an improved jitter measurement resolution. A voltage-controlled delay element that can be calibrated off-chip, is used in the delay line.

Another approach to measuring jitter in a data signal is to use two delay lines with slightly different delays, known as the Vernier delay line (VDL). As shown in **Fig. 10**, the VDL consists of two delay buffer lines and an N-bit counter constructed from a series of D flip-flops. For delay measurement, the number of 1's (or 0's) in the D flip-flops are counted. The delay of each buffer in the upper (lower) delay line is t_1 (t_2). t_2 is set to be slightly smaller than t_1 and their difference is denoted as Δt. A reference signal is applied to one of the delay line (the lower one in Fig. 10), while the jittery signal is applied to the other delay line (the upper one in Fig. 10). When signals propagate through these two delays lines, their phase difference will be decreased by Δt for each buffer stage. The exact stage when the phases of the two signals align can be identified by checking the digital content in the N-bit counter, from which the time difference between the two input transitions can be derived. With the ability to measure a time period between two transitions with a very high resolution, jitters in a jittery signal can be measured as long as a jitter-free reference signal is available. Based on this technique, a 30 ps jitter measurement resolution was demonstrated in Ref. 72). However, this method, whose resolution depends on the accuracy of the delay elements, incurs a non-trivial area overhead due to the need for a large

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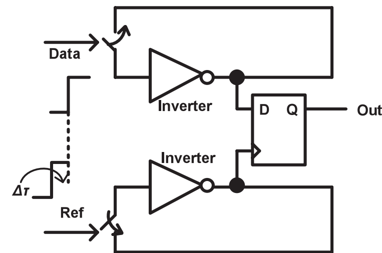

Fig. 11 Component-invariant Vernier delay line [73].

number of buffers and flip-flops in the delay lines.

To reduce the area overhead and to alleviate the matching requirements between buffers in the same delay line, as well as between pairing buffers of the two delay lines, the authors in Ref. 73) propose a component-invariant VDL in which ring oscillators constructed from inverters are used instead of using the buffer-counter chains. As shown in **Fig. 11**, the two input signals control the switches of the inverter loops, and thereby encoding their phase information into the ring oscillator frequencies. The output of the D flip-flop is connected to a phase detector, which keeps track of the phase difference between the two ring oscillators and records their changes. This modified VDL has demonstrated an improved jitter measurement resolution of 19 ps. One drawback of this approach is its requirement for a jitter-free reference signal. To eliminate the need of an external reference, the authors in Ref. 74) propose a self-referred VDL in which an extra self-characterizable delay element is inserted in front of one of the two ring oscillators. It was demonstrated that a 18.5 ps resolution can be achieved without the need of a jitter-free reference signal.

Under a similar principle, the authors in Ref. 75) use a pair of Vernier oscillators that oscillate at slightly different oscillation frequencies for jitter measurement. To measure the time interval between two transition edges, the first and the second oscillators are triggered respectively upon the detection of the first and second transition edges. The numbers of clock cycles for both oscillators are then counted until the two oscillator outputs are phase-aligned. Based on the difference in their cycle counts from the point the two oscillators are triggered till the point that their outputs are phase-aligned, along with the information of their oscillation frequencies, the time interval between the two transition edges can be accurately measured.

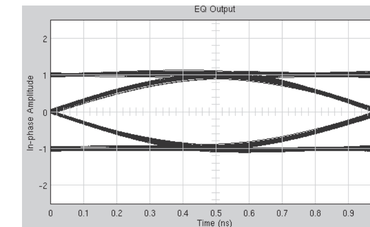

Fig. 12 An exemplar eye diagram.

The ability of a PLL to remain in-lock in the presence of jitter at different frequencies and magnitudes, known as *jitter tolerance*, can be characterized through the PLL's jitter transfer function. The authors in Refs. 76), 77) propose to measure the jitter transfer function by injecting an analog sine-wave to the input of the loop filter input and measuring the bit-error rate (BER) of the VCO output.

In addition to jitter measurement, BIST techniques for measuring other PLL performance parameters such as the lock time, lock range, output frequency, and duty cycles can be found in Refs. 69), 78), 79). A BIST technique targeting the measurement of the output frequency and the tuning range of the VCO can be found in Ref. 80).

3.3 DfT Techniques for Equalizers in HSSL

Equalizers (EQ) are important building blocks in high-speed serial links that compensate for the inter-symbol interference (ISI) resulting from the channel's limited bandwidth. A standard method for testing equalizers is to measure the eye quality using an external scope. **Figure 12** illustrates an exemplary eye diagram in which the horizontal axis represents the unit interval (UI) and the vertical axis is the voltage level. However, measuring the eye-opening at the equalizer output is not an easy task because of the lack of direct access to the signal in an integrated HSSL. Physically connecting the equalizer output to an external access point, as shown in **Fig. 13**, requires an extra pin. In addition, as a result of the probe contact, the eye characteristics captured through external probing have degraded signal integrity and differ from that actually observed by the clock and data recovery (CDR) circuit.

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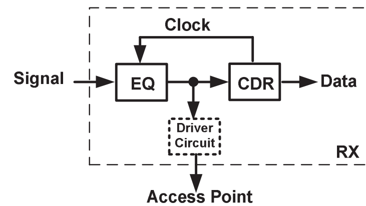

Fig. 13 Adding access point to the equalizer output in an HSSL.

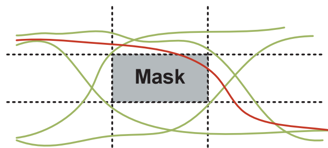

Fig. 14 Operation principle for one mask in Ref. 83).

On-chip eye-opening monitors have been proposed to address this problem. The monitor circuitry proposed in Ref. 81) measures the horizontal eye-opening at the equalizer output that is reported as an analog DC signal. The monitor circuitry in Ref. 82) only measures the vertical eye-opening. A two-dimensional monitor, proposed in Ref. 83), can report the effective eye-opening by capturing the data transition characteristics with respect to several rectangular masks. The vertical opening of a mask is defined by two reference voltages and the horizontal opening is set by two phases of the sampling clock. **Figure 14** illustrates the operating principle for one mask, in which one of the data transitions falls within the mask while other transitions all fall outside the mask. A mask error rate (MER) is defined as the number of data transitions that fall inside a given mask. With respect to a given MER threshold (e.g., MER = 0), the effective eye-opening can be derived based on the aggregated results for a set of masks, as shown in **Fig. 15**. Since the errors on the left and the right sides of the masks are counted separately, this approach can effectively capture the eye-opening of an asymmetric eye diagram, which is a more realistic scenario.

An on-die waveform-capture approach was proposed in Ref. 84) and its application to testing HSSL was reported in Ref. 85). The waveform capture circuit, functioning like an on-chip oscilloscope, is made possible by sweeping a set of timing phases and voltage levels and by checking the bit error rate with respect to each of these settings. The output waveform in response with a long data pattern is captured and the mean voltage at each sampling time is derived for characterizing the amount of noise and jitter.

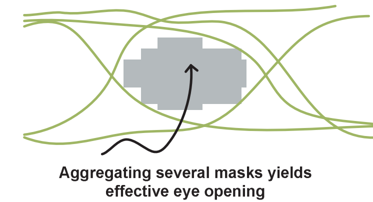

Fig. 15 Methods of obtain effective eye opening in Ref. 83).

These on-chip monitors enable characterization and testing of the eye quality. The output of such a monitor can be further used to automatically tune an equalizer's performance in a closed-loop control configuration [81),83),86)]. For example, in Ref. 86), an on-chip ISI monitor is used to measure the response from the channel and the equalizer on the fly is then compared with an ideal response. The control circuit then adjusts the equalizer parameters to minimize the difference. However, such self-tuning features in general incur a non-trivial overhead and thus may not be affordable for some cost-sensitive applications.

3.4 DfT and BIST Techniques for RF Circuits

A number of signal conversion devices, generally referred to as *sensors*, have been devised for RF BIST applications that also help alleviate the needs for high-frequency, high-performance RF testers. These sensors extract specific characteristics from high-frequency signals and typically convert them into low-frequency or DC signals for further analysis. For example, sensors that produce a DC signal whose voltage is proportional to the peak amplitude, power, or RMS power amplitude have been successfully developed and deployed. For RF transceivers and wireless SoCs, integrating multiple sensors on-chip to gain sufficient internal observabilty could facilitate cost-effective detection and localization of catastrophic and parametric faults. It also provides useful information for characterization and calibration [87),88)].

In addition to accurate conversion of an RF signal to a low-frequency or DC

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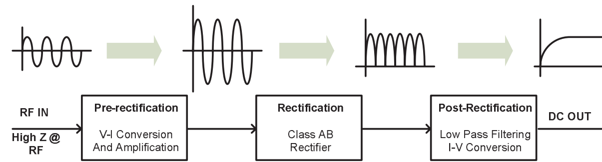

Fig. 16 The block diagram of the RF detector in Ref. 92).

signal, requirements for on-chip sensors include: 1) a low area overhead, 2) a high input impedance that minimizes the loading effect to the DUT, 3) a wide dynamic range and operation bandwidth such that accurate sensing can be made for signals in a wide range of amplitudes and frequencies, and 4) low power consumption such that it's affordable to continuously monitor the circuit and sense the target signal during the normal operation.

A single transistor amplitude detector presented in Ref. 89) has a dynamic range of approximately 10 dB at 2.5 GHz. The RMS power detector reported in Ref. 91) operates at 2.4 GHz with a 20 dB linear dynamic range, while the power detector reported in Ref. 90) operates at 5.2 GHz and has a dynamic range greater than 25 dB. The RF signals are rectified through a single diode-connected transistor in Refs. 90) and 91). An RF detector that has a detection dynamic range of 30 dB from 900 MHz to 2.4 GHz is reported in Ref. 92), the block diagram of which is shown in **Fig. 16**. The input pre-rectification stage, having a high-impedance, converts the voltage to a current signal, and also amplifies the current signal. In the rectification stage, the current signal is rectified using a full swing rectifier. In the post-rectification stage, the DC component of the recertified current signal is extracted through a LPF. While having a wide dynamic range, the power consumption of this sensor is greater than that of Ref. 90) —— it is evident that there is a tradeoff between the dynamic range extension and the power consumption.

The authors in Ref. 93) implemented an LNA BIST by incorporating a current sensor and two power sensors on-chip. The power sensors are built from cascading an amplitude detector followed by a log amplifier. The amplitude detector generates a DC voltage that is proportional to the input signal's amplitude. The log amplifier translates the DC voltage to the logarithmic scale. Using these sensors, the DC current, power gain and 1-dB gain compression point (P1dB) of the LNA-under-test can be measured. By building a correlation model between the sensor responses and circuit performances through regression, it was demonstrated in Ref. 94) that the gain and the input third-order intercept point (IIP3) of a LNA, a mixer, and a receiver chain can be predicted, with a small error, using a built-in amplitude detector.

Besides these sensor-based methods, on-chip spectrum analyzers are also feasible for BIST applications. The spectrum analyzer proposed in Ref. 95) is based on a low intermediate-frequency (IF) architecture, which is comprised of a LNA, a mixer, and a LPF. The output of the spectrum analyzer is further converted into digital signals using an ADC for further digital signal processing. An RF signal-quality measurement circuit, with only one tens of the size in comparison with the on-chip spectrum analyzer in Ref. 95), was introduced in Ref. 96). This measurement circuit converts the RF power at each frequency to a DC signal, which is then converted into digital signals for further analysis based on a sampling technique.

The authors in Ref. 97) utilize the received-signal strength indicator (RSSI) that is already built-in for most RF transceivers as a spectrum power indicator for BIST applications. The output of an RSSI is a DC-like signal that can be used to display the received signal strength on the signal strength indication bar for cell phones. Receiver non-idealities that result in harmonics, distortion, etc. in the output spectrum will also alter the RSSI magnitude. Because the input and the spectrum observation window (limited by the band-pass or low-pass filter before RSSI) are fixed, the receiver spectrum is shifted instead to capture these unwanted frequencies outputs. As a result, during the test mode, a fixed single- or two-tone RF signal is applied to the RF receiver while the divider ratio in the receiver's frequency synthesizer is varied in order to shift the receiver spectrum. The RSSI outputs in response to these inputs in different frequency ranges are captured. This method can observe the output spectrum of the frequency synthesizer and accurately measure the receiver's IIP3 with an error less than 1 dBm.

The authors in Ref. 98) propose to obtain the power spectrum density of the signal paths within an RF transceiver using a statistical sampler proposed in

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Ref. 99). This sampler, basically a comparator that compares the signal under analysis with the output of a white noise generator, produces a single-bit digital bit stream. The output of the noise generator has a zero mean and its maximum amplitude is set to be greater than that of the signal under analysis. The autocorrelation of the signal under analysis can be derived from the statistics of the bit stream. From the Fourier transformation of the autocorrelation function, the signal's power spectrum density can be computed. Because the analysis is completely done in the digital domain and thus can be performed using an on-chip DSP, this method could be employed for online monitoring of the circuit status [100].

4. Emerging Testing Paradigms

4.1 Loopback Testing

The loopback testing is a low-cost solution for testing converter pairs, multi-Gbps high-speed serial links (HSSL), and RF transceivers [2]. Since the converter/transceiver pairs are configured to test each other, the requirement for high-performance testers is alleviated.

As shown in **Fig. 17**, during loopback testing, the DUT is configured into several configurations, each of which basically routes the output of one component of the pair (e.g., the DAC or the transmitter) to the input of the other component of the pair (e.g., the ADC or the receiver). *Internal loopback* testing can be conducted prior to packaging and is, thus, applicable to wafer-level testing. *External loopback* path, configured with the loopback elements (i.e., the interconnects and circuitry used for connecting one component's output to the other component's input) included on the load board instead of built into the DUT, can test additional elements within the DUT, including the components' IO pads and packaging elements. Both internal and external loopback configurations are widely adopted since they enable cost-effective testing of various specifications of both components.

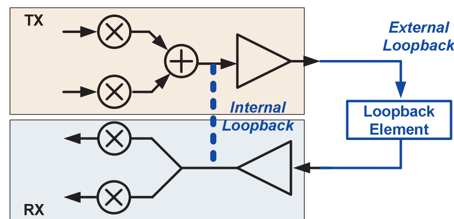

Fig. 17 Typical loopback testing setup (TX: transmitter, RX: receiver).

For HSSL, external loopback is often necessary because internal loopback does not test IO pads and external channel degradation, which are the primary jitter contributors during the system operation. External loopback has a number of variations that were discussed in recent literatures [101)–106)]. To mimic the channel effects, the loopback elements can be designed to introduce specific amount and types of jitters that are fully characterized prior to the loopback testing. The amount of injected jitter can also be made adjustable to improve the test and characterization quality [105]. An extensive discussion on the ATE requirements for facilitating the loopback testing can be found in Refs. 104), 107).

Using either internal or external loopback, the transceivers or converter pairs are tested as a single, end-to-end system (while the system is artificially created and is different from the system configuration used for normal operations). The well-known *fault-masking* problem [108] —— caused by testing multiple components together as a single unit —— could result in non-trivial test escapes of individual components. For example, testing a strong transmitter and a weak receiver together as a single unit may result in the test escape of the weak receiver. In addition, the loopback approach is not effective for debugging because fault localization is inherently difficult in a loopback setup.

To mitigate the fault masking problem and to allow detailed characterization of individual components in an external loopback configuration, additional information can be extracted by monitoring internal nodes or by designing specific loopback elements to serve this purpose. Yu, et al. [109] propose to characterize the noise of a sigma-delta ADC and a DAC by monitoring selected internal nodes in the loopback configuration. However, the selection of internal nodes for observation is circuit-dependent so the proposed method cannot be easily generalized. Some researchers propose to design reconfigurable loopback elements such as an analog filter [108] and an RF transformer [110] to enable adjustment to loopback signals and creation of different loopback responses for component-pair characterization. These enhanced loopback approaches, which do not require

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DfT modifications to the DUT, are general and applicable to a broader range of component pairs. However, if parallel testing of multiple component-pairs is desirable, multiple loopback elements, one for each of the component-pair, would be needed on the load board. The loopback elements for parallel loopback testing could be minimized by including an analog summer and an RMS detector which are shared by multiple component-pairs [111]. By analyzing the test responses at the outputs of these shared elements with respect to different test stimuli, the performance of an individual data converter can be derived.

The application of loopback testing for defect detection of GSM [112] and WLAN [113] transceivers has been demonstrated. In Ref. 112), a BIST solution to testing the bit error rate (BER) in a loopback configuration is proposed. As faults in an RF receiver will likely degrade the noise figure and thus increase the BER of the system, the BER is an effective metric for fault detection. However, deriving a reliable estimate of the BER would take an unacceptably long time due to the low BER specification of modern transceivers, typically in the range of 10^{-12} to 10^{-15}. To speed up the process, one solution is to increase the effective symbol error rate (SER) of the system – and, in turn, the BER because each symbol is comprised of several bits – during loopback BIST by intentionally injecting a predetermined amount of noise from the baseband processor [113]. The actual BER is then estimated based on the measured BER with respect to the test data with an elevated SER. Because a greater SER requires less test data for a reliable BER estimation, this simple strategy effectively reduces the overall test time. An embedded loopback testing solution for RF ICs is reported in Ref. 114). With the attenuation circuitry (for mimicking the channel effects) built on-chip, this loopback testing solution can be applied during both wafer probing and production testing stages. Furthermore, the authors in Ref. 115) propose a loopback testing-based BIST method, in which the on-chip DSP is reused for test stimulus synthesis and response analysis.

The characterization of individual components could possibly be achieved by obtaining circuit signatures at various locations in the loopback configurations. Suggested in Ref. 116), several sensors are inserted inside an RF transceiver, the locations of which are determined by an optimization algorithm. The responses of these sensors are then analyzed to predict the component performances. The details of the analysis for performance prediction, based on the principles of *alternate testing*, will be described in Section 4.2.

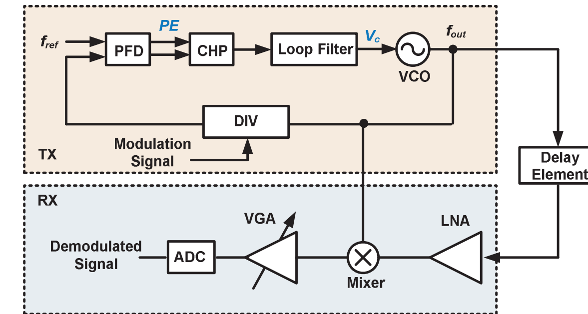

Fig. 18 A transceiver with a direct frequency modulator and a delayed loopback RF configuration [117].

Direct frequency modulators, as shown in **Fig. 18**, have been successfully incorporated into transmitters for many low-cost RF frontends. Under such an architecture, the local oscillator (LO) signal for the receiver-mixer and the transmit signal are produced by the same voltage-controlled oscillator (VCO). In a direct loopback setup, because the transmit signal that is configured to become one input to the receiver's mixer is the same as the other input signal of the mixer, the mixer will yield a DC signal. As the DC signal is often filtered out in the receiver path to prevent saturation, this type of transceiver architectures cannot be properly tested by direct loopback. Delayed-RF [117] (shown in Fig. 18) and offset loopback [118] configurations have been developed to address this problem and to enable loopback testing for such direct frequency modulator-based transceivers.

Some modern RF frontends incorporate multi-band, multi-standard transmitters and receivers. A cross-loopback testing approach for such transceivers was proposed in Ref. 119). In addition, *multisite testing* can be used to effectively increase the test throughput. In multisite testing, as shown in **Fig. 19**, the test stimulus for the receiver DUT is from a transmitter on the tester or from a pre-characterized transmitter. Similarly, the output of a transmitter-under-test is connected to a receiver on the tester or to a pre-characterized receiver. It was

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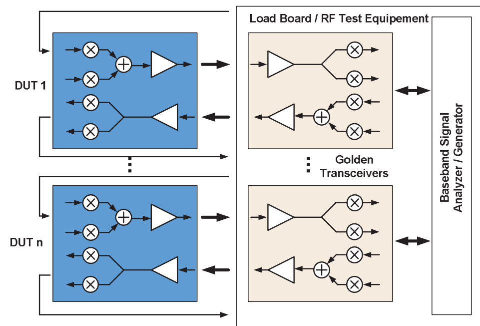

Fig. 19 Traditional multisite testing strategy for RF transceivers [122].

shown in Ref. 120) that octal-site testing —— i.e., testing eight transceivers at a time —— could achieve an 80% test cost reduction. Test strategies for optimizing multisite testing can be found in Refs. 120)–122).

4.2 Alternate Testing

A majority of the above mentioned test strategies aim at enhancing the efficiency and effectiveness of measuring circuit performances for their conformance to the specifications. The *alternate testing* approach provides a lower cost alternative. Instead of directly measuring the circuit performances, the approach predicts them based on a set of DUT's signatures that are captured from cheaper and simpler test setups and measurements.

The foundations of the alternate testing approach lay on the correlation between a DUT's parameter space P, signature space M, and specification space S [123)–126)]. The variations in circuit/device/process parameters (such as transistor widths, doping concentration, etc.), cause variations in the circuit performance (such as gain, power, bandwidth, etc.). These parameter variations also result in variations in certain circuit *signatures* that could be relatively easier to be captured/measured (e.g., a signal's peak or RMS amplitude). The space formed by the measurement of these signatures made by the alternative testing approach is referred to as the signature space M. **Figure 20** illustrates an exemplar effect of variations of a parameter P on a signature M and a specific performance S. There exists a complex nonlinear function f_{PS} that maps each point of interest in the parameter space P to a point in the specification space S, f_{PS}: $P \rightarrow S$.

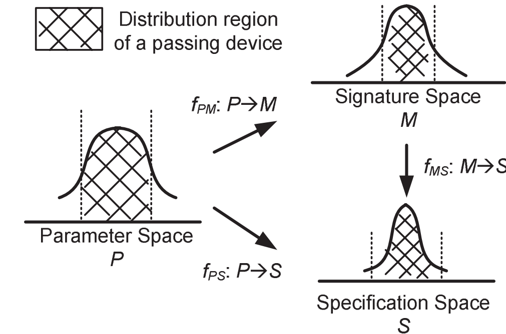

Fig. 20 Exemplar relationships between the parameter, signature, and specification spaces [126].

Similarly, a nonlinear function f_{PM} can be obtained that relates the data in the parameter space P to the signature space M, f_{PM}: $P \rightarrow M$. For a given acceptable range of performances defined in the specifications, there exists a corresponding acceptance region in the parameter space, which in turn has a corresponding acceptance region in the signature space. If the acceptance region in the signature space A_M can be identified, we can infer the passing or failing of a DUT with respect to a specification based on whether the measured signatures of the DUT fall within A_M or not.

Under the alternate testing paradigm whose main objective is to lower the test cost, test stimuli produced by an inexpensive test generator are applied to the DUT whose DC or low-frequency responses at selected nodes, referred to as the DUT's *signatures*, are captured using low-cost equipment. For example, in Refs. 123), 127), pseudo-random test patterns, which can be generated by a simple linear-feedback shift register followed by a DAC, are used as the test stimuli. It was demonstrated that the DUT's impulse response can be derived by computing the cross-correlation between the captured responses and the applied pseudo-random stimuli [127]. Such derived impulse response, which captures both static and dynamic performances of the DUT, can be used as signatures for fault detection. The derivation of the acceptance region in the signature space is based on Monte Carlo simulation. First, a large number of circuit instance models are generated and simulated, each of which is marked either as a pass or

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a fail depending on whether their performances pass specification requirements. In addition, the signatures for each of the simulated instances are also derived from the simulation results. Statistical classification methods are then used to optimally discriminate signatures of pass and fail markers to minimize test escapes and overkills. As a result, an acceptance region in the signature space is derived. This region is then used for pass/fail decisions in production testing that is solely based on the signature measurement, without explicit performance measurement.

Alternatively, as suggested in Ref. 126), the relationship between the signature and specification spaces, f_{MS}: $M \rightarrow S$, can be constructed using regression models such as multivariate adaptive regression splines (MARS)[128]. Based on f_{MS}, DUT's signatures can be used to predict circuit performance. This test strategy requires identification of proper signatures for measurements that can be reliably used for accurate prediction of circuit performances. In addition, suitable test stimuli that can produce the desired signatures and maximize their ability to differentiate good and bad parts are essential for the success of this test strategy.

The alternate testing flow suggested in Ref. 129), shown in **Fig. 21**, consists of two phases: calibration and testing. The calibration phase derives the mapping

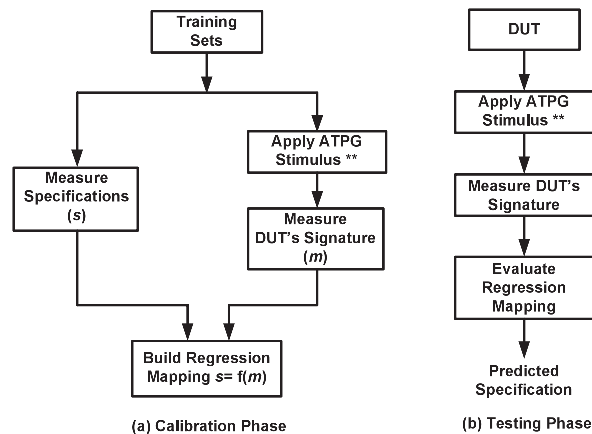

Fig. 21 Alternate testing flow: (a) calibration phase (b) testing phase[129].

function between the signatures and the circuit performances. This phase involves 1) elaborately measure the performance for each of a sample subset of the DUTs (usually on the order of 100 to 200[129]), and 2) obtain the circuit signatures in response to the applied alternate-test stimuli for the same subset of DUTs. The resulting information is then used for statistical learning to build a nonlinear regression mapping function. Note that this calibration phase is a one-time effort for each design.

The final testing of all DUTs is conducted in the testing phase. The same alternate-test stimuli used in the calibration phase is applied to each DUT to obtain the corresponding signatures that are used to predict the DUT's performance based on the constructed mapping function. The predicted performance is then compared to the specifications for a go/no-go decision or for performance binning.

In Refs. 126) and 129), a genetic algorithm is used to find the optimum alternate-test stimuli (the step marked with ** in Fig. 21). An optimization problem is formulated that automatically generates test stimuli with an objective function of minimizing the prediction error. The prediction error is defined as the difference between the predicted circuit performance and the actual circuit performance. Different templates and types of alternate-test stimuli including piecewise linear[126], multi-tone sinusoids[130], and digital pulse trains[131] have been developed as the bases for different applications. The test generation process, which searches for the optimal parameters for the given stimulus template, minimizes the objective function for the formulated optimization problem. Alternate testing has been successfully applied to a number of AMS/RF circuits including op-amps[126], ADCs[132], RF components[133)–136], and RF transceivers[137)–139].

Under the alternate testing paradigm, a DUT's signatures must be capturable by significantly less expensive test equipment/sensors than their performance counterparts. Furthermore, in contrast to conventional specification-based testing for which different circuit specifications often demand different instruments and test configurations resulting in high test overhead and cost, alternate testing can predict multiple circuit performances from a single acquisition of the DUT's signatures and, in turn, result in significant reduction in test time and cost. It was reported in Ref. 140) that the alternate testing approach achieved a 3X test time

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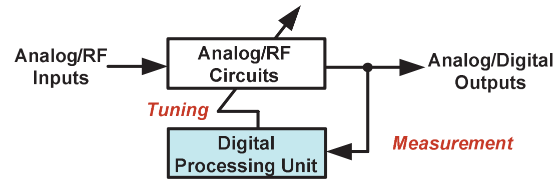

Fig. 22 The conceptual diagram of a digitally-assisted design.

reduction in an industrial production testing environment for an operational amplifier, in comparison to the conventional testing approaches, while maintaining the same level of test quality.

When a process shift occurs, the statistics in the parameter space changes, so do the correlations between the parameter, signature and specification spaces. Therefore, the regression model trained in the calibration phase must be re-trained. A test strategy that incurs a small test time overhead for the re-training process was proposed in Ref. 129).

4.3 Digitally-Assisted Testing

As technology scales, it becomes increasingly difficult to design high performance analog circuits. In addition, the area and power consumption of analog circuits scale at a slower rate than their digital counterparts. Reacting to these alarming trends, the *digitally-assisted* design style [141)], in which a portion of the analog tasks are shifted to the digital domain, has emerged as a solution to reducing the analog design complexity and power consumption.

A conceptual diagram of such a design style is shown in **Fig. 22**. These designs avoid the use of traditional precision analog circuitry by utilizing cheaper and lower-power digital logic to autonomously correct and compensate for the inaccuracy or distortion resulting from the imperfect analog circuitry. To implement more precise and higher performance analog functions, for example, a less precise analog circuit is implemented. Its accuracy in linearity or matching might not be acceptable, but it consumes significantly less power. A digital processing unit is then added to measure the circuit performance and, in turn, tune the analog block and minimize the difference between its current performance and a target value. The analog block must incorporate some built-in tuning knobs that will take instructions from the digital processing unit for performance tuning. Circuit examples that incorporate this design style can be found in digital intensive PLLs [1),142)], adaptive equalizers [143)–145)], and various digitally-calibrated designs such as ADCs [146)–148)], RF components [149),150)], and wireless transceivers [151),152)].

The digital logic is incorporated in these digitally-assisted designs in a closed-loop feedback configuration. Therefore, accessing the signals in the digital circuitry offers a non-intrusive solution to enhancing the controllability and observability to the AMS/RF circuitry. It has recently been shown that by analyzing only the digital information within the digital portion of the DUT, the overall performance of the AMS/RF DUT can be accurately predicted. This testing approach is referred to as the *digitally-assisted analog testing* [153)]. The DfT modifications required to support this testing approach are only in the digital domain that incur very low area overhead and do not degrade the performance at all. The digital circuitry can be tested using digital scan techniques to guarantee its correctness prior to testing the analog circuits. This testing approach uses cheaper digital test equipment in place of high-precision analog testers. As the measurement is completely in the digital domain, it is also much more repeatable and has greater noise immunity.

In the following, we illustrate how the digitally-assisted test strategies can be applied to test digitally-intensive PLLs, digitally-assisted adaptive equalizers (DA-AEQ), and digitally calibrated designs.

4.3.1 Testing digitally-intensive PLLs

Due to the reduced headroom as the technology scales, it is increasingly difficult to design a circuit with fine resolution in the voltage domain. On the other hand, enhancing transistor speed allows a faster clock rate and a sharper digital edge transition edges in the nanometer regime. Hence, instead of striving for voltage-domain resolution, designers have shifted toward time-domain resolution for various designs. All-digital phase-locked loop (ADPLL) [1)] is one of the most widely adopted successful circuit example following this design principle. ADPLL is in fact a digitally-intensive PLL in which a high resolution time-to-digital converter (TDC) and a digitally-controlled oscillator (DCO) are used to provide controllability and improved time-domain resolution. In addition, the conventional analog loop filter, which usually incorporates a large integrating capacitor for removing the static phase error, is replaced by a digital loop filter that is

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scalable and occupies a smaller area.

In Refs. 154), 155), an all-digital BIST approach for a wireless transmitter built upon an ADPLL is demonstrated. By analyzing the input and output signals of the digital loop filters, the phase error trajectory of the wireless transmitter could be accurately predicted. Furthermore, a modulation noise estimation module that detects excessive phase noise was proposed in Ref. 156). By checking whether the estimated modulation noise exceeds a pre-defined threshold, a pass/fail decision can be made. A BIST technique proposed in Ref. 157) detects excessive phase noise in the DCO. In addition, the authors in Ref. 157) also propose an efficient technique to test the frequency tuning varactors in the DCO. These testing techniques help achieve a high test quality for the individual components in the ADPLL-based wireless transmitter.

Another variation of the ADPLL is the analog-enhanced ADPLL (AE-ADPLL)[158], which intends to mitigate the spur/noise effects induced by the limited quantization error, non-linearity, and meta-stability of the TDC and DCO. The DCO gain of this PLL can be characterized by applying a digital code to the DCO and adjusting the fractional code applied at the input of the sigma-delta modulator (SDM). This characterization method was described in Ref. 159) and the silicon validation results were reported in Ref. 142). In addition, an approach to accurately predicting the 3-dB bandwidth of the AE-ADPLL is described in Ref. 158).

Although the above-mentioned techniques cannot be directly applied to test conventional PLLs, various calibration schemes that are built into the conventional PLLs can still be reused to facilitate characterization or testing of the PLLs. For example, in Ref. 160), the author proposes algorithms for characterizing the voltage-controlled oscillator (VCO) frequency by using a built-in digital self-alignment circuitry.

4.3.2 Testing digitally-calibrated designs

The conceptual diagram of digitally-calibrated design is shown in **Fig. 23**. Some aspects of the analog circuit's performance are captured and converted into digital data through ADCs or simply through comparators. Such information is the input to the digital calibration unit that derives the digital tap-coefficients based on an underlying digital adaptation algorithm. These digital tap-coefficients are converted into analog voltage signals, which in turn adjust the analog circuit performance through the built-in tuning knobs.

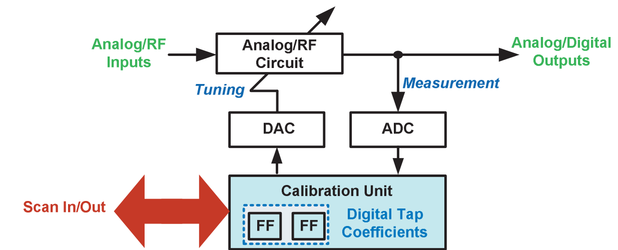

Fig. 23 The conceptual diagram of a digitally-calibrated design and the application of digitally-assisted testing strategies.

As shown in the red arrow in Fig. 23, by controlling and observing the digital tap-coefficients, the calibration unit can provide digital accessibility to the analog/RF circuitry. We could, for example, apply a pre-defined test stimulus from an arbitrary waveform generator (AWG) at the analog/RF input and analyze the convergence characteristics of the digital tap-coefficients in the calibration unit by observing them through scan. We could also stress the analog circuitry, with respect to different corners, by applying specific tap-coefficient values through scan. Observing the circuit performance under such testing scenarios could characterize the DUT and identify out-of-spec devices. Furthermore, we can directly control a subset of the digital tap-coefficients by setting them to specific values for tuning the analog circuitry and observe the resulting values in other coefficients for analysis and fault detection. In this method, the final values of the digital tap-coefficients, after the calibration process has converged, are considered as signatures for fault detection. To further enhance the fault detection capability, we can extract signatures from entire sequences of the tap-coefficient values during the calibration process instead of simply using their final values. These signatures should contain more distinct information for differentiating the fault-free and the faulty circuits.

For digitally-calibrated designs, production testing is conducted after the calibration process has reached convergence. However, the calibration process is often on the order of hundreds of milliseconds to seconds, which becomes a

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dominant proportion of the overall testing time in production. The authors in Refs. 161), 194) propose techniques to accelerate the calibration process of a digitally-calibrated pipelined ADC described in Ref. 146). In addition, to minimize the time overhead spent on calibrating the circuit, it is desired to terminate the calibration process as soon as it reaches convergence. A convergence detection method for the popular least-mean-square (LMS) adaptation scheme is described in Refs. 162), 194).

It is illustrated in Refs. 153), 163) that with minor DfT modifications to the calibration unit and by observing some digital signals in the calibration unit once the calibration process converges, the post-calibration circuit performance can be accurately predicted. Using these methods to predict a DUT's conformance to the specifications can thus significantly reduce the test cost as no additional testing time beyond calibration is needed. Furthermore, since the calibration process iteratively measures the circuit performance for tuning, the calibration process, once converged, could have already covered some specification testing items of the DUT implicitly. Therefore, some defective chips can be identified by analyzing the calibration data obtained during the calibration process, and thereby enabling early rejection without incurring any additional test time beyond that required for calibration. The application of such a screening approach to a digitally-calibrated pipelined ADC described in Ref. 146) was illustrated in Ref. 164).

4.3.3 Testing digitally-assisted adaptive equalizers

The block diagram of an adaptive equalizer, commonly seen in modern high-speed serial links, that follows the digitally-assisted design style is shown in **Fig. 24**. The compensation gain of the equalization filter is adjusted by the tap-coefficients from a digital adaptation unit. Note that the adaptation unit needs only to run at a fraction of the signal data rate because the variations of the channel characteristics, if any, are usually very slow.

The circuit structure of the digitally-assisted adaptive equalizer (DA-AEQ) shown in Fig. 24 follows closely the conceptual diagram of the digitally-calibrated design shown in Fig. 23. To support the application of the digitally-assisted test strategies for DA-AEQs [165)–167)], two DfT modifications are needed (as illustrated in **Fig. 25**). First, a scan structure and additional shadow registers are inserted into the digital adaptation unit so that the values of the tap-coefficients can be controlled and observed through scan and can be captured without interfering with the adaptation process. Second, the feedback signal to the adaption unit is made configurable, either from the equalizer output or from an external digital tester.

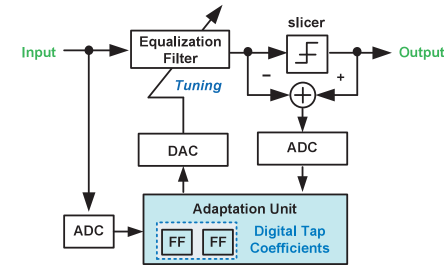

Fig. 24 Block diagram of a digitally-assisted adaptive equalizer.

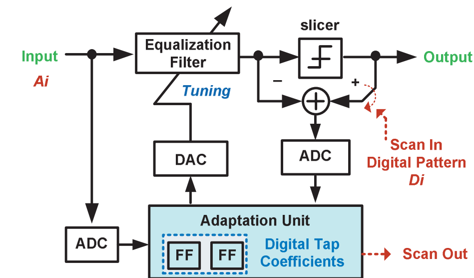

Fig. 25 Testable design of a digitally-assisted adaptive equalizer [165)].

An eye quality characterization method, which is based on analyzing the digital tap-coefficients without directly capturing the eye diagram, was proposed in Ref. 165). In their approach, a pulse that is distorted to mimic the effect of the inter-symbol-interference is applied from a tester as the test stimulus. After the adaptation process converges, the tap-coefficients are scanned out, based on which an eye-opening index η is computed. This eye-opening index η, computed based on the tap-coefficients and the parameters of the channel characteristics, provides a quantitative measurement of the equalizer's performance. According to the theory described in Ref. 168) and the validation results presented in

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Ref. 165), the greater the η value, the more open the eye. If $\eta \leqq 1$, the eye at the equalizer output is considered closed, and the channel is not properly equalized as significant ISI still exists. If $1 < \eta \leqq 2$, the eye is open. Therefore, the eye quality can be tested without explicitly capturing the eye diagram.

For production testing or debugging, we can configure the equalizer to break the feedback from the equalizer output, as indicated in Fig. 25. With this configuration, we can apply specific analog stimuli at the equalizer's input and the corresponding expected digital stimuli at this disconnected feedback point D_i. In response to such stimuli, the tap-coefficients of a fault-free device should converge to an expected set of values. Significant deviation from these fault-free values indicates the presence of defects or excessive variations. In Refs. 165), 166), the tap-coefficients *after* the adaptation process converges, in response to the above mentioned analog and digital test-stimuli pair, are scanned out and used for fault detection. These *steady-state* tap-coefficients are referred to as *static signatures* of a DA-AEQ.

It was illustrated in Ref. 167) that the static signatures (i.e., the final tap-coefficient values after the adaptation process converges) may fail to detect some parametric faults. It was observed that for many of those hard-to-detect faults whose final faulty tap-coefficients are similar to the fault-free ones, the convergence trajectories of the faulty tap-coefficients are quite distinct from those of the fault-free circuit. Therefore, instead of just examining the final values, periodically sampling and accumulating the tap-coefficient during the adaptation process would enhance the fault detection capability [167)]. Signatures extracted from the tap-coefficients' trajectories during the adaptation process are referred to as the *dynamic signatures*. Shadow registers need to be added to enable the observation and accumulation of the tap-coefficients during the adaptation process to ensure that signature capture and collection do not interrupt the normal system operation. It has been shown in Ref. 167) that combining the use of both static and dynamic signatures results in the best test quality.

The signature values and their fault detection capabilities are highly dependent upon the test stimuli. The stimuli should be designed to maximize the signature differences between the fault-free and the faulty circuits. Such stimuli can be automatically generated by solving an optimization problem with an objective function of maximizing the differences between the fault-free and the faulty signatures. An analog automatic test pattern generator based on the Genetic Algorithm for the above mentioned DA-AEQ was recently proposed in Ref. 192).

Interested readers can refer to Ref. 169) for an overview of test strategies for both continuous-time and digitally-assisted adaptive equalizers.

5. Quality Assurance beyond Production Testing

5.1 Characterization, Debugging, and Diagnosis

Due to the high sensitivity of AMS/RF circuitry to PVT variations and to environmental conditions, characterizing various aspects of the chip and locating the root cause of circuit failures become even more challenging than failure detection. The lack of controllability and observability to the internal nodes, resulting from the increasing level of integration, negatively impacts the characterization and debugging tasks. Recent methods developed to address these challenges can be broadly classified into three categories based on the underlying test principles used for supporting the diagnosis and characterization tasks: specification-testing-based, alternate-testing-based, and structural-testing-based approaches.

Specification-testing-based approaches further analyze the measured circuit performances for characterization and/or diagnosis. For example, it is shown in Ref. 170) that fault locations in a flash ADC can be identified by analyzing its DNL plots. A similar concept is demonstrated in Ref. 171) for sub-ranging ADCs. In Ref. 172), the authors propose to extract the poles and zeros from the measured FFT plots of a sigma-delta ADC for which the extracted information is useful for detailed characterization. For RF transceivers, information extracted from the constellation plots can facilitate characterization [173)–175)]. In Ref. 176), a method for decomposing the compound effects of non-idealities for a quadrature modulator is proposed. The authors in Ref. 177) report results for identifying failure components in an RF frontend through a series of specification measurements. Their method can identify most parametric and catastrophic RF faults but has weakness in diagnosing multiple parametric faults. Since techniques of this category leverage the results and the setup of specification-based testing, they incur very little extra overhead. However, they in general suffer

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from limited diagnostic resolutions and may not be able to locate the exact root cause of the failure or degraded performance.

Alternate-testing-based approaches are cost-effective solution for detailed characterization because the circuit signatures in response to the test stimuli designed specifically for alternate testing can be obtained in a low-cost fashion. Statistical learning methods can be used to identify the correlation between signatures and potential failure sources. The signatures are captured by built-in on-chip sensors for which the types, locations, and corresponding test stimuli can be chosen to optimize the diagnosis resolution. Recent examples following this principle for diagnosing RF transceivers can be found in Refs. 178)–180).

Structural-testing-based approaches involve DfT modifications that enable physical reconfiguration of the device under diagnosis to isolate either performance or structure of one building block from others during diagnosis. Examples of this category can be found in Refs. 181)–183) for ADCs and in Ref. 184) for DACs. Techniques in this category in general can obtain a finer diagnostic resolution but the required DfT circuitry may cost a non-trivial overhead and/or require modifications to performance-sensitive analog/RF nodes.

5.2 Built-In-Test-Assisted Performance Tuning

In addition to the manufacturing defects, operating environments, random noise, and interferences all add uncertainty to the performance of an AMS/RF SoC. Conventional solutions to assuring circuit quality under all conditions include increasing design margins, careful layout, and laser trimming. Furthermore, various off-line and online calibration schemes, as discussed in Section 4.3.2, are useful to combat PVT variations. While effective schemes for calibrating important circuit components are available, it is inherently difficult, if not impossible, to calibrate *all* performance parameters of concern. In particular, system-level specifications, such as the EVM and the BER, involve too many parameters to be effectively calibrated using a single calibration scheme. Current practices used for calibrating the performance of individual components could not guarantee the overall system-level quality of service. Therefore, even with a built-in calibration capability, sufficient design margins still need to be incorporated to tolerate environmental variations. Unfortunately, these worst-case designs often consume significantly more power than the near-margin designs.

To meet the quality requirement under all circuit operating conditions without incurring unnecessarily high power consumption, a built-in-test (BIT)-assisted performance tuning scheme can be employed [185]. This scheme incorporates a number of built-in tuning knobs into the design. Circuit signatures captured through various types of built-in sensors such as amplitude detectors [186] or envelope detectors [185] are inputs to an adaptation unit whose outputs in turn control the tuning knobs to optimize the performance of the target circuit/system.

BIT-assisted performance tuning consists of three steps that are executed iteratively: 1) capturing the circuit signatures through built-in test circuitry, 2) comparing the captured signatures against the desired targets and determining the adjustment amount, and 3) adjusting the AMS/RF circuit through the built-in tuning knobs. This procedure is similar to the conventional calibration process, which involves iterative execution of performance measurement, adaptation, and tuning [164]. However, since multiple circuit performances are implicitly captured concurrently in a single test, multiple circuit parameters can be adjusted simultaneously. As a result, BIT-assisted performance tuning can achieve better *overall system-level* performance than conventional block-by-block calibration techniques.

BIT-assisted performance tuning also offers power savings through adaptive power management. Under good operating conditions when the circuit performance exceeds the specification requirements, the supply voltage can be gradually reduced to save power, until the circuit performance degrades to the point marginally meeting the specification. The system-level performance is constantly monitored through the built-in online test circuitry and the power is dynamically and autonomously adjusted based on the captured signatures. This power management scheme can achieve significant power savings, which are made possible by the BIT support and on-chip adaptation.

BIT-assisted performance tuning and adaptive power management based on alternate testing techniques have been successfully applied to several types of RF transceivers [185–191].

6. Summary

This paper summarizes recent developments in testing techniques for the

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AMS/RF circuits. DfT and signal processing techniques help reduce the cost for performance measurement of high-performance AMS/RF circuits. In addition, test strategies such as loopback testing, alternate testing, and digitally-assisted testing can help reduce test time while achieving a high test quality. As it is becoming increasingly challenging to produce working chips, testing becomes an essential function not only for screening defective parts in the manufacturing line but also for supporting overall quality enhancement including post-silicon debugging, in-field testing, and performance tuning.

Future test strategies must be a part of an integrated solution for post-silicon quality assurance, which includes defect screening, silicon debugging, validation, and in-field tuning. Test resources must be shared for multiple of these quality assurance functions and test strategies must also support multiple purposes for overall cost reduction and quality improvement.

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