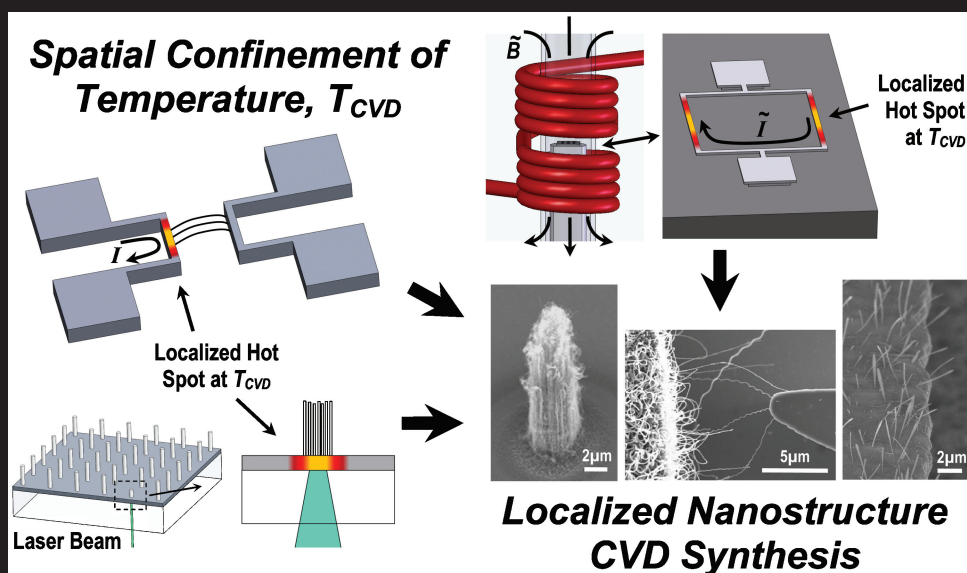


JOURNAL OF APPLIED PHYSICS



APPLIED PHYSICS REVIEWS—FOCUSED REVIEW:
Localized heating induced chemical vapor deposition
for one-dimensional nanostructure synthesis
by B. D. Sosnowchik, L. Lin, and O. Englander

APPLIED PHYSICS REVIEWS—FOCUSED REVIEW

Localized heating induced chemical vapor deposition for one-dimensional nanostructure synthesis

Brian D. Sosnowchik,^{1,a)} Liwei Lin,^{1,a)} and Ongi Englander^{2,a)}

¹*Department of Mechanical Engineering, Berkeley Sensor and Actuator Center, University of California, Berkeley, California 94720, USA*

²*Department of Mechanical Engineering, FAMU-FSU College of Engineering, Tallahassee, Florida 32310, USA*

(Received 28 October 2009; accepted 4 January 2010; published online 5 March 2010)

Localized heating has emerged as a viable technique for the site specific synthesis of one-dimensional (1D) nanostructures. By localizing the heat source, the extent of chemical vapor deposition synthesis reactions can be confined to well-defined, microscale regions. Resistive heating has been extensively used to realize highly localized regions of elevated temperature while maintaining a microelectronics-compatible thermal environment elsewhere. Other localized heating methods are being pursued as well. Overall, the approach is simple, flexible, and robust, and offers unique opportunities in 1D nanostructure synthesis, characterization, and integration. Herein, the recent progress of these techniques is reviewed and discussed. © 2010 American Institute of Physics. [doi:10.1063/1.3304835]

TABLE OF CONTENTS

I. INTRODUCTION AND BACKGROUND. 1
 A. Chemical vapor deposition for nanostructure synthesis. 1
 B. Localized CVD synthesis. 2
 II. MICROSCALE RESISTIVE HEATERS FOR LOCALIZED SYNTHESIS. 3
 III. ADVANCED METHODS FOR LOCALIZED HEATING. 5
 A. Laser-assisted nanostructure synthesis. 5
 B. Plasmon-assisted nanostructure synthesis. 5
 C. Nanostructure synthesis via induction heating. 5
 D. Thermochemical tip-based heating. 6
 IV. PROCESS PARAMETERS AND RESULTS OF LOCALLY SYNTHESIZED 1D NANOSTRUCTURES. 6
 V. ATTRIBUTES OF LOCALLY SYNTHESIZED NANOSTRUCTURES. 6
 VI. CHARACTERIZATION OF SYNTHESIS PROCESSES. 7
 A. Thermometry and temperature uniformity for localized synthesis. 8
 B. *In situ* control of synthesis and assembly. 10
 VII. LOCALIZED HEATING AS A BASIS FOR NANOSCALE DEVICES AND APPLICATIONS. 11

VIII. FUTURE OUTLOOK. 12
 IX. CONCLUSIONS. 13

I. INTRODUCTION AND BACKGROUND

A. Chemical vapor deposition for nanostructure synthesis

One-dimensional (1D) nanostructures have attracted considerable interest as potential building blocks and functional components in next generation nanoscale sensing, nano-electro-mechanical systems (NEMS), circuits, and interconnect applications,¹⁻⁴ and in recent years, a significant research effort has focused on the synthesis and characterization of a wide range of 1D nanostructures.^{1,5-10} With the wealth of well-characterized nanostructures and well-formulated processes to control material properties, demonstrations of nanoscale devices, particularly, sensing applications have become common place.^{2,5,11-13}

The controlled synthesis of 1D nanostructures is frequently realized through a bottom-up technique known as chemical vapor deposition (CVD) method. While several different approaches exist for nanostructure synthesis including plasma-enhanced CVD and vapor-solid synthesis, one of the most commonly used CVD approaches involves the vapor-liquid-solid (VLS) mechanism. First described in the 1960s,¹⁴ the mechanism was confirmed to mediate 1D nanowire synthesis with advanced instruments⁶ and has been applied in the synthesis of 1D nanostructures of various materials.^{1,4,6,15,16} While the synthesis mechanics for catalyst-assisted growth can vary by material system, the basic requirements for the reaction are similar—a metallic catalyst, a vapor phase reactant, and a high temperature environment. The catalysts may be dispensed as nanoparticles from

^{a)}Authors to whom correspondence should be addressed. Electronic addresses: bdsosnow@me.berkeley.edu, lwl@me.berkeley.edu, and englander@eng.fsu.edu.

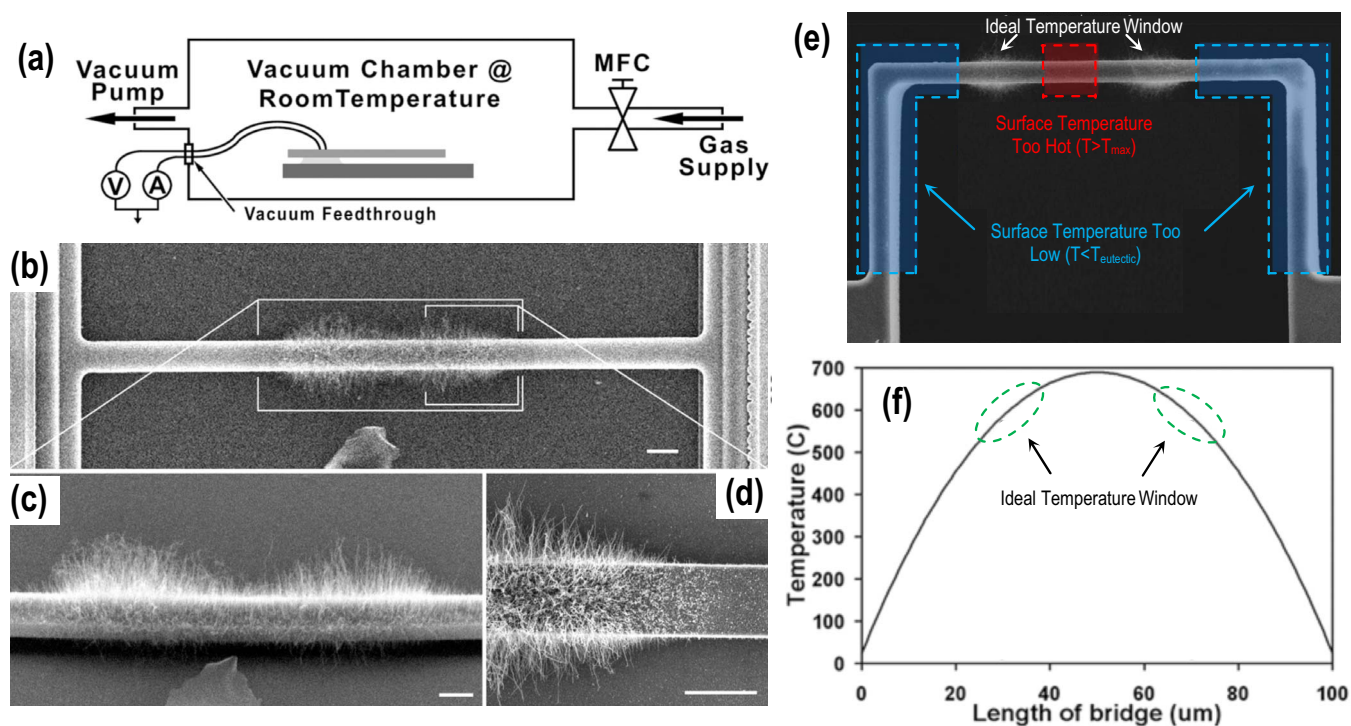


FIG. 1. (Color online) The experimental setup and resulting localized 1D nanostructure synthesis onto a suspended MEMS bridge. (a) A room temperature reaction chamber where the vapor phase reactant and pressure are controlled globally while the temperature is controlled locally by the remote heating of the MEMS bridge. (b) Silicon nanowire synthesis localized to a $30\ \mu\text{m}$ long region at the center of the MEMS bridge. [(c) and (d)] Close up views of the localized growth regions illustrating temperature-dependent growth rates (scale bars are $5\ \mu\text{m}$). (e) A MEMS silicon microbridge with two symmetric silicon nanowire growth regions and (f) the corresponding temperature distribution between the room temperature ends of the MEMS bridge. The growth regions illustrate the location of the ideal temperature environment required for the reaction to take place. Other noted regions exhibit local temperatures that are too high or too low for the reaction to take place.

solution,^{5,17–19} or formed upon the self-aggregation of thin films when heated.^{20–24} The resulting nanostructure diameter is directly related to catalyst diameter,^{5,19} and the choice of substrate can also significantly impact the formation of catalyst particles²⁵ and the resulting nanostructure growth.²⁶ The vapor phase reactant must not more favorably form a second phase with the catalyst.²⁷ Also, the thermal environment must simultaneously satisfy the energy needed for the decomposition of the vapor phase reactant and the growth kinetics of the nanostructure. The mechanics of these synthesis reactions have been widely described.^{1,5,15}

Under appropriate experimental conditions, these synthesis techniques allow for the production of large quantities of 1D nanostructures. However, there are practical limitations to the *bulk synthesis* approach. First, such techniques frequently require additional steps for nanostructure characterization and device integration. Such steps may include nanostructure harvesting, storage in solution, dispensing from solution, surface cleaning, and contact formation.^{12,28,29} Additionally, the high temperature requirements for most CVD reactions also prohibit synthesis on substrates with temperature sensitive materials or devices. This limits the ability of most high-quality, VLS-grown nanostructures to be *directly synthesized and simultaneously integrated* with standard complementary metal-oxide-semiconductor (CMOS) compatible fabrication techniques.

B. Localized CVD synthesis

As a result of these limitations, it has become clear that localized control of the catalyst nanoparticles, the thermal environment, the vapor phase reactant, or a combination of the three factors is highly desirable. For VLS synthesis, localizing the region of the nanoparticle catalyst is most commonly practiced^{22,24,30,31} but this approach requires additional patterning or processing steps that can be complicated and expensive. The localization of the vapor phase within channels of prepared catalysts has been demonstrated³² but is also a process-intensive approach.

An alternative approach that has gained in popularity recently is to confine the required thermal environment, as Englander *et al.*²⁰ first demonstrated with the site-specific synthesis of silicon nanowires and carbon nanotubes (CNTs) on suspended microbridges locally heated by Joule or resistive heating. The catalyst required for synthesis was deposited chip-wide and the vapor phase reactant was introduced into the room temperature reaction chamber. The experimental setup is illustrated in Fig. 1(a). The required heating was realized by the resistive heating of silicon microbridges. An example of 1D nanostructure growth on suspended microbridge is seen in Fig. 1(b), illustrating localized arrays of silicon nanowires in Figs. 1(c) and 1(d). In practice, the experimental setup requires a vacuum feed through into the synthesis chamber providing a connection to an external power supply. The microbridge design and, in particular, the geometry and doping levels determine the power input

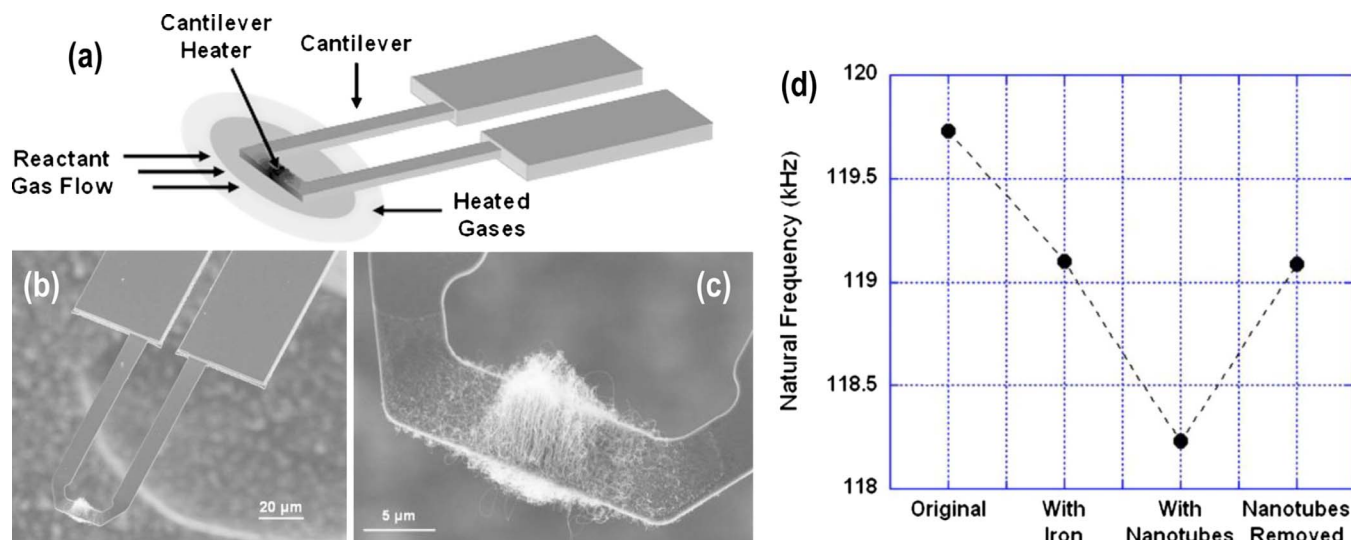


FIG. 2. (Color online) (a) Localized CNT growth at appropriately heated regions of a silicon microbridge. (b) Scanning electron microscopy (SEM) images after the synthesis illustrate the dependence of the CNT growth as a function of local temperature (c). (d) The increase in the mass was detected through a natural frequency shift in the microbridge using an AFM. Adapted with permission from E. Sunden, T. Wright, J. Lee, W. King, and S. Graham, *Appl. Phys. Lett.* 88, 033107 (2006). Copyright 2006, American Institute of Physics. (Ref. 35).

needed to realize the appropriate heating level for the reaction to take place. The power input required to carry out the localized process is significantly reduced from the power consumption of a high temperature, infrastructure-demanding furnace. Similarly, the approach also minimizes the processing time, as high temperature, steady-state synthesis conditions of the microheaters can be accomplished in seconds, significantly faster than that of large furnace environments (~ 1 °C/min heating rate). The localized heating approach further ensures a heterogeneous process limiting contamination and deposition onto chamber walls.

The advantages of leveraging the confined thermal environment required for the various bottom-up synthesis techniques may be summarized as follows:

- *Advancing Technology.* Such bottom-up synthesis techniques enable the advancement of directly integrating nanostructures with larger scale systems en route toward self-assembled devices and applications.
- *Room Temperature Processing.* The ability to maintain an on-chip room temperature environment during synthesis is critical for the integration of 1D nanostructures with devices and materials sensitive to high temperatures, including CMOS-compatible devices, biomaterials, and polymers, to name a few.
- *Versatile Synthesis, Monitoring, and Measurement.* Such environments enable the ability to readily direct the growth of the nanostructures through localized electric fields, and allow the *in situ* monitoring of connections and interfaces. Subsequent characterization may be performed quickly since the setup is straightforward and the devices are compatible with standard microfabrication techniques.

This paper reviews current efforts, innovations, opportunities, and future challenges for bottom-up nanostructure synthesis enabled by localized heating.

II. MICROSCALE RESISTIVE HEATERS FOR LOCALIZED SYNTHESIS

Since the catalyst is deposited on the entire chip and the vapor phase reactant is present everywhere within the synthesis chamber, the extent of the nanostructure growth region is determined by the temperature distribution in the heated microbridge. Because the temperature distribution of the heater varies from room temperature to high temperature while other experimental conditions are kept constant, the ideal temperature range required for the synthesis reaction may be readily identified.²⁰ By coupling the experimental data with modeling of temperature and heating behavior of the microbridge, the thermal synthesis conditions for common and novel material systems can quickly be determined. The microbridge geometry yields a roughly parabolic temperature distribution where the highest temperature is located at the center of the microbridge, while the anchor locations remain near room temperature due to solid state conduction to the substrate. An example of two symmetric silicon nanowire growth regions on a microbridge is seen in Fig. 1(e). The resulting synthesis suggests that the temperature at the central region of the microbridge was too high for the reaction to take place, while regions closer to the anchors were too cool to allow the reaction to take place. The growth regions clearly identify the ideal temperature environment for the reaction to take place [Fig. 1(f)]. This phenomenon has been reported by others, as well. Jungen *et al.*³³ noted that individual, small diameter CNTs grew in the central high temperature region of the microbridge while bundles of single and multiwalled CNTs were synthesized at colder locations. To further confine the resistively heated region and thus the CNT synthesis region, Sunden *et al.*³⁵ utilized suspended silicon microbridges with a lightly doped, resistive region at the center of the microbridge further indicating flexibility in microheater design, shown in Fig. 2(a). The localized CNT synthesis region is shown in Figs. 2(b) and

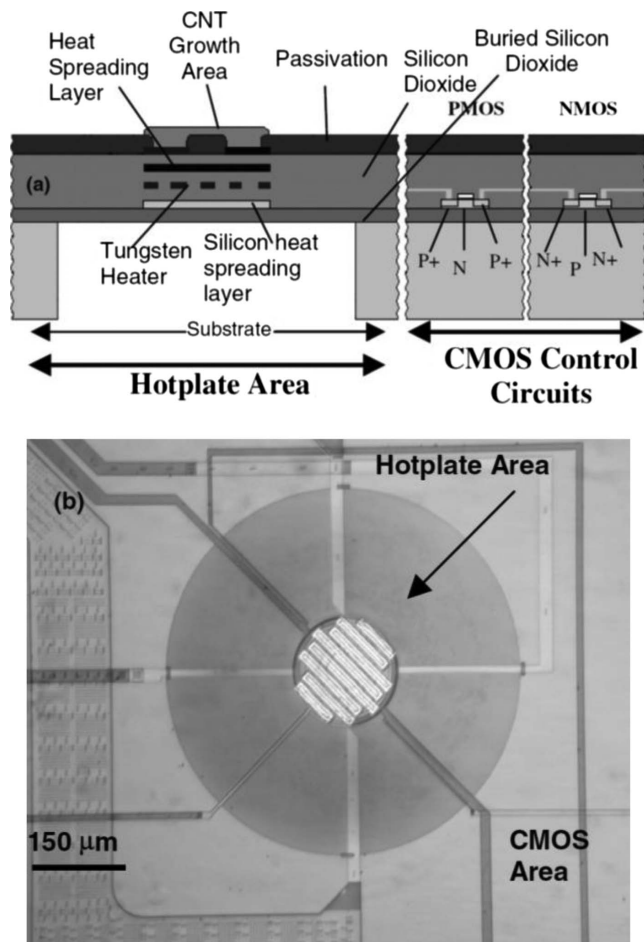


FIG. 3. Localized hotplate setup developed by Haque *et al.* Embedded tungsten heaters enable the localized growth of CNTs on chips with CMOS circuitry. (a) Schematic cross section of integrated hotplate-CMOS unit and (b) optical image of hotplate and CMOS areas. Adapted with permission from M. S. Haque, K. B. K. Teo, N. L. Rupensinghe, S. Z. Ali, I. Haneef, S. Maeng, J. Park, F. Udrea, and W. Milne, *Nanotechnology* 19, 025607, 2008. Copyright 2008, IOP Publishing Ltd. Ref. 41.

2(c), and the added mass of the CNTs, shifting the natural frequency of the microbridge, was detected using an atomic force microscope (AFM) [Fig. 2(d)].

While the use of silicon microbridges is extremely attractive, permitting the direct integration of 1D nanostructures with traditional microelectromechanical systems (MEMS) devices from well controlled resistive heaters, the approach is not limited to exclusively silicon. The use of tungsten,³⁶ titanium,³⁷ and molybdenum^{38,39} microline heaters fabricated on oxide and nitride covered silicon substrates for CNT synthesis have been demonstrated. Additionally, the localized tungsten oxide nanowire synthesis on tungsten microline heaters on oxidized silicon has also been reported.⁴⁰ More sophisticated tungsten MEMS microscale hotplate designs have also been utilized for the localized synthesis of CNTs.⁴¹ The latter demonstration, as seen in Fig. 3, was performed on-chip with nearby CMOS and indicates that the localized synthesis process does not affect CMOS performance—moreover, the CMOS circuitry was used for electrical characterization of the synthesized CNTs.⁴¹

The use of refractory metals as the micro resistive heaters is advantageous as these metals have high melting tem-

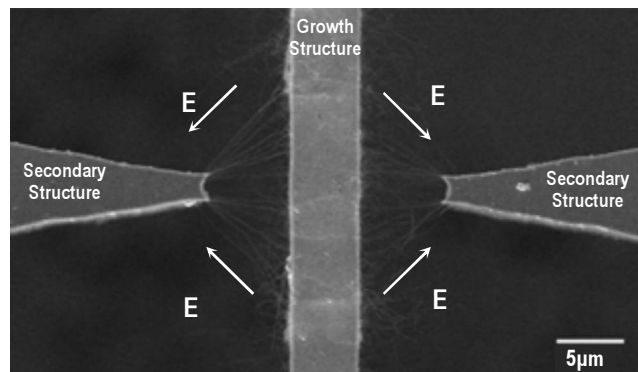


FIG. 4. The direct and site-specific integration of silicon nanowires among multiple MEMS structures. The central MEMS structure, the growth structure, is resistively heated facilitating localized nanowire synthesis. The secondary structures remain at room temperature. A local electric-field placed between the growth and secondary structures assists in guiding the synthesis and self-assembly to yield an organized nanowire array between the MEMS structures.

peratures (offering a wide thermal processing range), intrinsically low resistivity (eliminating need for precise doping in silicon microstructures), are compatible with microfabrication processes, and can be produced using a simple lift-off process. While the silicon microheaters of Englander *et al.* require additional microfabrication steps, the demonstrated architecture ensures preferred thermal and electrical isolation from the substrate, as well as non substrate-bound nanostructures, the benefits of which will be discussed in the following sections. Resistive heating is not limited to a single resistive heating element, but rather an array of resistive heaters can be designed onto a chip and multiple instances of localized nanostructure growth can take place simultaneously at discrete locations throughout the chip. Nagato *et al.*⁴⁰ showed localized heating of twenty 1 μm wide parallel tungsten lines to locally synthesize nanowires at multiple locations at once.

The localized heating approach offers additional opportunities toward the integration and self-assembly of 1D nanostructures into systems and devices, as demonstrated by Englander *et al.*^{42–44} for silicon nanowires and Kawano *et al.*^{21,45} for CNTs. The microscale design for this process includes adjacent microstructures where the synthesis process begins on a resistively heated microbridge and terminates upon contact with an opposing electrode, yielding a self-assembled two terminal micronanosystem. The distance between the bulk structures defines the length of the nanostructures and the application of a localized electric-field has been shown to effectively assist the alignment and orientation of 1D nanostructures between these electrodes.^{46–48} An example of a silicon nanowire array self-assembled among multiple MEMS structures with the assistance of a local electric-field is seen in Fig. 4. This particular approach enables a device architecture with suspended nanostructures. This approach is advantageous since it eliminates surface effects or interactions with the substrate during synthesis and assembly. Furthermore, by using microfabrication techniques to realize vertically offset microbridges and electrodes, ver-

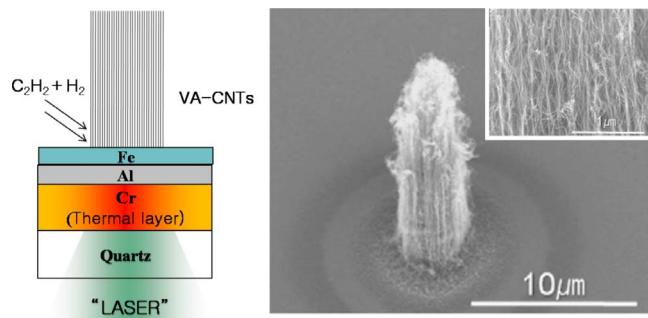


FIG. 5. (Color online) Example of vertically aligned CNT synthesis through laser-assisted CVD by Park *et al.* CNTs were synthesized in arrays with 4 μm diameters, held together by van der Waals forces. Adapted with permission from J. B. Park, S. H. Jeong, M. S. Jeong, S. C. Lim, I. H. Lee, and Y. H. Lee, *Nanotechnology* 20, 185604, 2009. Copyright 2009, IOP Publishing Ltd. Ref. 51.

tical self-assembly of nanostructures becomes a possibility, therefore, allowing opportunities for three-dimensional systems.

III. ADVANCED METHODS FOR LOCALIZED HEATING

It is important to note that the localized heating approach is not limited to MEMS-based resistive heating techniques and perhaps other methods could prove to be more effective in nanostructure integration and directed self-assembly. Recently, the utilization of laser-assisted,^{8,49–51} plasmon-assisted,^{52,53} and inductive heating techniques^{54,55} to realize narrowly confined high temperature regions have been demonstrated as well. Additionally, tip-based localized heating continues to offer unique fabrication capabilities.

A. Laser-assisted nanostructure synthesis

With laser-assisted techniques, the thermal environment required for the catalyst-assisted CVD is realized by tightly focusing a laser beam onto a catalyst-coated surface. A Gaussian shaped laser beam produces a localized “hot spot” on the surface with a high temperature gradient. In a recent example using this technique, Park *et al.* demonstrated the synthesis of vertically aligned CNTs pillars on catalyst-coated quartz substrates. The synthesis was fast, with CNT growth initiated within just one second of irradiation, and the technique was shown to grow columnar arrays four microns in diameter⁵¹ as seen in Fig. 5. In general, the extent of the confinement of laser-assisted CVD is inherently limited to the laser spot size,^{8,50} and timely, parallel synthesis would require a much more complex setup.

B. Plasmon-assisted nanostructure synthesis

In plasmon-assisted CVD processes, localized heating is realized when metallic nanoparticles are illuminated by a laser with a wavelength near the plasmon resonant frequency of the metal. The incoming laser excites surface plasmons in the metallic nanoparticles, and rapid, localized heating is enabled. Boyd *et al.*⁵³ report a temperature increase in several hundred degrees within picoseconds, which suggests a faster response than resistive heaters. In this process, the isolated nanoparticles seem to confine the heated region and prevent

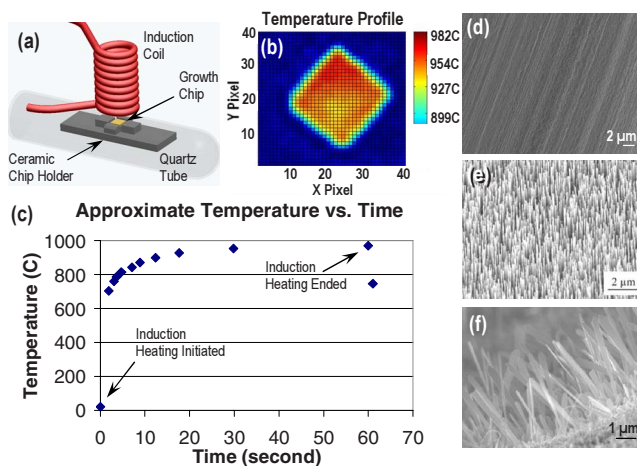


FIG. 6. (Color online) Experimental setup for CNT synthesis. (a) Schematic overview of the CNT synthesis chamber, chip holder, and induction heating coil. (b) Thermal profile of inductively heated silicon chip. (c) Estimated temperature profile for a one-minute test. Synthesis has been demonstrated for (d) CNTs, (e) zinc oxide nanowires, and (f) titanium dioxide nanoswords.

significant heating of the surface, and an inverse relationship is suggested between the laser scan rate and the deposition rate.⁵³ Gold catalyzed lead oxide nanowires were synthesized using the plasmon-assisted VLS approach. Using a similar approach, the plasmon-assisted synthesis of individual silicon and germanium nanowires and CNTs was also demonstrated.⁵² Multiple metallic catalysts (gold, nickel, iron, and titanium) are reported to successfully realize localized surface plasmon heating to catalyze these reactions. Sharp temperature gradients and a rapidly changing thermal environment have been demonstrated with silicon nanowire synthesized using this approach. Overall the high temperature region needed for the synthesis is shown to be confined to a radius of a few microns.⁵² Not surprisingly, the input power is shown to be correlated with the extent of the deposition region.⁵²

C. Nanostructure synthesis via induction heating

Recently, Sosnowchik and Lin⁵⁴ demonstrated a platform technology for the rapid synthesis of 1D nanostructured materials using an induction heating system. The versatile technique has been demonstrated for both large-scale synthesis and localized synthesis on MEMS structures, for both VLS-grown and VS-grown nanostructures. Though similar in setup, the two induction heating synthesis methods are principally different. For large-scale synthesis, eddy currents generated from the propagating high-frequency, alternating magnetic field in a conducting growth substrate, confine most of the Joule heating to within several skin depths of the material. For a material like nickel, the room temperature skin depth has been calculated to be only several microns, effectively confining heat generation to the substrate surface. An example of the setup is shown in Fig. 6(a), with a growth chip on a ceramic holder in a quartz tube within close proximity to the induction coil for synthesis. A characteristic thermal gradient measured via optical pyrometry is shown in Fig. 6(b) from a rapid, one-minute heating process shown in

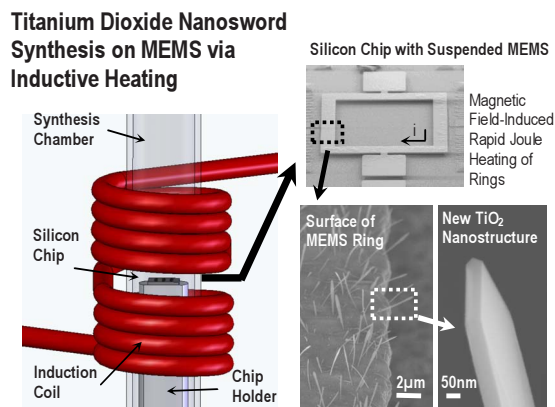


FIG. 7. (Color online) Synthesis of nanowords locally on MEMS structures by induction heating. The large, alternating magnetic field of the coil induces Joule heating in the MEMS ring, enabling localized synthesis of nanostructures in a matter of minutes.

Fig. 6(c). Such a technique was first demonstrated for the synthesis of CNTs,⁵⁴ with fast growth rates and turn-around times as quick as two minutes, and was later demonstrated for vertically aligned ZnO nanowires⁵⁵ and the discovery of TiO₂ nanowords⁵⁶ as shown in Figs. 6(d)–6(f), respectively.

For localized synthesis on MEMS by induction heating, suspended, conductive, ring-shaped MEMS were used. As shown in Fig. 7, the microstructures are positioned on a chip holder in the center of the inductor, and the chamber is conditioned for synthesis. Coil power is initiated, and the large, alternating magnetic field generates an EMF in the ring, rapidly causing localized Joule heating in the suspended MEMS structures, resulting in a temperature distribution similar to the one described by Englander *et al.*²⁰ This approach has been established for the chip-scale, localized synthesis of TiO₂ nanowords⁵⁷ shown in Fig. 7 and CNTs on MEMS,⁵⁸ and it is believed that with appropriate coil design,⁵⁹ this approach could be used for wafer-scale localized synthesis on MEMS.⁶⁰

D. Thermochemical tip-based heating

Thermochemical tip-based heating is another approach to provide localized heating. As opposed to the aforementioned MEMS-based resistive heating technique, in which nanostructures are synthesized directly on the thermal element, a heated tip may be used to locally conduct thermal energy to a growth substrate and initiate nanostructure synthesis. Though resistively heated AFM tips have been frequently studied for thermomechanical storage of data,^{61–63} recently, local thermochemical tip-based heating has been used for patterning of surface bound polymers^{64,65} with linewidths down to 28 nm.⁶⁶ The approach is fast, versatile, and may be integrated with AFM controls for precise tip positioning. However, the growth rates for nanomaterial CVD may be limited by the reaction kinetics or transport of vapor phase species. Furthermore, the tip design would have to allow for adequate delivery of thermal energy much higher than for polymer writing, while appropriate catalyst positioning might be required to permit growth.

IV. PROCESS PARAMETERS AND RESULTS OF LOCALLY SYNTHESIZED 1D NANOSTRUCTURES

Tables I and II detail previously reported results of localized nanostructure synthesis. Clearly, the application of the localized heating method for CNT synthesis has been widely practiced (Table I), while the application to other material systems remains largely untapped (Table II). The wide range of catalysts, vapor phase reactants, and temperature ranges used to effectively yield both single and multiwalled CNTs suggests the robustness and flexibility of the localized heating approaches. Although growth rates are not reported in all cases, reported values do indicate reasonably high growth rates. Growth rate of up to 100 $\mu\text{m}/\text{min}$ have been reported,^{21,38,39,45,51,67–69} and the unique thermal environment does not seem to inhibit the synthesis process. Considering the wide variation in process parameters and process goals, it is difficult to come up with a comparative matrix for reported experimental data, and additional studies into process dynamics and kinetics are needed.

V. ATTRIBUTES OF LOCALLY SYNTHESIZED NANOSTRUCTURES

The localized nanostructure synthesis process alters reaction parameters and most significantly influences the thermal environment through the length of the growing nanostructure. A number of interesting observations have been made with respect to nanostructures synthesized in such environment. For example, Dittmer *et al.* noted that in the localized heating configuration, the growth of single walled versus multiwalled CNTs can be controlled by selecting the vapor phase reactant. Specifically, single walled CNTs were exclusively synthesized when using ethylene (with hydrogen and argon) while the use of acetylene (with hydrogen and argon) resulted in multiwalled CNTs with otherwise identical process conditions.³⁶ The identical ethylene process in a global heating environmental has been shown to yield a mix of single and multiwalled CNTs.³⁶ An explanation for this behavior is still needed.

In another example, using a localized heating source, Hart *et al.*⁶⁷ illustrated a growth rate dependence on the temperature of the vapor phase reactants for CNT synthesis. By thermally preheating the incoming gas phase, the growth rate was shown to increase significantly. For example, in a room temperature furnace using a C₂H₄/H₂/Ar vapor phase mixture and a localized heater at 810 °C, a CNT forest grew at an average rate of 7 $\mu\text{m}/\text{min}$. Keeping all experimental conditions identical but preheating the gas source before it enters the room temperature synthesis chamber, the average growth rate increased to 100 $\mu\text{m}/\text{min}$. The authors suggested that preheating the vapor phase promotes the preactivation of the gas species. The preactivation is considered independent of the growth temperature and is theorized to provide more active species for interactions at catalyst locations. High resolution imaging of the CNTs revealed similar quality and diameter regardless of the thermal pretreatment of the vapor phase source.

Most recently, Molhave *et al.*⁷⁰ demonstrated the localized synthesis of epitaxial silicon nanowires onto single crys-

TABLE I. Locally synthesized CNTs and process parameters. (SCCM denotes standard cubic centimeter per minute at STP.)

CNT	Catalyst	Vapor phase reactant	Temperature/localized heating method	Pressure	Diameter (nm)	Growth rate ($\mu\text{m}/\text{min}$)
Single and multi walled CNTs ^a	Iron nitride, molybdenum and alumina nanoparticles	150 SCCM CH ₄	Resistive—suspended silicon	56 Torr	20	
Multiwalled CNTs ^b	1 nm thin film of iron supported on 5 nm of Al ₂ O ₃	10 SCCM C ₂ H ₂ , 300 SCCM H ₂ and 500 SCCM Ar	~800 °C tungsten/surface	Atm	6	
Single walled CNTs ^b	1 nm thin film of iron supported on 5 nm of Al ₂ O ₃	10 SCCM C ₂ H ₄ , 300 SCCM H ₂ and 500 SCCM Ar	~800 °C tungsten/surface	Atm	0.6–2	
Multiwalled CNTs ^c	2–4 nm of Fe	50 SCCM C ₂ H ₂ and 200 SCCM NH ₃	750 °C resistive—surface tungsten	4.9 Torr	30–80	
Multiwalled CNTs ^d	Nickel	10 SCCM H ₂ , 75 SCCM Ar and 50 SCCM C ₂ H ₂	Resistive—surface titanium		9–24	
Multiwalled CNTs ^e	10 nm iron	1000 CH ₄ , 500 H ₂ and 100 C ₂ H ₂ SCCM	800 °C resistive—suspended silicon	Atm	10–30	0.16–0.33
Multiwalled CNT films ^f	1/10 nm Fe/Al ₂ O ₃	115 C ₂ H ₄ /400 H ₂ /100 Ar SCCM	810 °C resistive—suspended silicon	Atm	10–20	7 or 100 w/ gas phase pretreating
Multiwalled CNT films ^f	1/10 nm Fe/Al ₂ O ₃	115/400/100 SCCM C ₂ H ₄ /H ₂ /CO	810 °C resistive—suspended silicon	Atm	10–20	100
Multiwalled CNT ^g	5 nm NiFe	50 SCCM C ₂ H ₂	850–950 °C resistive—suspended silicon	300 Torr	50	6–40
Single walled and multiwalled CNTs ^h	1 nm iron, Fe, on 5 nm Al ₂ O ₃	6 SCCM of C ₂ H ₄ , 300 SCCM H ₂ , and 500 SCCM Ar	800 °C resistive—surface molybdenum	Atm	1.5 single walled CNT	60
Multiwalled CNTs ⁱ	Nickel	Methane and ethylene				
Multiwalled CNT ^j	2/10/500 nm thick Fe/Al/Cr	100 SCCM H ₂ and 400 SCCM C ₂ H ₂	Laser-assisted heating	100 Torr	10	60
Multiwalled CNTs ^k	10 nm Fe	25/25/100 SCCM C ₂ H ₂ /H ₂ /Ar	620–720 °C resistive—surface silicon/Pt backside heater	0.3 Torr	15–110	7–10.5
Single walled and multiwalled CNTs ^l	5 nm aluminum and 2 nm invar (Fe–Ni–Co alloy)	200 SCCM C ₂ H ₂ and 500 SCCM Ar	550–850 °C resistive—suspended molybdenum	0.0075 Torr		0.9

^aReference 33.^bReference 36.^cReference 41.^dReference 37.^eReference 35.^fReference 67.^gReferences 21 and 45.^hReferences 38 and 39.ⁱReference 52.^jReference 51.^kReference 68.^lReference 69.

tal silicon (111) microbridges. As expected, the conditions for epitaxial growth were determined to be strongly correlated with surface temperature, and as a result, epitaxial growth was observed only at specific locations. Nonepitaxial silicon nanowire synthesis was observed at other regions. Molhave *et al.* also addressed the synthesis of nanostructures of various materials on a single chip by simply changing the vapor phase reactant and independently heating microbridges. Here, the localized synthesis of silicon nanowires

was followed by the localized synthesis of gallium nitride (GaN) nanowires on a nearby microbridge. To date, this is the only demonstration of the localized synthesis of multiple materials systems on a single chip.⁷⁰

VI. CHARACTERIZATION OF SYNTHESIS PROCESSES

The localized heating process opens up a wide range of opportunities for *in situ* process observation, monitoring, and

TABLE II. Locally synthesized 1D nanostructures and process parameters.

1D Nanostructure	Catalyst	Vapor phase reactant	Temperature / localized heating method	Pressure	Diameter / thickness (nm)	Growth Rate ($\mu\text{m}/\text{min}$)
Silicon nanowires ^a	5 nm Au–Pd thin film	100 SCCM 10% SiH ₄ in Ar	550–700 °C resistive—suspended polysilicon and single crystal	0.300 Torr	30–80	1–1.5
Silicon nanowires ^b	15 nm diameter gold nanoparticles	SiH ₄	Laser assisted	0.075–75 Torr	15–200	
Lead oxide nanowires ^c	Gold nanoparticles (approximately 23 average diameter)	Pb(C ₁₁ H ₁₉ O ₂) ₂ and Ar	~300–500 °C plasmon assisted	2–100 Torr		
Tungsten oxide nanowires ^d		0.5 SCCM O ₂	800 °C resistive—surface tungsten	3 × 10 ⁻⁴ Torr		
Silicon nanowires ^e	Nickel, titanium or iron	80 SCCM 2% SiH ₄ in Ar	Plasmon assisted	80 Torr		1
Germanium nanowires ^e	Gold	80 SCCM 2% GeH ₄ in Ar	Plasmon assisted	80 Torr		
Silicon nanowires ^f	40 nm diameter gold nanoparticles	0.2–5 SCCM SiH ₄ in H ₂	>800 °C for epitaxial growth Suspended silicon (111)	15–375 Torr	50	0.67
Gallium nitride nanowires ^f	40 nm diameter gold nanoparticles	3 SCCM TMG, 15 SCCM NH ₃ and 582 SCCM H ₂	Suspended silicon (111)	22.5 Torr		Very low yield
Zinc Oxide Nanowires ^g	2–3 nm Au	Vapor-phase Zn from graphite/ZnO powder	Chip-scale induction heating	Atm	20–120	1
Titanium Dioxide Nanoswords ^h		6 standard liters per minute C ₂ H ₂	Localized induction heating—suspended copper	50 Torr	50–60 nm thickness	1

^aReferences 20 and 42.^bReference 49.^cReference 53.^dReference 40.^eReference 52.^fReference 70.^gReference 55.^hReference 57.

diagnostics that would otherwise be incompatible with a global heating environment. The opportunity for gathering real-time information about the dynamics and kinetics of bottom-up nanostructure synthesis could significantly enhance the understanding of these processes and offer insight into the compositional control, reproducibility, purity, and functional performance of these nanomaterials.

A. Thermometry and temperature uniformity for localized synthesis

Temperature feedback is an important parameter for synthesis. Unfortunately, the microscale size and wide thermal range limit the use of most standard temperature measuring techniques. Finite element models, as well as visual feedback from heated microheaters (intensity²⁰ and color of emitted light⁷¹), are effective, alternative methods for predicting the temperature range. Other, more sophisticated analysis methods have been developed. Sunden *et al.*³⁵ used laser Raman

thermometry to calibrate the temperature in a silicon microheater to within 4 °C and were thus able to directly correlate input power to surface temperature. Jungen *et al.*⁷² used a scanning confocal Raman spectroscopy to perform phonon line position thermography which provides a direct measurement of absolute surface temperature. Similarly, Dittmer *et al.*³⁶ determined the temperature of a molybdenum heater using micro-Raman spectrometer to detect the emitted blackbody radiation. The spectra showed a very good fit to the blackbody formula. Additionally, these heaters have been shown to sustain a stable temperature distribution over extended periods of time (>1 h).⁴² Likewise, another facile approach that could be used for *in situ* thermal monitoring for localized synthesis techniques was demonstrated by Teyssieux *et al.*⁷³ In their setup, far-field optics and a simple charge-coupled device (CCD) camera were used to collect near-infrared radiation. They offer a detailed theoretical analysis of the technique, resulting in a spatial resolution of 450 nm ranging from 500 to 900 K for steady temperature ranges. Their data indicate that longer measurement times

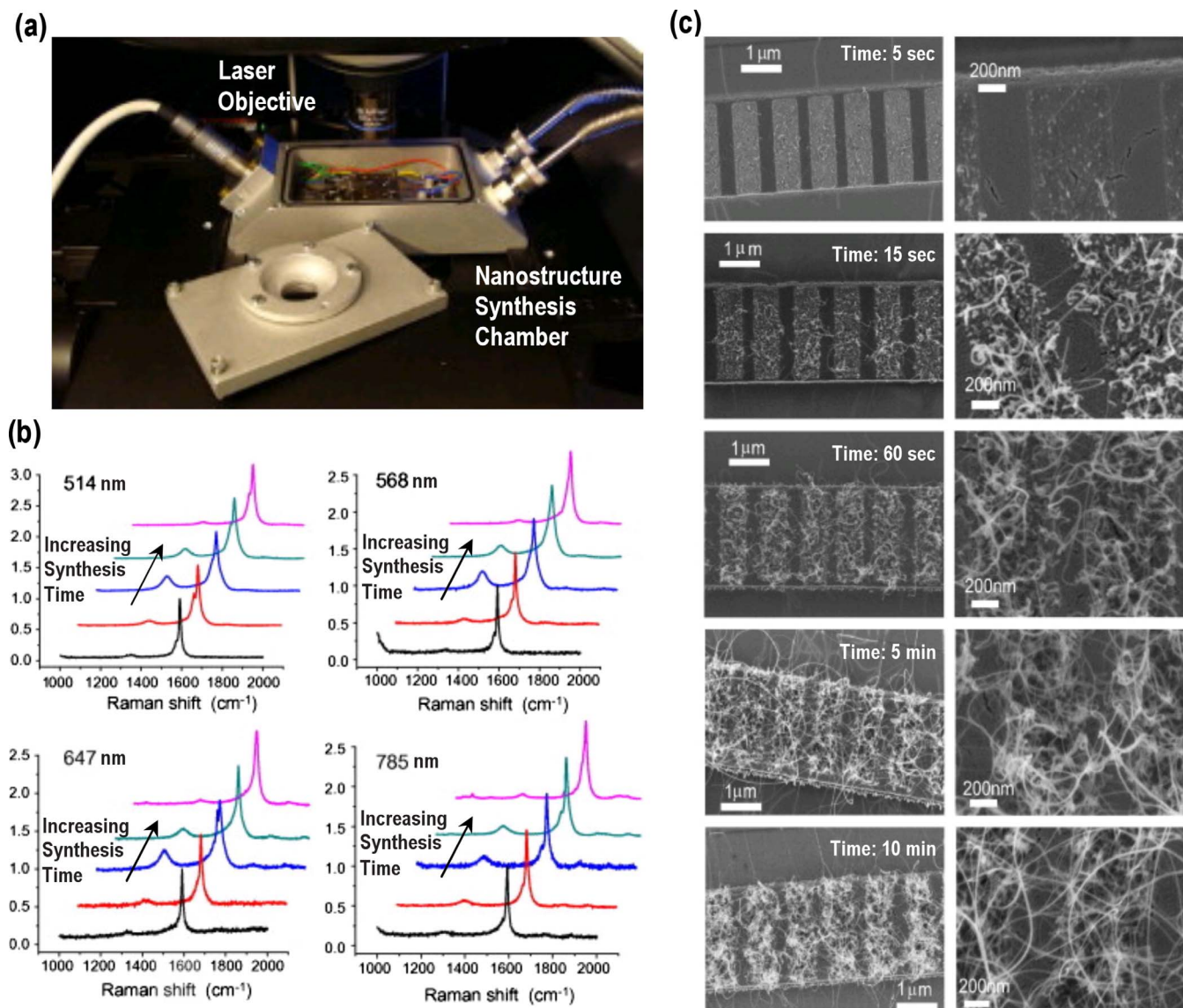


FIG. 8. (Color online) The *in situ* analysis of Raman spectra has been demonstrated to provide information about the growth of localized synthesis processes using the setup shown in (a) from Dittmer *et al.* Their results in (b) for different growth times (c) show that for various excitation wavelengths, the G/D ratio changes with time at constant growth temperature, indicating a greater percentage of larger diameter CNTs or an amorphous layer of carbon. Reprinted from Chem. Phys. Lett. 457, S. Dittmer, N. Olofsson, J. E. Weis, O. A. Nerushev, A. V. Gromov, and E. E. B. Campbell, *In situ* Raman studies of single-walled carbon nanotubes grown by local catalyst heating, 206–210, Copyright 2008, with permission from Elsevier. Ref. 38.

are needed for lower temperatures, which contradict the potential requirements for transient thermal analyses of the localized synthesis process, and the calibration would require additional equipments but nonetheless the technique is promising.

Dittmer *et al.*³⁸ further extended the concept of *in situ* monitoring and diagnosis by integrating *in situ* Raman spectroscopy for CNT growth. More specifically, a unique synthesis chamber was designed to fit on the stage of a Raman spectrometer shown in Fig. 8(a). Here, resistively heated surface-bound molybdenum heaters ($2\ \mu\text{m}$ by $300\ \mu\text{m}$, by $100\ \text{nm}$ thick) were used. Since the Raman signal intensity drops at the synthesis temperature, the power input to the heater is slightly reduced after a certain period of growth to enable the Raman data to be collected. The Raman data was collected as a function of growth time [Fig. 8(b)] and presents new detail with respect to the evolution of the synthesis

process [Fig. 8(c)]. Specifically, the Raman G/D ratio shows a time-dependent behavior potentially suggesting a shift toward large diameter CNTs with growth time and/or the appearance of amorphous carbon through the process.

In certain applications, temperature spatial uniformity may also be an important synthesis parameter. Many of the localized heating methods described in this work introduce large thermal gradients and thus, a highly non-uniform temperature field throughout the sample space. While the presence of these temperature gradients finely confines the extent of the synthesis region, there are practical and design considerations which must be addressed as these approaches become more widely adopted. Molhave *et al.*⁷⁰ for example, have noted higher quality nanowires (as defined by the level of nanowire kinking and bending) in regions of enhanced temperature uniformity created on the interior surfaces of U-shaped suspended silicon microbridges. On the other

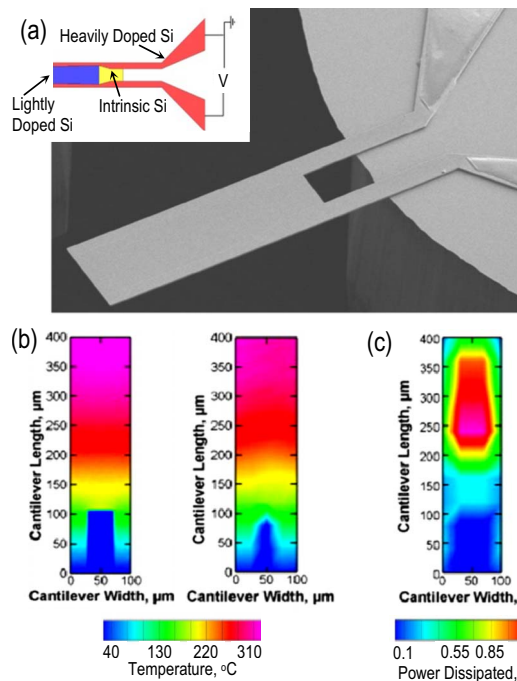


FIG. 9. (Color online) Design and properties of a microscale heater with high temperature uniformity. (a) SEM image of cantilevered heater with design schematic as the inset. Intrinsic silicon, lightly doped silicon, and heavily doped silicon regions are shown. (b) Simulated (left) and experimental (right) temperature distribution and (c) simulated power dissipation at a power input of 20 mW. Reprinted from *Sensors and Actuators A*, Vol. 152, N. L. Privorotskaya and W. P. King, *Silicon Microcantilever Hotplates with High Temperature Uniformity*, 160–167, Copyright 2009, with permission from Elsevier. Ref. 78.

hand, nanowires synthesized along the outer edges, where the temperature gradients are more extreme, illustrate significant kinking and bending especially with increasing length. In this case, temperature gradients are present both along the length of the heater, as well as in the ambient environment away from the surface of the heater. Temperature uniformity within microscale heaters has been extensively studied^{74–78} as these structures have found a wide range of applications. Heater geometry and local doping levels have been determined to greatly impact temperature uniformity in microscale heaters.^{75,78} More specifically, Privorotskaya and King⁷⁸ recently demonstrated that by strategically designing lightly and heavily doped regions in a cantilevered silicon microheater, as shown in Fig. 9(a), temperature uniformity of 2%–4% may be obtained over a 100 μm square region at the cantilever end shown in Fig. 9(b). The lightly doped region ensures high power dissipation, as simulated in Fig. 9(c), which combined with region size and cantilever geometry, are shown to contribute to better temperature uniformity control. Although nanostructure synthesis was not attempted in this work, the measured temperatures are similar to those required for germanium nanowire synthesis,⁷⁹ while further analysis may yield designs for higher temperature devices.

B. *In situ* control of synthesis and assembly

Localized synthesis techniques also enable several unique opportunities for control of synthesis parameters and assembly. For example, Sunden *et al.* demonstrated a mass

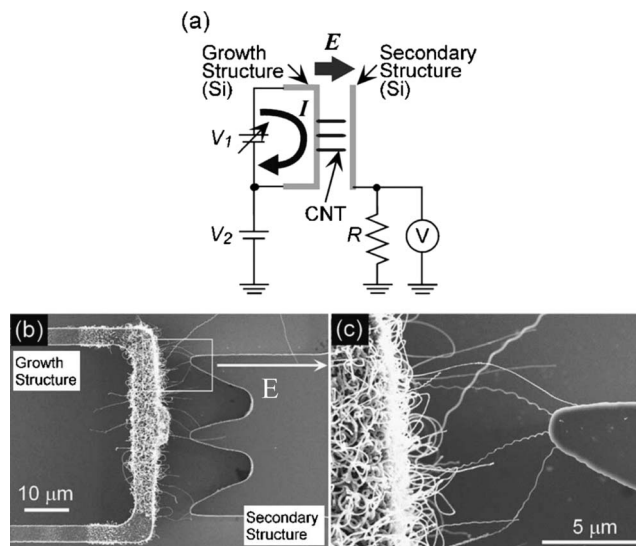


FIG. 10. A technique presented by Kawano *et al.* enables real-time feedback of localized CNT synthesis process. (a) The experimental set up for real-time monitoring where the voltage on the secondary structure is monitored as a function of time. (b) Localized synthesis of CNTs among the growth and secondary MEMS structures. (c) A close up view of the region between the top section of the growth structure and the opposing section of the secondary structure. A change in voltage was recorded with each CNT contact formed to the secondary structure.

sensing application evaluated by tracking the mechanical properties of a microbridge using an AFM. As CNTs continued to grow from microbridge, the increased mass caused a decrease in the resonance frequency³⁵ [Fig. 2(d)]. Using this approach, real-time characterization of the synthesis process may be enabled. Further, one can quantify the delay between the beginning of the nanostructure growth and the introduction of reactants, determine growth rates, track changes in the process, and tune growth rates as a function of time or synthesis conditions (flow rate, power input, and catalyst size)—all of which are important in the development of well-controlled synthesis processes and the development of novel material systems.

To more precisely control the number of CNT connections, Kawano *et al.*^{21,45} integrated yet another technique to track the localized synthesis process by monitoring the voltage of secondary electrode (Fig. 10). Essentially, the output voltage of this electrode remains constant until a CNT makes contact to the electrode, causing a step jump in the voltage. Since the distance between the resistively heated microbridge and the electrode is known, and the voltage is recorded as a function of time, and growth rate information may be recorded. Similarly, one may record the current between the two electrodes as a function of time and the onset of current would indicate the formation of an electrical connection. Again, and for novel materials with unknown growth rates, this real-time feedback is useful in quickly determining the ideal synthesis conditions.

Subsequently, an approach was demonstrated by Jiang *et al.*⁸⁰ to improve the contact resistance between CNTs and silicon microbridges by applying a voltage in excess of the native silicon oxide breakdown voltage. In doing so, the group “healed” a seemingly nonfunctioning CNT device by

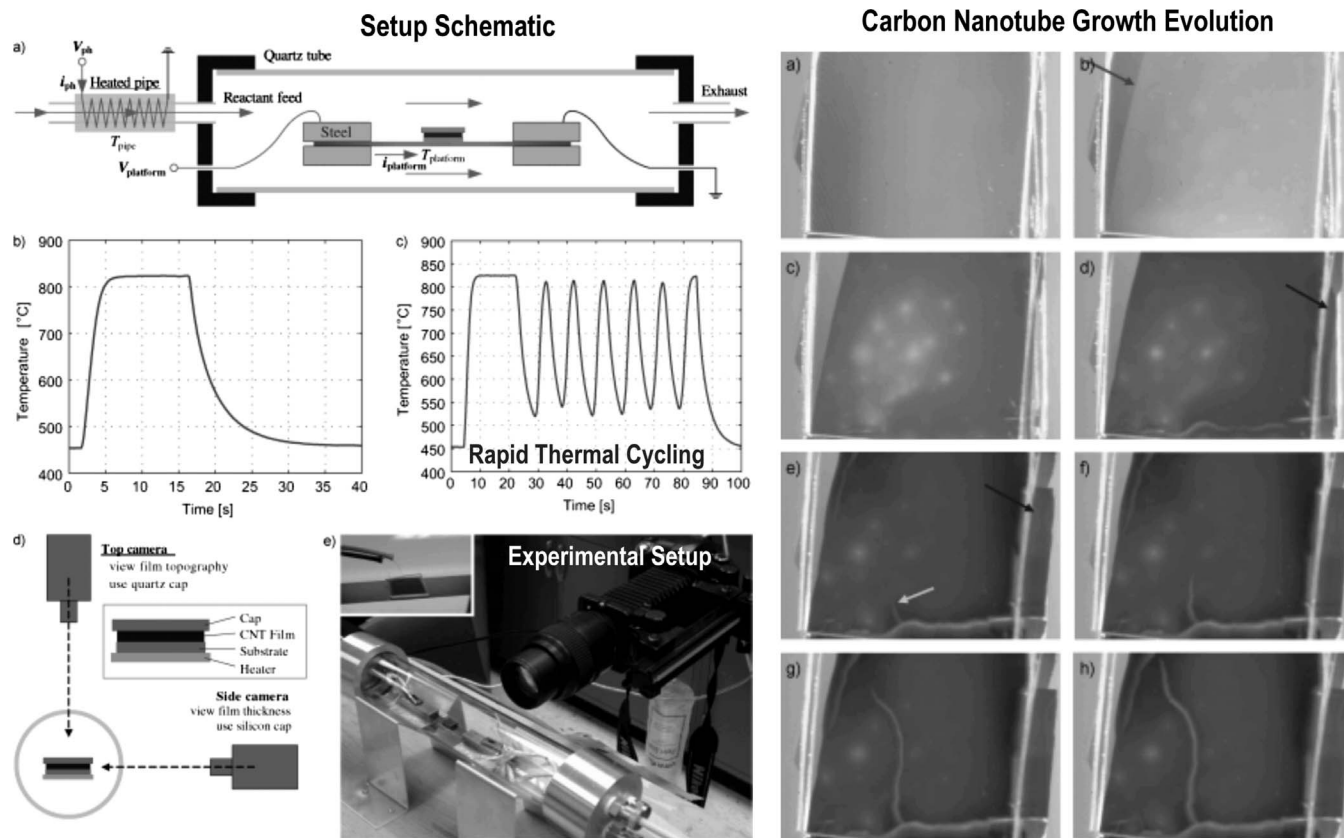


FIG. 11. The setup demonstrated by Hart *et al.* may provide valuable, real-time information about the dynamics and kinetics during nanostructure synthesis. By using a locally heated silicon substrate, the growth chip may be quickly heated and the quartz chamber may be monitored by a CCD camera to monitor the growth of the nanostructures, as shown in [(a)–(h)]. A. J. Hart, L. van Laake, and A. H. Slocum: Desktop growth of carbon-nanotube monoliths with *in situ* optical imaging. *Small* 2007. 3. 772–777. Copyright Wiley-VCH Verlag GmbH & Co. KGaA. Reproduced with permission. Ref. 67.

providing a conducting path through the native oxide layer. Since the native oxide was estimated to be 2 nm, only 10 V were needed for breakdown (“healing”) to occur, and the simple technique could be used to improve the yield of nanomicrocontacts of such devices using manageable voltages.

In an off-chip yet localized heating approach, Hart *et al.*⁶⁷ used a resistively heated a suspended silicon platform (85 mm long, 10 mm wide, and 300 μm thick) to confine the heating within the synthesis chamber. Although larger in size than resistive heaters described previously, the thermal mass and hence the heating and cooling time was still significantly reduced from that of typical tube furnaces. This approach localizes the heating required for large area CNT film growth. In this case, optical imaging and the movement of a “cap substrate” was used to determine growth rates of CNT forests and analyze the CNT thin film evolution during the synthesis process revealing important information about the synthesis mechanism. Such a technique enabled them to relate the final product to timed events during the synthesis process, specifically with respect to events that were previously thought to occur after the synthesis process.⁶⁷ This approach begins to offer information about synthesis kinetics and dynamics. A tilted cap, for example, provides an indication of growth rate variations within a sample. This type of *in situ* monitoring of growth rates can be further enhanced by using a laser displacement sensor.⁶⁷ The experimental setup and real-time feedback from this approach are shown in Fig. 11.

Ideally, by coupling elements of the above techniques, one can develop a sophisticated toolset for real-time analysis, monitoring and feedback of the synthesis, assembly, and quality control of growing nanostructures. Additional opportunities for optical analysis may exist as well.

VII. LOCALIZED HEATING AS A BASIS FOR NANOSCALE DEVICES AND APPLICATIONS

Beyond the real-time monitoring and diagnostics, the concept of localized heating provides significant advantages in the direct integration of 1D nanostructures with MEMS, microelectronics, and on-chip applications. Many current device applications based on 1D nanostructures separate synthesis and integration processes due to process incompatibilities, most commonly thermal requirements.^{2,12,13,34} While such processes have yielded robust proof-of-concept demonstrations, many device assembly approaches are not consistent for large-scale manufacturing and production.

Sensing applications using self-assembled, two-terminal based micronanosystems have been demonstrated.^{43–45} Proof-of-concept demonstration of silicon nanowire based hydrogen sensing,⁴³ CNT based pressure sensing^{44,81} as well as electrothermal gas sensing⁴⁵ have been demonstrated. Additionally, as shown in Fig. 12, a CNT-based bioprobe has also been realized using this technique.⁸¹ The device has the advantages of being integrated with MEMS-based microactuators and having a much smaller diameter compared to

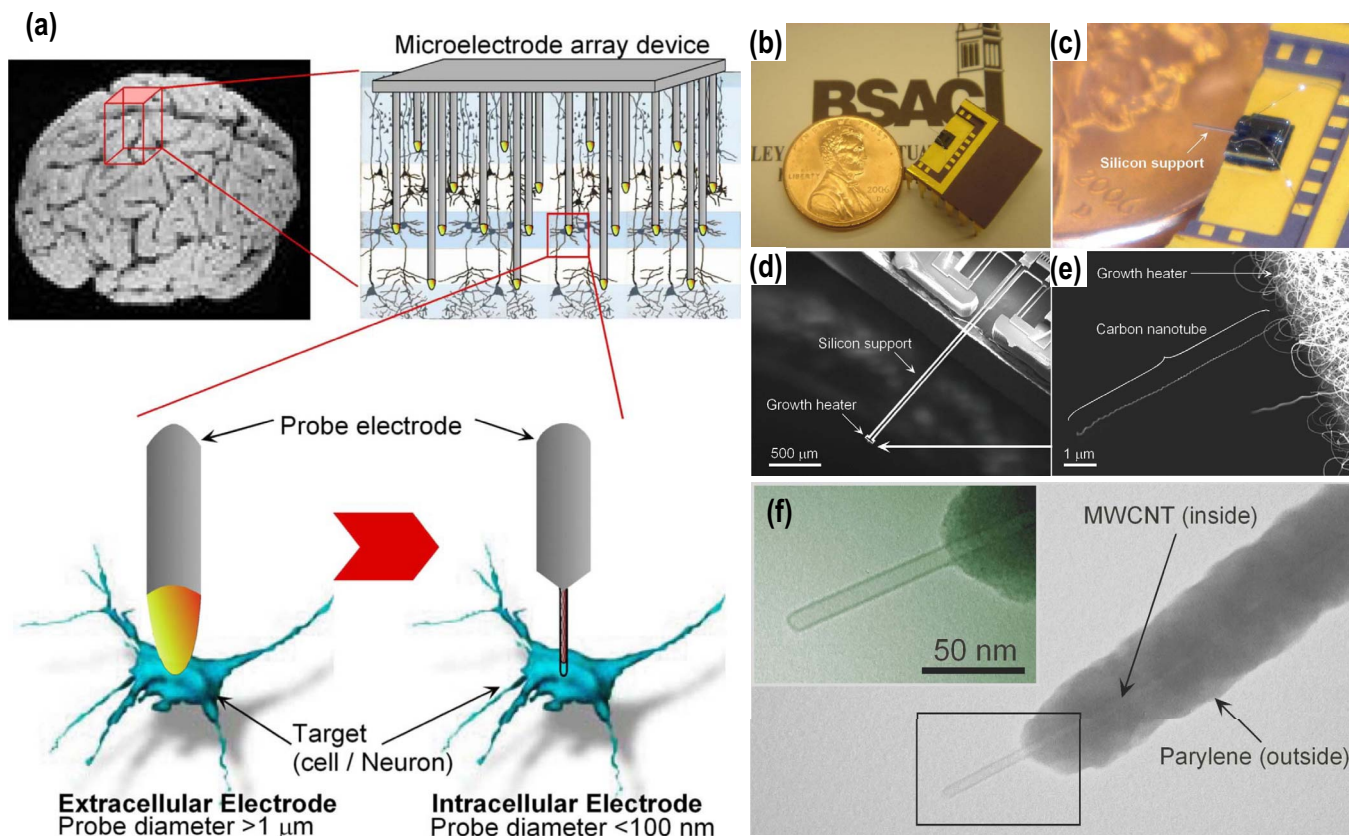


FIG. 12. (Color online) (a) Schematic of a multiprobe array for neural recording. Typical probe diameters exceed $1 \mu\text{m}$, which is too large for the probing of neurons. Conversely, using insulated CNTs, the probe diameter may be reduced significantly. [(b)–(e)] Demonstration of a packaged MEMS-based CNT probe of Kawano *et al.* (f) transmission electron microscopy (TEM) inspection of the probe verifies the 50 nm thick C-type paralyene layer surrounding the 10 nm diameter CNT.

conventional probes, permitting the accurate probing of smaller cellular components, as shown in Fig. 12(a). The packaged MEMS device, shown in Figs. 12(b)–12(f), has a protruding, parylene-coated CNT with a diameter of 10 nm .

Additionally, the suspended nanostructure-based device architecture, in particular, proves beneficial over substrate-bound nanostructures as the surface area available for sensing is increased. Sensing applications can be further enhanced by the direct integration with microscale heaters, as the sensors' response and selectivity may be improved when operated above room temperature. In addition, sensor recovery can be made more efficient at slightly elevated temperatures.^{12,13,82} This device architecture is also consistent with nanoscale resonator (NEMS) applications^{83,84} and expands the sensing capabilities of these systems to include the detection of mass, displacement, and force.

VIII. FUTURE OUTLOOK

While the localized heating approach provides significant advantages in 1D nanostructure integration and assembly and numerous synthesis methods have been explored, several aspects of the technique remain largely unexplored and deserving of future investigation. Examples include the structure-property relationships as a function of synthesis technique, additional studies on the performance of locally-synthesized nanostructures in functional devices, the influ-

ence of the nonisothermal synthesis environment, and the impact of the resulting micronanointerface. The latter two are discussed here.

Compared to nanostructure synthesis in bulk, high temperature furnace environments, the localized process imposes a nonisothermal synthesis environmental, which depending on nanostructure length introduces a potentially large temperature gradient on the growing nanostructure as it extends away from the heat source. The effect of such thermal environment on the quality, defect concentration, dopant distribution, and axial uniformity of the nanostructures has yet to be studied in depth. Molhave *et al.*⁷⁰, however, have speculated that a potential degradation in nanostructure quality may arise as a result of large thermal gradients. While doping levels and microstructure design may mitigate thermal gradients within the device and preheated gas may reduce gradients in the ambient,⁶⁷ controlled comparative studies of the growth mechanism under the different thermal environments are needed in order to validate the approach. Laser guided localized processes and their derivatives, on the other hand may present a more vertically isothermal growth environment when compared to resistive heating. However, in this case, the extent of vertical cooling due to gas flow and enhanced heating due to interactions with the substrate have yet to be studied.

Traditionally, nanostructure contacts to larger scale systems are realized using top-down fabrication techniques, and

while micronanointerfaces are still not well understood, in a research environment, quality contacts can be obtained using these approaches. In contrast, the *in situ* contacts formed as part of the localized synthesis process are fundamentally different—the contact area of these interfaces can be significantly smaller than their top-down contacted counterparts as the area of micronanointerface region may be defined by the nanostructure's end cross-section or diameter. Therefore, thermal and electrical barriers at these interfaces may change the performance and must be evaluated in additional depth.

IX. CONCLUSIONS

Localized heating has emerged as a robust method for the integration of 1D nanostructures with microelectronics, MEMS, and more. The direct integration and process compatibility of the approach are very attractive for large scale production and manufacturing. The approach is flexible, applicable to a wide range of nanomaterials, and presents opportunities for the controlled self-assembly of nanoscale and hybrid devices. The localization of the heating source also presents unique characterization opportunities that should provide new insights and broader understanding of the kinetics and dynamics of bottom-up synthesis mechanisms. Additionally, the *in situ* monitoring, diagnostics, and feedback mechanisms enabled by a room temperature environment allow for a more efficient study of novel 1D material systems and their synthesis parameters, and permit the optimization of synthesis conditions for widely used materials.

- ¹Z. L. Wang, *J. Phys.: Condens. Matter* **16**, R829 (2004).
- ²F. Patolsky, G. Zhang, and C. M. Lieber, *Anal. Chem.* **78**, 4260 (2006).
- ³Z. L. Wang, *Mater. Sci. Eng., R.* **64**, 33 (2009).
- ⁴C. M. Lieber and Z. L. Wang, *MRS Bull.* **32**, 99 (2007).
- ⁵Y. Cui, L. J. Lauhon, M. S. Gudiksen, J. Wang, and C. M. Lieber, *Appl. Phys. Lett.* **78**, 2214 (2001).
- ⁶Y. Y. Wu and P. D. Yang, *J. Am. Chem. Soc.* **123**, 3165 (2001).
- ⁷K. K. Lew, L. Pan, E. C. Dickey, and J. M. Redwing, *Adv. Mater.* **15**, 2073 (2003).
- ⁸S. N. Bondi, W. J. Lackey, R. W. Johnson, X. Wang, and Z. L. Wang, *Carbon* **44**, 1393 (2006).
- ⁹K.-K. Lew, L. Pan, E. C. Dickey, and J. M. Redwing, *J. Mater. Res.* **21**, 2876 (2006).
- ¹⁰Y. Xia, P. Yang, Y. Sun, Y. Y. Wu, B. Mayers, B. Gates, Y. Yin, F. Kim, and H. F. Yan, *Adv. Mater.* **15**, 353 (2003).
- ¹¹C. Staii, A. T. Johnson, M. Chen, and A. Gelperin, *Nano Lett.* **5**, 1774 (2005).
- ¹²D. C. Meier, S. Semancik, B. Button, E. Strelcov, and A. Kolmakov, *Appl. Phys. Lett.* **91**, 063118 (2007).
- ¹³C. Yu, Q. Hao, S. Saha, L. Shi, X. Kong, and Z. L. Wang, *Appl. Phys. Lett.* **86**, 063101 (2005).
- ¹⁴R. S. Wagner and W. C. Ellis, *Appl. Phys. Lett.* **4**, 89 (1964).
- ¹⁵W. Lu and C. M. Lieber, *J. Phys. D: Appl. Phys.* **39**, R387 (2006).
- ¹⁶J. Westwater, D. P. Gosain, S. Tomiya, S. Usui, and H. Ruda, *J. Vac. Sci. Technol. B* **15**, 554 (1997).
- ¹⁷A. I. Hochbaum, R. Fan, R. He, and P. Yang, *Nano Lett.* **5**, 457 (2005).
- ¹⁸Y. Wu, Y. Cui, L. Huynh, C. J. Barrelet, D. C. Bell, and C. M. Lieber, *Nano Lett.* **4**, 433 (2004).
- ¹⁹C. L. Cheung, A. Kurtz, H. Park, and C. M. Lieber, *J. Phys. Chem. B* **106**, 2429 (2002).
- ²⁰O. Englander, D. Christensen, and L. Lin, *Appl. Phys. Lett.* **82**, 4797 (2003).
- ²¹T. Kawano, D. Christensen, S. P. Chen, C. Y. Cho, and L. W. Lin, *Appl. Phys. Lett.* **89**, 163510 (2006).
- ²²A. J. Hart and A. H. Slocum, *J. Phys. Chem. B* **110**, 8250 (2006).
- ²³M. Kirkham, X. Wang, Z. L. Wang, and R. L. Snyder, *Nanotechnology* **18**, 365304 (2007).
- ²⁴M. Tabib-Azar, M. Nassirou, R. Wang, S. Sharma, T. I. Kamins, M. S. Islam, and R. S. Williams, *Appl. Phys. Lett.* **87**, 113102 (2005).
- ²⁵A.-C. Dupuis, *Prog. Mater. Sci.* **50**, 929 (2005).
- ²⁶H. T. Ng, J. Han, T. Yamada, P. Nguyen, Y. P. Chen, and M. Meyyappan, *Nano Lett.* **4**, 1247 (2004).
- ²⁷X. Duan and C. M. Lieber, *Adv. Mater.* **12**, 298 (2000).
- ²⁸F. Patolsky, G. Zheng, and C. M. Lieber, *Nat. Protoc.* **1**, 1711 (2006).
- ²⁹D. Whang, S. Jin, and C. M. Lieber, *Jpn. J. Appl. Phys., Part 1* **43**, 4465 (2004).
- ³⁰M. S. Islam, S. Sharma, T. I. Kamins, and R. S. Williams, *Nanotechnology* **15**, L5 (2004).
- ³¹R. R. He, D. Gao, R. Fan, A. I. Hochbaum, C. Carraro, R. Maboudian, and P. D. Yang, *Adv. Mater.* **17**, 2098 (2005).
- ³²C. Y. Peng, A. K. Kalkan, S. J. Fonash, B. Gu, and A. Sen, *Nano Lett.* **5**, 439 (2005).
- ³³A. Jungen, C. Stampfer, M. Tonteling, S. Schiesser, D. Sarangi, and C. Hierold, *Digest Tech. Papers Transducers*, **1**(5-9), 93 (2005).
- ³⁴C. Hierold, A. Jungen, C. Stampfer, and T. Helbling, *Sens. Actuators, A* **136**, 51 (2007).
- ³⁵E. Sundén, T. Wright, J. Lee, W. King, and S. Graham, *Appl. Phys. Lett.* **88**, 033107 (2006).
- ³⁶S. Dittmer, O. A. Nerushev, and E. E. B. Campbell, *Appl. Phys. A: Mater. Sci. Process.* **84**, 243 (2006).
- ³⁷W. C. Lin, Y. J. Yang, G. W. Hsieh, C. H. Tsai, C. C. Chen, and C. C. Liang, *Sens. Actuators, A* **130**, 625 (2006).
- ³⁸S. Dittmer, N. Olofsson, J. E. Weis, O. A. Nerushev, A. V. Gromov, and E. E. B. Campbell, *Chem. Phys. Lett.* **457**, 206 (2008).
- ³⁹S. Dittmer, S. Mudgal, O. A. Nerushev, and E. E. B. Campbell, *Low Temp. Phys.* **34**, 834 (2008).
- ⁴⁰K. Nagato, Y. Kojima, K. Kasuya, H. Moritani, T. Hamaguchi, and M. Nakao, *Appl. Phys. Express* **1**, 014005 (2008).
- ⁴¹M. S. Haque, K. B. K. Teo, N. L. Rupensinghe, S. Z. Ali, I. Haneef, S. Maeng, J. Park, F. Udrea, and W. Milne, *Nanotechnology* **19**, 025607 (2008).
- ⁴²O. Englander, D. Christensen, J. Kim, L. Lin, and S. J. S. Morris, *Nano Lett.* **5**, 705 (2005).
- ⁴³O. Englander, D. Christensen, J. Kim, and L. Lin, *Sens. Actuators, A* **135**, 10 (2007).
- ⁴⁴O. Englander, D. Christensen, and L. W. Lin, *Int. J. Mater. Prod. Technol.* **34**, 77 (2009).
- ⁴⁵T. Kawano, H. C. Chiamori, M. Suter, Q. Zhou, B. D. Sosnowchik, and L. Lin, *Nano Lett.* **7**, 3686 (2007).
- ⁴⁶P. A. Smith, C. D. Nordquist, T. N. Jackson, T. S. Mayer, B. R. Martin, J. Mbindyo, and T. E. Mallouk, *Appl. Phys. Lett.* **77**, 1399 (2000).
- ⁴⁷E. Joselevich and C. M. Lieber, *Nano Lett.* **2**, 1137 (2002).
- ⁴⁸Y. G. Zhang, A. L. Chang, J. Cao, Q. Wang, W. Kim, Y. M. Li, N. Morris, E. Yenilmez, J. Kong, and H. J. Dai, *Appl. Phys. Lett.* **79**, 3155 (2001).
- ⁴⁹H. Abed, A. Charrier, H. Dallaporta, V. Safarov, H. Jamgotchian, and D. Tonneau, *J. Vac. Sci. Technol. B* **24**, 1248 (2006).
- ⁵⁰J. Shi, Y. F. Lu, K. J. Yi, Y. S. Lin, S. H. Liou, J. B. Hou, and X. W. Wang, *Appl. Phys. Lett.* **89**, 083105 (2006).
- ⁵¹J. B. Park, S. H. Jeong, M. S. Jeong, S. C. Lim, I. H. Lee, and Y. H. Lee, *Nanotechnology* **20**, 185604 (2009).
- ⁵²L. Y. Cao, D. N. Barsic, A. R. Guichard, and M. L. Brongersma, *Nano Lett.* **7**, 3523 (2007).
- ⁵³D. A. Boyd, L. Greengard, M. Brongersma, M. Y. El-Naggar, and D. G. Goodwin, *Nano Lett.* **6**, 2592 (2006).
- ⁵⁴B. D. Sosnowchik and L. W. Lin, *Appl. Phys. Lett.* **89**, 193112 (2006).
- ⁵⁵L. Luo, B. D. Sosnowchik, and L. Lin, *Appl. Phys. Lett.* **90**, 093101 (2007).
- ⁵⁶B. D. Sosnowchik, J.-Y. Ha, and L. Lin, Third IEEE Nano/Micro Engineered and Molecular System Conference (IEEE, Sanya, Hainan Island, China, 2008).
- ⁵⁷B. D. Sosnowchik, J.-Y. Ha, L. Luo, and L. Lin, 21st IEEE Micro Electro Mechanical Systems Conference (IEEE, Tucson, AZ, USA, 2008).
- ⁵⁸B. D. Sosnowchik and L. Lin, 20th IEEE Micro Electro Mechanical Systems Conference (IEEE, Kobe, Japan, 2007).
- ⁵⁹V. Rudnev, D. Loveless, R. Cook, and M. Black, *Handbook of Induction Heating* (Marcel Dekker, New York, 2003).
- ⁶⁰H.-A. Yang, M. Wu, and W. Fang, *J. Micromech. Microeng.* **15**, 394 (2005).
- ⁶¹G. Binnig, M. Despont, U. Drechsler, W. Häberle, M. Lutwyche, P. Vettiger, H. J. Mamin, B. W. Chui, and T. W. Kenny, *Appl. Phys. Lett.* **74**, 1329 (1999).

- ⁶²P. Vettiger, M. Despont, U. Drechsler, U. Durig, W. Haberle, M. I. Lutwyche, H. E. Rothuizen, R. Stutz, R. Widmer, and G. K. Binnig, *IBM J. Res. Dev.* **44**, 323 (2000).
- ⁶³W. P. King, T. W. Kenny, K. E. Goodson, G. Cross, M. Despont, U. Durig, H. Rothuizen, G. K. Binnig, and P. Vettiger, *Appl. Phys. Lett.* **78**, 1300 (2001).
- ⁶⁴R. Szoszkiewicz, T. Okada, S. C. Jones, T.-D. Li, W. P. King, S. R. Marder, and E. Riedo, *Nano Lett.* **7**, 1064 (2007).
- ⁶⁵D. B. Wang, R. Szoszkiewicz, M. Lucas, E. Riedo, T. Okada, S. C. Jones, S. R. Marder, J. Lee, and W. P. King, *Appl. Phys. Lett.* **91**, 243104 (2007).
- ⁶⁶O. Fenwick, L. Bozec, D. Credgington, A. Hammiche, G. M. Lazzarini, Y. R. Silberberg, and F. Cacialli, *Nat. Nanotechnol.* **4**, 664 (2009).
- ⁶⁷A. J. Hart, L. van Laake, and A. H. Slocum, *Small* **3**, 772 (2007).
- ⁶⁸T. Xu, J. Miao, H. Li, and Z. Wang, *Nanotechnology* **20**, 295303 (2009).
- ⁶⁹D. Y. Kim, J. H. Choi, A. R. Zoukarniev, M. H. Yang, I. T. Han, H. J. Kim, S. I. Kim, C. W. Baik, J. H. Park, J. B. Yoo, and J. M. Kim, *IEEE Electron Device Lett.* **30**, 709 (2009).
- ⁷⁰K. Mølhave, B. A. Wacaser, D. H. Petersen, J. B. Wagner, L. Samuelson, and P. Boggild, *Small* **4**, 1741 (2008).
- ⁷¹B. D. Sosnowchik, Ph.D thesis, University of California, 2008.
- ⁷²A. Jungen, C. Stampfer, and C. Hierold, *Appl. Phys. Lett.* **88**, 191901 (2006).
- ⁷³D. Teyssieux, L. Thiery, and B. Cretin, *Rev. Sci. Instrum.* **78**, 034902 (2007).
- ⁷⁴J. Lee, T. Beechem, T. L. Wright, B. A. Nelson, S. Graham, and W. P. King, *J. Microelectromech. Syst.* **15**, 1644 (2006).
- ⁷⁵J. Lee and W. P. King, *Sens. Actuators, A* **136**, 291 (2007).
- ⁷⁶K. Park, A. Marchenkov, Z. M. M. Zhang, and W. P. King, *J. Appl. Phys.* **101**, 094504 (2007).
- ⁷⁷Z. Dai, W. P. King, and K. Park, *Nanotechnology* **20**, 095301 (2009).
- ⁷⁸N. L. Privorotskaya and W. P. King, *Sens. Actuators, A* **152**, 160 (2009).
- ⁷⁹K. Kang, D. A. Kim, H. S. Lee, C. J. Kim, J. E. Yang, and M. H. Jo, *Adv. Mater.* **20**, 4684 (2008).
- ⁸⁰Y. Jiang, M. Q. H. Zhang, T. Kawano, C. Y. Cho, and L. Lin, *MEMS 2008* (IEEE, Arizona, USA, 2008), pp. 725–728.
- ⁸¹T. Kawano, C. Y. Cho, and L. Lin, *NEMS* (IEEE, Bangkok, Thailand, 2007), pp. 895–898.
- ⁸²K. Ryu, D. Zhang, and C. Zhou, *Appl. Phys. Lett.* **92**, 093111 (2008).
- ⁸³V. Sazonova, Y. Yaish, H. Ustunel, D. Roundy, T. A. Arias, and P. L. McEuen, *Nature (London)* **431**, 284 (2004).
- ⁸⁴X. L. Feng, R. He, P. Yang, and M. L. Roukes, *Nano Lett.* **7**, 1953 (2007).