

A Cost-Effective Approach to the Design and Layout of a 14-b Current-Steering DAC Macrocell

Janusz A. Starzyk, Russell P. Mohn, and Liang Jing

Abstract—This brief discusses the economical design of a 14-b current-steering digital-to-analog converter (DAC) macrocell for integration with other analog and digital macrocells in a system-on-chip (SOC). The DAC design is targeted for a standard 0.13- μm six-metal single-poly CMOS process. A novel algorithm sets the switching order of individual current sources and minimizes systematic mismatch errors. The design approach minimizes total fabrication cost of the SOC without a loss to specified DAC design requirements. Total macrocell design area is 2.9 mm^2 .

Index Terms—CMOS macrocell, digital-to-analog converter (DAC), good die yield, INL yield, SOC integration, switching algorithm, systematic error reduction.

I. INTRODUCTION

Since the macrocell is a significant component within a mixed-signal system-on-chip (SOC), its fabrication cost is critical for a cost-effective SOC design. At the same time, the design must satisfy high data-conversion-rate and high accuracy requirements in addition to linearity and spurious free dynamic range (SFDR) requirements. This brief explains an approach in which the entire SOC's fabrication yield is maximized while meeting digital-to-analog converter (DAC) specifications.

Several recent papers ([1]–[4]) addressed current steering CMOS DAC design and recommended solutions to a variety of DAC design problems. Typically, an N -bit current steering DAC is designed using a segmented architecture in which input bits are divided into two groups with B lower significance bits switching binary coded current sources and $(N - B)$ higher significance bits switching thermometer coded unary current sources [4]. Both binary and unary sources use identical or matched transistors where the transistor area is designed using statistical process parameters like S_β and A_β to attain a desired accuracy [2]. In addition, the current sources are split into four symmetrical locations to reduce systematic errors like temperature and electrical gradients and process variations. They are placed in a two-dimensional (2-D) common centroid array and switched with a scheme that minimizes the effects of layout asymmetries and systematic errors.

While increasing their area improves precision of individual current sources, it cannot guarantee improvement in DAC accuracy because of the corresponding increase of systematic errors. A layout dependent switching sequence that minimizes the systematic errors is presented. Using the results in [7] as a basis, a new cost-oriented approach to optimize the design area is developed. The tradeoff between the need to increase design area for improved transistor matching and the need to reduce the design area and improve fabrication yield is analyzed. The optimum design can be obtained by reducing the area of the current source transistors. Table I shows that the designed DAC has a small size in comparison to equivalent subsystems reported in the literature.

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TABLE I
ACTIVE SILICON AREA OF 12-BAND 14-B DACS

DAC area (mm^2)	N (bits)	Process Tech.	Reference
2.9	14	0.13 μm CMOS	this work
11.8	14	0.35 μm CMOS	[9]
12.2	14	0.5 μm CMOS	[7]
13.1	14	0.5 μm CMOS	[6], [4]
14.4	14	0.8 μm CMOS	[8]
3.2	12	0.5 μm CMOS	[3]

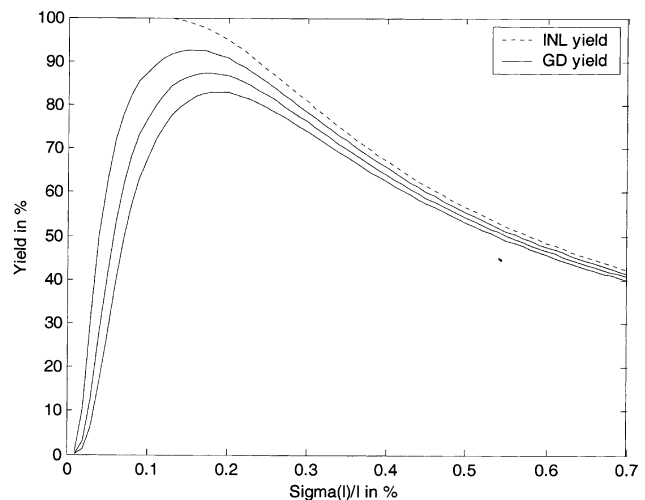


Fig. 1. Yield as a function of the current source matching.

II. DESIGN COST CONSIDERATIONS

Using the results from [2], the relationship between $\sigma(I)/I$ and the INL yield for a 14-b DAC is shown by the upper (dashed) curve in Fig. 1. This relationship is based on a statistical analysis in which a number of mismatched current sources were combined and the INL error was calculated based on the mismatch. The INL yield is the percentage of designs for which the INL error is below a specified limit, usually 0.5 least significant bits (LSB), relative to the total number of designs. For instance, to achieve 99.8% INL yield, the $\sigma(I)/I$ of the current sources must be set to 0.12%. Then the required $\sigma(I)/I$ is used to compute the minimum design area for current source transistors as derived in [5]

$$A = \frac{1}{2 \left(\frac{\sigma(I)}{I} \right)^2} \left[A_\beta^2 + \frac{4A_{VT}^2}{(V_{GS} - V_T)_{CS}^2} \right]. \quad (1)$$

This approach was taken in most of the designs reported in the literature. A justification for selecting 99.8% INL yield was not given. Is INL yield the only important figure of merit for designing a DAC? Certainly not. No one suggests a design with 100% INL yield and for a good reason. It would be too expensive. Such perfect design would require $\sigma(I)/I$ approaching zero and, according to (1), the required current source transistor area would approach infinity. The fabrication cost would follow.

While using $\sigma(I)/I = 0.12\%$ will guarantee that 99.8% of fabricated and functional DACs would meet the INL design specification, it does not mean that an overall optimum was reached with respect to fabrication defects. The increase in the design area associated with

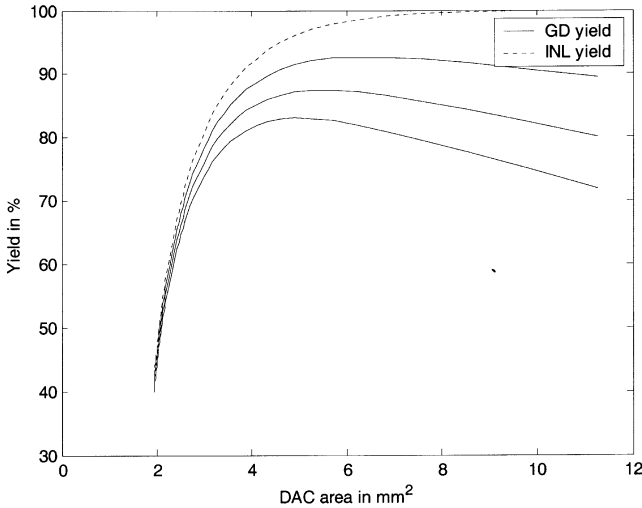


Fig. 2. Yield as a function of the DAC design area.

meeting the INL requirement would result in larger size of the entire fabricated chip and a lower manufacturing die yield.

For a given process technology, let D represent the fixed number of statistical defects per unit area. Then, the manufacturing die yield can be estimated using Murphy's model from

$$\text{die yield} = \left(\frac{1 - \exp(-A_d D)}{A_d D} \right)^2 \quad (2)$$

where A_d is the die area. When $\sigma(I)/I$ is reduced, the die area increases and the die yield goes down. In the following analysis, we assume that the area of the current source array dominates the DAC area and therefore DAC area is proportional to $2^N A$.

Define the good die yield (GDY) as a product of the INL yield and the manufacturing die yield. GDY reveals the percentage of the manufactured dies that will work according to specifications and can be computed from

$$\text{GDY} = \text{erf} \left(\frac{1}{2\sqrt{2^{N+1}} \frac{\sigma(I)}{I}} \right) \left(\frac{1 - \exp(-2^N A D)}{2^N A D} \right)^2 \quad (3)$$

where N is the DAC precision in bits, D is the process-dependent defects level, and A can be computed from (1) to give GDY as a function of $\sigma(I)/I$. Since an increase of $\sigma(I)/I$ leads to a decreased INL yield and increased manufacturing yield, the GDY reaches a maximum at some value of $\sigma(I)/I$ which is a chosen design parameter. The curves labeled GD yield on Fig. 1 show the good die yield computed for a 14-b DAC with typical defect levels. The curves from top to bottom have one, two, and three defects per cm^2 , respectively. For instance, as we can see in Fig. 1, the $\sigma(I)/I$ that maximizes GDY with $D = 3$ is $\approx 0.2\%$, a significantly larger value than that which guarantees 99.8% INL yield. While a specific result is a function of many design parameters and depends on the fabrication process, the GDY will always peak at a unique value of $\sigma(I)/I$.

Since the yield figure is related to the overall design area, the maximum yield for a 14-b DAC corresponds to the total area A_d from 5 to 6 mm^2 as illustrated on Fig. 2. Again, a clear optimum can be found depending on specific technology and the DAC precision. This is not true when only INL yield is considered, in which case the bigger design gives a better yield.

Finally, assuming the fabrication cost increases at least linearly with the chip area, the optimum DAC size is even smaller than the 5–6 mm^2 . In Fig. 3 from top to bottom, the curves show the cost per working DAC macrocell fabricated as a separate chip with three, two, one, and zero

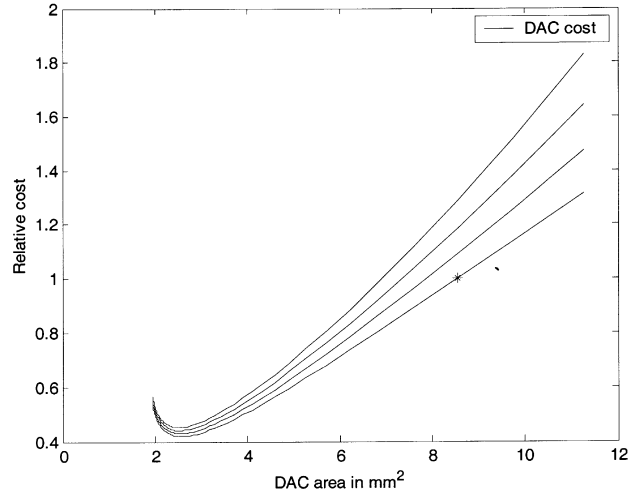


Fig. 3. DAC macrocell relative cost as a function of the DAC design area.

defects per cm^2 , respectively. Cost numbers shown in Fig. 3 are relative to the cost of fabricating a single DAC macrocell designed to satisfy an INL yield of 99.8%. A DAC design area of 8.5 μm^2 is required for a 99.8% INL yield for 0 defects per area; this point is marked with an asterisk (*). The area that minimizes the design cost of the DAC is then selected for a cost-oriented DAC design. More specifically for a 14-b DAC, the optimal area is now between 2 and 4 mm^2 . By using a cost-oriented design, the fabrication cost of the DAC is reduced by more than two times, and the DAC design area is reduced by more than three times in comparison to the fabrication cost and design area of a DAC based exclusively on the 99.8% INL yield requirements.

Similar results are obtained if the DAC is fabricated as a macrocell within an SOC. The area of the other circuit components integrated with the DAC must be considered when optimizing the DAC area for minimized SOC cost. In the SOC, the area of the components exterior to the DAC was approximately 16 mm^2 . The combined fabrication cost for the SOC as a function of the DAC area is illustrated by the three broken-line curves on Fig. 4 for defect levels of three, two, one, and zero per cm^2 . The relative cost of the SOC is minimized at about 4 mm^2 and rises sharply as the DAC area is reduced further toward 2 mm^2 . As the DAC size becomes much smaller than the fixed size of other SOC components, it is less important to optimize its cost. When considering overall SOC cost, the optimum size of the DAC is slightly larger (4 mm^2) than the DAC area when considering the cost of fabricating a separate DAC chip (2–3 mm^2). In a cost-oriented design strategy, DAC size should be determined by the combined INL and manufacturing yield statistics, which results in a smaller design area and cost than if the design is solely based on the INL statistics. Once the transistor area is determined from the cost considerations, geometry of current source transistors can be uniquely determined considering required current and voltage overdrive. In this design, the current source transistor geometry was 16.2 μm by 8.46 μm .

III. REDUCTION OF SYSTEMATIC ERRORS

Based on glitch and sizing analysis, the 8 most significant bits (MSBs) of the 14-b digital input controlled unary current sources and the remaining 6 LSBs controlled binary current sources. Splitting unary current source transistors symmetrically into several locations nullifies the systematic linear errors and reduces quadratic errors. Each unary current source is split into four locations as in Fig. 5. As a result, all linear errors are completely compensated. Optimizing the switching scheme and switching sequence mitigates quadratic systematic errors.

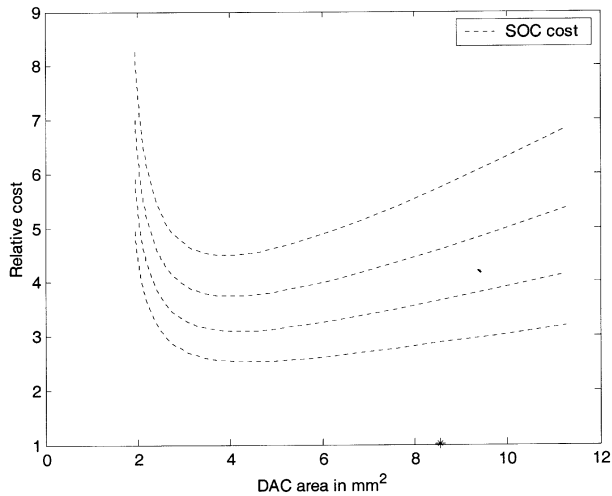


Fig. 4. SOC relative cost as a function of the DAC design area.

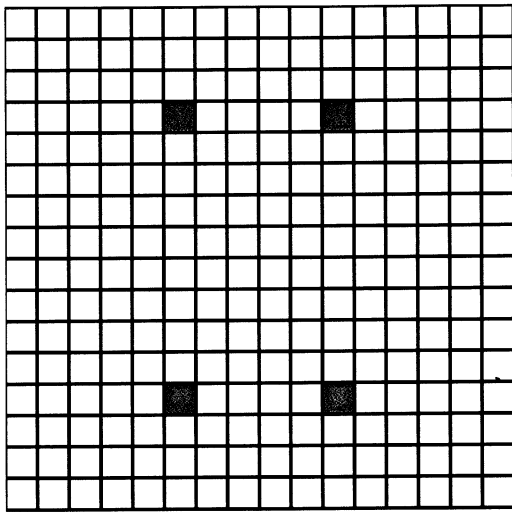


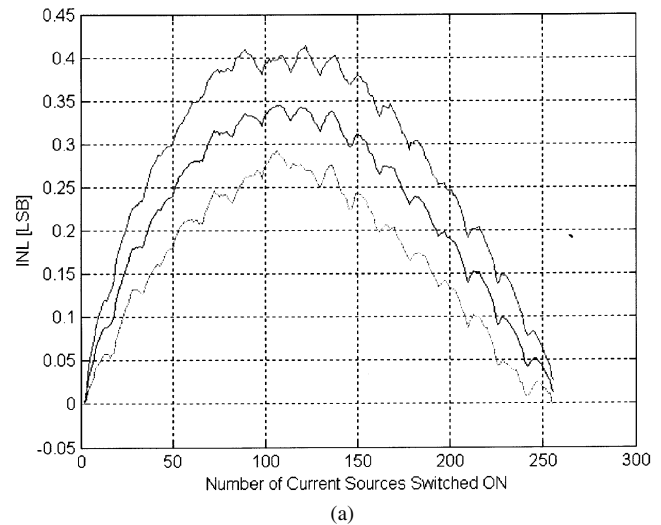
Fig. 5. Compensation of the linear errors by splitting the unary current sources.

Since each unary source consists of 64 basic current sources, if they are divided into four locations, there are 16 current sources in each location. Those were grouped together and controlled by a single pair of switch signals to reduce effect of charge injection during switching. An array, 16×16 , of quarter unary current sources comprises one quadrant of the entire array. One quadrant is copied and flipped to create the entire array such that the current sources have a common centroid. In addition, two rows and two columns of dummy sources surround this array. Binary sources are implemented in the dummy ring surrounding the unary source array.

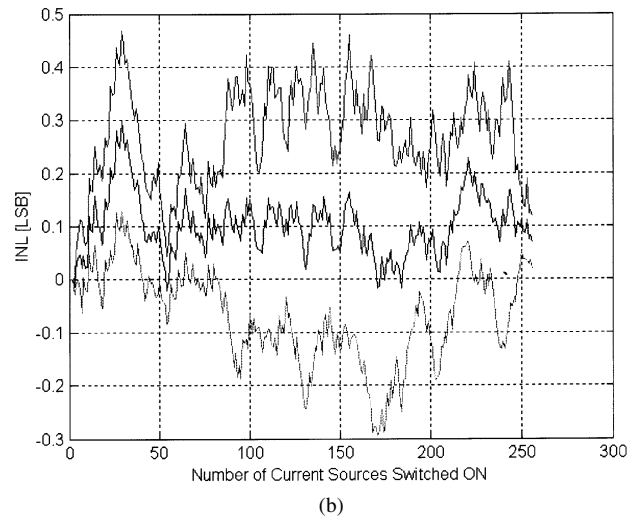
Although each quadrant contains a 16×16 array of quarter unary cells the thermometer section addressing these cells and latches are organized in an 8×32 array. This makes the layout more compact. Quadratic error compensation with a symmetrical selection sequence was inadequate as indicated in [3] with the INL error in LSB growing with area and distance as

$$\text{INL} = 2^{N/2} k S_{\beta} D \quad (4)$$

where S_{β} is technology-dependent mismatch parameter, D is the distance between the current sources, and k is a layout constant greater than one. To reduce this error, a Q^2 random walk switching scheme was used in [4] together with splitting of the unary sources into 16 cells.



(a)



(b)

Fig. 6. INL error for current sources (a) spread into 16 locations and (b) unspread with random walk.

Fig. 6 shows the effect of spreading and block random walk on the total current array error. In Fig. 6(a), current sources were spread into 16 locations without random walk; while in Fig. 6(b) the random walk was applied without spreading. Fig. 7 shows a combination of random walk and spreading into four and sixteen locations, respectively. Both figures are the results of 30 statistical experiments with random distribution of mismatch errors, and illustrate the maximum, mean, and minimum INL error distribution.

This analysis was done to analyze the benefits of the random walk switching scheme, spreading, and their combination. Spreading unit transistors increases routing difficulty and possibly area; spreading into 16 requires more wiring than spreading into 4. Spreading into four with the random walk is as efficient as spreading into 16 with random walk. Thus, we implemented the simpler spreading scheme to reduce the wiring complexity and related capacitive loads.

The Q^2 random walk switching sequence uses a fixed, two-level switching scheme. This scheme is independent of layout and, as was demonstrated in [10], it is not an optimum solution for the minimization of the systematic errors. A new optimized permuting algorithm capable of reducing the systematic errors to a minimum is as follows.

- 1) Start with setting the accumulated error equal to zero.
- 2) Find the current source with biggest absolute error ($\text{Max}_{\text{error}}$).
- 3) Find the next current source, which, after added to accumulated error, makes it closer to $(-\text{Max}_{\text{error}}/2)$.

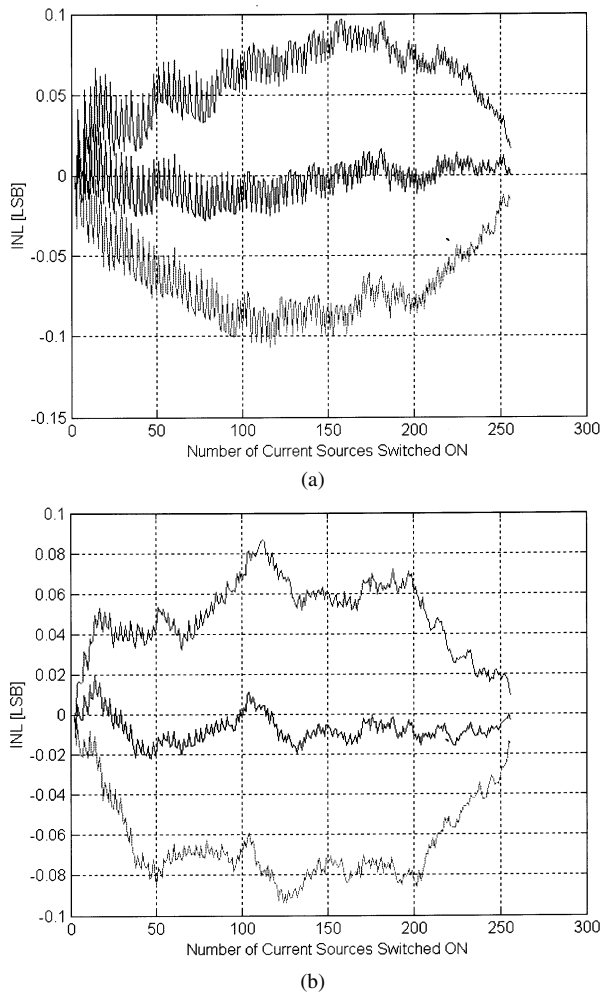


Fig. 7. INL error for current sources (a) spread into four locations with random walk and (b) spread into 16 locations with random walk.

- 4) Set the current source found in step 3) to be the next one switched, update the accumulated error, and delete the used current source from the list.
- 5) Repeat steps 3) and 4) until no more such current sources can be found.
- 6) Set the current source found in step 2) to be the next one switched, update the accumulated error, and delete the used current source from the list.
- 7) With the updated current source, repeat steps 2)–5) until no more current sources are left.

With the switching order generated by this algorithm, the INL error is between $0.5 \times \text{DNL}$ and DNL . The algorithm produces a switching sequence that is layout-dependent. It takes as an input the unary cell dimensions and cell placement and produces the switching sequence array optimized for these parameters. This algorithm attains similar performance in terms of INL error as the INL bounded algorithm presented in [10]; however, it has the advantage of being computationally inexpensive and directly produces an optimum switching sequence.

This approach requires two-level thermometer encoding that yields a simplified implementation of the encoding logic. A 3-b thermometer encoder and a 5-b thermometer encoder are used to encode the 8-b binary vector into thermometer code. According to the results of the permuting algorithm, individual sources are addressed in a pseudorandom order. It is very difficult to manually implement a wiring scheme to connect these sources to their switching latches; therefore a grid of uni-

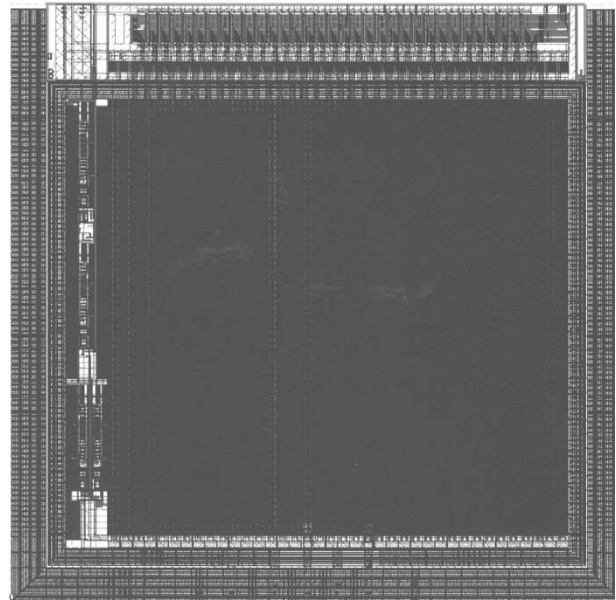


Fig. 8. Compact DAC macrocell layout.

formly spaced wires and an automated via placement algorithm were implemented in software.

A grid of horizontal and vertical wires covers the current source array reaching to individual current sources. Vertical wires connect to the digital latches and through programmable vias are connected to horizontal wires, which connect to individual current sources. The current source transistors are separated from the wiring grid by a layer of metal at ground potential. A metal shielding layer is also in place above the wiring grid metal layers. Since the wiring is over the current source array, no additional layout area was used for control signal routing, and the two metal layers over the current sources provide an additional shield from external interference. The space needed by the wiring is an additional justification for our choice of limiting current source spreading to four locations instead of 16 locations which would require twice as many wires.

The DAC was required to convert at 200 megasamples per second (MSPS), although it was designed and simulated correctly up to 500 MSPS. Simulated power dissipation at the full-scale current is below 90 mW at all operating conditions. Simulated power dissipation in power down mode is $15 \mu\text{W}$. The macrocell has simulated INL of 0.12 LSB and DNL of 0.03 LSB for nominal operating conditions with a differential output voltage range of -1 to 1 V, and it has INL of 0.27 LSB and DNL of 0.15 LSB for the worst case operation with analog and digital voltage lower by 10% than the nominal and temperature of -40°C . Simulated DAC operation at 10% higher than the nominal voltage levels and higher temperature ($+125^\circ\text{C}$) was only slightly worse than in nominal conditions. Fig. 8 shows the compact DAC layout with an area of 2.9 mm^2 including the $100\text{-}\mu\text{m}$ wide guard-band.

IV. CONCLUSION

In this brief, we demonstrated that using a cost-oriented approach to DAC design results in a very compact macrocell layout. In this approach, systematic errors are less severe than in the traditional design approach based on maximizing the INL yield. A unique algorithm was developed to produce an optimized, layout dependent switching sequence. The smaller size and minimization of systematic errors resulted in a higher yield for SOCs that integrate this DAC macrocell.

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Stable High-Order Delta-Sigma Digital-to-Analog Converters

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Abstract—Stability analysis of high-order delta-sigma loops is a challenge. In this brief, a sufficient design criterion is presented for high-order multibit error-feedback digital-to-analog converters (DACs) which are especially suitable for high-speed operation. This analytical criterion might be too conservative, but it allows for the design of stable, robust, and high-resolution delta-sigma DACs. Both analytical and numerical analysis are performed for verification. Also, experimental results of a discrete-component multiplier-free prototype demonstrate 10-b operation at a very low oversampling ratio of 4.

Index Terms—Digital-to-analog converter (DAC), data conversion, delta-sigma, error feedback, high order, high speed, sigma-delta, stability, stable.

I. HIGH-ORDER DELTA-SIGMA MODULATORS

Since a delta-sigma ($\Delta\Sigma$) modulator uses oversampling and quantization error shaping, it trades speed for resolution, and analog-circuit accuracy for digital-circuit complexity. A possible way to obtain a high-resolution and high-speed delta-sigma analog-to-digital

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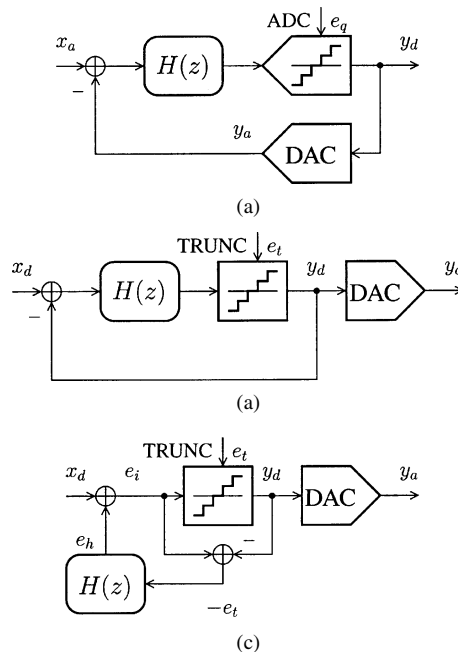


Fig. 1. Single-loop delta-sigma modulator topologies: (a) output-feedback ADC, (b) output-feedback DAC, and (c) error-feedback DAC.

converter (ADC) or digital-to-analog converter (DAC) is to use a high-order or/and multibit modulator. High-order quantization error shaping can be achieved by either single-loop or multiloop (i.e., cascaded or MASH) architectures [1].

The choice of the quantization error or quantization noise transfer function (NTF) plays a significant role in the achievable performance of the modulator. While the in-band attenuation of the NTF is provided by its zeros, the out-of-band gain (OBG) of the NTF is controlled by its poles. Reducing the OBG improves the loop's stability, but it increases the in-band noise, thus deteriorating the signal-to-noise ratio (SNR) of the modulator. For high-order loops (i.e., larger than one), it is possible to gain more performance by moving out the zeros of the NTF from dc, and arranging them in the signal band to provide maximal noise suppression for a given oversampling ratio (OSR) [2]. Also, high-order modulators are prone to become unstable for large input signals [1, chs. 4–5].

Due to the presence of a nonlinear truncator or quantizer¹ in the system, the stability analysis of high-order loops (i.e., larger than two) is a challenge. "Unstable" means that the modulator exhibits large, although not necessarily unbounded, states and a poor SNR compared to those predicted by linear models [1, Sec. 4.1]. Many excellent papers deal with the issue of stability, e.g., [1]–[11].

The chain of integrators or accumulators with feedback or feed-forward summation are popular topologies for delta-sigma ADCs [Fig. 1(a)] and DACs [Fig. 1(b)], respectively. Let us refer to these as *output-feedback* (OF) modulators. To ensure stability, a conservative empirical rule of Lee [4] or/and the root-locus method [5] along with extensive simulations must be used. Lee's rule applies for single-bit modulators and it requires an OBG of the NTF of less than 1.5. Several functional ICs [12], [13] demonstrate that using Lee's rule yields to stable modulators. For multibit high-order designs, a more relaxed value, e.g., of 3.5 [14], is sufficient for stability. In any case, while this requirement empirically ensures stability, it drastically limits

¹"Quantizers" and "truncators," and "integrators" and "accumulators" are used in delta-sigma ADCs and DACs, respectively.