Transparent Optical Packet Switching: Network Architecture and Demonstrators in the KEOPS Project

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Abstract— This paper reviews the work carried out in the ACTS KEOPS (Keys to Optical Packet Switching) project, describing the results obtained to date. The main objective of the project is the definition, development, and assessment of optical packet switching and routing networks, capable of providing transparency to the payload bit rate, using optical packets of fixed duration and low bit rate headers in order to enable easier processing at the network/node interfaces. The feasibility of the KEOPS concept is assessed by modeling, laboratory experiments, and testbed implementation of optical packet switching nodes and network/node interfacing blocks, including a fully equipped demonstrator. The demonstration relies on advanced optoelectronic components, developed within the project, which are briefly described.

Index Terms—Asynchronous transfer mode (ATM), frequency conversion, internet, optical fiber communication, optical fiber delay lines, packet switching, photonic switching systems, semiconductor optical amplifiers (SOA's), space division switching, synchronization, traffic control (communication), wavelength division multiplexing (WDM).

I. INTRODUCTION

TELECOMMUNICATION traffic is expected to grow dramatically in the next years, as a consequence of the offer of new diffusive and interactive services [1]. The range of future services is very diverse in terms of required channel capacity (i.e., bit rate), channel occupancy (continuous or bursty), connection duration, connection set up time, and frequency. This evolution calls for high-capacity networks and nodes, allowing dynamic bandwidth sharing between different types of users in a flexible and efficient way. Although, today, routing and switching of data streams are performed electrically, restricting optics to transmission-only optical networks exploiting wavelength division multiplexing (WDM) techniques, will be implemented [2] with optical cross-connects (OXC's) and/or optical add–drop multiplexers (OADM's).

The advantages of WDM transparent networking can be merged with the flexibility afforded by the packet transfer mode, benefiting from its capacity to provide simultaneous traffic flows. The network considered is a high-capacity path-routed network which, in the longer term, could evolve into a fully switched network, making virtual circuits available on demand to the users once the need for such high speed services on a per-call basis is present.

The routing of packets on the basis of the virtual path address read from the packet header will be achieved by means of optical packet switches. The space and wavelength domains are used to achieve connections between one inlet and one outlet [3]–[5].

Several major issues must be specifically addressed, however, in order to assess their fundamental feasibility:

- Proper wavelength resource management and the dynamic time sharing utilized by packet networking;
- Contention resolution in the absence of viable random access optical memories;
- The synchronization interfacing functions for packet phase alignment at switch inlets.

Within this context, the ACTS (advanced communications technologies and services)[1] KEOPS (keys to optical packet switching) project addresses the analysis and demonstration of bit rate optical transparent packet (OTP) switching within all-optical network architectures, by means of network and system studies and laboratory demonstrators based on components developed in the project. Partners contributing to the KEOPS project are: Alcatel Alsthom Recherche, France Telecom-

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CNET, CSELT, the Technical University of Denmark, Alcatel CIT, Alcatel SEL, the University of Bologna, ETH-Zurich, and the University of Strathclyde. Progress on network and system issues, system demonstrators, and components, realized since the start of the project in September 1995, is reported in this paper, which is structured as follows.

Section II reviews the basic network concepts adopted within the project. It starts with the network evolutionary model, which describes how optical packet networking is likely to emerge and will interact with other networks, whether they are electronic or photonic. Then the optical packet format is discussed. The access interface to the optical packet network, with some performance evaluation, node design issues, the node/network interfaces, and synchronization issues, is discussed in Section III. Section IV reports on demonstration related activities, including the description of the packet switching nodes (structure, traffic performance, and experimental results), packet synchronization interfaces, and the high-speed assessment of optoelectronic components. Section V summarizes the effort dedicated to the development of enabling technologies required not only for the demonstrator work, but also for the requirements of optical transport networks [6].

II. NETWORK CONCEPTS FOR OPTICAL TRANSPARENT PACKET SWITCHING

A. Network Reference Structure

This paragraph describes a design framework for the OTP network layer for the purpose of demonstrating the functionalities required for interworking with present and future networks, such as optical WDM transport networks, ATM and internet protocol (IP).

A protocol reference model has been designed which takes into account the concepts of bit rate transparency and WDM. Three main layers are considered (Fig. 1).

- *High Layers*: Users of the OTP layer are likely to be in the short-term existing standard networks, such as ATM, IP, and local area networks (LAN's), so that all aggregate customers, even if they are end-users, such as workstations or video servers, can be foreseen as future clients of the OTP layer.
- *OTP Layer*: It provides service-dependent functions to the upper layer and is, in turn, subdivided into three sublayers whose functions are the following.
  — The upper optical sublayer (UOS) adapts the higher layer data flow to that of the optical packet layer.
  — The network optical sublayer (NOS) carries out transparent packet routing functionalities, including header generation and updating, packet switching, and scheduling.
  — The lower optical sublayer (LOS) generates the optical packet data flow according to the optical packet format and transmits it on the optical link, hence supporting the multiplexing-demultiplexing functionalities (optical idle packets are inserted to adapt the packet flow between the UOS and the LOS prior to multiplexing). As the OTP layer makes use
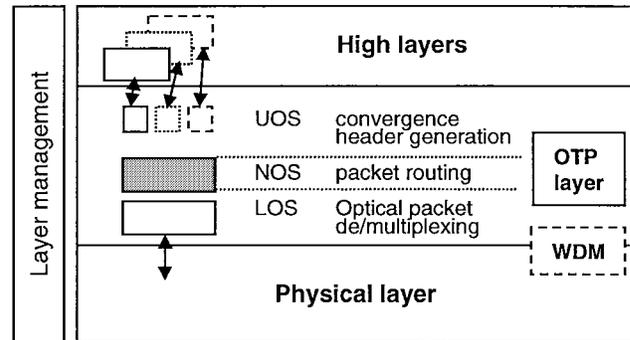

Fig. 1. Reference model for an OTP.

of the wavelength domain for switching purposes, and possibly for contention resolution, wavelength shifting is mandatory at the interface to adapt the wavelength allocation to the WDM transmission layer requirements.

- *Transmission Layer:* This is responsible for transparent bit transport on wavelength channels. This layer is supposed to be based on optical fibers working in WDM. It provides the upper layer with transparent lightpaths built on a steady (or reconfigurable on a long time scale) concatenation of wavelength channels.

B. Transparent Optical Packet Format

The optical packets used in the OTP layer are placed into a fixed duration time slot, allowing for a synchronous operation of the switching nodes and fiber-delay line packet buffering. These packets contain a 622 Mbit/s header (which is electronically processed in the nodes) and a payload with fixed duration and variable bit rate (e.g., up to 10 Gbit/s). The term transparent optical packet arises from this latter characteristic, which provides a flexible bit rate evolution, according to the needs of each OTP layer user. Finally, guard times must be inserted to account for the optoelectronic device switching time, the jitter experienced by the payload in the nodes (mainly in the fiber delay lines), and the finite resolution of the synchronization units at the network/node interfaces (synchronization issues will be discussed in Section III-D).

The key elements in defining an OTP format are, then, the time slot and payload duration. To this end, issues such as packetization efficiency, maximum fiber delay line length, and performance of the interworking unit (IWU) must be analyzed (Section III-A). The first results [7] indicate that the best trade-off is reached for a time slot duration between 1.5 and 3 μs. A possible packet format was proposed in the first year of the KEOPS project. It is based on a 1.646-μs time slot (e.g., 128 bytes @ 622 Mb/s) with an overall guard time of 12 bytes (Fig. 2). The packetization efficiency is, then, slightly lower than 80%.

III. NETWORK FUNCTIONAL SUBBLOCKS

A. Access Interface (IWU)

At the moment, the operational principles of the IWU between high layers and the OTP layer are a major focus of the

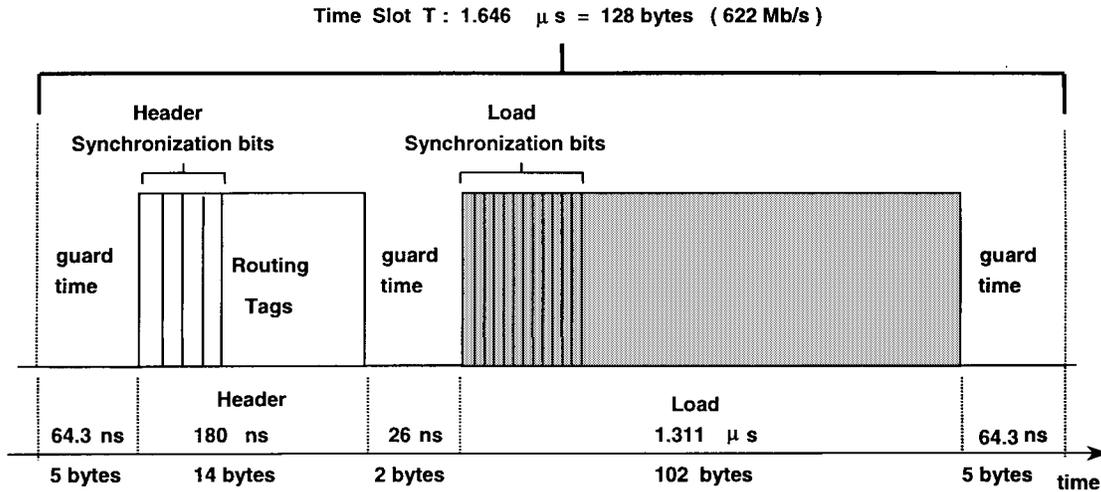Time Slot T : 1.646 μs = 128 bytes (622 Mb/s)

Fig. 2.   Example of the OTP format proposed by KEOPS.

project [8], [9]. This unit adapts the flow of user information so as to allow for the generation of optical packets, relying on electronic storage of the incoming bits.

The main assumption is that at the optical network boundaries, the peak bit rate of the incoming (electrical) bit stream is lower than that of the optical output link (no traffic concentration is performed at the IWU).

The proposed functional implementation for the IWU works as follows:

- incoming information on a link from the electrical layer is stored in the electronic memory of the corresponding UOS;
- when enough information to fill an optical packet is available, or a preset maximum waiting time is reached, the UOS creates the OTP (also generating the related header) and sends it to the LOS;
- the OTP's are then queued (still in electronics) in the LOS and transmitted on the optical link, according to a first-come-first served policy.

The issues considered in assessing the performance of such an IWU are: access delay; traffic shaping; and optical link utilization. Since no traffic concentration is made, packet loss does not occur and therefore packet loss probability is not considered. The following is a brief discussion of these various issues.

The first issue is the access delay, which plays an important role in determining the end-to-end network performance. The access delay δ is made up of two parts:

1) p packetization delay in the UOS, necessary to gather an amount of information on one input link to fill up an optical packet;
2) q queuing delay in the LOS, where the packet flows from several UOS's are multiplexed.

In principle, p is not bounded since it depends on the arrival rate from the source. For instance, in the case of a source with a low average bit rate, a very long time would be necessary to fill an optical packet. To avoid this event a threshold W is set and when $p > W$ a packet is sent, even if it is not full. In principle, this policy can result in a waste of network

TABLE I
QUEING DELAY (q) FOR THREE VALUES OF THE OUTPUT LINK SPEED ASSUMING THAT ALL THE INPUT LINKS ARE EQUAL, WITH SPEED 155.52 Mbit/s AND THAT $T = \mu s$

Output Speed (Gbit/s)	q (μs)
2.488	42
10	156
40	620

resources. Simulation studies [8] have shown that W can be quite small, with an almost negligible effect on network utilization (for instance $W = 0.5$ ms leads to waste of less than 1% of the available bandwidth in the case of 155-Mbit/s links, multiplexed on a 2.488-Gbit/s optical link).

With regard to q, if N is the number of UOS's multiplexed on one LOS, and T is the time length of the optical packet, then the following bound holds:

$$q \leq q_M = (N + 1)T.$$

The worst case for the queuing delay is when all the UOS's have an OTP to send at the same time (note that, in the assumption of no concentration, when this happens no OTP's may be waiting to be transmitted in the LOS). The final information in the last packet will wait NT to be transmitted. An additional packet time T must be added to take into account the discrete time nature of the system (packets transmitted in one slot must arrive in the previous slot). As an example, some values of q_M, as a function of the output link speed, are reported in Table I. Of course q_M increases with the output to input speed ratio (i.e., greater N), but the absolute values are always in the order of magnitude of a fraction of millisecond.

In conclusion, δ is bounded as follows:

$$\delta < \delta_M = (N + 1)T + W$$

and the results obtained up to now suggest that, in the worst cases, δ_M can be less than a few milliseconds.

Finally, significant results have been obtained, even with regard to traffic reshaping. Due to its multiplexing function, the optical packet stream generated at the IWU is, in general,
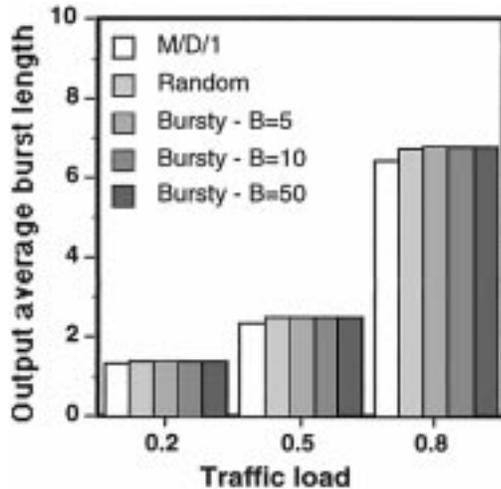
Fig. 3. Average burst length of the output traffic (output from an M/D/1 system, random and bursty, with increasing burstiness) from the IWU for various traffic types for $T = 2.8$ ms and 14 input links at 155.52 Mbit/s, multiplexed on an output link at 2.488 Gbit/s.

Fig. 4. Generic structure of an all-optical packet switching node.

less bursty than the incoming electronic traffic. For instance, in Fig. 3, the average burst length at the output of the IWU is shown for various traffic types. It happens that the output traffic has an almost constant behavior, regardless of the input traffic.

B. Switching Node

An all-optical packet switching node generally will not be restricted to a simple switching matrix. As described in Fig. 4, a generic structure of such a node could composed of at least three main blocks.

- The first block integrates an input synchronization block for performing phase alignment of the incoming packets. In order to realize this function, a delineation phase of the payloads is added. Header detection is needed at this stage in order to operate in a synchronous way. In order to minimize the number of packet synchronizers within the network, it would be interesting to use WDM structures for the major part of the nodes and to alternate with single channel structures, when required, in order to suppress the jitter between the header and the payload.
- The second block is the switching matrix itself, the role of which is to achieve routing and to solve contention in real time [10]. An electronic control must be implemented for the control of the key devices. The routing process is managed by accessing routing tables stored in electronic memories. Some additional functions could be implemented. In particular, by taking advantage of the presence of drivers for the switching elements, it would be convenient to erase the header of each packet. In addition, the empty payload management could be advantageously done in the packet switching matrix itself.
- The third block is a regenerative interface. Extinction ratio (ER) degradation, degradation of the optical signal-to-noise ratio (SNR), power variations between packets, jitter accumulation, and bit duration reduction are some of the impairments that may affect any signal crossing an
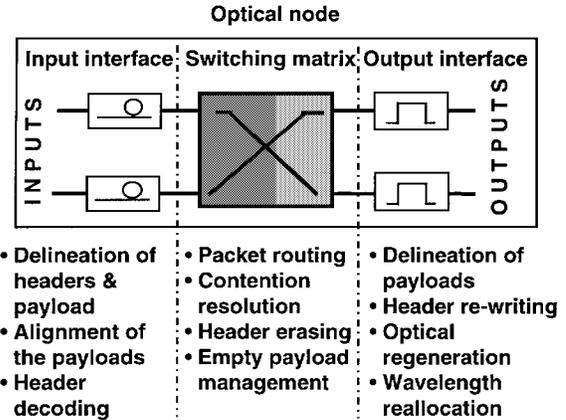
optical node, so that a regeneration of the data streams may be required. The structure will depend on the network size: for example, a 3R regenerative structure could be needed to suppress the jitter accumulation at the bit level. Then payload delineation must be implemented in order to be able to rephase the arrival of payload in an asynchronous mode.

C. Network and Node Synchronization

Due to the synchronous operation of the switching nodes (on a time slot basis equal to the packet length), packets must arrive within the same phase at the node inputs. This function is performed through the packet streams synchronization interface and requires an exact determination of the time shift between the local reference packet timing and the incoming packets, and its possible recovery. The phase alignment is done in the optical domain, in order to keep the payload transparency, but can be electrically controlled through the evaluation of the packet phase at the node input by decoding, after O/E conversion, the header packet start pattern.

In principle, the simplest way to cope with this problem is to arrange all fiber spans interconnecting nodes to be equal to a multiple of the packet length (duration). In practice, this may not be a very realistic situation, especially in a public network environment. Furthermore, fiber chromatic dispersion and temperature-induced path variations have to be considered, together with packet-to-packet jitter caused by the use of different wavelengths for packet routing and buffering internally to the node.

Packet synchronization schemes, operating transparently with respect to the packet bit rate and format on each node input link, have been studied and experimented [11], [12]. These synchronization units can be of different types, depending on their speed and time resolution. In the context of a general all-optical packet network, a coarse/slow synchronization unit is necessary at each incoming link of a node (once wavelength demultiplexing has been performed), in order to compensate for the static phase differences (due to the link length and to the wavelength used) and for the phase wander (due to the temperature). Each of these units is followed by a fast and fine synchronization unit, which compensates the packet-by-packet

time variations (jitter), due to use of different wavelengths for the routing and buffering processes in the previous nodes.

The node reference control signals are supposed to be derived from a clock distribution network, which could be dedicated or derived from an existing one, i.e., the synchronization network of the synchronous digital hierarchy (SDH). In the case of a plesiochronous network, the difference in clock frequencies between the nodes could cause failures in the synchronization process and, consequently, packet loss. This can be controlled by using the empty packets to recover the right phase. The proposed synchronization schemes are consistent with the clock accuracy normally used in the plesiochronous networks (e.g., $\Delta F/F_0 = 10^{-3}$) allowing a packet loss probability below 10^{-12} for a traffic load $L = 0.8$.

IV. DEMONSTRATION ACTIVITIES

The experimental implementation and assessment of system architectures in the KEOPS project is done through one demonstrator and several testbeds, adopting advanced optoelectronic devices developed within the project (described in Section V). The main objective is the feasibility demonstration of switching and interfacing blocks, including their scalability to real system dimensions in terms of size, transparency to the bit rate, and cascadability. In this section, a short review of the node architectures developed in KEOPS and their performance is reported, as well as some experimental results obtained on the wavelength-routing switch (WRS) node demonstrator (which is the main KEOPS demonstrator), the broadcast and select switch testbed, the packet synchronizer testbed, and the ultra high-speed assessment of optoelectronic components.

A. Wavelength Routing Switch

1) Basic Principles and Architecture: The WRS demonstrator (Fig. 5) relies upon the use of dynamic wavelength conversion at the packet level to perform the routing of packets from each inlet to their destination outlet. A wavelength converter, together with a demultiplexer performs a $1 \times N$ spatial routing switch, N being equal to the size of the wavelength comb. Packets from different inlets may compete at a given time slot for the same output. In the WRS, this contention problem is solved by the use of a buffer delay line memory. The structure and dimensioning of this buffer memory are of prime importance to the performance of the switch, in terms of packet loss probability. The buffer memory used in the WRS is very effective for medium and large dimension switches and compatible with standard packet loss performances of electronic switches [13]. Signal degradation within the switch is kept as low as possible, since only two wavelengths conversions are required. Moreover, due to their regenerative action, the use of interferometric wavelength converters in the second stage improves the overall performance.

The switch works on a time slot basis, therefore the input packets should be aligned within the local time slot within a few bytes' accuracy. Alignment at the bit level is not required since the 622-Mbit/s header can be recovered on the fly, thanks to the synchronization patterns at the header beginning.
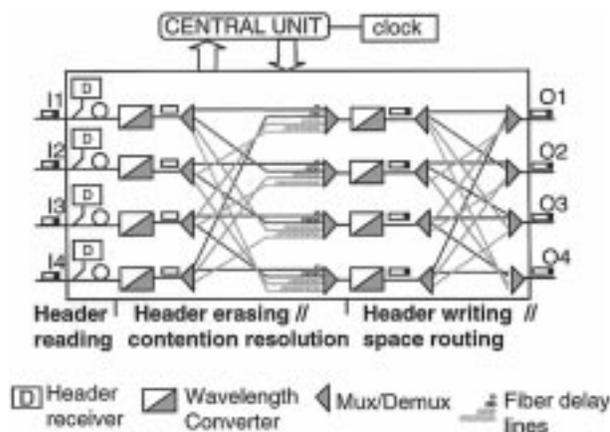

Fig. 5. Architecture of the WRS.

The switch is under the control of an electronic unit, which drives the probe lasers and semiconductor optical amplifiers (SOA's) of the wavelength converters. At a given time slot, these driving signals are a function of the incoming packet headers and of the optical buffer memory occupancy, which is monitored in the electronic control.

The packets are routed through two successive wavelength conversion stages. At the first stage, incoming packets are routed to one position of the buffer delay line memory. In the second stage, they are routed to their destination output. The routing and buffering algorithm minimizes the delay in the switch, taking into account the following constraints: two packets cannot be routed to the same output at a given time slot, and the sequence integrity must be preserved for any connection.

Headers also are updated in the switch in a two-stage process. In the first stage, headers are erased by switching off the SOA used for wavelength conversion and in the second stage, a new header is rewritten at a time position chosen in order to keep the payload to header time distance roughly constant, due to a payload position measurement at the switch input.

2) Teletraffic Performance: In the WRS architecture, packet scheduling for first-in-first-out (FIFO) output buffer emulation is achieved by providing access, for each input port, to a small set of optical delay lines with nonconsecutive delays [13]. By taking advantage of the statistical multiplexing on a tagged output buffer of the delay accesses that are available to the switch inlets [14], this scheme allows the emulation of rather large buffers.

Two kinds of WRS architectures for WDM packet networks have been evaluated, based on how the wavelength resources are managed.

If the principle of wavelength circuit set up per connection is followed, packets belonging to a given connection cannot be spread over more than one wavelength of the same fiber. Hence, switching nodes are provided with one queuing system per outlet, toward an outgoing channel. Relying in part on statistical multiplexing for packet scheduling, the WRS architecture has good scalability and allows the implementation of large switches, while keeping the wavelength set required for
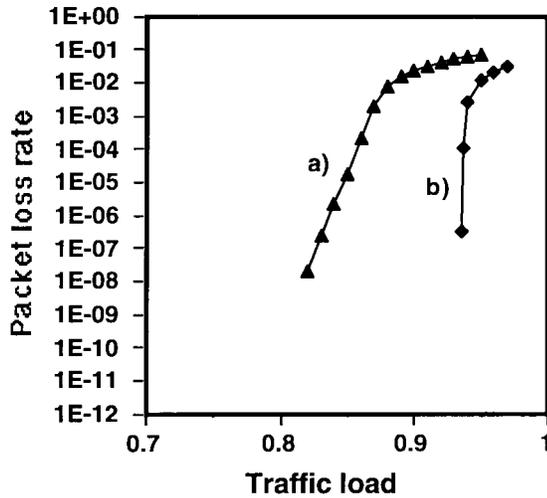
Fig. 6.   Packet loss rate versus Bernoulli traffic load for a) a 64 × 64 WRS (a 32-wavelength set is required) and b) for a four-fiber × four-fiber WRS, interconnecting 16-wavelength WDM links (queue length < 15 packets).

Fig. 7.   Header synchronization. The data out curve refers to the signal after synchronization, synchronization failures occur for BER > 10^{-4}.

their proper operation low enough to be practical [curve a) in Fig. 6].

If dynamic sharing of the whole optical bandwidth is carried out, due to dynamic wavelength allocation at the packet level, queuing packets contend only for their output fiber. Dynamic allocation of wavelengths allows address conflicts to be resolved, in the context of bursty traffic, without implementing large buffers. The implementation of the flow control functions may take advantage of small optical buffers in order to alleviate the transfer delay and packet delay variation issues, which are crucial for real time services (curve b) in Fig. 6).

3) Experimental Results: The WRS is the main KEOPS demonstrator and is being implemented as a fully equipped 4 × 4 switching node, including also header processing and all electronic control functions [15]. At present, experimental results are available for a one-stage 4 × 4 switch, using cross-gain modulation (XGM) wavelength converters. The header and the payload are at 622 Mbit/s and 2.5 Gbit/s, respectively, and the four wavelengths comb ranges from 1534–1546 nm.

The robustness of the header recovery has first been checked under a poor SNR at the header photodetector input (Fig. 7). Synchronization failure occurs only when the bit error rate (BER) on the header is higher than 10^{-4}, under such conditions the BER on the 2.5-Gbit/s payload is much higher and the header detection process cannot be considered as the main cause of failure [15].

The overall performance of this initial demonstrator has been characterized in terms of the BER penalty in comparison with the back-to-back configuration. All 16 optical paths were tested, with input packets on the four possible input wavelengths, and in each case the penalty was lower than 1.5 dB (Fig. 8).

B. Broadcast-and-Select (BS) Switching Matrix

1) Architecture: The BS packet switching matrix architecture [16], shown in Fig. 9, relies on the use of wavelength encoding and fast wavelength selection in order to achieve
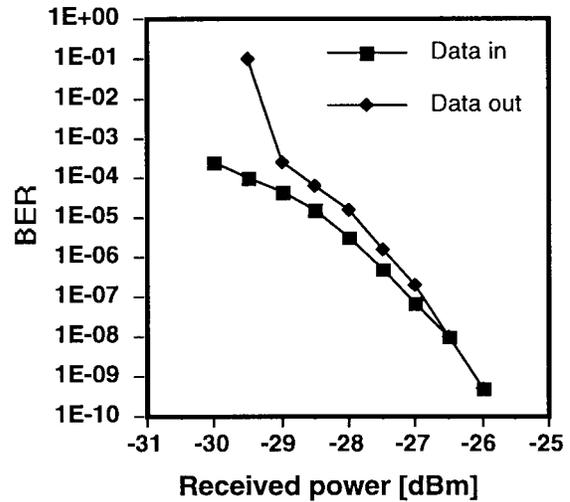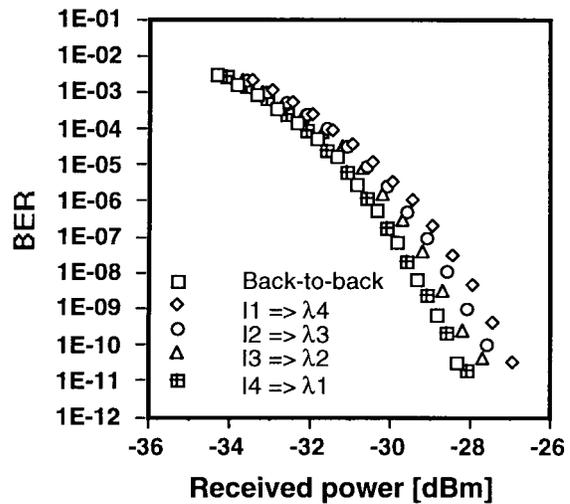
Fig. 8.   BER penalty through the WRS switch (output 4). The four output curves are related to a signal routed from the four different inputs (four different wavelength conversions).
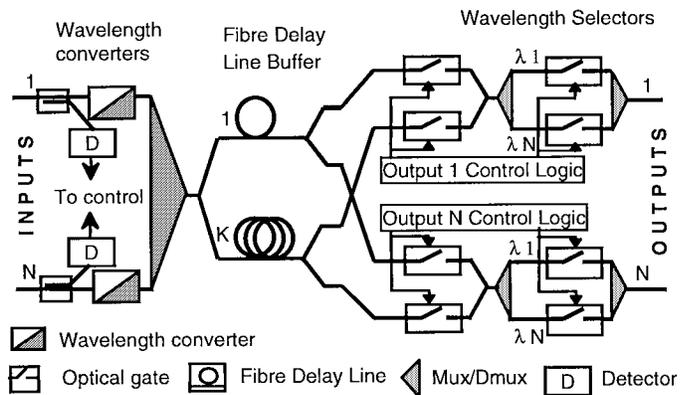
Fig. 9.   Architecture of the BS packet switch.

packet routing and on the exploitation of optical fiber delay lines accessed through fast optical gates, to perform packet buffering and time-switching. The principle of operation is
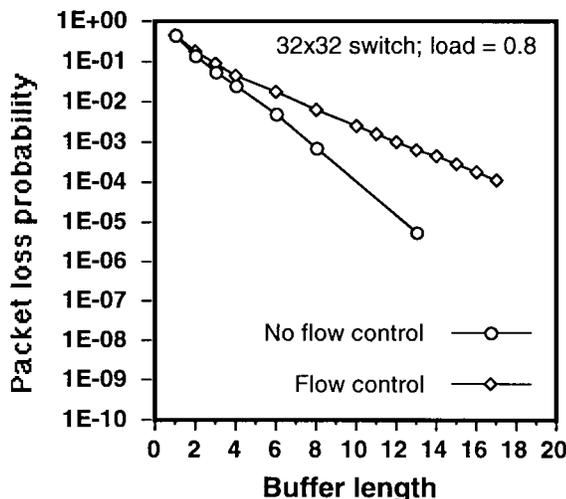
Fig. 10. Packet loss probability for a 32 × 32-BS switch built with 8 × 16 and 16 × 16 switching elements, loaded with uniform traffic (traffic load 0.8), both with and without the introduction of interstage flow control.

Fig. 11. BER performance at 10 Gbit/s in a switching regime (guard band is 1.8 ns).

depicted below. Each incoming packet is assigned one wavelength, identifying its input port, and then fed into the fiber delay line (FDL) buffer. All packets are broadcast to all delay lines and thus made available during K consecutive time slots. The buffer gates select one time slot, corresponding to the appropriate delay as determined from actual traffic conditions at the input. Finally, the wavelength selector only discriminates as to one outgoing packet/cell at a time, on the basis of its wavelength, i.e., its input address.

2) Teletraffic Performance: The BS switch achieves pure output queuing and its performance can be obtained by classical analysis [17]. Multistage configurations are used to build large switches, because a large monolithic switching matrix is not feasible with current technology [16]. For this reason, the performance of multistage switches, realized by adopting a three-stage Clos architecture, has been studied. Different architectural options and functions have been investigated: in particular, interstage flow control techniques have been shown to be effective in reducing packet loss, with the limited buffer amount available with present technology (typically about 32 packet positions). Due to the discrete-time nature of the switch, when a buffer at stage i is full, only one packet can be accepted from stage $i-1$, chosen from among those in contention, according to a defined policy. The flow control technique is realized by sending a signal backward from stage i to stage $i-1$, in order to stop all but the incoming packet directed to the full buffer. To minimize the overall packet loss probability, the packet that has been waiting for the longest time in the FDL's at stage $i-1$ is chosen [18].

The benefit of such a flow control policy is shown in Fig. 10. A packet loss probability of 10^{-10} is reached, with something more than 20 packet places per buffer, that is well below the technological limit. It is worth noting that, without flow control, larger buffers would be required.

An in-depth investigation into the case of multicast and broadcast traffic has been also performed. The main result obtained is that performance with point-to-multipoint traffic
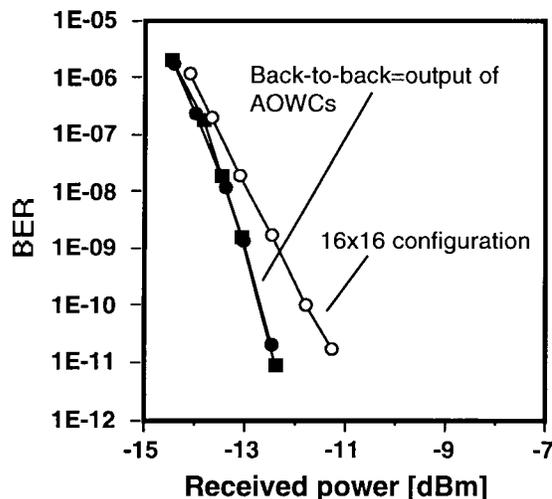
does not differ significantly from the case of point-to-point traffic, with the same traffic load on switch output. Therefore, it is possible to say that the result in Fig. 10 can be considered significant for multicast traffic as well.

3) Experimental Results: A switch laboratory testbed has been designed and sufficiently equipped to assess the feasibility of a 16 × 16 switching matrix, operating at 2.5 and 10 Gbit/s [19]. The switching module is mainly composed of the following blocks:

- a wavelength conversion block, equipped with two XGM SOA wavelength converters emitting, respectively, at $\lambda_1 = 1547.8$ nm and $\lambda_2 = 1549.5$ nm;
- a time-switching block, representative of a 16-position buffer, using couplers, attenuators, two FDL's, and two clamped-gain (CG) SOA gates, well-suited for multiwavelength operation;
- a wavelength selector, made by assembling one input optical demultiplexer, two CG-SOA gates and an output optical multiplexer.

Finally, 14 additional modulated lasers, ranging from 1535–1559 nm feed the time-switching block, in order to simulate the operation of a complete 16 × 16 switching module.

Key system results have been obtained such as:

- a very low sensitivity penalty, respectively, at 2.5 and 10 Gbit/s for a matrix size of 16 × 16 input/output ports with a 16-position buffer due, in particular, to the use of CG amplifier gates;
- no major degradation of the system performance in a real 16-channel WDM regime, due to a relatively constant behavior of the optical amplifiers in the 1535–1559 nm range.

BER curves were successively recorded at 2.5 and 10 Gbit/s under both transmission and switching regimes. Fig. 11 shows BER characteristics at 10 Gbit/s per input in a 2 × 1 switching regime with the additional 14 WDM channels. Less than 1 dB sensitivity penalty at 10^{-9} BER was recorded with guardbands between consecutive packets as low as 1.8 ns. This result
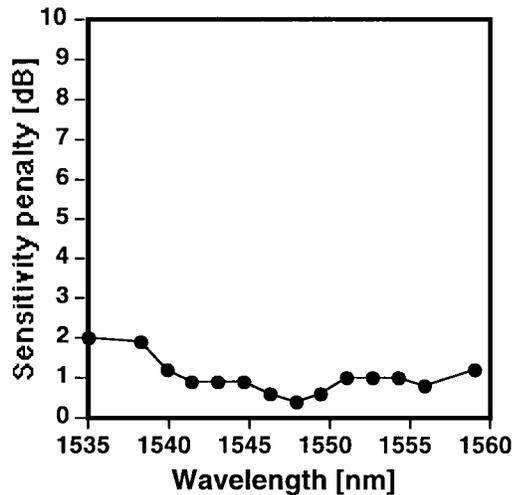
Fig. 12. Evolution of the detection sensitivity at 10 Gbit/s in the spectral range of 1535–1559 nm.
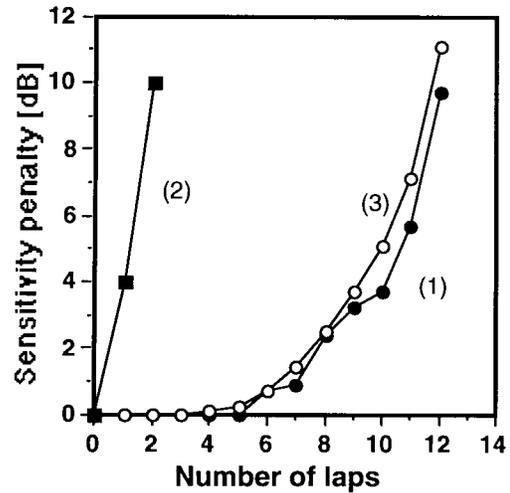

Fig. 13. Evolution of the sensitivity penalty versus the number of laps through: (1) the regenerative interface; (2) network section without interface; and (3) network section with interface.

shows that, with respect to pure transmission through the matrix, switching can be performed without any additional degradation of the sensitivity.

Fig. 12 shows the sensitivity penalty at 10 Gbit/s as a function of the input channel wavelength. As shown by the curve, it has been possible to fully operate the switch over the 24-nm bandwidth without any major degradation of the sensitivity. From 1535 to 1559 nm, which correspond to 16 channels with a 200-GHz channel spacing, the penalty variation is lower than 2 dB due, in particular, to the gain flatness of both the SOA's and the fluoride-fiber erbium-doped fiber amplifiers (EDFA's).

The combination of two all-optical wavelength converters can act as a regenerative interface performing, in addition to wavelength conversion, the extra functionalities required for packet-switching applications, such as suppression of the packet-to-packet power fluctuations and some form of regeneration, thereby enabling the cascade of all-optical packet-switching nodes.

The regenerative interface used basically consists of the combination of two wavelength converters (WC's), the first, an XGM SOA and the second, based on cross-phase modulation (XPM) of such an amplifier in a Mach–Zehnder interferometric (MZI) structure [20]. Basically, the role of the first WC is to convert fast power fluctuations between consecutive packets into ER variations, in order to enhance the signal-to-amplified spontaneous emission (ASE) ratio and to provide the second WC with a predetermined input wavelength and a constant input power. The second converter is, in turn, mainly used to regenerate the ER, due to its nonlinear interferometric transfer function, and to provide the output wavelength.

The regenerative interface and a subequipped testbed of the switching matrix were successfully tested in the recirculation loop.

Each path in the loop can be seen as the propagation, through a network section including a packet-switching node with its regenerative interface, and an amplified transmission link. As shown in Fig. 13, the sensitivity penalty rapidly increases in the absence of any regeneration.
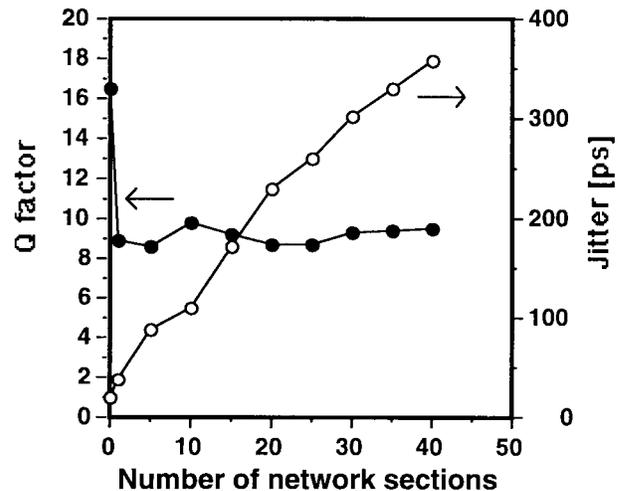
Fig. 14. Evolution of the Q factor and the jitter versus the number of network sections.

The cascade of eight network sections, each consisting of the 16×16 switching matrix, with the above mentioned regenerative interface and 50 km of dispersion-shifted fiber, led to a total penalty of 3 dB (Fig. 13). Preservation of the signal quality in the amplitude domain has been demonstrated in the same system environment through Q factor measurements. Fig. 14 shows that, even after 40 laps, there is neither degradation of the ER, nor degradation of the noise distribution on each symbol. Fig. 13 shows, however, a degradation of the BER performance in the cascade, which is mainly due to a jitter accumulation, as shown in Fig. 14. This effect would actually limit the number of such nodes that could be cascaded to less than ten. For a larger network size, a 3R regenerative structure would be needed.

C. Packet Synchronizer Testbed

As described previously, nodes used in optical packet switching networks operate in a synchronous way, thus requiring packet synchronizers (which have to operate
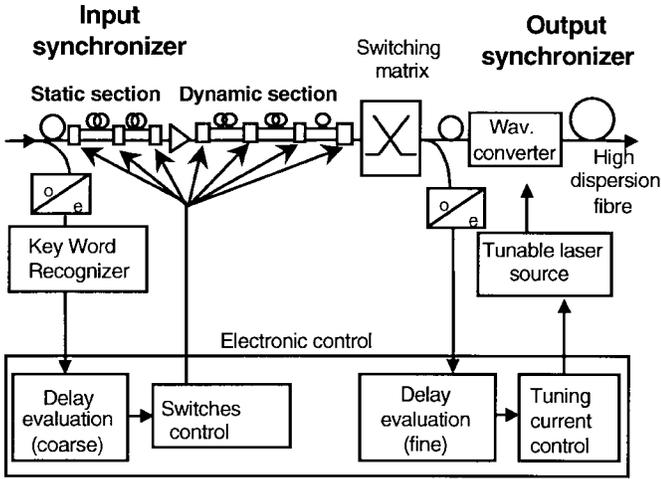
Fig. 15. Packet synchronizer testbed setup.

Fig. 16. Power penalty at 2.5 Gbit/s for the coarse synchronizer.

transparently with respect to incoming packets) at each node input. As the node itself may introduce jitter among packets, a fine synchronizer may also be necessary, at each node output, in order to restore the correct packet cadence, or at the network boundaries to recover the payload.

The input synchronizer is realized using switchable fiber delay lines of different lengths (in decreasing exponential sequence) [21]. The first section acts slowly and recovers only the fixed part of the delay, the second part is set, packet by packet, and recovers the varying part of the misalignment.

The fine synchronizer is realized by means of a tunable wavelength converter and a high dispersion fiber [21]. The electronic control assigns a proper wavelength to the outgoing packet in order to compensate for the jitter of the signal, with the delay accumulated inside the high dispersion fiber.

The testbed (Fig. 15) is designed to operate with up to 2.5-Gbit/s optical packets in a network in which clock distribution is carried out and the time misalignment, due to thermal effect and phase drift clocks, is bounded by a value T_m. The coarse synchronizer is composed of four delay lines set by five 2 × 2 cross-bar thermo-optic switches (static section) and two delay lines, set by two InP cross-bar fast switches and one fast LiNbO$_3$ "Y" switch (dynamic section). The time resolution R_c of the coarse synchronizer is equal to the delay set by the last delay line. Choosing $R_c = 3.2$ ns (two bits at 622 Mb/s), nine delay lines are necessary, in principle, to recover all possible misalignments for one packet. In the KEOPS demonstrator, a 200 ns operation range is experimented on.

The electronic control of the coarse synchronizer is composed of two main blocks: the packet start identifier, which identifies the beginning of the incoming packets through recognition of key words, and the delay evaluation block, which calculates the misalignment between the incoming packet and the local reference, with a 1.6-ns resolution. Fig. 16 shows that a very limited penalty, due mainly to interferometric noise, is introduced by the coarse synchronizer.

In the fine synchronizer, once the misalignment T_0 between packet arrival and internal reference is evaluated, an equalization circuit translates this information into a current for the tuning input of a CW operated DBR laser with a tuning range
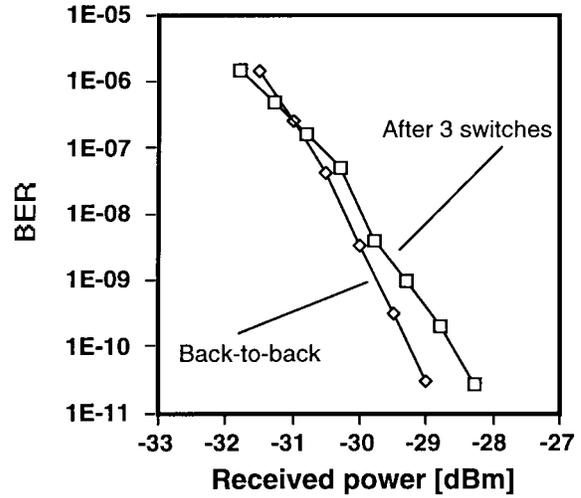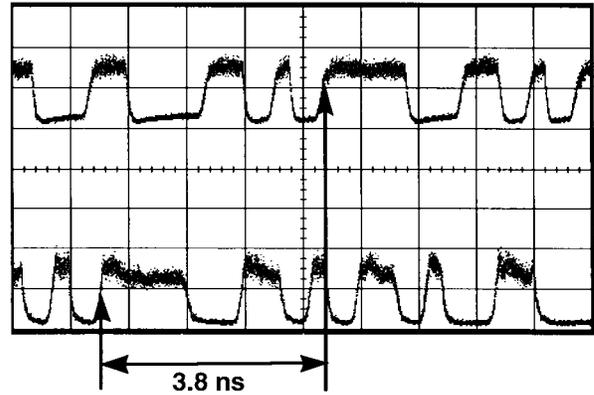

Fig. 17. Data pattern at the output of the fine synchronizer at the extremes of the DBR tuning range.

and tuning step of 15 and 0.6 nm, respectively. The output from the SOA-based wavelength converter is sent to a 4.2 km long high dispersion fiber ($D = 60$ ps/nm · km), resulting in a 3.8-ns delay range with <200 ps resolution. Fig. 17 shows the output data stream at the extremes of the fine synchronizer range, resulting in a 3.8-ns delay between the two traces.

D. High-Speed Assessment Of Components

In KEOPS, special attention has been paid to the assessment of the ultimate performance of components and functions and, in particular, to wavelength converters. High-speed wavelength conversion at 40 Gbit/s has previously been demonstrated [22], exploiting XGM in speed optimized SOA's. However, XGM converters suffer from wavelength dependency, making conversion to longer wavelength difficult. Furthermore, a large chirp results for the converted signals, which limits the transmission on nondispersion-shifted fibers.

XPM interferometric converters, on the other hand, feature high ER's for the converted signals, as well as wavelength independence and, potentially, polarization independence and small chirp. The chirp introduced by XPM conversion even supports transmission over nondispersion-shifted fiber, allowing transmission beyond the dispersion limit [23].
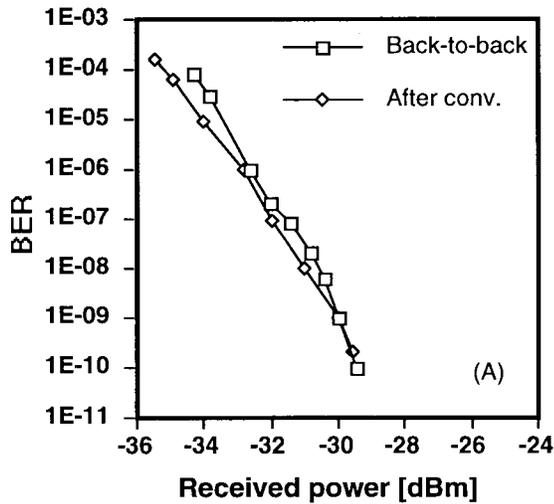
(a)
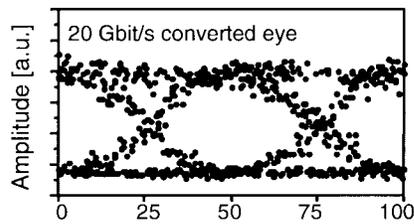
(b)

(c)

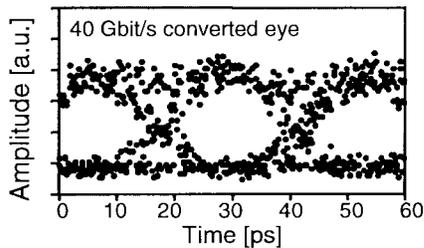Fig. 18. High-speed wavelength conversion using an all-active multiquantum-well MI wavelength converter. (a) BER for 20-Gbit/s conversion from 1555 (input power is 9 dBm) to 1560 nm (input power is 6 dBm). (b) 20-Gbit/s converted eye diagram at 1560 nm. (c) 40-Gbit/s converted eye diagram for conversion from 1558 (input power is 8 dBm) to 1562 nm (input power is 9 dBm).

High-speed XPM converters (>10 Gbit/s) can be obtained by using high-input powers and high-injection currents. Additionally, theoretical and experimental studies have shown that a high optical confinement factor and high differential gain for the SOA's will enable high bit rate operation. As an example, the compact (1.3 mm long) all-active multiquantum-well-based monolithically integrated Michelson interferometer (MI) wavelength converter, described in [24], has demonstrated excellent performance at both 20 and 40 Gbit/s, as shown in Fig. 18. ER's above 10 dB are easily reached at these high bit rates, together with signal-to-ASE ratios exceeding 25 dB (1 nm bandwidth), which is of great importance for the cascadability. This excellent performance is exemplified through the penalty free operation at 20 Gbit/s [Fig. 18(a)], as also illustrated by the converted eye diagram in Fig. 18(b). This speed-optimized MI converter enables high-speed oper-
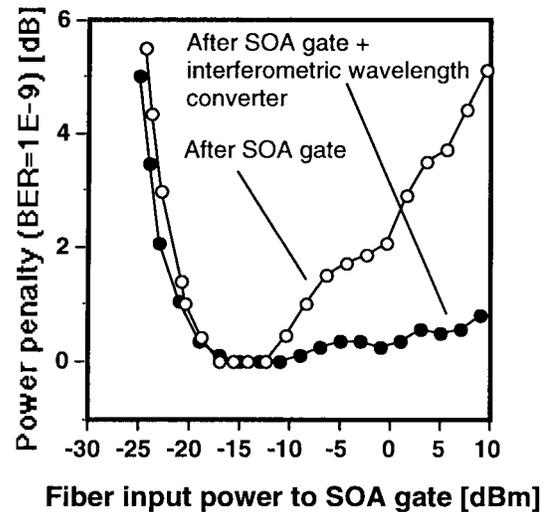

Fig. 19. Power penalty (@BER = 10^{-9}) at 20 Gbit/s as function of the input power (at 1555 nm) to the SOA gate. The curve indicated by (°°°) is measured after the SOA gate, while the curve given by (•••) is measured after the SOA gate and MI wavelength converter that converts the signal to 1560 nm.

ation and even 40 Gbit/s wavelength conversion from short (1558 nm) to longer wavelengths (1562 nm) is possible, as shown by the clear and open converted eye diagram in Fig. 18(c).

The high ER's for the converted signals also enable signal regeneration of distorted signals. This is of importance when using SOA's as gates in the switch nodes, since their cascadability is limited due to noise and, especially, gain saturation. The ER degradation induced by gain saturation at high input power levels can be counteracted by utilizing the ER enhancing capability of the interferometric wavelength converters [25]. The important role of the wavelength converter as a regenerative device is illustrated in Fig. 19, which gives the power penalty (BER = 10^{-9}) for coupling a 20-Gbit/s signal through an SOA gate and for a 20-Gbit/s signal coupled through first, the SOA gate and second, through the MI converter. Without the converter, an input power dynamic range of ~12 dB is found. With the converter, the input power dynamic range is increased by more than 15 dB.

V. Enabling Technology

The essential component-level functionalities required for the optical packet switching architectures, described previously, include tunable all-optical wavelength conversion, fast optical space switching/gating, and wavelength selection. Advanced devices achieving these functions are being developed within the KEOPS project. Similar functionalities are required for WDM routing (cross-connect) applications, as studied within the ACTS optical pan-European network (OPEN) project [6]. The devices developed thus represent a flexible and broadly applicable technology base.

A. All-Optical Wavelength Conversion

The required technologies for tunable wavelength conversion include both multiwavelength laser sources and all-optical
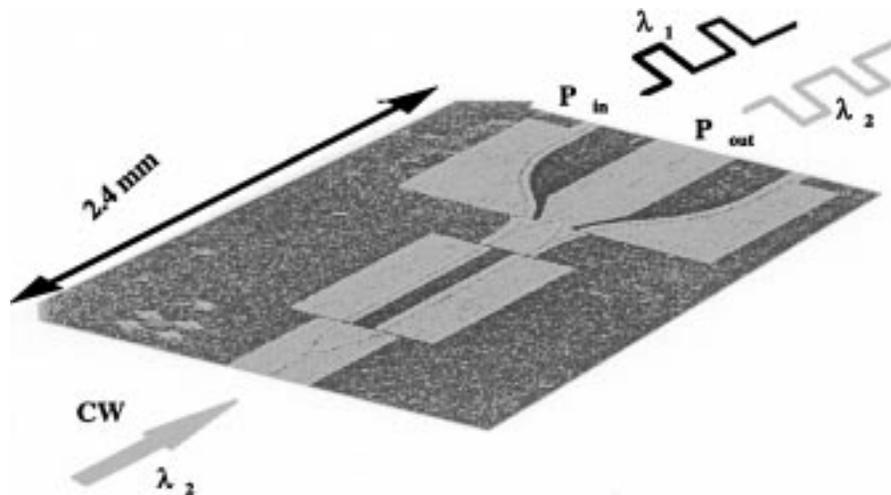
Fig. 20.   SEM photograph of an all-active MZI wavelength converter and operation principle.

wavelength converters. For the WRS, where fast access to a set of pretuned fixed wavelengths is required, a 1×4-DBR laser array, monolithically integrated with a passive waveguide 4×1 combiner section, has been developed. Accurate wavelength spacing ($/pm0.2$ nm) and fast switching times (4 ns), enabled by dedicated GaAs MESFET driver circuitry, have been demonstrated [26]. Tunable Y-lasers [27] and DBR lasers [28] have also been developed for application in the fine synchronizer, where fine tuning over a large wavelength range is required. In particular, the accessibility of 38 regularly spaced wavelength channels, over a 15-nm tuning range, has been demonstrated with two-section DBR lasers [28].

Key requirements for all-optical wavelength converters include bit rate transparency (up to 10 Gbit/s), polarization insensitivity, wavelength up-and-down conversion capability, ER enhancement to enable cascadability, and broad wavelength tunability (1530–1560 nm). Interferometric structures utilizing XPM in SOA's can meet all of these requirements [29]–[31]. In particular, they offer the possibility of strong ER enhancement, together with optical noise squeezing, for both wavelength-up and wavelength-down conversion. The operating principle is illustrated in Fig. 20 for an MZI converter. The amplitude-modulated input signal, coupled into one arm of the MZI, modulates the gain and output phase of the CW probe. This phase modulation is transformed into amplitude modulation by the interferometer. Both in-phase and out-of-phase (input and converted signals) operation are possible. Also, since the input and converted signals counterpropagate in the device, no optical filter is needed to select the converted signal wavelength at the device output, in principle, conversion to the same wavelength is therefore possible.

B. Multiwavelength Space Switches

The principal system requirements for space switching are: polarization independence; low crosstalk; low noise; low fiber-to-fiber insertion losses (or even gain); and compatibility with multiwavelength operation. In addition, optical packet
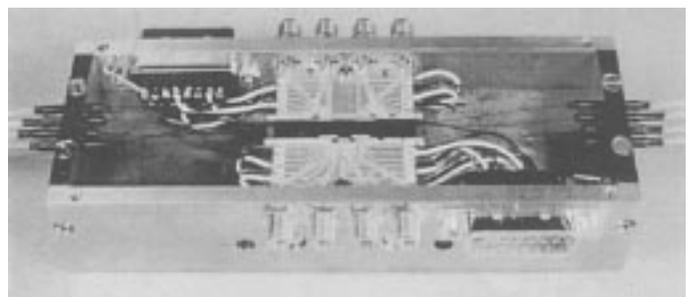

Fig. 21.   Photograph of MZI electro-optic space switch module with driving electronics.

switching requires fast switching, compatible with packet guard times in the ns range. Both electro-optic space switches and CG-SOA gates are attractive potential technologies and both are pursued within the KEOPS project.

Polarization-insensitive InGaAsP/InP switch matrices with four 2×2 Mach–Zehnder electro-optic space switches have been fabricated which, due to the inclusion of integrated optical mode adapters, exhibit fiber-to-fiber insertion losses as low as 5 dB [32]. Fast switching times, below 200 ps, have been achieved using modules incorporating high-speed driver electronics (see Fig. 21). Crosstalk levels of -30 dB were achieved in dilated switching configurations.

Whereas conventional SOA's generate crosstalk in multi-wavelength operation, CG-SOA's exhibit low-penalty operation in the presence of a large number of channels. DBR-based clamped-gain SOA modules with 14-dB fiber-to-fiber gains, gain variations below 1 dB in the 1530–1560 nm range, switching times <1 ns, and polarization sensitivities <0.5 dB have been fabricated [33]. Modules incorporating arrays of four such CG-SOA devices (Fig. 22) have also been fabricated as a preliminary step toward larger scale integration. Excellent uniformity of performance parameters, including gain, polarization independence, noise factor, and saturation power, were achieved on and between array devices and modules, indicating significant potential for this technology.
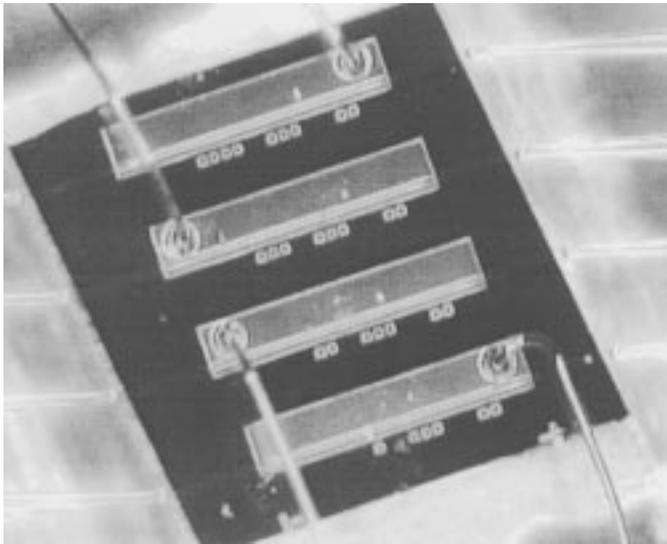
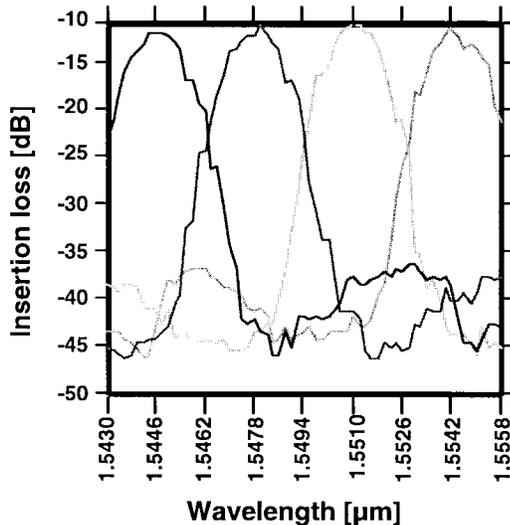Fig. 22.   Photograph of a packaged 4-DBR CG-SOA gate array.

Fig. 23.   Four-channel InP-phased array wavelength demultiplexer.

C. Wavelength Selectors

The wavelength selection function is required, for example, in the BS switch architecture, operating with respect to a fixed set of wavelengths. A straightforward way to realize the selection function is to combine wavelength demultiplexers and optical gates (SOA's). This approach allows convenient digital control, a considerable potential advantage over tunable filter-type components. The wavelength demultiplexer can be realized on SiO_2 or InP, the latter offering potential for future monolithic integration. Within KEOPS, extremely compact polarization-insensitive wavelength demultiplexers have been fabricated on InP with adjacent-channel crosstalk levels as low as -28 dB for four-channel devices (Fig. 23) and -20 dB for 16-channel components [34]. As the signals are demultiplexed before entering the SOA's, conventional SOA's can be used in the selector, provided that the input power dynamic range is sufficient to allow low sensitivities at high bit rates. Using self-aligned flip-chip mounting of SOA gate arrays on silicon

submounts [35], a four-SOA array module has been fabricated within KEOPS, which exhibited fiber-to-fiber gain values of 16 ± 1 dB.

VI. CONCLUSION

Photonic packet switched networks are becoming a viable option for coping with the future requirements of capacity, flexibility, and performance arising from the growth of existing services and the introduction of new ones.

In this paper, the main objectives and achievements of the ACTS KEOPS project have been summarized. The concept of transparent optical packet networks and the issues related to their introduction in the future telecommunication scene have been reported, from network architectures, through the performance evaluation of switching nodes and interfaces and the experimental validation of the concepts, relying on advanced optoelectronic components developed within the project. The work being carried out in the KEOPS project on transparent optical packet switching is providing a complete basis for the establishment of specifications of new classes of optical networks, their transport layers and sublayers, their capabilities for supporting services, and their corresponding requirements as to technology. It is expected that KEOPS will make a major contribution, within the telecommunications community, to the definition of a complete flexible photonic network infrastructure.

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