Digital Signal Processing in Bio-implantable Systems: Design Challenges and Emerging Solutions

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Abstract
Implantable systems that monitor biological signals require increasingly complex digital signal processing (DSP) electronics for real-time in-situ analysis and compression of the recorded signals. While it is well-known that such signal processing hardware needs to be implemented under tight area and power constraints for small footprint and increased battery-life, new design requirements emerge with their increasing complexity. Use of nanoscale technology shows tremendous benefits in implementing these advanced circuits due to dramatic improvement in integration density and power dissipation per operation. However, it also brings in new challenges such as reliability and high leakage power. Besides, programmability of the device and security of the recorded information are desirable features, which need to be considered during the design of such systems. Programmability is important to adapt to individual subjects as well as to the temporal fluctuations in subject condition. On the other hand, information security is rapidly becoming an important design parameter since the recorded signal often needs to be transmitted outside the body through wireless channels. In this paper, we analyze the emerging issues associated with the design of the DSP unit in an implantable system. We note that conventional design solutions may not be attractive for such systems. However, novel algorithm-architecture-circuit co-design solutions, which leverage on the nature of the signal processing algorithms can be effective to realize ultra low-power, robust, programmable and secure hardware for on-chip real-time signal processing in implantable systems.

Keywords
Bio-implantable systems, digital signal processing, neural interface, ultralow power design

1. Introduction
With great advances in electronics and electrode technology, it has become possible to implement implantable systems, which interface with the biological organisms to monitor various biological signals and even manipulate the actions using electrical/chemical stimulation. One of the success stories in the field of biomedical devices is the cardiac pacemaker [1], which has been implanted in countless human beings. With numerous biomedical devices being used for interfacing with different body parts to save or enhance lives of millions, pervasive implantable devices are rapidly becoming a reality. Fig. 1(a) shows some example applications of bio-implantable devices. These devices are increasingly being used to recognize and treat symptoms of various diseases like epilepsy, heart disease, Parkinson's disease, blindness, urinary incontinence etc.

Researchers are also using the implantable devices as interfaces to the central nervous system to achieve better understanding of the mechanisms of neural communication and control. By studying simple organisms with tractable nervous systems, one can gain insight into the correlation between patterns of neural activity at the level of individual neurons and the resultant behavior of the organism [8]. Such behaviorally meaningful patterns can range from single spikes in a single neuron to timed bursts of neural spikes from a population of neurons, depending on the granularity of the behavior being studied. Numerous efforts have been made to use arrays of electrodes and associated electronics for understanding the signals in a complex nervous system [2]. Implantable neural interfaces have been explored in diverse contexts including neural stimulation, as in cardiac pacing and Functional Electrical Stimulation (FES). FES of nerves or muscles is used to assist patients in grasping, standing, or urination, while deep brain stimulation (DBS) has been shown to be an effective treatment for Parkinson's disease. Cochlear implants are commercially available for treating deafness in children, while visual prostheses have had preliminary success in creating sensations of vision. Extensive research has been done on developing Brain Computer Interfaces (BCI) [3] in which a tetraplegic person can control movement of a computer cursor or a robotic arm. Current implementations of these systems, however, do not perform in-situ signal processing using digital circuits, although some of them use simple control algorithms based on external sensor data.

The need for a closed-loop neural system, which records from multiple neurons, analyzes the neural activity and stimulates some neurons based on the analysis, has been emphasized before [4]. However, most of the current neural interface systems employ sophisticated data analysis performed on an external computer. Real-time closed-loop neural control can greatly benefit from in-situ signal processing using low-power miniaturized hardware. Such in-situ processing is more important for chronic implantations as well as to facilitate ambulatory movements of a patient. Although intense research has been carried out on designing the analog front-end circuitry [2, 5] as well as algorithms for off-line signal analysis, the design of algorithms and digital circuits for online signal processing inside the implantable system is comparatively new. In the context of neural signal processing, Harrison proposed a simple thresholding scheme for on-chip spike detection

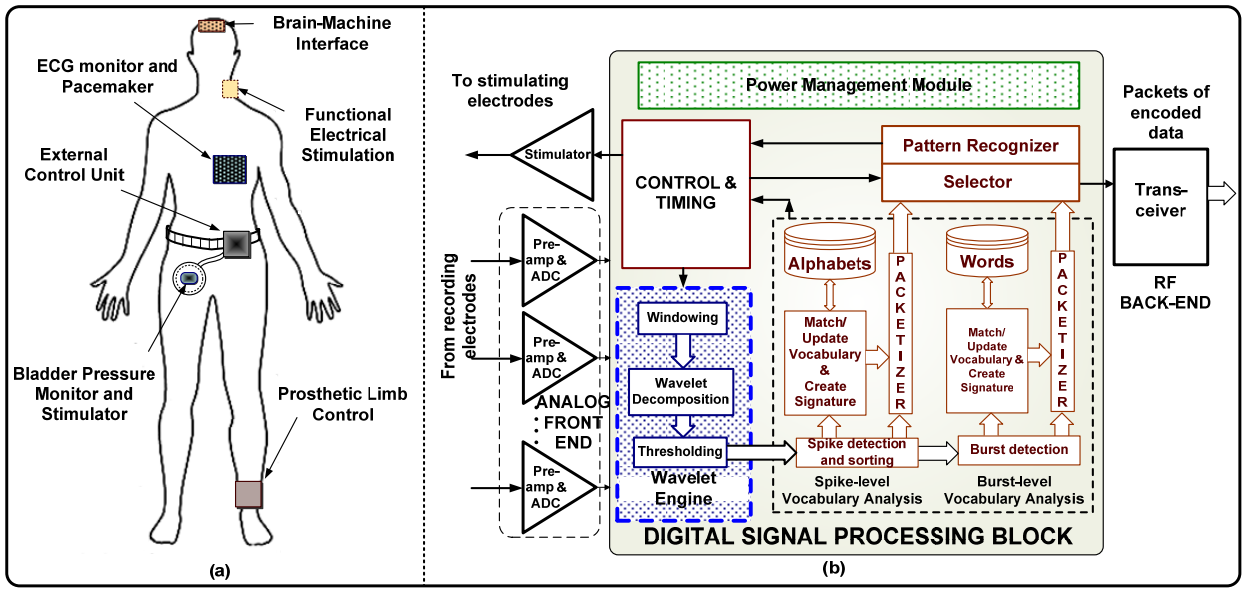

Figure 1: (a) Examples of different application areas for bio-implantable systems. (b) Overall block diagram of a typical bio-implantable system, highlighting the Digital Signal Processing block.

using analog comparators [5]. Olsson et al [6] proposed an on-chip data compression circuit which detects spikes using a simple adaptive thresholding scheme and transmits their amplitudes. Chae et al reported a spike detection (energy-filter-based) and sorting (max-min clustering-based) algorithm and its hardware implementation [7]. Wavelet-based spike detection [8] and custom hardware implementation of discrete wavelet transform (DWT) for multichannel data compression [9-10] have also been investigated before.

A typical implantable system contains a sensing circuitry for recording biological signals; circuits for signal conditioning and analysis; and transceiver circuits for external communication. The functional blocks for hardware implementation of a wavelet-based neural signal processing algorithm [8] are shown in Fig. 1(b). As the number of recording sites increases and more complex data analysis needs to be performed online, the digital signal processing unit in the implantable system needs to have increased computational power. The digital signal processing block serves two main purposes: 1) it recognizes meaningful patterns to trigger appropriate measures e.g. neuromodulation or drug delivery; and 2) it performs data compression to reduce the amount of raw data to be transmitted wirelessly to the external control unit. For example, neural recording from an array of 100 electrodes sampled at 25 kHz per channel with 10-bit precision yields an aggregate data rate of 25 Mbps, which is well beyond the reach of state-of-the-art wireless telemetry.

A computational task for real-time online multi-channel neural signal analysis requires special purpose, low-power, robust and area-efficient hardware, since conventional microprocessor or Digital Signal Processing (DSP) chips would dissipate too much power and are too large in size for an implantable device. For hardware implementation of this signal processing block, nanoscale technologies offer great potential due to their tera-scale integration density, low switching power and high performance. However, this also brings in number of design challenges, such as exponential increase in leakage power [11], reduced yield and lack of robustness due to reduced noise margin [12]. It is therefore important to develop circuit/architecture level design solutions tailored to the computational algorithms for neural signal processing that can leverage the benefits of nanoelectronics while addressing its limitations.

In this paper, we analyze the requirement of DSP hardware design for implantable signal processing systems and identify emerging design challenges. We consider the conventional design requirements in terms of power, area and real-time performance. We note that long-term reliable operation of such system is becoming an important design challenge in the nanoscale technology regime due to the reduced robustness of the nanoscale transistors. Besides, programmability of the system is becoming important to adapt to individual patient conditions and/or to any temporal change. Finally, different security issues including information security to protect the recorded data are becoming significant in implantable telemetry systems. We propose novel circuit/architecture co-design flow for implementing ultralow power and robust on-chip signal processing in implantable systems. We also propose a light-weight security solution to provide high level of security of the recorded neural signals at low hardware overhead. We show that one can exploit the nature of the signal processing algorithms to achieve efficient solutions in the target design parameter space.

2. Design challenges

The major design challenges for signal processing electronics used in implantable systems are highlighted in Fig. 2. The first two parameters are the most significant and have been known to implantable system designers for ages. The implantable system needs to fit within a small area and

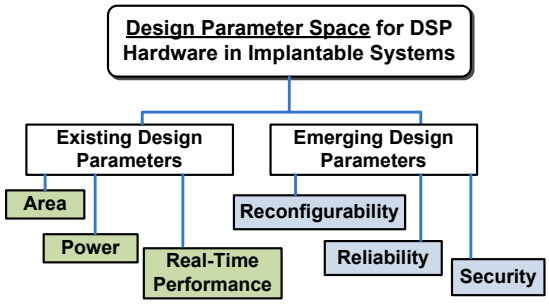

Figure 2: Design parameter space for designing DSP hardware in implantable systems.

hence, the chips inside the system should have small form factor as well. The second design parameter is power. There are two reasons behind the quest for ultra-low power. First, the implantable systems are equipped with a small battery with limited capacity for supplying energy to all the active circuits. If the circuits consume too much power, the lifetime of the system becomes reduced. Nowadays, rechargeable batteries with RF or inductive powering techniques, as well as methods for harvesting energy from within the body are used to increase the availability of power to the implantable system without increasing the area too much. But, the second reason for using low power circuits is to limit the power dissipation and avoid the associated problems like tissue damage due to overheating or temperature-induced circuit reliability degradation.

Performance is typically not a constraint when considering bio-signal processing, because of the inherently low frequency content and hence, low sampling frequency of these signals. However, the processing circuits need to perform their computations in real-time, so that the feedback loop can be closed without too much latency. As the number of recording channels increases, the requirement for time multiplexing of the signal processing hardware increases their operating frequency requirements to tens of MHz. The other three issues in bio-implantable systems are reliability, reconfigurability and security. It should be noted that design solutions for addressing these issues should not come at the expense of increase in area or power consumption. Hence, overhead is an important design parameter when considering different solutions for these new challenges.

1) Reliability: As the number of channels increases, the requirement for complex signal processing circuitry necessitates the use of nanoscale technologies which give us better performance, high transistor density and low area and power. However, to fully leverage the potential of nanoscale devices in implantable system design, we need to address some major design challenges, such as the exponential increase in standby leakage, lack of robustness due to reduced noise margin and yield loss with process fluctuations. Further, temporal parameter variations (due to environmental variations and device aging effects) also affect robustness of operation. The various techniques [11] for reduction of dynamic and standby power tend to have adverse effects on the robustness of the design at nanoscale because of process-induced parameter variations. Variations in manufacturing process can lead to wide variations in circuit parameters, causing loss in yield. Conventionally one needs to follow a worst-case design approach with a wide design margin in order to avoid failures caused by process and temporal variations, which are intrinsic to nanometer technologies. However, such a design approach considerably compromises power dissipation and die area.

Parameter variations can cause a loss in both yield and reliability. Yield is defined as the probability of failure of an as-processed device, while reliability is defined as functional failure of the device during its operation. A process with low yield (due to various extrinsic defects) is unacceptable to begin with, but even a process with high yield (low initial defects) but relatively large degradation rates (poor reliability) is unacceptably expensive in the long term. For bio-implantable systems, reliability of various components is an issue of major interest since the implanted chips are expected to function without failure for a long period of time (e.g. 10 years) under harsh operating conditions. There are two types of temporal variations - short-term and long-term, which can lead to degradation in robustness of operation. Short-term variations can be caused by environmental changes like temperature and voltage fluctuations. Long-term variations can be caused by aging-induced effects like NBTI (Negative Bias Temperature Instability), HCI (Hot Carrier Injection) and TDDB (Time-Dependant Dielectric Breakdown). In order to address the reliability issue without compromising area and power consumption, we propose to exploit the nature of the signal processing algorithm and perform architecture/circuit co-design as described in Section 3.

2) Reconfigurability: The next important design issue for implementing signal processing algorithms in implantable systems is introduction of reconfigurability. The various parameters which are kept tunable in a software implementation need to be assigned fixed values in hardware. However, variations in the nature of biological signals from patient-to-patient and temporal variations in signal and noise characteristics even for the same patient necessitate regular calibration and tuning of the various parameters. To achieve this, one can use software reconfigurability, where the algorithm is coded in an embedded microprocessor [1]. However, compared to a custom implementation, this can be extremely poor in terms of area and power requirements. Also, certain algorithms require special instructions which might require the use of special DSP chips, which are also area and power-hungry. An alternative is to consider hardware reconfigurable platforms. However, existing FPGA systems are also beyond the area and power budget affordable by implantable systems. This necessitates the investigation of alternative reconfigurable architectures like Memory Based Computing [13], which can be custom-designed to implement a particular algorithm within the area, power and performance bound, but keeps the option of reconfigurability in order to suit patient-to-patient and temporal variability. Such a memory based reconfigurable computing (MBC) framework that uses a dense memory array as underlying computing

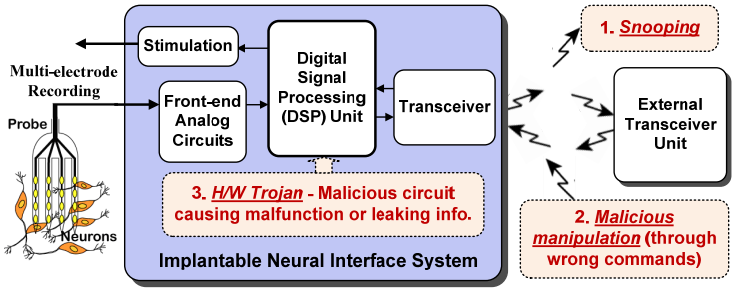

Figure 3: Different attack models which can affect the security of bio-implantable systems.

element, leading to nearly 2X power reduction at iso-performance along with significant improvement in resource usage compared to state-of-the-art FPGA has been presented in [13]. In order to satisfy the area and power constraints of implantable systems, we should use a judicious mix of reconfigurable memory-based computing and custom logic which can give us the required adaptability. Again, we can use the properties of the algorithm to perform this division between custom logic implementation and reconfigurable hardware.

3) Security: Security is another new aspect of implantable system design, which has not been given much consideration. However, with increasing awareness among people regarding the issues of privacy and security, and with computationally affordable solutions available for breaking simple codes and encryption, it has become necessary to include this aspect when considering the design issues of bio-implantable systems. Recently, researchers have articulated security concerns about implantable medical devices which use wireless communication protocols. The lack of authentication and integrity mechanisms put patients at risk from attack by anyone with a transceiver. Various security threats considering different aspects of the implantable device usage have been described in [14]. Here, we focus on three kinds of attack scenarios, as illustrated in Fig. 3 for implantable systems.

a) The security of data communicated over a wireless interface can be compromised. An attacker can eavesdrop on the wireless communication channel in order to get access to sensed data.

b) For implantable stimulation/drug-delivery systems, the attacker can initiate malicious control signals leading to malfunction, injury or even death.

c) Malicious circuits, referred to as hardware Trojans, can be inserted by the attacker during design or fabrication inside a chip in order to facilitate leakage of information or to cause malfunction. These circuits are typically well-hidden to evade detection during post-manufacturing functional testing.

For the first scenario, it is useful to encrypt the data based on a secure key to prevent it from being understood by snoopers. For the second scenario, one can use an authentication key to ensure that the input commands are coming from a safe and valid source. For the first two attack scenarios, the attacker is assumed to be aware of the communication protocol and in possession of an external transceiver device capable of communicating with the implantable system. However, the attacker does not destroy the implanted device or remove it in order to extract the stored key. In the third scenario, which represents a multiple-level attack, the attacker has access to the circuit during its design or fabrication stages and incorporates extra circuitry (like a back-door for snooping). The inserted circuitry can be designed cleverly to escape detection by normal functional testing and exhibits its malicious effect during run-time, being triggered by rare circuit conditions or attacker-enabled instructions. The various types of hardware Trojan circuits and existing detection solutions are summarized in [15]. One needs to investigate the effectiveness of the existing Trojan detection solutions in the context of implantable systems.

In this paper, we initially focus on the reliability issue and propose a circuit/architecture co-design approach for ultra low power and robust implementation without unnecessary design overhead. Finally, we look at an ultra-light weight security solution which can be implemented by exploiting the nature of the signal processing algorithm.

3. Low-power and robust circuit-architecture co-design approach

Miniature size and low energy consumption are two primary design requirements for implantable systems. Though the size of an implantable system is still limited by the size of battery, antenna and off-chip components, the area of the signal processor can be significant with increased requirement for on-chip processing of signals from multiple channels. While nanoscale (sub 90-nm) technologies provide high integration density, faster switching speed and lower switching power per transition, they also bring new challenges. These include exponential increase in leakage current [11] and reliability issues due to process induced parameter variations as well as temporal parameter variations due to temperature and voltage variations (collectively termed as P-V-T variations) [12]. To decrease power consumption, one can use popular techniques such as clock gating and supply voltage gating. Clock gating saves dynamic power in the clock line which drives the sequential elements such as flip-flops and latches. Supply gating saves leakage power due to the stacking effect [11]. Both approaches require identification of idle cycles for a logic block during which it can be "gated". Voltage scaling along with commensurate scaling of frequency is an effective power reduction approach due to quadratic dependence of power on supply voltage. Static or dynamic change in transistor threshold voltage (V_{th}) is another method of achieving low power operation. However, the effectiveness of dual-V_{th} designs diminishes at nanoscale technologies due to increase in band-to-band tunneling leakage current and impact of process variations on parametric yield.

To achieve ultra low power operation, supply voltage can be scaled below the transistor threshold voltage, when the circuit starts operating in the sub-threshold region. This leads to huge reduction in both dynamic and leakage power with a corresponding increase in path delays, leading to ultra low frequency operation. Sub-threshold design [16] is a

well-researched design technique, especially suited for low-sampling rate applications like biomedical signal processing. However, it comes at the cost of increased vulnerability of a design to variation induced failures leading to reduced reliability and yield loss. At scaled voltage, digital circuits can suffer from functional failure due to variations in circuit delays. For example, in low-power DWT hardware, the time required for computation of the most significant approximation coefficients can be affected due to voltage scaling, causing the clocked storage elements (flip-flops) to latch wrong logic values. With increasing die-to-die and within-die parameter variations in nanoscale technologies, maintaining high yield and reliability of operation in sub-threshold design is becoming a major challenge. On the other hand, super-threshold design, although more effective in terms of yield and reliability, usually dissipates much higher power. Hence, a design technique that merges the advantages of both worlds is most desirable. Next, we will evaluate both approaches and investigate design solutions to enable low-power and robust operation, by exploiting the nature of the neural signal processing algorithm.

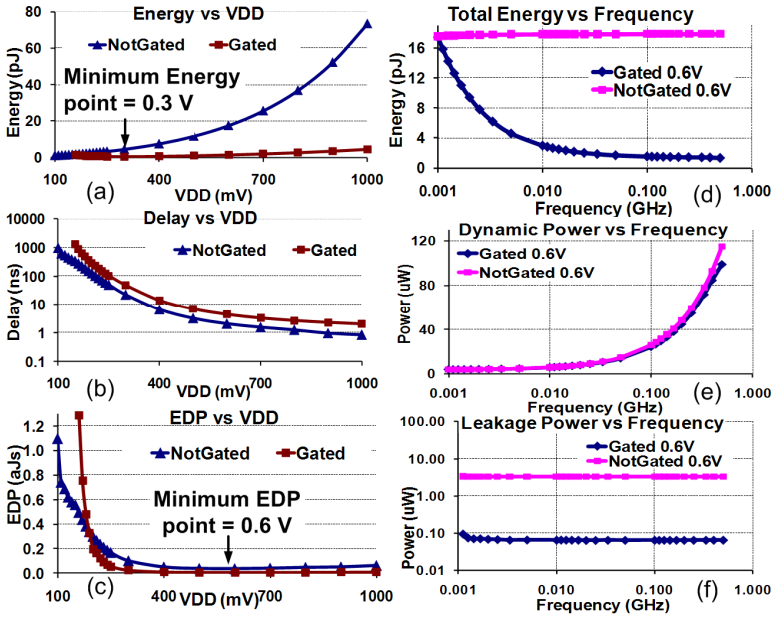

Figure 4: Finding the optimal operating voltage and frequency for the main processing element (PE) of a Discrete Wavelet Transform (DWT) block. a) Energy vs. supply voltage (VDD). (b) Delay vs. VDD. (c) Energy-delay product (EDP) vs. VDD. (d) Energy vs. operating frequency. (e) Dynamic power vs. frequency. (f) Leakage power vs. frequency. The results for both gated and non-gated designs are compared at different voltages and frequencies to compare sub-threshold and super-threshold energy consumption.

3.1 Sub-threshold vs. super-threshold operation

We performed HSPICE simulations at 70nm Predictive Technology Model (PTM) [18] for the main Processing Element (PE) of the DWT algorithm [10, 17]. The effect of voltage scaling on total energy consumption, critical path delay and Energy-Delay Product is seen in Fig. 4. It should be noted that the minimum energy point (see Fig. 4(a)) has a much lower supply voltage than the point with the minimum EDP (see Fig. 4(c)), which again corresponds to 0.6V. Taking this as our nominal super-threshold voltage, we simulated the savings in Energy obtained by increasing supply gating idle time window, by increasing frequency of operation. As seen for the simple adder circuit, here also we get similar trend for total energy (Fig. 4(d)), dynamic power (Fig. 4(e)) and leakage power (Fig. 4(f)). Hence, we can obtain comparable energy savings by performing sub-threshold operation at ultra low frequency and super-threshold operation at medium-to-high frequencies, while extensive power gating is applied. We also performed simulations with power gating applied to the sub-threshold design, but the functionality of the circuit was hampered at extreme low voltages (<0.10V) and the delay target was crossed at slightly higher voltages (< 0.15V).

Since both sub-threshold design and super-threshold design (with power gating) have similar energy consumption, we can opt for either technique to implement our design. However, at nanoscale technologies, process variations can cause wide variations in circuit parameters like critical path delay, causing delay failures under extreme conditions. The detrimental effects of process variations are exacerbated in designs with low-power techniques applied. Hence, we performed an analysis of how process variations (modeled as V_{th} variations) impact critical path delay of a PE at different supply voltages, with and without supply gating transistors (which are kept on during Active mode, but still affect performance). The sleep transistors were sized to have maximum power savings, allowing up to 30% performance degradation under nominal conditions. The increase in critical path delay, T_{crit} (normalized with respect

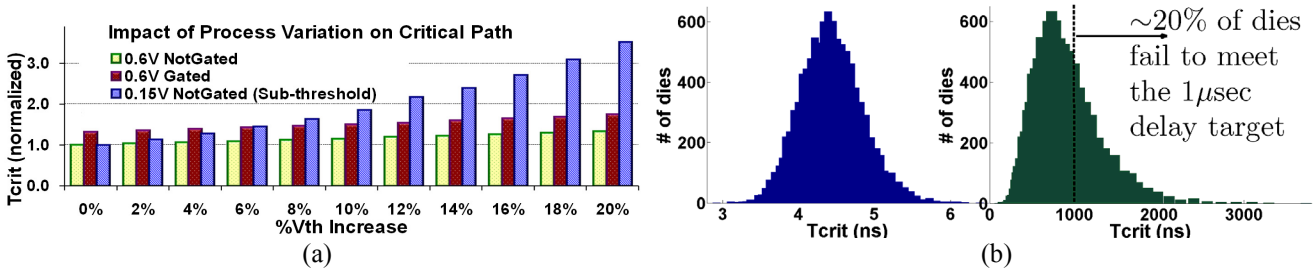

Figure 5: (a) Impact of process variations on critical path delay at sub-threshold and super-threshold voltages with supply gating. (b) The impact on parametric yield.

to delay of non-gated design at same supply voltage) is plotted for increasing V_{th} variations in Fig. 5(a). The delay values of the three cases under nominal process conditions are:

1) Super-threshold non-gated design at 0.6V - 3.34ns
2) Super-threshold gated design at 0.6V - 4.39ns
3) Sub-threshold non-gated design at 0.15V - 732.40ns

It is seen that under extreme process variations, the delay of a sub-threshold design can increase by up to 3.5X, causing extreme yield loss, while a super-threshold design with supply gating, has a comparatively minimum impact under variation, even though the performance overhead under nominal conditions is relatively larger. The yield results, considering only inter-die variations, are obtained by assuming a Gaussian distribution with 30% standard deviation for the V_{th}. The resultant delay distributions for 10,000 dies (obtained using Monte Carlo simulations in HSPICE) for super-threshold (0.6V) gated design and sub-threshold (0.15V) non-gated design are shown in Fig. 5(b). Given a delay target of 1µsec, the yield in case of the sub-threshold design is 79.94%, while all super-threshold designs pass the delay target of 30 ns, corresponding to an operating frequency of 33.33 MHz.

3.2 Preferential Design approach

We can achieve comparable energy reduction by sub-threshold low frequency operation and super-threshold operation with extensive power gating. However, the former can cause huge yield loss and decrease in robustness under large parameter variations. Moreover, operation in the super-threshold domain opens avenues for architecture-level design techniques like Preferential Design to further decrease energy consumption with graceful degradation in robustness. Low-power and robustness of operation typically impose contradictory design requirements. In logic circuits, the principal failure mechanism under device parameter variations at nanoscale technologies is delay failure, which occurs when the max path delay of a circuit exceeds the clock period. Low power design using voltage scaling accentuates delay failure probability under variations. To avoid these delay failures, conventionally, one needs to follow a worst-case design approach. However, such a design approach considerably compromises power dissipation and die area. On the other hand, if we go for a nominal design, any variation-induced failure might cause drastic changes in the outputs which are more critical in terms of signal quality, because of timing failure in the max delay paths.

In the preferential design approach [17], critical components in terms of performance (e.g. the important approximation coefficients in DWT) are designed with more relaxed timing margin than non-critical ones. In such an approach, possible variation-induced failures are confined to non-critical components of the system, thus allowing graceful degradation in performance under variations. Preferential design methodology for a parallel architecture [17] of the DWT block is shown in Fig. 6. Further, due to higher timing margin in critical components, the system becomes suitable for application of low power design techniques. It is to be noted that the preferential design approach uses the nature of the signal processing algorithm to reduce the design overhead. This allows us to maintain high reliability of operation without having to adopt a worst-case design approach. The results of using Preferential Design in implementing a neural signal processing algorithm are provided in [17].

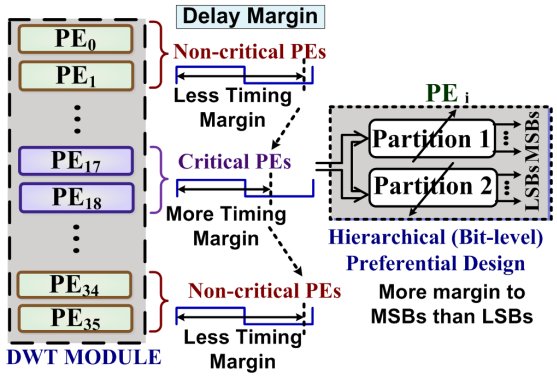

Figure 6: Preferential design methodology for a parallel DWT architecture.

4. Light-weight security solution

The importance of data security in health-care applications has been emphasized before, in the context of body area networks where multiple biomedical sensors are implanted on or inside the body and communicate with each other through an unsecured link [14]. The devices can also communicate with a master device which monitors the implanted devices and collects all the data before making them accessible to the concerned health-care provider. Separate techniques are used for securing the information from the implantable devices to the external unit and from the external unit to the internet, since the former has tighter resource constraints than the latter. Conventional encryption techniques used for securing the data passing over wireless links have been proposed earlier, assuming the presence of implanted micro-controllers for implementing heavy-weight cryptography, even suggesting the use of cryptographic co-processors. However, it is to be noted that conventional encryption techniques, whether implemented in hardware or

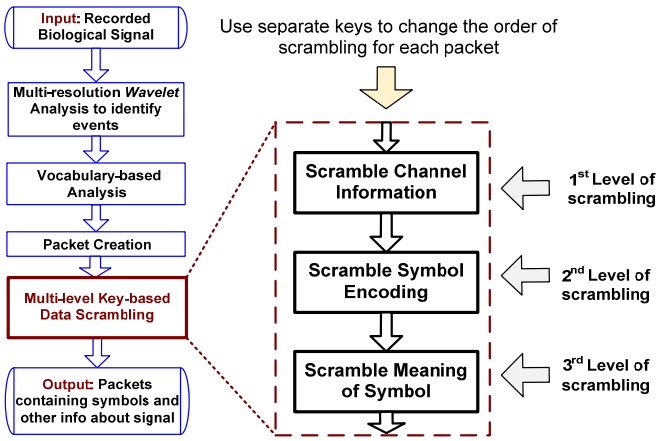

Figure 7: The biological signal processing algorithm considering security of recorded signals.

software, require some penalty in terms of area and power overhead, which might be unavailable for a resource-constrained implantable system.

In fact, we note that it is possible to exploit the nature of the biological signal and the signal processing algorithm in order to derive a light-weight key-based data obfuscation solution which can provide several levels of security against a potential attacker without incurring too much overhead. For the neural spike detection and vocabulary-based analysis which we consider as an example implantable system, the following properties are particularly useful. The neural signal consists of low frequency signal, which is characterized by intermittent bursts of sharp events called spikes (which allows us to use wavelet transform for de-noising) and the repetitive nature of these patterns helps us develop a vocabulary-based algorithm [8] for neural data compression and efficient neural data analysis. The main steps for the data security algorithm are shown in Fig. 7. We use multiple levels of data scrambling when creating the packets of data by using the already existing hardware resources for the vocabulary-based algorithm. The details of the implementation are provided in [19].

5. Summary

We have analyzed the design parameter space for digital signal processing hardware in implantable systems and presented a design methodology for low-power, robust, area-efficient and secure signal processing. With increasing spatial and temporal resolution of the recording array, DSP unit in implantable systems requires increasing computational power. To address this increase in complexity, we consider using nanoscale technologies, which provide the advantages of high-performance and high integration density. To achieve the ultralow power and robust operation, we exploit the nature of the algorithm as well as signal acquisition characteristics. We also provide a light-weight security solution, which employs a low-overhead scrambling approach (instead of conventional cryptography solutions) to achieve high level of data security leveraging on the specific signal processing algorithm. We note that an efficient design solution that adequately addresses all the important design parameters can be achieved through an algorithm-circuit-architecture co-design approach. Future work will involve application of the approach to other biomedical signal processing tasks and fabrication of test chip for hardware validation.

6. Acknowledgment

We would like to thank Prof. Hillel J. Chiel, Department of Biology, Case Western Reserve University, for his help and guidance in developing the neural signal processing algorithm and supplying us with *in vivo* neural recordings from sea-slug (*Aplysia californica*).

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