Unified P4 (Power-Performance-Process-Parasitic) Fast Optimization of a Nano-CMOS VCO

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ABSTRACT

In this paper, we present the design of a P4 (Power-Performance-Process-Parasitic) aware voltage controlled oscillator (VCO) at nano-CMOS technologies. Through simulations, we have shown that parasitics and process have a drastic effect on the performance (center frequency) of the VCO. For process variation analysis, we propose a methodology called Design of Experiments-Monte Carlo (DOE-MC), which offers up to 6.25x time savings over a traditional Monte Carlo (TMC) method. A performance optimization of the VCO along with dual-oxide power minimization technique has been carried out in the presence of worst case process. The end product of the proposed methodology is a process aware, performance optimized, dual oxide VCO physical design. We have achieved 25% power (including leakage) minimization with only 1% degradation in center frequency compared to target frequency, in the presence of *worst-case process* and parasitics. The dual-oxide physical design of the VCO is carried out at $90nm$. To the best of the authors' knowledge, this is the first research reporting a dual-oxide nano-CMOS VCO design simultaneously optimized for power (including leakage), performance, parasitics and process.

Categories and Subject Descriptors

B.7.1 [**Integrated Circuits**]: Types and Design Styles—VLSI (very large scale integration)

General Terms

Design

Keywords

VCO, Dual Oxide Technology, Process Variation, Parasitics, Power Aware Design, Performance Aware Design, Nano-CMOS

1. INTRODUCTION

The battle to deliver maximum performance has taken center stage in the evolution of Radio Frequency Integrated Circuits (RFICs). Minimum power expenditure is demanded in addition to performance. Power conservation impacts every budget, whether technological or financial. Product acceptability, reliability and profitability depend as much on power efficiency as they do on performance.

There is a difference between low-power design and power-aware design [23]. Low-power design refers to minimizing power with or without a performance constraint. Power-aware design refers to maximizing some other performance metric, subject to a power budget. Two of the biggest challenges to maintaining performance are the increasing power specifications because of leakage power and potential yield loss caused by increasing process variations. The impact of variations in process parameters and operating conditions on the performance factors of a design is much higher for today's nanometer than the sub-micron technologies of the past [9]. Hence, the nominal operating point, which is the center of the distribution of the parameters for a given process, may not be the best operating point for design yield. An automated way is required to maximize design yield such that the design operates as specified across the entire process and operating environment.

One of the difficulties for analog circuits in high frequency applications is that the exact performance prediction is very challenging due to many parasitic effects [22]. Unfortunately, before circuit layout and implementation, it is difficult to estimate the parasitic effect. Therefore, in order to improve design efficiency and reduce the time-to-market, it is crucial to be able to predict parasitic effects for accurate performance. The objective of this paper is to present a design methodology of general RFIC components, using a Voltage Controlled Oscillator (VCO) in nano-CMOS technology as a case study. To accomplish this goal, a current starved topology has been exploited and a new P4 (power-performance-process-parasitic) optimization technique is proposed. The center frequency of VCOs is one of the most critical performance parameters. Thus, this paper deals with the optimization of the center frequency.

2. NOVEL CONTRIBUTIONS OF THIS PAPER TO THE STATE OF THE ART

The novel contributions of this paper are in multiple forms:

(1) We propose a P4 (Power-Performance-Parasitic-Process) optimal design flow for nanoscale CMOS analog circuits.

(2) The design of a P4 optimal RF circuit (VCO) is presented.

(3) The P4 optimization of the VCO has been carried out using a dual-oxide process technique. This technique is effective in minimizing the power of a circuit [19], as thick-oxide transistors consume less power (including leakage) than thin-oxide transistors. However, their judicious use is necessary to com-

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pensate the performance penalty due to use of higher oxide thickness.

(4) A dual-oxide physical design of the VCO is presented for $90nm$ CMOS technology.

(5) A novel *worst case process analysis* technique called Design of Experiments-Monte Carlo (DOE-MC) approach is proposed, which offers up to 6.25x computational time savings over traditional Monte-Carlo (TMC).

The rest of the paper is organized as follows: related research works are discussed in section 3. Section 4 presents the proposed design flow for P4 optimization of the VCO. Section 5 discusses the baseline logical design of the VCO. The process variation analysis is discussed in section 6. P4 optimization is presented in section 7. The paper is concluded with directions for future research in section 8.

3. RELATED PRIOR RESEARCH

RFIC design is highly sensitive to layout parasitics. This has motivated a lot of research in the parasitic aware synthesis area to overcome degradations due to device and package parasitics to achieve optimal performance [22, 3]. Simulated annealing is used for synthesizing RF power amplifiers in [6]. Optimization techniques such as particle swarm optimization are proposed for parasitic aware design in [7].

In [8], an LC VCO has been subjected to a parasitic-aware synthesis. A parasitic and process aware design flow has been proposed in [10]. In [26], a Design of Experiments (DOE) approach has been used to optimize the center frequency, but the methodology is not parasitic aware. The simulation-based circuit synthesis example in [28] also does not include the layout parasitics in the design.

Process variation in analog circuits [4] and power aware design is on the research forefront now. In [21], an analysis of the process parameters affecting a ring oscillator's frequency performance is performed. In [9], a current-controlled oscillator has been subjected to process variations. In [11], the authors propose a dual-oxide technique for power and delay optimization at circuit level. In [19], the authors have shown the effect of simultaneous variation of supply and process parameters on power consumption of datapath components.

Analog and mixed-signal designs require accurate frequency or time reference signals. Generally, Phase-Locked Loops (PLLs) are used to provide such stable references [5] and one of the important components of a PLL is the VCO [1]. A number of PLL and VCO designs have been presented in [24, 14]. The authors in [27] and [16] have studied high performance designs using CMOS processes. Low-power LC VCOs have been presented in [15, 25, 20, 17]. Jitter and phase noise are studied in [18] and [12]. A tabular comparison of our research with existing literature (Table 1) reveals our design to be low power, high-performance at nanoscale technology.

Table 1: Performance comparison of the proposed VCO.

Reference	Technology	Performance	Power
Tiebout [20]	$250nm$	$1.8GHz$	$20mW$
Dehghani [25]	$250nm$	$2.5GHz$	$2.6mW$
Long [17]	$180nm$	$2.4GHz$	$1.8mW$
Kwok [15]	$180nm$	$1.4GHz$	$1.46mW$
This Work	$90nm$ dual-oxide	$2.3GHz$	$158\mu W$

4. THE PROPOSED NOVEL RFIC P4 OPTIMAL DESIGN FLOW

The proposed design flow is shown in figure 1. We call this a P4 optimal design flow because it accounts for parasitics, process, power, and performance in the circuit in an unified manner. Once the logical design is done to meet the required specifications, an initial physical design is prepared. The physical design is subjected to Design Rule Check (DRC), LVS (Layout vs. Schematic) and parasitic (RCLK) extraction. A worst case process variation analysis of the physical design with respect to performance (center frequency) is carried out, where the worst case process is identified and the physical design is subjected to it. This is followed by thick-oxide assignment (T_{oxpth}, T_{oxnth}) to the power-hungry transistors (NMOS, PMOS) of the VCO using the *thick oxide model file*. The rest of the transistors in the circuit operate on the *baseline model file*. We call this technique "intelligent dual-oxide assignment", used to minimize power consumption of the VCO circuit [19]. The parasitic netlist obtained from the initial layout is then parameterized for parameter set D (widths of transistors and T_{oxpth}, T_{oxnth}). We call this "parameterized parasitic netlist". The parameterized parasitic netlist is then subjected to a conjugate gradient based optimization loop in order to meet the specifications (performance, power) in a worst case process environment. Once the parameter values for which the specifications are met are obtained, a final physical design of the VCO is created using these parameter values. Hence, the physical design which involves tedious manual work for designers, needs to be done only twice. Once before the optimization (initial physical design), and then after the optimization (final physical design). The optimization loop is automatic and done using a simulator [13]. Hence we obtain a P4 optimal dual-oxide VCO layout as a result of the proposed design flow.

5. DESIGN OF THE VCO FOR $90NM$ CMOS

A current starved VCO has been considered in this paper. The design, as shown in figure 2, comprises of three stages: (1) input stage consisting of two transistors with high impedance, (2) an odd numbered chain of inverters along with two current source transistors per inverter, which limit the current flow to the inverter and (3) buffer stage. The circuit has no stable operating point and it will oscillate at some frequency that is determined by the number of inverters, size of the transistors in the circuit, and the current flowing through the inverter, which is dependent upon the input voltage to the VCO. The operating frequency of the VCO, f_0 can be determined using the relation [2]:

$$f_0 = \left(\frac{I_{inv}}{N \times C_t \times V_{DD}} \right), \tag{1}$$

where V_{DD} is the supply voltage, I_{inv} is the current flowing through the inverter, N is the odd number of inverters in the VCO circuit and C_t is the total capacitance given by the sum of the input and output capacitances of the inverter. The operating frequency of the VCO can be mainly controlled by an applied DC input voltage, which adjusts the current I_{inv} through each inverter stage. The expression for C_t is:

$$C_t = \left(\frac{5}{2} \right) \times C_{ox} \times (W_p \times L_p + W_n \times L_n), \tag{2}$$

were C_{ox} is the gate oxide capacitance per unit area, W_n and W_p are the widths and L_n and L_p are the lengths of the inverter NMOS and PMOS transistors, respectively. C'_{ox} is formulated as:

$$C_{ox} = \left(\frac{\epsilon_{SiO_2} \times \epsilon_0}{T_{ox}} \right), \tag{3}$$

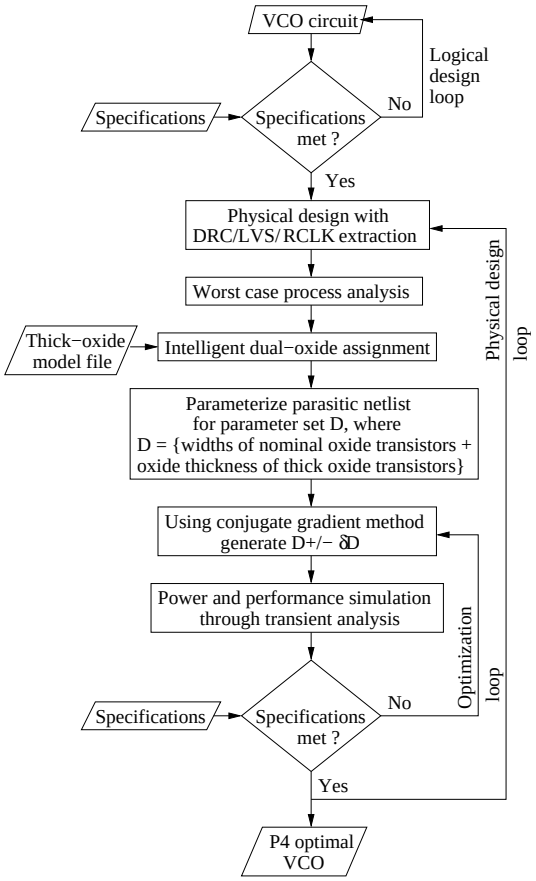


Figure 1: The proposed novel RFIC P4 optimal design flow.

where ϵ_{SiO_2} is the relative dielectric constant of SiO_2, ϵ_0 is vacuum dielectric constant and T_{ox} is the gate oxide thickness.

The functional specification for the design is the center frequency. The target center frequency has been kept at a minimum of 2 GHz. The number of stages is fixed to 13 for high frequency requirement. For baseline design, we have chosen $L_n = L_p$ = 100 nm, W_n = 250 nm and $W_p = 2 \times W_n$ = 500 nm. C_t is calculated using equation 3. Finally, I_{inv} is calculated using equation 1, and the current starved NMOS and PMOS devices are sized to provide the required current I_{inv}. Thus we obtained $L_{ncs} = L_{pcs}$ = 100 nm, and W_{ncs} = 500 nm and $W_{pcs} = 10 \times W_{ncs} = 5\mu m$, where W_{ncs} and W_{pcs} are the widths and L_{ncs} and L_{pcs} are the lengths of the current-starved NMOS and PMOS transistors, respectively.

From these equations, we obtain the minimum sizes of transistors needed for successful operation. The initial physical design of the VCO is then carried out using these transistor sizes (shown in figure 2).

6. PROCESS VARIATION ANALYSIS OF VCO

The process variation analysis has been carried out on the initial physical design with parasitics extracted ($RLCK$). We present two methods for process variation study of the VCO: (1) Traditional Monte-Carlo (TMC), and (2) Design of Experiments-Monte Carlo (DOE-MC) method. The DOE-MC methodology offers the advantage of faster computation over TMC. For process variation, we have considered variation in 5 process parameters, namely: (1)V_{DD}: Supply voltage, (2) V_{tn}: NMOS threshold voltage, (3) V_{tp}: PMOS threshold voltage, (4) T_{oxn}: NMOS gate oxide thickness, (5) T_{oxp}:

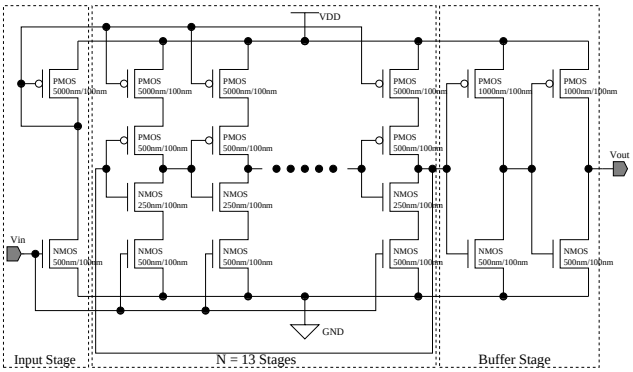


Figure 2: Logical design of the VCO.

PMOS gate oxide thickness. A correlation coefficient (cc) of 0.9 is assumed between T_{oxn} and T_{oxp}. Each of these process parameters is assumed to have a Gaussian distribution with mean (μ) taken as the nominal value in the process design kit, and a standard deviation (σ) equal to 10% of the mean. TMC with $N = 1000$ runs gives the oscillation frequency (f_0) having a Gaussian distribution with μ = $1.54GHz$ and σ = $103.5MHz$. The plot is shown in figure 3.

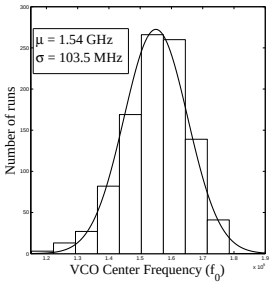
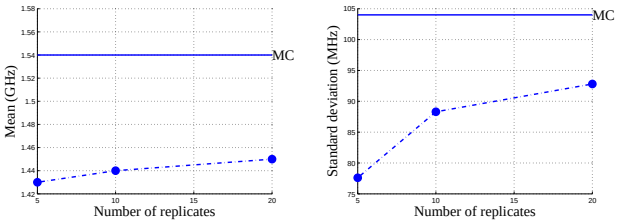


Figure 3: Traditional Monte Carlo result for f_0.

The DOE-MC methodology has also been used for the study of effect of process variation on f_0. A *two level full factorial design* is run for the 5 process parameters, where level 1: μ - 2 $\times$ σ, (μ= mean, σ = 10% of μ) and level 2: μ + 2 $\times$ σ. A full factorial run requires 2^5 = 32 trials. 5 MC replicate runs are run for every trial, and the μ and σ of f_0 are recorded for every trial. Hence we obtain 32 values of μ and σ for f_0, one for every trial. The final μ and σ for f_0 are recorded as the average of the 32 trials. Considering 5 replicates per trial, we get a total of 32 $\times$ 5 = 160 runs (as compared to 1000 runs for traditional MC). $\mu(f_0)$ and $\sigma(f_0)$ for DOE-MC approach are recorded in figures 4. This technique is less accurate than traditional MC, but saves on computing time. The results for MC replicates per trial = 10 and 20 and the percentage error in μ and σ is also presented in Table 2.

Table 2: Statistical information from DOE-MC approach.

MC runs per trial	Total runs	% error (μ)	% error (σ)	Time saving over TMC
5	160	7.47	25.1	6.25X
10	320	6.78	14.7	2X
20	640	5.78	10.3	1.5625X



(a) Mean of f_0 distribution (b) Standard deviation of f_0 distribution

Figure 4: DOE-MC approach for accuracy vs. speed trade-offs.

From the above methods, we have identified the worst case process for f_0 to be the one in which V_{DD} reduced by 10%, and all the other process parameters (V_{tn}, V_{tp}, T_{oxn}, T_{oxp}) are increased by 10%.

7. P4 OPTIMIZATION OF THE VCO

In this section, we demonstrate how the performance (f_0) discrepancy (caused by parasitics and worst case process) is overcome along with power minimization of the VCO using dual-oxide technique. After full-extraction($RCLK$), a 25% degradation in the performance (center frequency) is observed between the physical design and target frequency. Furthermore, a 43.5% discrepancy is observed between the physical design and target frequency when the VCO is subjected to *worst case process* (section 6). Details are given in Table 3.

Table 3: Results showing performance discrepancy and worst case process values for a target frequency $>= 2GHz$.

Parameter	Initial Physical Design	Initial Physical Design + Process Variation	Final Physical Design + Process Variation
f_0	$1.56GHz$	$1.13GHz$	$1.98GHz$
discrepancy	25%	43.5%	1%
V_{DD}	$1.2V$ (nominal)	$1.08V$ (-10%)	$1.08V$
V_{tn}	$0.1692662V$ (nominal)	$0.186193V$ ($+10\%$)	$0.186193V$
V_{tp}	$-0.1359511V$ (nominal)	$-0.149546V$ ($+10\%$)	$-0.149546V$
T_{oxn}	$2.33nm$ (nominal)	$2.563nm$ ($+10\%$)	$2.563nm$
T_{oxp}	$2.48nm$ (nominal)	$2.728nm$ ($+10\%$)	$2.728nm$

Hence we obtain the following parameters:

- Target center frequency f_0 = 2 GHz.
- Initial Physical design center frequency $f_{0\mathrm{p}}$ = 1.56 GHz.
- Initial Physical design center frequency in a worst case process variation environment $f_{o\mathrm{p}-\mathrm{p}}$ = 1.13 GHz.
- Initial average power consumption (including leakage) (P_{VCO}) = $212\mu W$.

7.1 Intelligent Dual-Oxide Assignment

A transient analysis is run on the physical design of the VCO, and the average power consumed by all the transistors is measured. The input stage transistors (shown by solid circles in figure 5) collectively consume 48% of the total average power of the VCO circuit, hence are most suitable candidates for higher thickness oxide assignment (T_{oxpth}, T_{oxnth}). The buffer stage transistors (shown by dashed circles in figure 5) consume 11.5% of the total average power, and hence may be treated to higher thickness oxide, for further power minimization. In this paper, we have subjected the input stage transistors to dual-oxide assignment. These transistors follow a different model file called *thick oxide model file*. The other transistors in the VCO circuit follow the *baseline model file*.

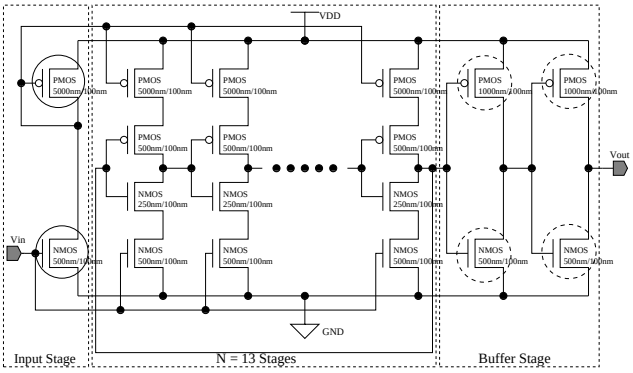


Figure 5: Possible candidate transistors for intelligent dual-oxide assignment.

7.2 Parameterizing the Parasitic Netlist

Followed by the dual-oxide assignment, the parasitic-aware netlist generated from the first layout is then parameterized with optimization parameters. The parameter set includes the widths of PMOS and NMOS devices in the inverter (W_n, W_p), the PMOS and NMOS devices in the current-starved circuitry (W_{ncs}, W_{pcs}), and T_{oxpth}, T_{oxnth}.

7.3 Conjugate Gradient Optimization

After parametrization of the netlist, we subject this netlist to conjugate gradient based optimization, where the parameter set takes on different values, till the specifications are met. The candidates for optimization are widths of the inverters (W_n, W_p) and current-starved transistors (W_{ncs}, W_{pcs}), and the oxide thicknesses (T_{oxnth}, T_{oxpth}) of thick-oxide (input stage) transistors. While the thicker oxide thicknesses minimize power consumption of VCO, the higher widths of the devices maximize performance. Our specifications include $f_0 >= 2GHz$, and $P_{VCO} = min$. The algorithm is shown as algorithm 1. Table 4 shows the final values of the parameter set for P4 optimal VCO.

Table 4: Optimized values of the parameter set.

D	C_{low}	C_{up}	D_{opt}
W_n	$200nm$	$500nm$	$210nm$
W_p	$400nm$	$1\mu m$	$415nm$
W_{ncs}	$1\mu m$	$5\mu m$	$8.5\mu m$
W_{pcs}	$5\mu m$	$10\mu m$	$5\mu m$
T_{oxpth}	$2.48nm$	$5nm$	$5nm$
T_{oxnth}	$2.33nm$	$5nm$	$3.54nm$

Algorithm 1 Algorithm for P4 optimization in VCO.

1: **Input:** Parasitic Aware netlist, Baseline model file, Thick oxide model file, Specifications $F = [f_0, P_{VCO}]$, Stopping criteria S, parameter set $D = [W_n, W_p, W_{ncs}, W_{pcs}, T_{oxpth}, T_{oxnth}]$, Lower parameter constraint C_{low}, Upper parameter constraint C_{up}.
2: **Output:** Optimized objective set F_{opt}, Optimal parameter set D_{opt} for $S = \pm\beta$. {where $1\% \leq \beta \leq 5\%$}
3: Run initial simulation in order to obtain feasible values of parameters for the given specifications.
4: **while** ($C_{low} < D < C_{up}$) **do**
5: Use **finite difference perturbation** to generate new set of parameters $D' = D \pm \delta D$.
6: Compute $F = [f_0, P_{VCO}]$.
7: **if** ($S == \pm\beta$) **then**
8: **return** $D_{opt} = D'$.
9: **end if**
10: **end while**
11: Using D_{opt}, construct final physical design and simulate.
12: Record F_{opt}.

The physical design of the VCO is then carried out using these parameter values, and the following results are obtained:

- Target center frequency f_0 = 2 GHz.
- Final Physical design center frequency $f_{0\mathrm{p}}$ = 2.3 GHz.
- Final Physical design center frequency in a worst case process variation environment $f_{0\mathrm{p-p}}$ = 1.98 GHz.
- Final average power consumption (including leakage) (P_{VCO}) = $158\mu W$

Hence we obtained a final optimized dual-oxide layout, with $1.98GHz$ center frequency under worst case process variation, and $2.3GHz$ center frequency in nominal process conditions and 25% power minimization. The frequency versus voltage characteristics show acceptable linearity.

7.4 P4 Optimal Dual-Oxide Physical Design of the VCO

The dual-oxide physical design of the VCO has been carried out using a generic 90 nm Salicide 1.2V/2.5V 1 Poly 9 Metal process design kit. At high frequencies, parasitic inductance has a major impact on chip performance. Hence it is necessary to extract self (L) and mutual (K) inductance so that the impact of inductive coupling could be assessed and minimized on the layout. A full extraction of the layout was carried out (including resistors (R), capacitors (C), inductors (L) and mutual inductors (K)). The P4 optimal physical design is shown in figure 6. The final optimal widths of the P4 optimal circuit and thick oxide transistors are shown in figure 7.

8. CONCLUSIONS

In this paper, we present the design of a P4 (Power-Performance-Parasitic-Process) optimal nano-CMOS VCO. The presented design flow may be used for optimization of nanoscale circuits in general. The center frequency has been treated as the target specification. The degradation of the center frequency due to parasitic and process variation effects has been narrowed down from 43.5% to 1%, along with 25% power minimization using dual-oxide technique. The performance summary of the VCO is given in Table 5.

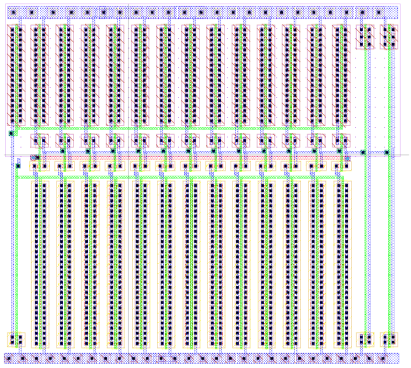


Figure 6: P4 optimal dual-oxide layout of the VCO.

The end product of the proposed design flow is a P4 optimal dual-oxide VCO physical design. For future research, we plan to consider thermal effects in the VCO design as well. Alternative optimization techniques such as simulated annealing and genetic algorithms are also being explored, so that a fair comparison with other approaches for the P4 design flow may be done.

Table 5: Measured performance of the optimal VCO.

Parameters	Values
Technology	$90nm$ CMOS $1P\ 9M$
Supply Voltage (V_{DD})	$1.2V$
center frequency (Nominal process)	$2.3GHz$
Process and supply variation	V_T ($+10\%$), T_{ox} ($+10\%$), V_{DD} (-10%)
center frequency (Worst-case process)	$1.98GHz$
Parameter set	6 (W_n, W_p, W_{ncs}, W_{pcs}, T_{oxpth}, T_{oxnth})
Number of objectives	2 ($f_0 >= 2GHz$, P_{VCO}=$minimum$)

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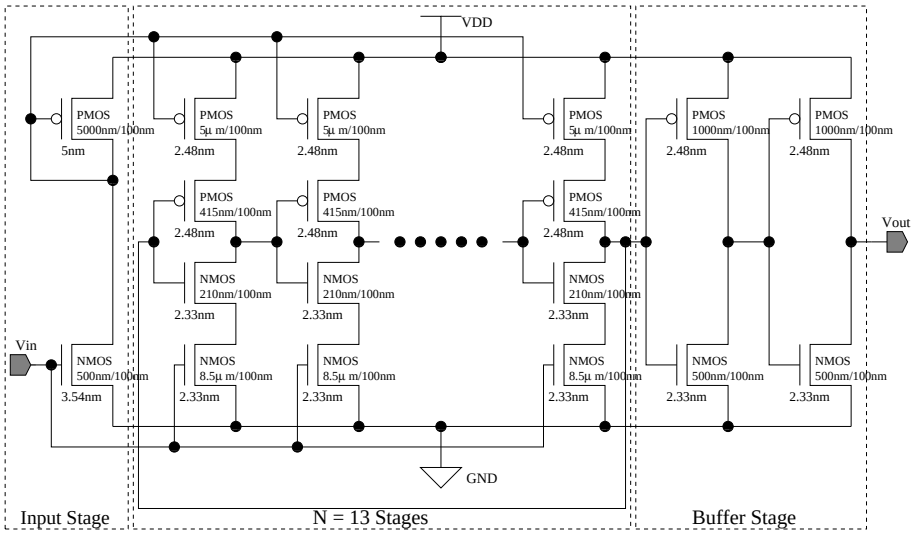

Figure 7: Optimal widths and oxide thicknesses of transistors of the P4 optimal VCO.

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