

A Low-Voltage 5.1–5.8-GHz Image-Reject Receiver with Wide Dynamic Range

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Abstract—A monolithic 5–6-GHz band receiver, consisting of a differential preamplifier, dual doubly balanced mixers, cascaded injection-locked frequency doublers, and a quadrature local oscillator generator and prescaler, realizes over 45 dB of image-rejection in a mature 25-GHz silicon bipolar technology. The measured single sideband (50 Ω) noise figure is 5.1 dB with an IIP3 of -4.5 dBm and 17-dB conversion gain at 5.3 GHz. The 1.9×1.2 mm² IC is packaged in a standard 32-pin ceramic quad flatpack and consumes less than 50 mW from a 2.2-V supply.

Index Terms—Image-reject mixing, low-noise amplifiers, low-power design, low voltage design, RFIC design, simultaneous noise/power matching, wireless receivers.

I. INTRODUCTION

THE SUCCESS of cellular telephony and the Internet has resulted in greater demand for high-speed wireless connectivity. Spectral allocations in the 5–6-GHz band offer 300–400 MHz of unlicensed spectrum in many regions [1], [2], with the potential to realize both fixed and portable wireless multimedia applications at data rates between 20–150 Mb/s. Radio frequency integrated circuit (RF IC) technology is needed to meet the aggressive cost, size, and power consumption targets demanded by these applications.

This paper describes a single-chip 5.1–5.8-GHz image-reject receiver fabricated in a mature medium-performance (25-GHz f_T) 0.5- μ m silicon bipolar technology. Designed for operation from a single sub-3-V supply, the receiver IC incorporates a fully differential low-noise preamplifier (LNA), dual doubly balanced mixers, a local oscillator (LO) divide-by-two prescaler, and the active elements needed to implement a voltage-controlled oscillator (VCO). An on-chip three-filament (trifilar) transformer couples the LNA and mixers, allowing improved gain and linearity and lower overall noise figure and power consumption compared to conventional IC designs. A new technique for low-power regenerative frequency doubling multiplies the LO reference source by a factor of either two or four. A companion analog divide-by-two or frequency divider circuit is designed for low-voltage operation and generates

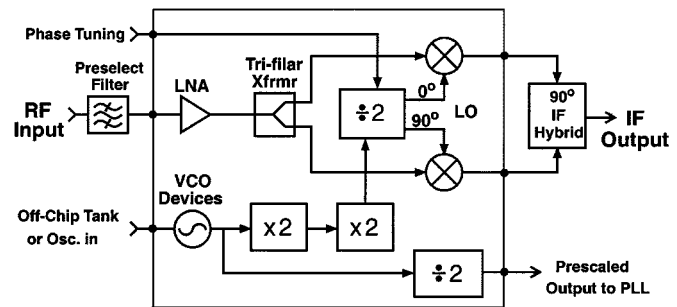


Fig. 1. Receiver front-end block diagram.

in-phase (I) and quadrature (Q) LO signals in the 5–6-GHz band. An important feature of the divider circuit is its ability to realize precise adjustments of the phase relationship between I and Q LO components. A regenerative divide-by-two prescaler (with output buffer) enables an $f_{LO}/4$ output to drive external PLL synthesizer ICs designed for operation below 2 GHz (i.e., commercially available PLL synthesizer ICs).

II. 5–6-GHz RECEIVER ARCHITECTURE

The frequency allocations for unlicensed operation in North America (UN-II) have been split into two bands: 5.15–5.35 and 5.725–5.825 GHz [1], [3]. However, in Europe the HiperLAN standard specifies the upper band at 5.47–5.725 GHz [2]. Other potential applications lie in the 5.8–5.9-GHz region, where international allocations have been made for intelligent transportation system (ITS) services using dedicated short-range communications [3]. The objective for this work is a monolithic implementation that covers the entire 5–6-GHz band in order to widen the scope of applications for the IC.

Fig. 1 shows a block diagram of the receiver RF IC. The functions indicated within the bounded region have been implemented on-chip. Balanced circuitry is used throughout the IC to reduce crosstalk between the circuit blocks. This doubles the power consumption for many of the circuit functions (e.g., LNA) compared to conventional single-ended realizations, and therefore low-voltage circuit topologies are emphasized to conserve power in portable equipment. Low-voltage operation is also desirable to maintain compatibility with receiver backend signal processing circuits that will likely be implemented in deep-submicron CMOS technologies. In the 5–6-GHz band, the gain available in the RF front-end is restricted by limitations of the 25-GHz technology used for this implementation [4]. The on-chip interstage coupling transformer improves the efficiency of the RF circuits (i.e., dynamic range for a given supply voltage/bias current in the LNA and mixer) through resonant

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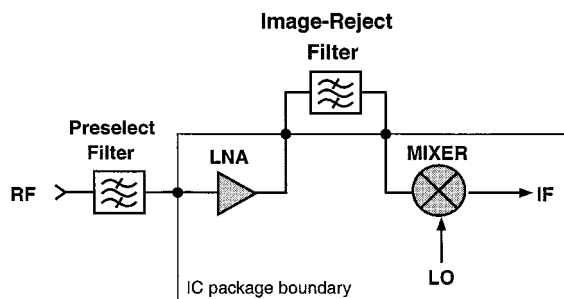


Fig. 2. Conventional heterodyne receiver IC front-end.

parasitic absorption, and allows operation at supply voltages as low as 0.9 V. This topology has been described previously in [5] and [6]. A standard 32-pin quad flatpack (QFP) was selected to package the IC to reduce costs at the expense of larger parasitics at 5–6 GHz (e.g., lead and bondwire inductances).

Quadrature (0° and 90° phased) LO signals are required to drive the doubly balanced mixers. The divide-by-two circuit in Fig. 1 generates these two LO phases. The double-frequency drive signal for the divider is derived from cascaded frequency doublers. The fundamental LO is multiplied by 4 and then divided by 2, for a net $\times 2$ multiply (e.g., a 2.75-GHz LO is scaled to 5.5-GHz I and Q signals at the mixer LO inputs). A cascade of multipliers allows the option of using a single multiply-by-two followed by the divider to service the 2.4-GHz ISM band. Thus, this LO scheme could service both 2.4 and 5–6-GHz bands. However, this option was not pursued for this work. Note that only the active devices for the VCO are implemented on-chip.

A. RF Filtering and Image Rejection

Downconversion in a heterodyne receiver translates signals from both the “image” and RF bands to the same intermediate frequency (IF), as both bands share the same frequency difference with respect to the LO. To eliminate the possibility of interference from the image band, image-reject (IR) filters tuned to the RF band are inserted in the signal path ahead of the mixer, as shown in Fig. 2. However, in a highly integrated receiver module the interstage IR filter introduces losses in the RF signal path, adding cost, packaging complexity, and power consumption through the additional $50\text{-}\Omega$ interface. Off-chip fixed-frequency filters also limit system flexibility in an open standard environment. In addition, a 5–6-GHz band receiver operating at MB/s data rates will likely require a much wider IF bandwidth than today’s 2.4-GHz ISM band systems.

Monolithic techniques, such as VCO tracking notch filters [7], [8], image-reject or single-sideband mixing [9], and direct-conversion [10] receivers do not require the interstage IR filter. However, the complexity in implementation must be weighed against other constraints such as cost and performance. For example, a fully differential receiver employing tracking notch filters was recently reported by Copeland [8]. This design uses 14 monolithic inductors (excluding VCO) and therefore requires a relatively large chip area (approximately 4 mm^2). In addition, a high IF on the order of 1 GHz is used to separate the RF and image bands to prevent the notch filter from attenuating the desired RF signal.

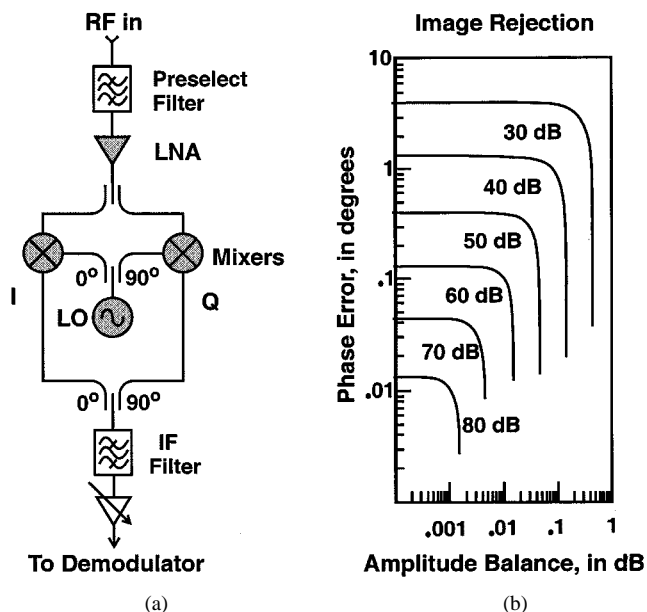


Fig. 3. Image-reject (Hartley) receiver front-end. (a) Hartley receiver downconverter. (b) Image rejection versus amplitude and phase errors in quadrature signals.

An alternative to electronic filtering is image-reject downconversion (see Fig. 3), which is the method chosen for this work. A preselect filter bandlimits the spectral input to the LNA to help prevent overloading or desensitization and suppresses out-of-band interferers. It also provides some rejection of the image if the receiver is designed to have a first IF greater than the width of the preselect filter’s passband. The filtered RF signal is then amplified by the LNA, and coupled to two downconverting mixers. Quadrature LO signals drive each mixer, producing in-phase and quadrature IF outputs. The image band is rejected if the I and Q mixer outputs are then summed in phase quadrature; the resulting image suppression as a function of phase and amplitude errors between the I and Q LOs is illustrated in Fig. 3(b). Note that the interstage off-chip filter is no longer required if the combined rejection from the preselect filter and IR mixing stages is sufficiently high. Of course, the I and Q mixer outputs could also be used at baseband (as in a direct conversion receiver) by appropriate selection of the LO frequency. Thus, a distinct advantage of this approach is its ability to address both direct conversion and heterodyne architectures.

B. Quadrature Signal Generation

Quadrature LO signals are often generated using a digital divide-by-two flip-flop [9] or an RC polyphase network [11] in systems where the quadrature LO cannot be directly obtained from the VCO. For 40 dB of image rejection, the phase and amplitude errors must be controlled to within 1° and 0.1 dB, respectively, over the entire range of input frequencies [see Fig. 3(b)]. A regenerative frequency divider (analog divide-by-two) with quadrature outputs [12] was selected for this design. Compared to an RC polyphase filter (for quadrature signal generation), the regenerative technique is less susceptible to process gradients and tolerances, requires less chip area, provides signal gain, and affords precision phase tuning control over about one octave in frequency. The analog method of division is preferred over the

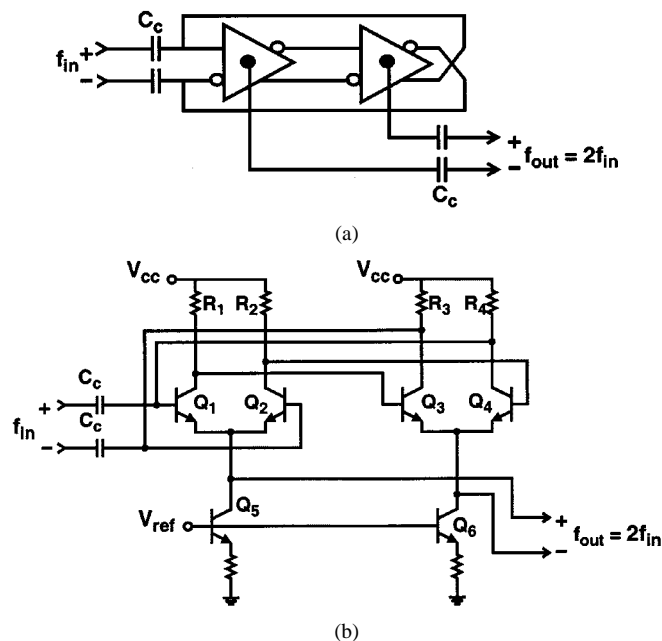


Fig. 4. Regenerative frequency doubler. (a) Block diagram. (b) Simplified schematic diagram.

more common digital master–slave frequency dividers because of lower power consumption and degradation in phase noise, quieter operation (less spurious content and crosstalk with other circuit blocks), and higher maximum operating frequency [13]. However, using a divide-by-two method to generate I and Q signals requires an input signal that is at least twice the frequency of the desired output. For a 5–6-GHz integrated receiver, this implies that an internally generated 10–12-GHz frequency (\pm the IF) is required for either high- or low-side LO downconversion. This signal is generated from a lower frequency source through the use of a monolithic frequency doubling circuit.

C. Frequency Doubler

There are a number of IC-compatible frequency doubling circuits available [14]–[17]. A new regenerative frequency doubling technique [18] is shown in Fig. 4. It is essentially a two-stage quadrature ring oscillator, which is coupled through C_c to an input signal (i.e., f_{in}). The fundamental frequency of the oscillator is synchronized to f_{in} by injection locking [19]. Each of the differential amplifiers is a simple emitter-coupled differential pair with resistive loads. The nonlinear characteristic of the differential pair produces a strong double-frequency component at the emitter-coupled node when the circuit is driven large-signal. At high frequencies (i.e., $> f_T/10$), the transistor parasitics attenuate higher harmonics so that the collector voltage is predominantly sinusoidal. The double-frequency ($2f_{in}$) differential signal is extracted across the emitter nodes of the two amplifiers in the ring [see Fig. 4(b)]. The “+” and “–” outputs are antiphase because the fully differential inputs to each amplifier stage are held close to quadrature phase (i.e., 0° and 90° phase, respectively) by the ring topology. Capacitive coupling at the input allows the oscillator to maintain a stable dc bias point through negative feedback and high dc gain. The common mode or fundamental component at f_{in} is suppressed from coupling efficiently to the output by the balanced topology.

Regenerative frequency doubling has a number of properties which make it suitable for monolithic integration. First, the output amplitude is almost independent of the input signal level. Also, regenerative circuits are power efficient and can provide substantial gain at high frequencies (approaching the transistor $f_T/2$). In addition, a very wide locking range (over an octave) is possible with low levels of input signal drive as the oscillator is locked in its fundamental mode rather than at a subharmonic. The low impedance outputs (at the emitters) have good signal-driving capability. The circuit is also relatively compact because inductors are not required. Finally, the output signal has low spurious content and does not require filtering, and multiplier stages can be cascaded to realize higher orders of multiplication without the need for interstage filtering.

Resistively loaded ring oscillators typically have a low Q-factor, and so a slight phase shift in the feedback loop can significantly alter the frequency of the oscillator from its natural frequency. When injection locked, the I and Q outputs of the oscillator are in quadrature (90° phase shifted) with a small phase error of approximately $< \pm 3^\circ$. The magnitude of the phase error depends on the difference between the injected and free running frequency of the oscillator, the ring oscillator Q, and as a higher order effect, the injected signal amplitude. However, the I – Q outputs are not suitable for driving the mixers directly. This is because the phase error is too large for the image-reject mixer application, and the error is both frequency and gain dependent.

This error is a result of the imbalance introduced by signal injection, which adds or subtracts phase from the oscillation at only one stage [i.e., the first stage in Fig. 4(b)] of the ring. Signals at the emitter-coupled output nodes of the quadrature oscillator are therefore nearly 0° and 180° phase shifted (within approximately $\pm 6^\circ$). Together they comprise a differential doubled-frequency output pair with a small common-mode signal component. For a 6° error, the common-mode signal is approximately 20 dB below the differential signal.

III. CIRCUIT DESCRIPTION

The receiver RFIC can be subdivided into two main blocks. The first block is the RF downconverter consisting of LNA, coupling transformer and balanced mixers (see Fig. 1). The remaining circuitry generates the quadrature (I – Q) LO signals needed to drive each mixer.

A block diagram of the subsystem used to generate the I – Q LOs used for downconversion is shown in Fig. 5. The first frequency-doubling stage is a four-stage ring oscillator that is injection locked to the LO input signal at a frequency of $f_{LO}/2$. The doubled-frequency differential output at f_{LO} is extracted from two emitter-coupled nodes at opposite (and quadrature) sides of the first stage (see the detailed schematic in Fig. 6). The f_{LO} differential signal is then fed to the next stage of frequency doubling via a buffering amplifier. This increases the injection-locking range of the second frequency doubler by increasing the amplitude of the injected signal. The buffer also improves the isolation between the two regenerative doubler stages and prevents the possibility of unintentionally locking the first stage to the second one.

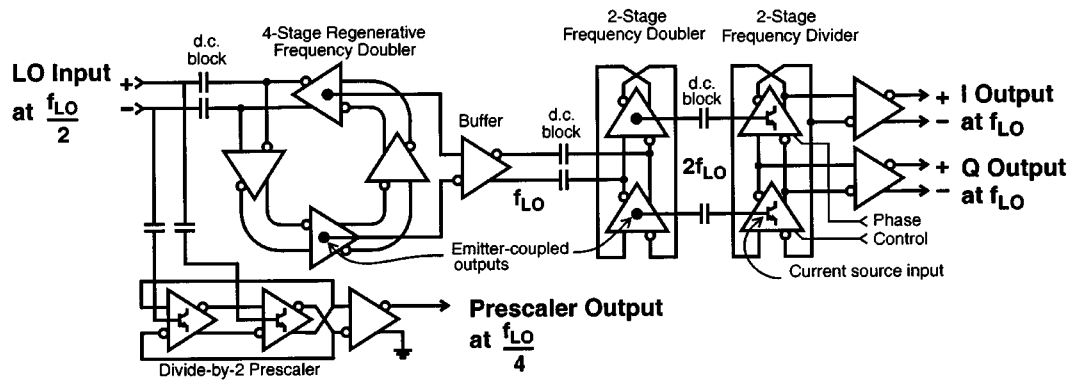
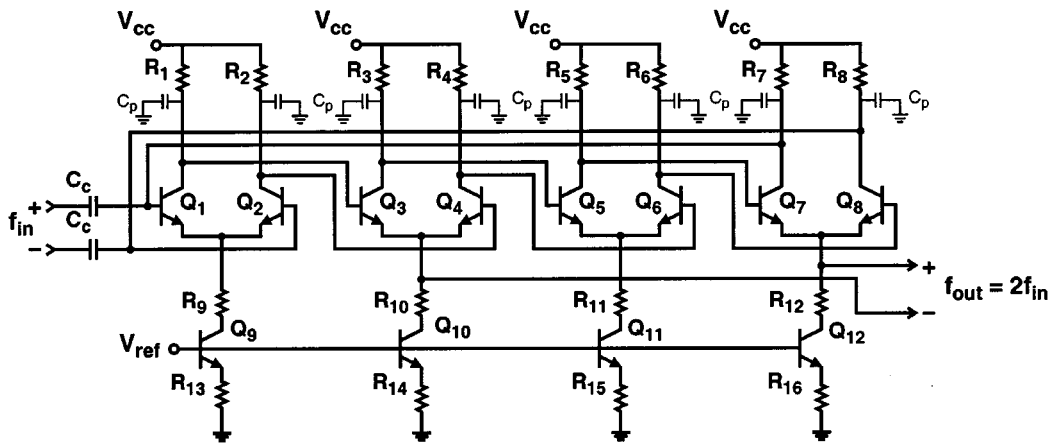
Fig. 5. I - Q LO subsystem.

Fig. 6. Four-stage (first) frequency doubler.

A. First Doubler Stage

A schematic of the first frequency doubler circuit is shown in Fig. 6. Polysilicon resistors loads R_1 through R_8 are used in conjunction with their parasitic capacitances (C_p) to set the dominant pole for each amplifier in the ring. The parasitic capacitances (C_p) of the poly resistors vary proportionally with resistor area, thereby allowing their value to be controlled through layout. It should also be noted that resistors greater than minimum width are less susceptible to fabrication tolerances. Thus, the process variation of the resistors is reduced and explicit capacitor loads are not required. The use of a four-stage ring instead of a two-stage ring allows the doubled frequency signal to be extracted from the emitter-coupled nodes of Q_3 - Q_4 and opposite pair Q_7 - Q_8 rather than directly from the emitter-coupled node of the input transistors Q_1 - Q_2 . If a single-ended input source is used for injection, this topology will improve the suppression of the fundamental signal at the output due to the common-mode rejection ratio provided by the first stage (i.e., Q_1 - Q_2). Resistors R_9 - R_{12} increase the real output impedance of each bias current source at high frequencies and increases the common-mode rejection of each stage.

B. Second Doubler Stage

The second frequency doubler in the system (from Fig. 5) is implemented using a two-stage differential ring oscillator injection locked to f_{LO} . Its free-running frequency is centered at

twice the free-running frequency of the preceding stage (i.e., ~ 5.5 GHz). This second stage of doubling provides an output at $2f_{LO}$ (or four times the input to the first doubling stage) when locked.

Fig. 7 illustrates the second frequency doubler in the LO subsystem. Two stages are used because a four-stage ring consumes excessive power and cannot operate at 5–6 GHz. Collector resistors R_1 - R_4 are shown as segmented resistors in Fig. 7 to illustrate the distributed nature of parasitic capacitance C_p . In the 5–6-GHz band, parasitic reactances in the loads are low enough to affect performance and therefore an accurate estimate of the RC time constant for the load is necessary. With a single π -section to model the entire resistor, one-half of the total parasitic capacitance for each collector load is shunted to ac ground (V_{CC}). This gives an overly optimistic estimate of the loop gain for the ring oscillator and an incorrect free-running frequency. To avoid this, the parasitic capacitance is distributed across multiple π -sections, as shown in Fig. 7. For values less than 1 k Ω (as in this design), a series connection of three π -models is sufficient to model the effect of parasitic capacitance distributed along the resistor's length up to 6 GHz.

In order to increase the loop gain of the oscillator, the dominant pole of the amplifying stages is set as high as possible by reducing the parasitic capacitance at the collector nodes, while additional (and much needed) phase lag is introduced in the feedback path of the loop of the oscillator using an RC delay line consisting of resistors R_5 - R_8 . Low-pass filtering caused by the

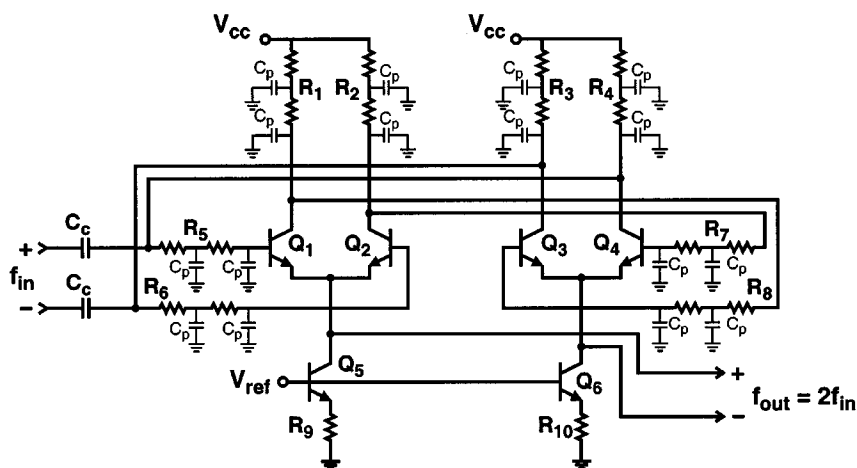
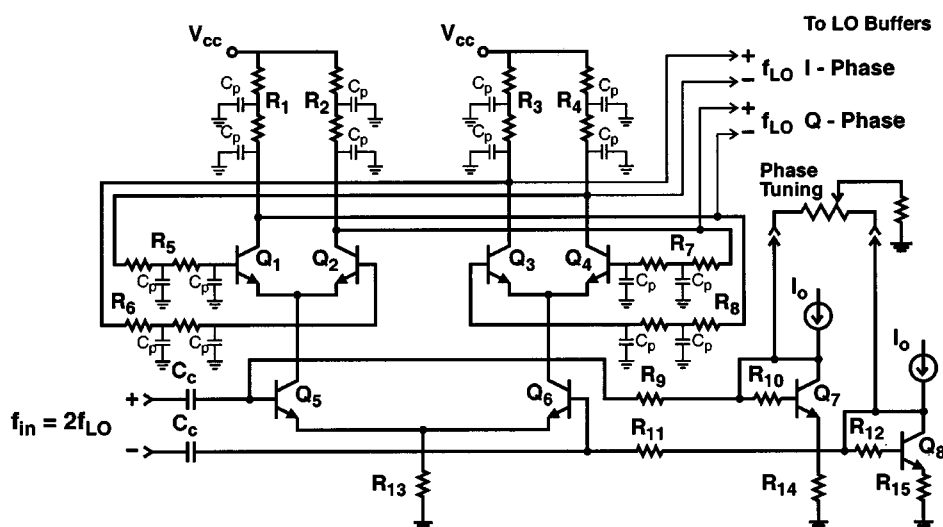


Fig. 7. Second-stage regenerative frequency doubler.

Fig. 8. Frequency divider with I - Q outputs and phase tuning.

parasitic capacitance of these series-connected resistors (which is determined by their area) lowers the free-running frequency with little degradation in the loop gain.

C. I - Q Regenerative Divider and Prescaler

Again referring to Fig. 5, the $2f_{LO}$ signal provided by the second doubling stage (at ~ 10 – 12 GHz) is divided into accurate I and Q signals by a two-stage regenerative frequency divider. The two-stage doubler and two-stage divider used here are virtually identical ring oscillators running at the same fundamental frequency (~ 5 – 6 GHz). The two circuits are coupled by the input differential pair to the divider (Q_5 and Q_6 in Fig. 8). The two-stage doubler (Fig. 7) is asymmetrically driven, leading to small I - Q phase errors (less than approximately 3°). However, the divider is symmetrically driven by a $2f_{LO}$ signal injected differentially into its emitter-coupled nodes. Due to this symmetry, the I and Q outputs of the divider remain in quadrature (i.e., 90° phase-shifted), with an error of less than 1° .

Fig. 8 shows a schematic diagram of the frequency divider used to generate I and Q LO signals for the downconverting mixers. The circuit consists of cascaded differential amplifier

stages in a ring oscillator configuration. Differential pair Q_5 - Q_6 converts the $2f_{LO}$ input voltage to a differential current which synchronizes the ring oscillator (Q_1 - Q_4) to the input signal. The input differential pair (Q_5 - Q_6) also isolates the divider from the preceding stages. Resistors R_9 and R_{11} isolate the $2LO$ input from the parasitics of bias transistors Q_7 and Q_8 . The divided I and Q outputs at f_{LO} are buffered by differential amplifiers and then ac coupled to the inputs of the mixer quads.

The time delays through each stage of the divider are well matched, resulting in quadrature output signals with less than 1° of phase error throughout its frequency locking range, which is approximately one octave. By disturbing the symmetry of the ring oscillator in a controlled manner, the phase angle between I and Q outputs can be altered. Since the frequency of the oscillator is fixed by the injection locking of the circuit to the $2f_{LO}$ input signal, only the phase relationship between the outputs can be changed. Note that the amplitude is determined by the maximum output swing of the differential amplifier stages. In this way, the phase relationship between I and Q LO outputs is tuned. A convenient way of adjusting the symmetry of this circuit is to (differentially) alter the bias currents of Q_5 and Q_6 . This increases the phase delay of one output of the input pair

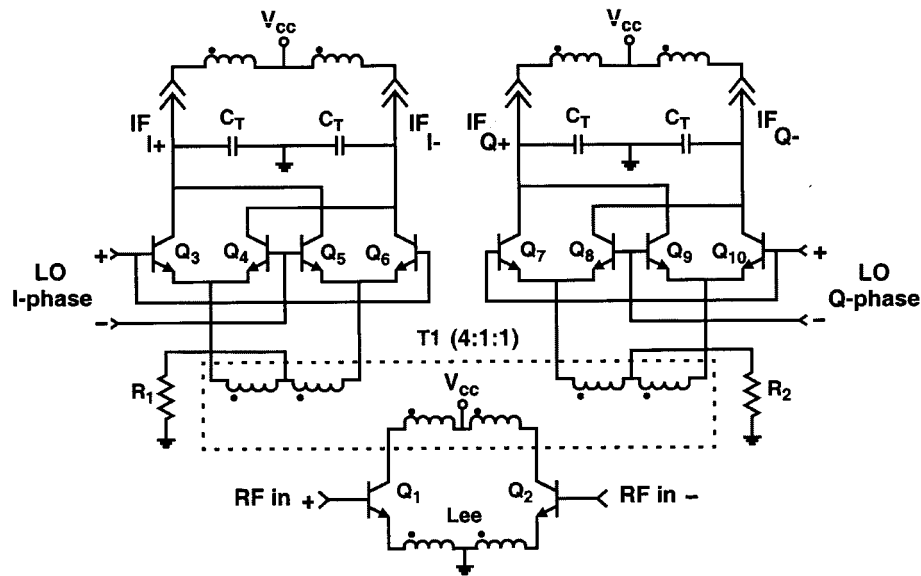


Fig. 9. RF downconverter schematic diagram.

while reducing delay through the other. Note that diode-connected transistors Q_7 and Q_8 (shown in Fig. 8) bias each stage of the divider. The bias currents through Q_5 and Q_6 are therefore isolated from each other but are referenced back to a common reference source (I_o). The simple potentiometer shown in the figure illustrates how the bias currents (and hence $I-Q$ phase) were altered in testing. It is proposed that this method of phase control could be implemented monolithically with a simple current-biasing digital-to-analog converter.

The prescaler is identical to the frequency divider shown in Fig. 8 except that the component values are altered to lower free-running frequency to $f_{LO}/4$. Note that for the prescaler, only one of the divider outputs is required. The output of the prescaler is buffered by an open collector differential amplifier, which consumes 4 mW of power.

D. RF Downconverter

A complete circuit schematic of the RF signal path is shown in Fig. 9. The off-chip matching, bias and quadrature-combining networks at the IF ports used in testing and evaluation of the IC performance are not shown on the schematic for simplicity. Parasitics for the 32-pin package were accounted for in the design. The topology used for the RF section is similar to that described in [5], [6], however, there are significant differences in this design. First, a new fully monolithic interstage coupling transformer with a noninteger turns ratio is designed to increase the overall preamplifier gain and improve coupling efficiency. Also, given the narrow operating margin for the receiver in this technology (i.e., f_T/f_{RF} is less than 5), the transistor sizes, degeneration inductance, and transformer parameters are carefully selected to maximize dynamic range (i.e., minimum noise figure with a high input intercept), improve the input match, and minimize power consumption in a standard IC package.

T_1 is a fully symmetric monolithic transformer design [20] which acts as an interstage coupling circuit and also feeds dc bias to the LNA and mixers. In order to realize 15-dB LNA gain above 5 GHz with a few milliamperes of bias current, the

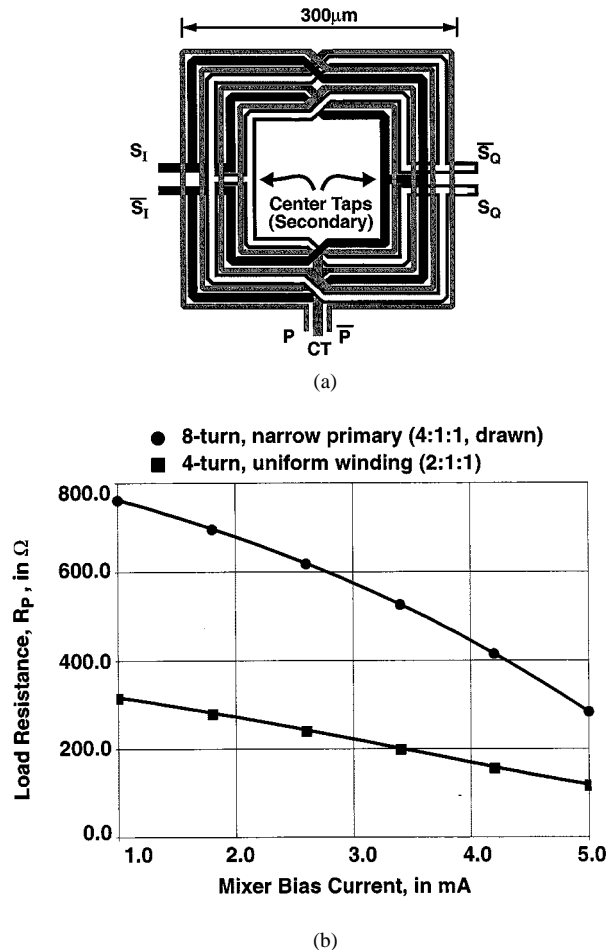


Fig. 10. Monolithic transformer. (a) Physical layout. (b) Resistance seen at the primary ($f = 5.5$ GHz).

impedance reflected from the secondary to the primary winding of the transformer must be on the order of 300–400 Ω per side. This was realized by designing a noninteger turns ratio transformer with minimal parasitic loading. The shunt parasitics ap-

pear in parallel with the reflected impedance, thereby limiting the impedance seen at the primary terminals. The turns ratio is 4 : 1 : 1 as drawn in the physical layout [see Fig. 10(a)]. However, the primary winding has a narrower line width than the secondaries, which results in a step-up factor in addition to the geometric turns ratio. The final design consists of eight turns of 5 and 10- μm -wide Al top-level metal with a metal-to-metal spacing of 3 μm , measures 300 μm on a side, and has three ports: one on the primary (LNA) side and two for the mixing quads. DC bias is fed to the LNA and mixer circuits via the center taps. A program written to simulate the behavior of arbitrary configurations of microstrip lines on silicon [21] was used to extract a SPICE model for the transformer, which was used in circuit simulations of the RF path.

The doubly balanced mixers (Q_3 – Q_{10} in Fig. 9) consist of four-transistor Gilbert-type switching quads. The impedance seen at the common-emitter side of the switching quad is proportional to the transconductance of bipolar junction transistors (BJTs) in the quad. Hence, the bias current is selected to provide the desired load impedance for the preamplifier when reflected from secondary to the primary side of the transformer. The load resistance at the transformer primary as a function of the mixer bias current is plotted in Fig. 10(b). A resistance less than 300 Ω is seen at the primary for a 2 : 1 : 1 turns ratio design (four turns of 8- μm -wide top-level metal with a metal-to-metal spacing of 2.8 μm , measuring 275 μm on each side). The load impedance increases to above 600 Ω when the geometric turns ratio is increased (i.e., 4 : 1 : 1 layout) and a narrower width primary winding are used. However, the improvement is less than predicted by the change in turns ratio (due to parasitic losses) and is limited to about a factor of three.

The preamplifier stage consists of transistors Q_1 and Q_2 (from Fig. 9), which are driven differentially from the RF inputs. Differential drive improves the Q-factor of the trifilar transformer and emitter degeneration inductor by approximately 50% [22]. Also, the preamplifier is designed so that an impedance match at the RF input realizes both minimum noise figure and maximum power transfer for the stage for the load impedance seen at the transformer primary. A simultaneous matching procedure employing both series feedback from the emitter via inductor Lee and shunt feedback via the collector–base (i.e., Miller) capacitance is used [6]. An emitter area of $20 \times 0.5 \mu\text{m}^2$ was selected after careful optimization including all parasitic effects. For 5–6-GHz operation, simulations predicted that a noise figure of 2.2 dB and gain of 15 dB is realizable at a bias current of 2.5 mA per transistor and $Lee = 0.8 \text{ nH}$, with a coincident noise and power match at the input.

IV. EXPERIMENTAL RESULTS

The test IC was packaged in a 32-pin ceramic quad flatpack (CQFP) and mounted in a custom test fixture for evaluation, using the configuration shown in Fig. 11. The RF and LO signals are delivered to the IC differentially via 50- Ω microstrip lines. Losses for the RF input signals (including connectors) in the fixture are approximately 1 dB.

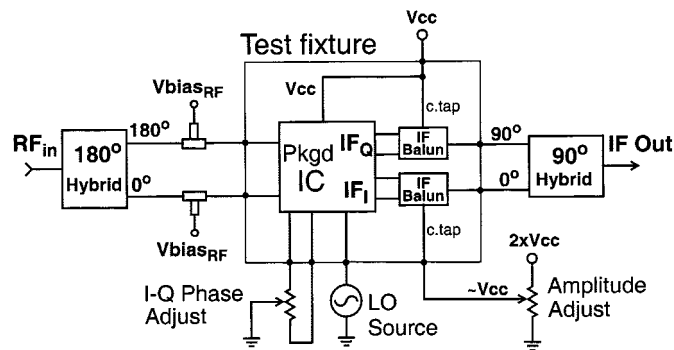


Fig. 11. Experimental test configuration.

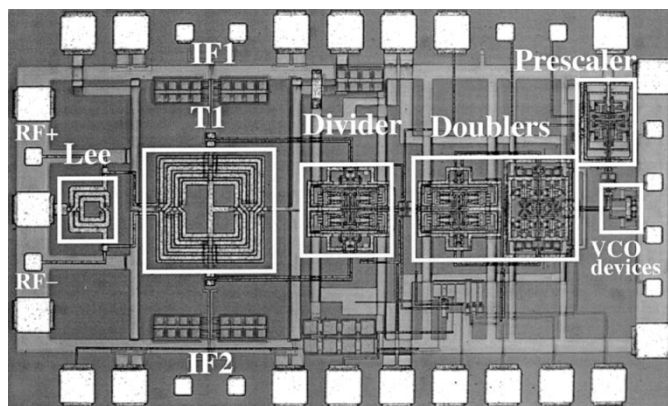


Fig. 12. Photomicrograph of the receiver IC.

A photomicrograph of the receiver RF IC is shown in Fig. 12. The main circuit blocks are highlighted and annotated on the figure. The overall die size is $1.9 \times 1.2 \text{ mm}^2$, which includes the bonding pads. The active area is considerably smaller, as extra bondpads were added to aid in testing. Substrate coupling between the multiplier, divider, mixer, and LNA circuits is minimized through component separation in layout, separate supply bussing and the use of grounded p+ diffusion guard rings to isolate the various blocks. This, in addition to the use of fully differential RF, LO, and IF signals, results in greater than 60 dB of isolation for the packaged device in the test fixture.

Discrete transformer baluns with a 4 : 1 turns ratio are used to present a differential impedance of approximately 800 Ω at the open-collector mixer outputs of the test chip. The IF baluns have a minimum loss of 1.3 dB at 75 MHz, thereby restricting the IF used for measurement. A lower turns ratio discrete balun operates at a higher IF but with a lower impedance transformation, which reduces the overall conversion gain. To compensate for parasitic losses and mismatches, a three element matching network was designed to match the balun output to the (50 Ω) quadrature IF combiner of Fig. 11.

As can be seen in Fig. 11, potentiometers are used to adjust the amplitude (via the supply voltage of one of the mixers) and phase (via bias current of the quadrature LO frequency divider) in the I and Q paths to maximize the image rejection. It is proposed that in a real application, these controls would be set during a self-calibration period upon startup or during idle times. A digital or analog tau-dither-type feedback circuit

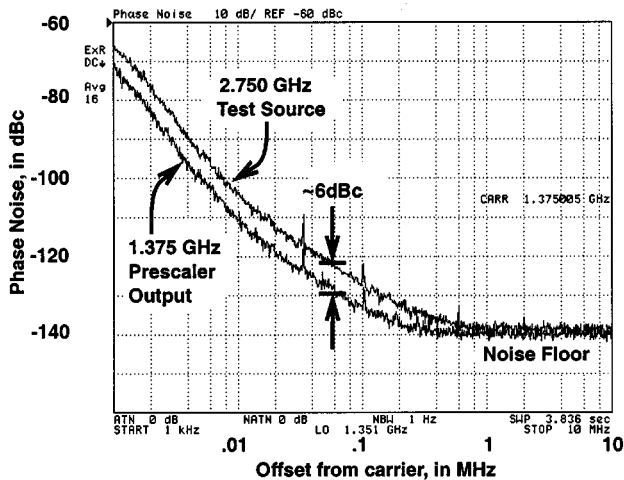


Fig. 13. Measured single sideband phase noise of the prescaler. $V_{CC} = 2$ V.

[23] could alternately adjust phase and amplitude controls for maximum rejection of an internally generated test carrier in the image band (e.g., generated by the transceiver's up-converter). The received signal strength indicator (RSSI) found in most demodulator systems could be used to measure image-rejection during calibration. The phase errors in the LO were measured at less than 0.011° (as inferred from the measured image rejection) by manually following this routine. This level of I - Q accuracy cannot be achieved without the use of trimming, tuning, or self-calibration techniques.

The entire chain (multipliers and divider) is locked from a -18 dBm input (LO) signal source over the frequency range of 1.9 to 3.2 GHz, which in turn generates I and Q output signals for the mixers in the range from 3.8 to 6.4 GHz. The $4 \times$ LO frequency range that is generated and fed to the mixer divide-by-two is 7.6 to 12.8 GHz, which is greater than one-half of the 25-GHz transistor unity gain frequency. This very high fraction of f_T is achieved through the use of regenerative circuits. The power dissipation of the entire LO subsystem (excluding the optional LO prescaler) is 44 mW from a 2.2-V supply. All undesired harmonics, including the fundamental ($f_{LO}/2$) input, are suppressed by over 30 dBc in the f_{LO} output for single-ended excitation, and by more than 35 dBc for a differential input source.

It should be noted that the power dissipation of the LO system reported here is 11 mW higher than the 22 mW reported in [18]. The receiver IC was modified to lower the center frequency and broaden the locking bandwidth. This increase in power affords an increase in the relative locking bandwidth from 26% (previously) to over 50%. The added margin may not be necessary for a 5–6-GHz receiver application, but it clearly illustrates the ability to achieve a very wide operating range using injection-locking techniques.

The prescaler dissipates 1.5 mW from a (minimum) 1.5-V supply and remains locked over an input frequency range of 600 MHz to 4.0 GHz (for a -6 dBm LO input signal to the IC). It should be noted that this type of regenerative divider does not have any other dominant modes of division (other than divide-by-two) and so unpredictable mode locking to unwanted harmonics is not a concern.

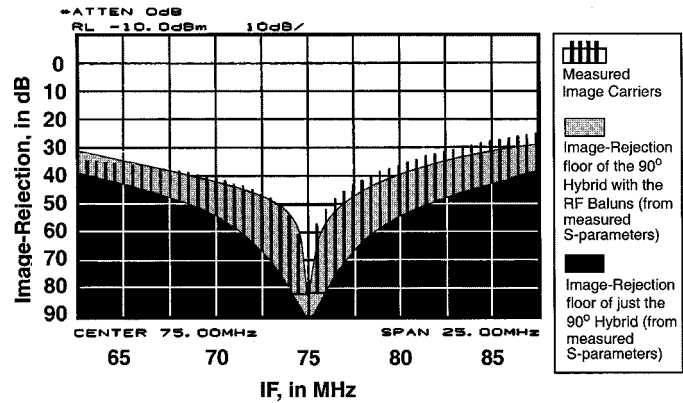


Fig. 14. Measured image rejection for a 75 MHz IF (test set-up of Fig. 11).

The single sideband phase noise of the prescaler output is plotted in Fig. 13. A supply voltage of 2.2 V (4.3-mW power dissipation in the prescaler) is used for the measurement. This is consistent with the bias conditions for the other injection-locked circuits in the LO system. The phase noise of the divider output closely follows the theoretical 6-dB improvement compared to the phase noise for the input source predicted for an ideal divide-by-two. The noise floor of the analog divider is less than -140 dBc (i.e., noise floor of the test instrument) with no spurious components. From this result, it can be inferred that the I and Q outputs at f_{LO} driving the downconverting mixers have close to 6 dB greater phase noise than the $f_{LO}/2$ input carrier (the theoretical minimum), since the analog regenerative technique used for frequency dividing in the prescaler is also used for frequency doubling and dividing in the LO chain.

The measured image rejection (IR) over a wideband using a discrete 90° quadrature IF combiner centered at 75 MHz is plotted in Fig. 14. The black-shaded IR floor (i.e., lower bound on IR) shows the lowest possible IR for the 90° external IF combiner employed in the test setup. This floor was calculated from s -parameter measurements of the combiner, which characterize its frequency dependent phase and amplitude variations. Prior to computing the maximum IR, systematic phase and amplitude offset errors are subtracted from the measured parameters to center the maximum rejection at 75 MHz, thereby simulating an ideal trim of phase and amplitude errors. The grey-shaded region in Fig. 14 shows the lowest possible image rejection when the s -parameters of the IF combiner, transformer baluns, and matching stages are considered. The vertical lines are actual measurements of the image suppression, showing the wideband performance achieved experimentally. A maximum IR of approximately 80 dB is obtained at the 75-MHz center frequency. This implies that a phase-tuning precision of better than 0.01° is achieved by adjusting I - Q phase relationship via the frequency divider stage. Also, the measured IR is within ± 5 dB of the maximum IR predicted for this test setup. Discrepancies between the measured and expected results (i.e., vertical lines and the grey-shaded region) are likely due to component variations. The grey-shaded region is estimated for s -parameters of a single transformer balun and does not account for variations between the two baluns and matching networks actually used in the experimental setup.

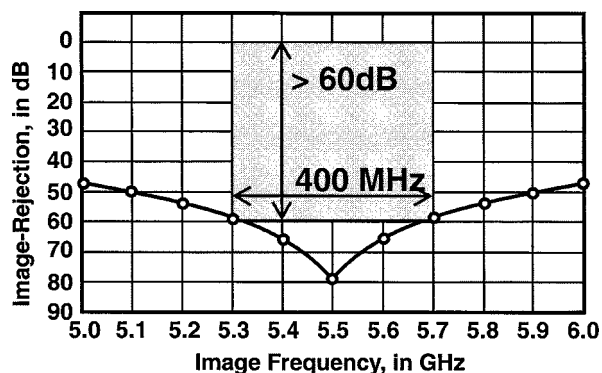


Fig. 15. Image rejection across the RF band for a swept RF LO. IF = 75 MHz.

TABLE I
SUMMARY OF EXPERIMENTAL MEASUREMENTS

Parameter	25 GHz f_T Silicon Bipolar			45 GHz f_T SiGe [ref. 5]
	5.3	5.8	5.5	5.8
RF Input, GHz	5.3	5.8	5.5	5.8
VCO Input Frequency, GHz	2.6875	2.9375	2.7875	5.55 (no VCO)
IF, MHz	75			250
Supply Voltage, V	2.2		2.34	1.8
Conversion Gain, dB	15.1	14.9	17.0	14.2
Input IP3, dBm	-9.4	-10.5	-4.5	-5.9
RF Input Return Loss, dB	14.0	14.6	14.3	(wafer probe)
SSB Noise Figure (50 Ω), dB	5.1			6.8
LO to RF Isolation, dB	60			63
Maximum Image Rejection	80dB (tuned at center of IF) implies 0.01 $^\circ$ precision in phase			36.5 dB
Power Dissipation, mW	44.4		55.0	18.5

A measurement of the image rejection was also performed with a constant IF of 75 MHz. The purpose of this test is to measure the phase and amplitude variations of the I and Q LO outputs driving the mixers as a function of the LO frequency. In order to do this, the RF and LO frequencies are swept together across the 5–6-GHz band maintaining a constant frequency difference of 75 MHz between them. The phase and amplitude of the LO is trimmed only once for maximum IR with an RF input at the center of the 5–6-GHz band (i.e., 5.5 GHz) prior to beginning the sweep. As shown in Fig. 15, this results in an image rejection of nearly 80 dB. As the RF (and LO) is swept away from 5.5 GHz, the image rejection decreases because of increasing phase and amplitude errors in the quadrature LOs, however, between 5.1–5.8 GHz the IR is maintained at better than 50 dB without retuning. The results of this test infer that the phase variations in the LO are less than 0.064 $^\circ$ over a 1-GHz sweep.

Table I lists a summary of the measured results of the receiver's performance. An IF of 75 MHz was used. It should be noted that the IF is not restricted by the receiver topology. The RF input is unmatched externally, however, an input return loss >-14 dB was measured across the receive band. The minimum conversion gain measured for the receiver is approximately 15 dB across the 5.3–5.8-GHz band, which is close to the design value. A relatively low overall single sideband noise figure (50 Ω) of 5.1 dB was measured along with an input third-order intercept of -9.4 dBm, giving the receiver a wide dynamic range despite the low supply voltage (2.2 V) and bias

current (10 mA) used for the LNA and mixers. These results compare very favorably with those reported for similar designs in the same technology at 1–2 GHz as well as other 5–6-GHz designs [8], [24]–[26].

A significant improvement in both gain and linearity is realized when the supply voltage is raised from 2.2 to 2.34 V. This is due to the larger LO signal drive presented to the mixer quads as a result of increased voltage headroom. At 2.34 V, the conversion gain rises to 17 dB and the input intercept point (IIP3) improves by 5 dB to -4.5 dBm, while the noise figure is unchanged.

V. CONCLUSION

A 5–6-GHz image-reject receiver IC is implemented in a 0.5- μ m 25-GHz silicon bipolar technology that draws just 22 mA from a 2-V supply. The image rejection obtainable with this IC (up to 80 dB) is sufficient to eliminate the off-chip interstage RF filter in a heterodyne receiver, thereby simplifying packaging requirements and decreasing costs. New methods of regenerative frequency doubling, I - Q phase error compensation, and RF interstage coupling make this design possible. Low-voltage circuit topologies are used throughout to minimize power consumption and ensure compatibility with deep-submicron CMOS (baseband) application-specific integrated circuits (ASICs) operating from low-voltage supplies. The wide dynamic range and low power consumption of this receiver IC demonstrates that silicon technology is capable of addressing the requirements for RF interfaces in emerging applications at 5–6 GHz.

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