Experimental Analysis of Thermal Coupling in 3-D Integrated Circuits

Ioannis Savidis, *Member, IEEE*, Boris Vaisband, and Eby G. Friedman, *Fellow, IEEE*

***Abstract*— A 3-D test circuit examining thermal propagation within a through-silicon via-based 3-D integrated stack has been designed, fabricated, and tested. Design insight into thermal coupling in 3-D integrated circuits (ICs) through both experiment and simulation is provided, and suggestions to mitigate thermal effects in 3-D ICs are offered. Two wafers are vertically bonded to form a 3-D stack. Intraplane and interplane thermal coupling is investigated through single-point heat generation using resistive thermal heaters and temperature monitoring through four-point resistive measurements. Thermal paths are identified and analyzed based on the metric of thermal resistance per unit length. The peak steady-state temperature due to die location within a 3-D stack is described. The reduction in peak temperature through fan-based active cooling is also reported. Thermal propagation from a heat source located on the backside of the silicon is examined with both back metal and on-chip thermal sensors. A comparison of thermal coupling between two different heat sources on the same device plane is also provided.**

***Index Terms*— 3-D heat transfer, 3-D integrated circuit (IC), 3-D thermal effects, thermal propagation.**

I. Introduction

TWO of the most omnipresent and challenging issues in high-performance 3-D systems are power delivery and thermal management. The interdependence of these issues is of critical importance to 3-D systems, as high current loads on the power network can produce severe hot spots within a 3-D stack. The effect of hot spots on circuit operation is well documented in 2-D integrated circuits (ICs) [1] and is greatly exacerbated in 3-D ICs, requiring novel thermal mitigation and management techniques. Enhanced understanding of these interrelated design challenges in 3-D integration is therefore necessary to develop design techniques and methodologies to effectively deliver power while managing thermal effects.

Through-silicon via (TSV)-based 3-D ICs have rapidly progressed over the past decade to continue the trend of higher transistor density. Although possible to reduce system-level power with 3-D ICs by reducing the length of the global interconnect, vertical stacking of computational blocks within a smaller footprint increases the power density within the 3-D IC [2]–[4]. In addition, stacking device planes (interchangeable with the term dies) limits the thermal pathways available to efficiently remove heat from those dies farthest from the heat sink. A schematic depiction of a two-die stack with a hot spot on one die affecting the second die is shown in Fig. 1. The increased thermal profile due to the higher power density and the lack of thermal conduits remains a limiting issue for 3-D ICs.

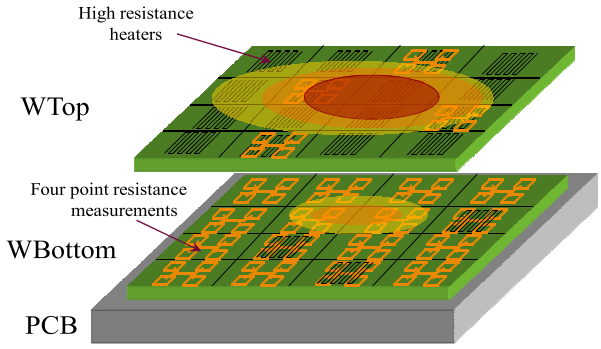

Fig. 1. Heat propagation from one device plane spreading into a second stacked device plane.

Prior work has focused on the simulation [5] and modeling [6]–[8] of hot-spot formation and propagation within 3-D ICs. Tools such as 3-D-ICE [9] and a 3-D extension to HotSpot [10], [11] to model thermal profiles of 3-D circuits have been developed and provide a visual interpretation of hot-spot formation based on the power requirements of each device plane. Models and simulations have been extended to block level floorplanning including global wire congestion, permitting the location of the highly active blocks within a 3-D IC to be adjusted based on the location of the thermal hot spots [12], [13], [15], [18]. Additional mitigation techniques, including the use of passive techniques such as thermal TSVs (TTSVs) [16] and active techniques such as microchannel or microfluidic cooling [17], [22], have been proposed to address heat removal in 3-D ICs.

Although extensive theoretical work has provided an understanding of heat flow in 3-D ICs, there have been limited experimental results quantifying the flow of heat between device planes. Meindl *et al.* [19], King *et al.* [20], and Dang *et al.* [21] experimentally characterized the effect of microfluidic cooling techniques on both 2-D and 3-D circuits. Additional experimental results have characterized microfluidic cooling methods [22]. Experiments characterizing

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I. Savidis is with the Department of Electrical and Computer Engineering, Drexel University, Philadelphia, PA 19104 USA (e-mail: isavidis@coe.drexel.edu).

B. Vaisband and E. G. Friedman are with the Department of Electrical and Computer Engineering, University of Rochester, Rochester, NY 14627 USA (e-mail: bvaisban@ece.rochester.edu; friedman@ece.rochester.edu).

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an interplane cooling system for a vertically stacked dynamic RAM (DRAM)/multiprocessor system-on-chip have been described [23]. Numerical and experimental characterization of thermal hot spots within a packaged DRAM-on-logic 3-D IC has also been described [24]. Similar to this paper, interplane thermal propagation was investigated. The primary purpose of the results described in this paper, however, is to characterize intraplane and interplane thermal coupling to improve design methodologies and techniques for stacked ICs. The experimental results discussed herein provide insight into the effects of the location of the heat source and active cooling on thermal gradients within 3-D ICs.

A test circuit has been fabricated by Tezzaron semiconductor in a 130-nm CMOS technology with 1.2-μm diameter TSVs. A face-to-face bonding technique to vertically stack the two logic device planes is used. This test circuit is designed to also evaluate the effects of interplane and intraplane thermal resistance on hot-spot formation.

This paper is composed of the following sections. A theoretical model of thermal flow is presented in Section II. The thermal propagation test circuit is described in Section III. The experimental characterization of thermal coupling for a set of test configurations is presented in Section IV. A discussion of the experimental results including the effects of hot-spot formation and mitigation techniques is provided in Section V. A comparison of the experimental results with simulations is provided in Section VI. Some conclusions are offered in Section VII.

II. Model of Thermal Flow

Thermal flow in materials is described by the Fourier law

$$\vec{q} = -k \cdot \nabla T. \tag{1}$$

Thermal analysis within a 3-D structure is based on the heat flux density (the energy that flows through a unit area per unit time, or alternatively, the amount of power that flows through a unit of area) ($\vec{q}$) [W/m^2], the thermal conductivity, a property of the material (k) [W/m·°C], and the temperature gradient ($-\nabla T$) [°C/m]. To avoid a computationally expensive analysis, the 3-D form in (1) is reduced to a 1-D form, as described by (2). This simplification is sufficiently accurate in 3-D structures [25] as any thermal path may be decomposed into vector components in either the horizontal or vertical dimension. The diagonal paths (in both the horizontal and vertical dimensions) may be superimposed using 1-D segments

$$q_x = k\frac{dT}{dx}. \tag{2}$$

Integrating both sides of (2) and assuming that the material in each layer is uniform, the heat transfer equation becomes

$$Q = kA\frac{\Delta T}{\Delta x} \tag{3}$$

where Q [W] is the heat transfer rate and A [m^2] is the surface area through which the heat is transferred.

Analogous to electrical interconnect, thermal conduits are characterized in terms of the thermal resistance R_{th} [°C/W] [25]. A thermal analogy to Ohm's law is described by

$$R_{\text{th}} = \frac{\Delta T}{Q} \Longleftrightarrow R = \frac{\Delta V}{I} \tag{4}$$

where R_{th} is analogous to the electrical resistance R, ΔT is analogous to the difference in electrical potential ΔV, and Q is analogous to the electrical current I. Substituting (3) into (4) yields a linear relationship between the thermal resistance and thermal conductivity, which is analogous to the linear relationship between electrical resistance and electrical conductivity as

$$R_{\text{th}} = \frac{1}{k} \cdot \frac{\Delta x}{A} \Longleftrightarrow R = \frac{1}{\sigma} \cdot \frac{L}{A}. \tag{5}$$

The thermal resistance per unit length is an effective metric to characterize the thermal behavior of the horizontal and vertical paths

$$\frac{R_{\text{th}}}{\Delta x} = \frac{1}{k} \cdot A. \tag{6}$$

Previous literature [26]–[30], dating to the early 1960s, has explained that within the relevant range of temperatures (−55 °C to 125 °C), k decreases with higher temperatures in materials commonly used in ICs (e.g., silicon, aluminum, and tungsten). For example, the thermal conductivity of silicon decreases by 47% with an increase in temperature, from 190 (W/m·°C) at −53.2 °C to 100 (W/m·°C) at 126.9 °C [26]–[28].

III. Thermal Propagation Test Circuit

A 3-D test circuit comprised two silicon layers with back metal on one of the device planes has been fabricated to experimentally analyze horizontal and vertical thermal coupling in 3-D ICs. The experimental results are useful for evaluating thermal propagation paths within TSV-based 3-D structures.

A. 3-D IC Fabrication Technology

Each device plane is individually processed in a 130-nm CMOS technology, provided by Chartered Semiconductor, before 3-D bonding, TSV fabrication, and wafer thinning by Tezzaron. The chartered fabrication process includes low-power 1.5 and 2.5 V transistors, six metal layers per device plane, a single polysilicon layer, dual gates for the 2.5 V transistors, and low and nominal threshold devices [31]. The sixth metal level on each die is allocated for face-to-face bonding to vertically stack the two logic device planes.

B. Test Circuit Design

The test structures are used to investigate thermal coupling between adjacent planes and include both resistive thermal sources and thermal sensors. The thermal sensors use four-point voltage measurements. Each thermal source is paired with a resistive thermal sensor on an adjacent metal level, and these pairs are distributed throughout each plane within a two layer 3-D logic stack. The heaters are

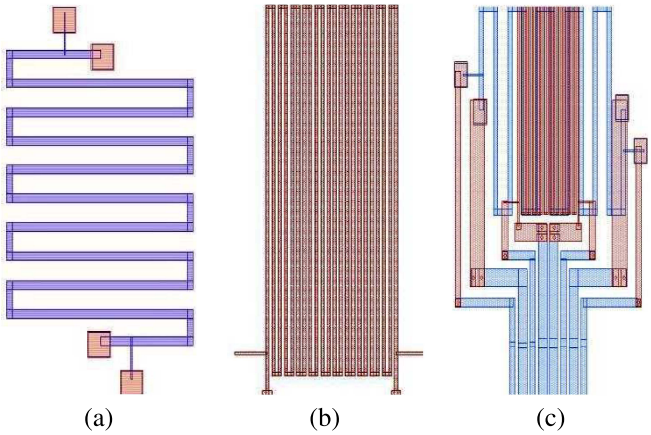

Fig. 2. Physical layout of the (a) on-chip resistive heater, (b) on-chip four-point resistive thermal sensor, and (c) overlay of the resistive heater and resistive thermal sensor.

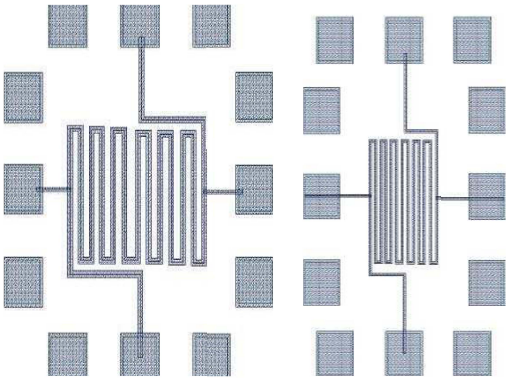

Fig. 3. Physical layout of the (a) back metal resistive heater, and (b) back metal four-point resistive thermal sensor.

200 μm × 210 μm, similar to the dimensions of the heaters in [24], and are in metal 2. Within this area, the total length of the heater is 2120 μm. The thickness of metal 2 is 0.42 μm, the width is 6 μm, and metal 2 has a nominal sheet resistance of 0.053 Ω/□. The resistance of the heaters is therefore 18.7 Ω. Joule heating through the resistive heater is adjusted by controlling the current flow. The thermal sensors, with dimensions of 200 μm × 86 μm, are placed directly above the heaters in metal 3. The thermal sources are heater resistors with a maximum applied voltage of 28 V, producing a maximum applied current of 1.5 A. The total length of the sensors is 4442 μm. The resistance of the sensors is 117.7 Ω based on a width of 2 μm, a metal 3 thickness of 0.42 μm, and a nominal sheet resistance of 0.053 Ω/□. The temperature sensor provides a calibrated four-point measurement tested at a low current to avoid joule heating. The resistive heater, thermal sensor, and combined heater and sensor are shown in Fig. 2.

Similar resistive heaters and thermal sensors are included in the aluminum backside metal layer, as shown in Fig. 3(a) and (b). The differences between the heaters and sensors located in the logic planes and the backside metal include: 1) the heaters and sensors are not vertically stacked on adjacent metal layers as in the logic planes, as there is only a single backside metal layer; 2) the backside metal layer is almost three times the thickness of either metal 2 or 3 (1.2 μm as compared with 0.42 μm); and 3) due to the greater width and thickness, larger currents can pass through the backside metal. The heaters and sensors on the backside metal support thermal coupling through the thinned silicon to the thermal sensors on the internal logic layer, providing enhanced understanding of the effects of thermal spreading through the silicon to the neighboring device planes.

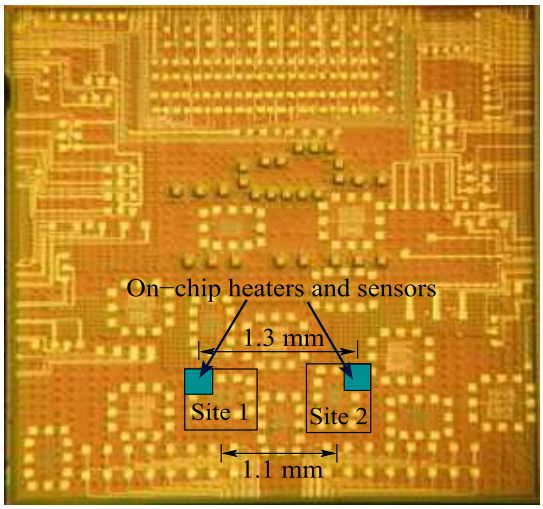

Fig. 4. Microphotograph of the test circuit depicting the back metal pattern with an overlay indicating the location of the on-chip thermal test sites.

The location of the on-chip thermal sensors and resistive heaters with respect to the backside sensors is shown in Fig. 4. A microphotograph of the 5 mm × 5 mm 3-D IC depicts two locations from which thermal data are collected. The center-to-center distance between the back metal sensors is 1.1 mm, while the on-chip sensors are 1.3 mm apart. A cross-cut view of the complete 3-D IC stack is shown in Fig. 5. Each device plane, labeled as WTop and WBottom in the figure, includes a thermal sensor on metal 3 and a resistive heater on metal 2. The backside metal heaters and sensors are at the top of the stack, as shown in Fig. 5. In addition, the thickness of both the WBottom silicon and the active portion of the test structure is included in the illustration shown in Fig. 5, indicating a significantly smaller thermal resistive path to the top of the 3-D stack rather than to the board below.

TSVs with 1.25-μm diameter are placed 100 μm apart across both WTop and WBottom. The effects of the TSVs on the thermal propagation process are minimal. The focus of the test circuit is to investigate horizontal and vertical thermal coupling in stacked ICs. In addition, more recent work has indicated that placing excessive TSVs, particularly TSVs with small diameters where a larger portion of the area is occupied by insulating material (i.e., SiO_2), actually increases the on-chip temperature as the insulating material has poor heat conducting properties as compared with the silicon it replaces [32]. The more critical parameter influencing the heat dissipation characteristics is the physical nature of the silicon substrate [33].

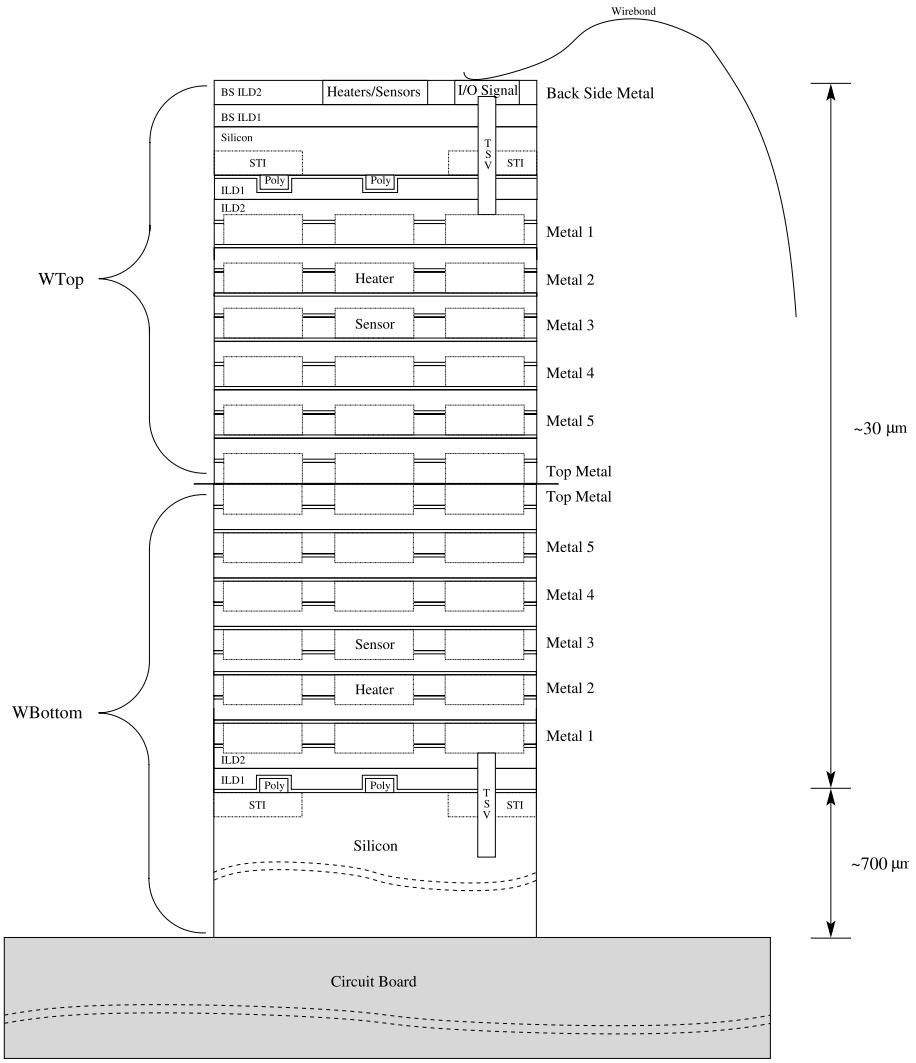

Fig. 5. Placement of thermal heaters and sensors, respectively, in metals 2 and 3 in the two stacked device planes. The placement of the back metal heaters and sensors is also shown.

IV. Setup and Experiments

The on-chip and back metal thermal sensors require calibration prior to the experimental analysis of thermal coupling between logic planes. Calibration is performed by setting the die temperature through a thermal chuck and measuring the resistance of the sensors at each temperature from room temperature (27 °C) to 120 °C. The resistance as a function of temperature for each calibrated sensor is shown in Fig. 6. All of the sensors exhibit a linear response to temperature. The on-chip sensors, shown in Fig. 6(a), produce consistent results on the same logic layer. A difference in resistance exists between the top and bottom logic layers, as shown in Fig. 6(a). Within a given die, the sensors produce consistent results, demonstrating that the thermal sensors can be calibrated from a single sensor. This behavior, however, is not the case with the back metal sensors, as shown in Fig. 6(b). The difference in resistance between the two sites on the back metal reveals greater process variations on the back metal layer than the on-chip metal layers, requiring each thermal sensor to be individually calibrated and normalized at room temperature.

The experimental setup includes the use of an HP 4145B semiconductor parameter analyzer and an HP 16058-60003 Personality Board. In addition, Interactive Characterization Software from Metric Technology Inc. is used to determine the settings for the parametric analyzer. A Keithley 2420 SourceMeter is used as a current source to supply the on-chip and back metal heaters with current ranging from 0 to 110 mA (130 mA for the back metal). The parametric analyzer sweeps the voltage on the sensor from 0.1 to 0.6 V in 0.01 V increments, which permits the average resistance to be determined across this voltage range. Measurements are made at each site and each sensor (a total of six data locations) for each current value. In addition, there are six different heater locations, as shown in Fig. 5. The resistance measurements are converted to temperature based on the results shown in Fig. 6.

The resistive heaters are controlled to provide different test conditions to emulate common on-chip devices and to investigate the effects on the temperature profile and thermal conduits within the 3-D stack. A current is individually supplied to the heaters on WBottom and WTop. These results are shown in Fig. 7(a) and (b). The power density of the resistive heaters

TABLE I
POWER DENSITY VALUES FOR COMMON ON-CHIP CIRCUITS

Circuit	Description	Power density [$Watt/mm^2$]	Reference
Power transistor	Output stage of a Buck voltage converter	32.5	[34]
SC	Switched capacitor converter for different technologies	0.77 to 4.6	[35]
PWM	Pulse width modulator	1.39	[36]

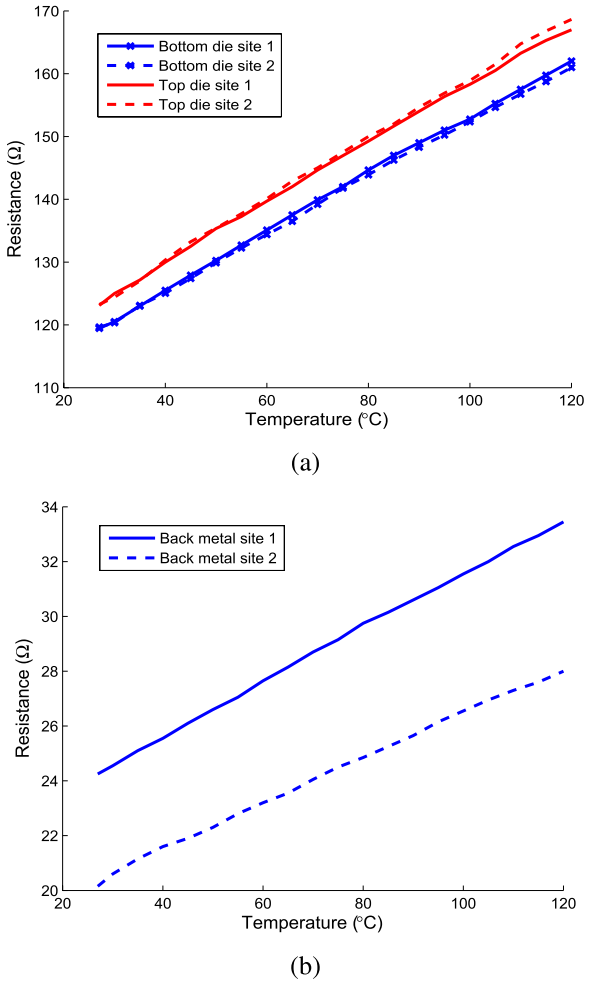

Fig. 6. Calibration of (a) on-chip thermal sensors, and (b) back metal thermal sensors.

ranges up to 17.4 W/mm^2 for the heaters placed on metal 2 of each die and up to 24.3 W/mm^2 for the heaters placed on the back metal (determined from the currents, resistances, and effective areas). The power density of the common on-chip devices is listed in Table I. Note that the power density generated in these experiments is consistent with practical circuits.

The results from different test conditions are shown in Fig. 7. The effects of the metal heat spreaders (metal interconnect) on the in-plane thermal profile are examined by removing the metal heat spreaders that surround the sensors and heaters located at WTop site 2. The results from this experiment are shown in Fig. 7(c) and compared with the experimental results from WTop site 1 shown in Fig. 7(b). The effects of placing two highly active device blocks on the thermal gradients are explored. In this case, two separate conditions are examined: 1) the heaters on WBottom and WTop are simultaneously active and stacked directly above each other, and 2) the heaters on WBottom and WTop are simultaneously active and physically nonaligned. These results are shown in Fig. 7(d) and (e). A fourth test condition is used to evaluate the flow of heat from a back metal heat source to the on-chip thermal sensors. One of the two back metal sensors operates as a heater, while the other sensor detects the temperature. The effects of placing the CMOS 3-D IC in a location where heat may couple from the backside of a thinned silicon substrate are shown in Fig. 7(f). The final test condition examines the effects of active cooling on heat dissipation within a stacked IC. A 12 V, 0.13 A, 6500 RPM, and 8 CFM (cubic feet per minute) fan is placed 1 inch above the 3-D stack for convective heat removal. The fan is used for three different resistive heater conditions: 1) active heater in WBottom site 1; 2) active heater on WBottom and WTop site 1; and 3) active heater on back metal site 1. The results of this cooling experiment are shown in Fig. 7(g)–(i).

V. DESIGN CONSIDERATIONS BASED ON THE EXPERIMENTAL RESULTS

The experimental test conditions described in Section IV provide insight into the thermal propagation paths and hot-spot formation within 3-D ICs. All of the test configurations include heaters placed in metal 2, which emulate the heat generated by the active devices within a device plane. Design considerations to minimize hot-spot formations are discussed below.

A. Effect of Block Placement on Hot-Spot Formation and Mitigation Techniques

The effects of stacking two dies on the temperature profile of a 3-D IC are significant, as shown in Fig. 7(a) and (b). The maximum observed temperature on WBottom site 1 increases by 65.7% when the resistive heater is active on WBottom as compared with an active heater on WTop (100.9 °C from 60.9 °C), as shown in Table II. The maximum observed temperatures occur for the maximum applied current of 110 mA. For heater currents less than 110 mA, the percent increase in temperature for WBottom as compared with WTop decreases due to the exponential drop in temperature as the current is reduced. Data from the remaining five thermal sensors reveal a temperature increase of 6.1% to 13.0% (Table II), with the 13.0% increase occurring on the sensor located directly above the active heater on WTop. Although the measured temperature is lower at the thermal sensors 1.3 mm away from the hot spot, the drop is not as significant, as reported in [24], where over a 50% drop in temperature is measured at a distance of 500 μm. The observed temperature

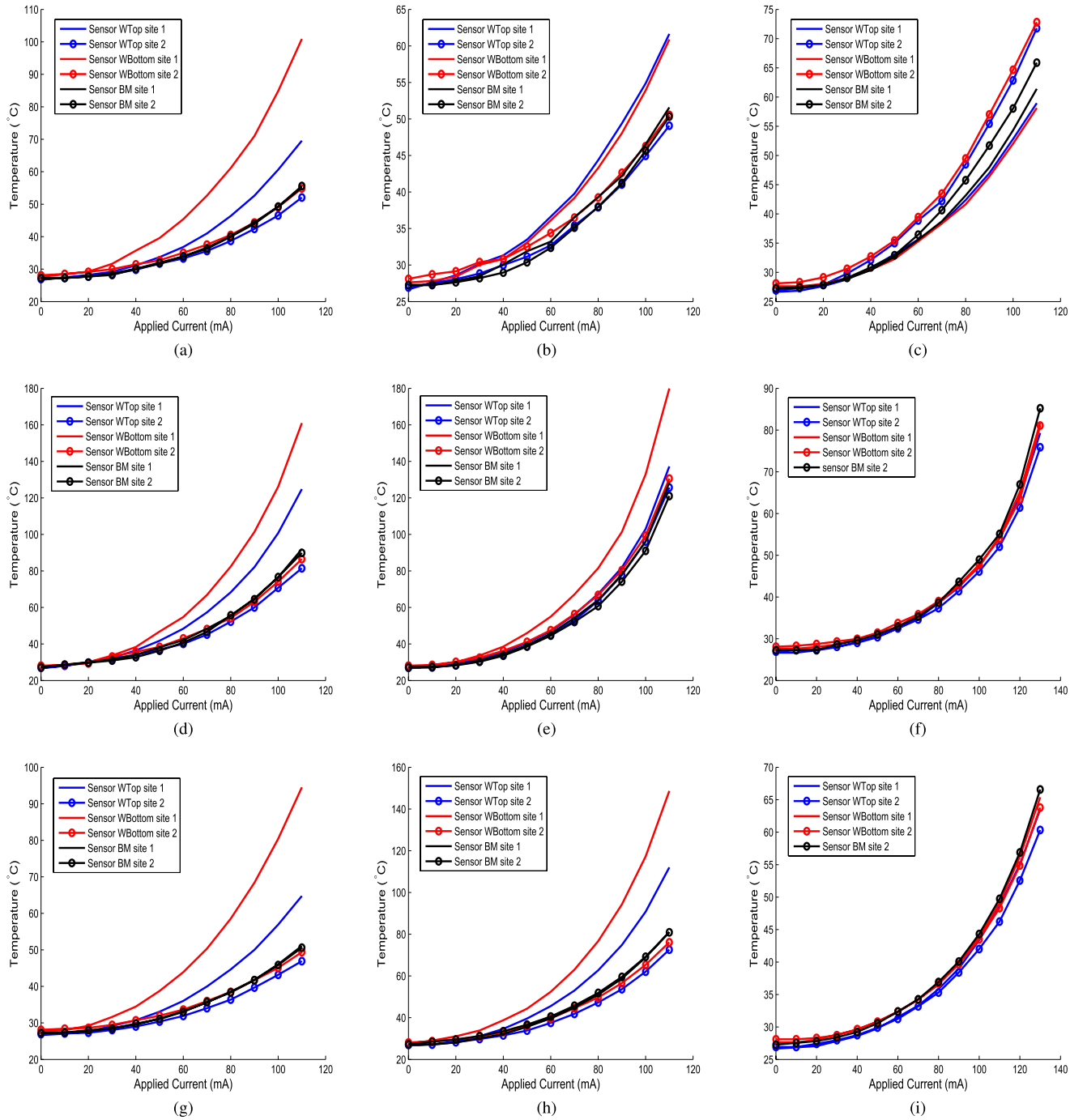

Fig. 7. Experimental results for the different test conditions. Each label describes the device plane, site location of the heater, and whether active cooling is applied. (a) WBottom site 1; no fan. (b) WTop site 1; no fan. (c) WTop site 2; no fan. (d) WBottom site 1, WTop site 1; no fan. (e) WBottom site 1, WTop site 2; no fan. (f) Back metal site 1; no fan. (g) WBottom site 1; fan. (h) WBottom site 1, WTop site 1; fan. (i) Back metal site 1; fan.

on WBottom when a resistive heater is active on WBottom site 1 is within 20% of the measured temperature at the same WBottom sensor when an active heater is on WTop site 1, for all heater currents less than 50 mA. Placing a highly active device block in WBottom requires special consideration as the thermal resistance along the path to the top of the 3-D stack is higher than to a block placed in WTop.

Three potential mitigation techniques can be considered. During placement and routing, blocks with high current loads can be placed in those locations that minimize the thermal resistance between the block and the heat sink. The current load greatly affects the thermal profile (as revealed by less than a 20% change in temperature for currents less than 50 mA). Another approach to control the activity of the block is to ensure that the average current load remains below an acceptable value, thereby not forming hot spots. Passive and active cooling techniques such as TTSVs and microfluidic channels can also be used to remove heat from the internal device planes by changing the thermal resistive paths within the highly active circuit blocks.

TABLE II

PERCENT INCREASE IN TEMPERATURE WHEN ACTIVE CIRCUIT IS LOCATED IN INTERNAL PLANE (WBOTTOM)

Heater location	Sensor location	Current (mA)											
		0	10	20	30	40	50	60	70	80	90	100	110
WBottom, Site 1	WTop, Site 1	0.00	-0.72	-1.39	-3.31	-0.64	0.60	0.55	3.02	4.50	6.48	10.38	12.99
% increase as compared to	WTop, Site 2	0.00	-0.73	-1.42	-1.04	-0.67	1.93	1.83	0.56	2.11	3.41	3.56	6.11
WTop, Site 1	WBottom, Site 1	0.00	2.16	2.82	5.33	15.91	19.64	25.76	34.44	41.11	47.61	57.33	65.68
	WBottom, Site 2	0.00	-0.70	0.00	-1.32	2.27	0.62	1.74	3.01	3.32	3.99	6.05	8.50
	Back Metal, Site 1	0.00	0.00	0.36	1.77	3.79	3.95	4.63	4.27	5.53	7.77	7.66	9.54
	Back Metal, Site 2	0.00	0.00	-0.36	-1.05	0	0.31	2.11	-0.55	1.78	4.03	5.81	7.75

TABLE III

PERCENT INCREASE IN TEMPERATURE FROM INTRAPLANE THERMAL SPREADING

Heater location	Sensor location	Current (mA)											
		0	10	20	30	40	50	60	70	80	90	100	110
WTop, Site 2	WTop, Site 1	0.00	-2.81	-3.39	-4.52	-1.87	-1.17	-2.69	-3.48	-4.50	-4.89	-3.71	-4.35
% increase as compared to	WTop, Site 2	0.00	-0.70	-0.68	3.33	7.06	12.39	18.97	19.24	27.89	35.09	39.83	46.23
WTop, Site 1	WBottom, Site 1	0.00	-0.72	-1.41	-3.35	-1.31	-2.45	-2.25	-2.09	-3.81	-3.46	-3.50	-4.53
	WBottom, Site 2	0.00	-1.45	0	0.69	6.12	9.06	14.73	19.17	26.08	33.75	39.77	44.05
	Back Metal, Site 1	0.00	0.00	0.34	1.32	0.94	2.38	7.15	6.01	9.77	13.73	16.74	19.05
	Back Metal, Site 2	0.00	0.69	0.68	3.01	6.52	8.41	12.62	15.78	20.50	25.35	27.14	30.94

TABLE IV

PERCENT INCREASE IN TEMPERATURE WHEN TWO ACTIVE CIRCUIT BLOCKS ARE VERTICALLY ALIGNED

Heater location	Sensor location	Current (mA)											
		0	10	20	30	40	50	60	70	80	90	100	110
WTop, Site 1 and	WTop, Site 1	0.00	2.12	6.89	11.35	17.01	24.05	31.40	39.88	47.29	55.98	66.19	79.43
WBottom, Site 1	WTop, Site 2	0.00	2.81	7.62	12.15	14.22	16.45	20.41	26.85	35.03	41.58	52.10	56.47
% increase as compared to	WBottom, Site 1	0.00	0.71	2.76	6.40	7.43	18.24	20.72	27.04	34.85	42.77	48.64	59.55
	WBottom, Site 2	0.00	0.00	0.72	10.48	13.36	17.40	22.97	28.33	33.81	42.36	51.18	57.61
WBottom, Site 1	Back Metal, Site 1	0.00	4.49	7.82	10.53	13.22	20.76	24.25	32.03	37.98	46.12	55.42	66.86
	Back Metal, Site 2	0.00	5.18	7.13	9.70	8.80	13.66	20.28	28.60	39.29	46.81	55.63	61.65

B. Horizontal and Vertical Thermal Conduits

The experiment examining in-plane thermal spreading [Fig. 7(b) and (c)] requires additional design consideration. By removing the in-plane metal heat spreaders surrounding the thermal sensors and resistive heaters, the ability of heat to spread horizontally is diminished. The maximum temperature from a sensor directly above an active heater in WTop site 2 is 16.4% higher than an active heater in WTop site 1 for a heater current of 110 mA. All other sensors exhibit temperatures 14.9% to 27.7% higher than when metal heat spreaders are present and a 110-mA heater current is applied, as listed in Table III. The increase in temperature at site 2 when the heater on WTop site 2 is active is expected; however, the lower temperature indicated by the negative change for the on-chip sensors at site 1 is not as large as expected. The thermal resistance from site 2 to the heat sink is larger as the horizontal metal heat spreaders have been removed, resulting in higher on-chip temperatures. Placing thermal spreaders to horizontally distribute the heat and thereby lower the effective thermal resistance reduces the maximum temperature experienced by those blocks 1.3 mm and a device plane away. It is therefore critical to reduce both the interplane and intraplane thermal resistances by providing paths for the heat to flow from the hot spots to the heat sink.

C. Multiple Aligned Active Blocks

The placement of two highly active circuit blocks aligned directly above one another has a significant effect on the thermal profile of a 3-D IC. Placing an active block on WBottom produces a higher thermal resistive path than a block placed on WTop. An analysis of two vertically aligned active circuit blocks has been performed by comparing the temperature for a single heater placed on WBottom with the increase in temperatures caused by placing two active heaters located at WTop and WBottom site 1. The largest temperature increase occurs at WTop site 1, where a 79.4% increase in temperature is observed (from 69.6 °C to 124.8 °C) for an applied current of 110 mA. The maximum on-chip temperature occurs on WBottom site 1, where the maximum temperature increases from 100.9 °C to 161.0 °C when a current of 110 mA flows through one active heater and two active heaters, producing a 59.6% increase in temperature. The remaining four sensors reveal an increase in temperature of 56.5% to 66.9%, corresponding to absolute temperatures of 81.4 °C to 91.9 °C from 52.1 °C to 55.6 °C. The percent increase in temperature when two active circuit blocks are vertically stacked as compared with a single active block is listed in Table IV, and the corresponding temperatures are listed in Table VIII.

The magnitude of the current also has a significant effect on the thermal profile within a 3-D IC. When applying 40 mA through both heaters, the increase in temperature remains below 20% for all thermal sensors as when applying 40 mA to just the WBottom heater. Two mitigation techniques include limiting the current flow, or deactivating the circuit block to allow heat to flow from the hot spot. Deactivation is particularly useful in high-activity circuit blocks. Active and passive heat removal techniques such as microfluidic channels and thermal TSVs also apply.

D. Multiple Nonaligned Active Blocks

The effect of increased spacing on the maximum temperature between vertically nonaligned active circuits is evaluated.

TABLE V
PERCENT INCREASE IN TEMPERATURE WHEN TWO ACTIVE CIRCUIT BLOCKS ARE NOT VERTICALLY ALIGNED

Heater location	Sensor location	Current (mA)											
		0	10	20	30	40	50	60	70	80	90	100	110
WTop, Site 2 and WBottom, Site 1	WTop, Site 1	0.00	-0.69	-1.94	-2.41	-2.16	-2.86	-2.91	-2.14	-1.23	-0.26	2.22	9.94
% increase as compared to WTop, Site 1 and WBottom, Site 1	WTop, Site 2	0.00	-3.41	-4.51	-4.22	0.57	5.26	12.21	17.06	21.83	29.47	35.85	54.27
	WBottom, Site 1	0.00	-1.40	0.00	0.00	0.53	-1.77	0.38	0.32	-1.08	0.00	5.41	11.75
	WBottom, Site 2	0.00	0.00	2.85	-1.90	1.77	7.17	10.41	16.99	23.32	27.35	33.85	51.01
	Back Metal, Site 1	0.00	-3.63	-5.36	-4.47	-1.39	1.00	5.95	7.65	9.80	14.22	18.90	31.63
	Back Metal, Site 2	0.00	-4.92	-3.81	0.00	5.80	8.14	12.05	16.50	14.90	21.06	25.41	42.87
WTop, Site 2 and WBottom, Site 1	WTop, Site 1	0.00	1.41	4.82	8.68	14.48	20.51	27.57	36.89	45.49	55.57	69.89	97.28
% increase as compared to WBottom, Site 1	WTop, Site 2	0.00	-0.70	2.77	7.42	14.87	22.58	35.11	48.49	64.51	83.32	106.63	141.39
	WBottom, Site 1	0.00	-0.71	2.76	6.40	8.00	16.14	21.18	27.45	33.39	42.77	56.68	78.29
	WBottom, Site 2	0.00	0.00	3.59	8.38	15.37	25.82	35.77	50.14	65.02	81.31	102.34	138.01
	Back Metal, Site 1	0.00	0.69	2.04	5.59	11.64	21.97	31.64	42.12	51.49	66.90	84.81	119.64
	Back Metal, Site 2	0.00	0.00	3.05	9.70	15.11	22.92	34.77	49.82	60.04	77.73	95.18	130.95

TABLE VI
PERCENT DECREASE IN TEMPERATURE WITH CONVECTIVE COOLING

Heater location	Sensor location	Current (mA)													
		0	10	20	30	40	50	60	70	80	90	100	110	120	130
WBottom, Site 1	WTop, Site 1	0.00	-1.41	-2.06	0.00	-1.25	-1.75	-2.14	-2.42	-3.67	-5.00	-6.10	-6.91	—	—
% decrease as compared to WBottom, Site 1 (fan)	WTop, Site 2	0.00	-0.70	-1.38	-1.35	-2.58	-4.25	-4.06	-4.35	-6.02	-6.45	-7.17	-9.87	—	—
	WBottom, Site 1	0.00	-1.41	0.00	0.00	-3.42	-2.07	-3.19	-4.37	-4.17	-3.66	-5.23	-6.34	—	—
	WBottom, Site 2	0.00	-0.37	-1.79	-1.74	-2.33	-2.25	-3.90	-4.22	-4.97	-6.00	-8.07	-10.01	—	—
	Back Metal, Site 1	0.00	0.34	0.00	-0.33	-1.88	-1.20	-1.96	-2.86	-3.82	-5.85	-6.50	-7.27	—	—
	Back Metal, Site 2	0.00	0.34	1.02	1.00	-0.94	-2.96	-2.52	-1.58	-4.07	-5.04	-6.89	-8.97	—	—
WTop, Site 1 and WBottom, Site 1	WTop, Site 1	0.00	-2.77	-5.16	-4.21	-4.86	-5.23	-5.81	-7.48	-8.23	-8.85	-9.88	-10.23	—	—
% decrease as compared to WTop, Site 1 WBottom, Site 1 (fan)	WTop, Site 2	0.00	-3.41	-5.15	-6.63	-7.37	-8.39	-6.31	-7.38	-9.46	-10.65	-12.31	-10.87	—	—
	WBottom, Site 1	0.00	1.41	3.36	0.60	1.07	-5.31	-4.22	-5.77	-6.96	-6.98	-7.03	-7.67	—	—
	WBottom, Site 2	0.00	0.73	0.71	-6.33	-7.08	-6.05	-7.89	-7.54	-8.34	-10.35	-11.91	-11.94	—	—
	Back Metal, Site 1	0.00	-4.62	-5.99	-5.07	-5.57	-6.75	-5.70	-7.20	-7.78	-9.47	-10.01	-11.88	—	—
	Back Metal, Site 2	0.00	-0.66	-0.63	0.92	2.32	0.79	-0.47	-1.87	-6.85	-7.69	-9.74	-9.96	—	—
Back Metal, Site 1	WTop, Site 1	0.00	0.73	-0.71	-0.69	-2.00	-2.55	-3.01	-4.50	-7.16	-7.97	-8.84	-10.12	-14.12	-19.92
% decrease as compared to Back Metal, Site 1 (fan)	WTop, Site 2	0.00	-1.40	-0.35	-0.34	-0.99	-1.58	-3.85	-4.19	-5.45	-7.29	-8.93	-11.19	-14.47	-20.48
	WBottom, Site 1	0.00	0.00	0.00	0.70	-1.01	-1.29	-1.85	-3.99	-5.30	-6.26	-7.02	-9.99	-13.72	-20.00
	WBottom, Site 2	0.00	-0.74	-1.45	-2.13	-1.05	-2.00	-4.04	-4.70	-5.96	-7.43	-8.94	-10.56	-13.39	-21.32
	Back Metal, Site 1	—	—	—	—	—	—	—	—	—	—	—	—	—	—
	Back Metal, Site 2	0.00	1.03	2.07	-0.99	-1.27	-1.52	-1.73	-2.96	-4.45	-8.15	-9.49	-9.75	-15.09	-21.88

A comparison is made between two vertically aligned resistive heaters (both heaters in site 1) and two heaters separated by 1.3 mm (WBottom heater site 1 and WTop heater site 2). A 0.0% to 5.4% reduction in temperature for all six thermal sensors up to a current of 30 mA is observed when shifting the WTop heater from site 1 to site 2. The on-chip thermal sensors at site 1 reveal a temperature change between −2.9% and 0.5% for currents up to 90 mA. A maximum increase in temperature at site 1 of 11.8% at WBottom and 9.9% at WTop is measured for a peak current of 110 mA, as listed in Table V. The on-chip thermal sensors at site 2 detect an exponentially increasing temperature from an applied current of 40 mA (0.6% for WTop and 1.8% for WBottom) to a peak current of 110 mA (54.3% for WTop and 51.0% for WBottom). The exponential increase in temperature at the back metal sensors for currents above 30 mA indicates strong thermal coupling through the back metal layer. A maximum on-chip temperature of 179.9 °C occurs at WBottom site 1. The maximum temperature at WTop site 1 is 137.2 °C, while the remaining sensors exhibit a maximum temperature ranging from 121.0 °C to 130.6 °C.

Three primary design issues are noted.

1) Moving highly active circuit blocks on the same plane apart reduces the maximum temperature as compared with vertically aligned circuits.
2) Although nonaligned circuit blocks reduce the maximum temperature, the effective thermal resistance to the heat sink (air in this case) significantly affects the maximum on-chip temperature, as indicated by the increase in temperature for currents above 30 mA.
3) Proper floorplanning within 3-D ICs requires analysis of the heat generated by each circuit block and the appropriate placement of hot blocks in both the vertical and horizontal directions, as placement algorithms must consider these issues to minimize peak on-chip temperatures.

E. Additional Design Considerations

The 3-D structures are particularly beneficial for heterogeneous systems. Some of these circuits commonly have blocks bonded to the backside of the silicon [37]–[39] (e.g., vertical cavity surface-emitting lasers (VCSELs) within an optical interconnect system [40]). The thermal heaters on the back metal emulate these blocks and support the analysis of the thermal profile and conduits from the back side of the silicon to the rest of the 3-D structure.

The fourth and fifth test conditions evaluate, respectively, heat flow from a source on the backside of the silicon to the on-chip thermal sensors and the reduction in the maximum temperature when a fan is used to convectively cool a 3-D IC. All of the thermal sensors produce the results within 6% of each other for all current load conditions through the back metal heater. The heat flows from a source on the back metal, evenly dispersing heat to the rest of the 3-D IC. Thermal spreading from a hot spot on the back metal is more

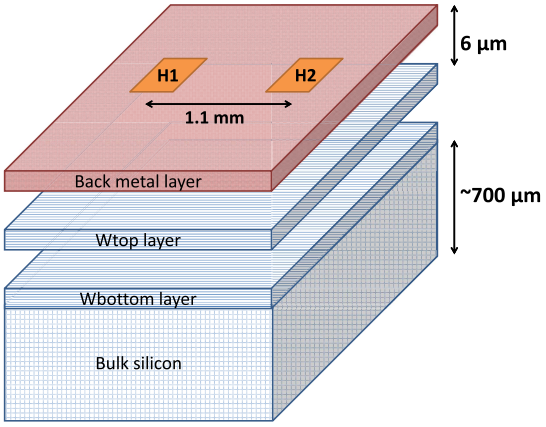

Fig. 8. Structure of the 3-D test circuit consisting of two silicon layers and one back metal layer. Each layer has two separately controlled heaters (H1 and H2). The back metal is connected to WTop using TTSVs.

pronounced. It is, however, more difficult to isolate a circuit block from thermal effects caused by a back metal heat source. For the fifth test condition, a fan 1 in above the 3-D IC reduces the temperature by 0.7% for a 10-mA current through a back metal heater to 21.9% for a current load of 130 mA. In the case where both on-chip heaters in site 1 are active, the maximum temperature is reduced by 0.7% and 11.9% for, respectively, currents of 10 and 110 mA. The percent reduction in temperature for three different heater configurations and heater currents from 0 to 110 mA is listed in Table VI. Despite an approximately 12% reduction in peak temperature with the use of a fan, additional heat removal techniques like TTSVs and microfluidic channels are necessary for those hot spots located deep within the 3-D IC.

VI. Verification of the Experimental Results With Simulations

Simulations of the fabricated 3-D test circuit have been conducted and compared with the experimental measurements. Temperatures are extracted from the simulations, and the thermal resistance per unit length is determined. The experimental data are supported by these simulations, and good agreement is observed.

A. Simulation Setup and Tools

The HotSpot simulator [10], [11], [41] is used in this paper to analytically investigate thermally conductive paths within 3-D structures. The structure shown in Fig. 8 is used to analyze heat propagation within a 3-D stack, including the dependence of thermal conductivity on temperature. This stack consists of two silicon layers and a single aluminum back metal layer (i.e., WTop, WBottom, and back metal layers). The back metal is connected to WTop using TTSVs, modeled as 6-µm high tungsten vias. Thermally passive (no heat is generated) layers are included in the simulation to better resemble the 3-D test circuit (e.g., silicon dioxide, bulk silicon, and the metal layers). Two heaters, modeled as heat dissipating blocks, are placed 1.1 mm apart on the back metal, and 1.3 mm apart on metal 2 of WTop and WBottom. Six heater/sensor sites are placed

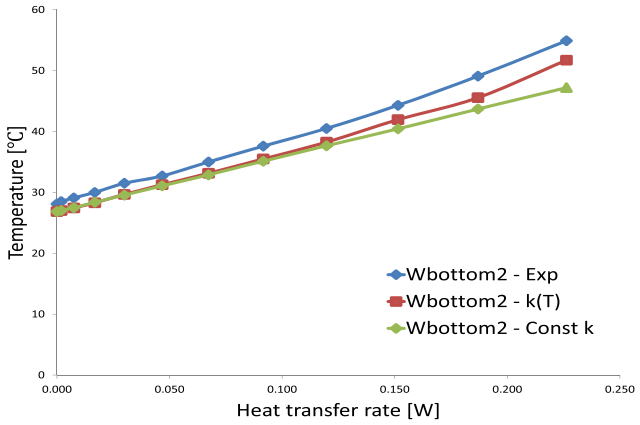

Fig. 9. Comparison of temperatures for a horizontal path (length = 1300 μm).

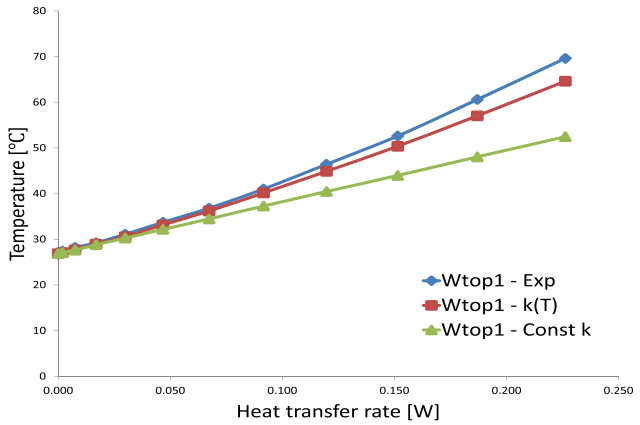

Fig. 10. Comparison of temperatures for a vertical path (length = 10 μm).

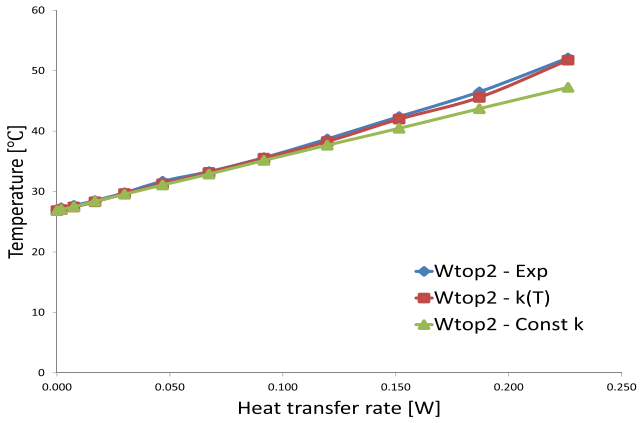

Fig. 11. Comparison of temperatures for a diagonal path (length = 1300 μm).

across the structure to evaluate the propagation of heat in both the horizontal and vertical dimensions. Different heaters are turned on to model different on-chip power dissipating blocks and related thermal paths. The temperatures are determined at each of the six sites.

B. Comparison With Experimental Results

A comparison of the measured temperatures with the simulations is shown in Figs. 9–11 for, respectively, the horizontal,

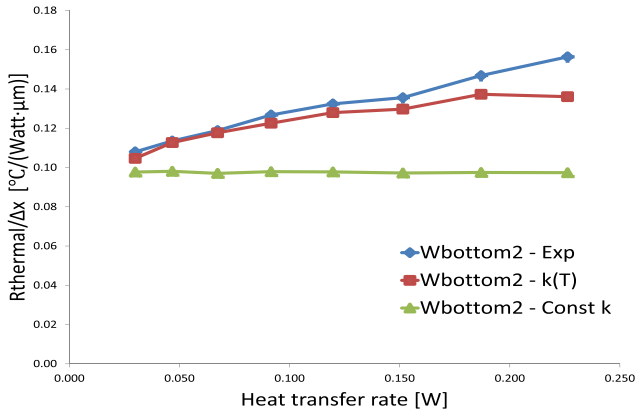

Fig. 12. Comparison of thermal resistance per unit length for a horizontal path (length = 1300 μm).

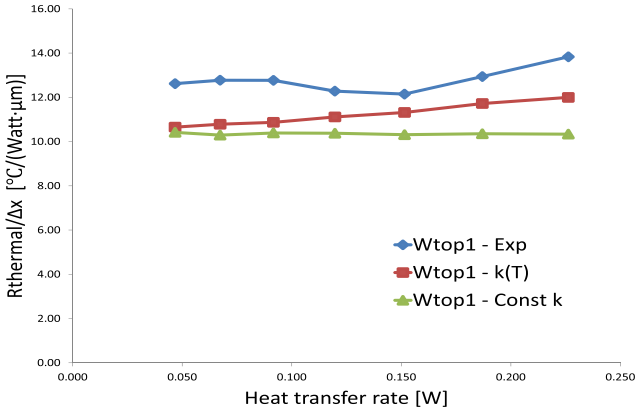

Fig. 13. Comparison of thermal resistance per unit length for a vertical path (length = 10 μm).

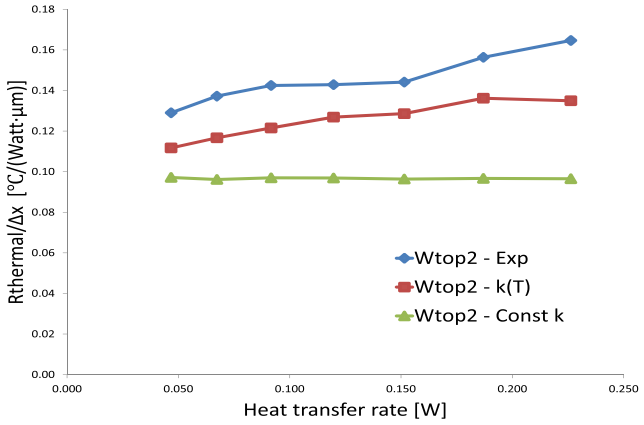

Fig. 14. Comparison of thermal resistance per unit length for a diagonal path (length = 1300 μm).

vertical, and diagonal paths. A diagonal path is a path from WBottom layer site 1 to WTop layer site 2. The worst case temperature difference between the experiment and simulation with a constant thermal conductivity is 25%, while the worst case difference with a temperature-dependent thermal conductivity is 7%.

The thermal resistance per unit length is compared in Figs. 12–14 for, respectively, the horizontal, vertical, and diagonal paths. The first datum shown in Figs. 13 and 14 deviates from the trend of the experimental data and the simulated results; hence, it is assumed to reflect measurement error, and is therefore not considered when evaluating the difference between the simulated and experimental data. The worst case difference between the experimental results and simulation assuming a constant thermal conductivity is 38%, while the worst case difference assuming a temperature-dependent thermal conductivity is 19%. It is therefore important to model the temperature dependence of the thermal conductivity. Both the experiments and simulations indicate that the lateral thermal paths conduct more heat than the vertical thermal paths. The thermal resistance per unit length of the vertical path is two orders of magnitude larger than the thermal resistance per unit length of the horizontal path, since the thermal conductivity of SiO_2 is much lower than the thermal conductivity of silicon.

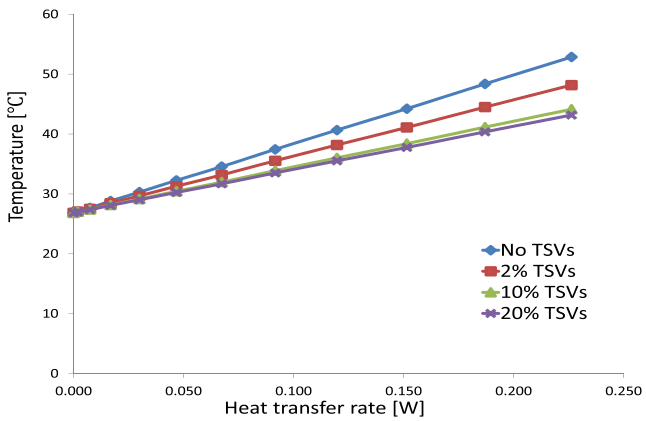

Fig. 15. Simulated temperature at the WTop site 1 sensor for four densities of TSVs placed between the WTop site 1 heater/sensor pair and the back metal.

C. Effect of Density of TSVs on Thermal Coupling

The number of TSVs has a significant effect on thermal coupling between the planes. TSVs are commonly fabricated using copper or tungsten, materials with higher thermal conductivity as compared with the insulating layer [42], [43]. The TSVs, therefore, form thermal paths to conduct heat from the on-chip hot spots to the heat sink.

The extension to HotSpot presented in [44] has been used to capture the effects of the TSV density on the temperature profile. This ability of the tool to characterize materials on a per block basis supports different simulation setups with an increasing number of TSVs. The WTop site 1 heater/sensor pair has been analyzed in this simulation for four different setups: 1) no TSVs; 2) 2% TSVs; 3) 10% TSVs; and 4) 20% TSVs. The simulated TSVs are characterized with a 1.25-μm diameter, a 100-μm pitch, and a resistivity of 0.005 m·K/W, similar to the TSVs in the fabricated 3-D test circuit. Each test structure has been simulated over the full power range of the heater in WTop site 1. The simulation results are shown in Fig. 15.

These results demonstrate that the temperature measured at WTop site 1 decreases with increasing density of TSVs.

TABLE VII

RESISTANCE AS A FUNCTION OF TEMPERATURE FOR CALIBRATING THE ON-CHIP AND BACK METAL THERMAL SENSORS

Heater location	Temperature (°C)																			
	27	30	35	40	45	50	55	60	65	70	75	80	85	90	95	100	105	110	115	120
WBottom, Site 1	119.5	120.5	123.0	125.5	127.9	130.3	132.7	135.1	137.5	139.9	142.0	144.7	147.0	149.0	151.0	152.8	155.3	157.5	159.8	162.0
WBottom, Site 2	119.7	120.4	123.1	125.1	127.4	129.9	132.3	134.4	136.5	139.2	141.8	143.9	146.3	148.3	150.3	152.4	154.7	156.8	158.8	161.0
WTop, Site 1	123.1	125.0	127.2	130.0	132.5	135.4	137.3	139.7	142.0	144.7	147.0	149.3	151.7	154.0	156.4	158.3	160.5	163.3	165.3	167.0
WTop, Site 2	123.3	124.4	127.0	130.4	133.3	135.4	137.7	140.1	142.9	145.0	147.5	150.0	152.0	154.7	156.9	158.9	161.5	164.8	166.8	168.7
Back metal, Site 1	24.25	24.55	25.10	25.55	26.10	26.60	27.05	27.65	28.15	28.70	29.15	29.75	30.15	30.60	31.05	31.55	32.00	32.55	32.95	33.45
Back metal, Site 2	20.15	20.60	21.15	21.60	21.90	22.30	22.80	23.20	23.55	24.05	24.50	24.85	25.25	25.65	26.15	26.55	26.95	27.30	27.60	28.00

TABLE VIII

TEMPERATURE MEASUREMENTS FROM THE FOUR ON-CHIP AND TWO BACK METAL THERMAL SENSORS FOR DIFFERENT HEATER ACTIVITIES

Heater location	Convective cooling	Sensor location	Current (mA)													
			0	10	20	30	40	50	60	70	80	90	100	110	120	130
WBottom, Site 1	No	WTop, Site 1	26.7	27.4	28.2	29.2	31.1	33.7	36.8	41.0	46.4	52.6	60.6	69.6	—	—
		WTop, Site 2	26.9	27.3	27.7	28.5	29.8	31.7	33.3	35.6	38.7	42.4	46.5	52.1	—	—
		WBottom, Site 1	27.6	28.4	29.2	31.6	35.7	39.6	45.4	52.7	61.1	71.0	84.8	100.9	—	—
		WBottom, Site 2	28.1	28.5	29.1	30.0	31.5	32.7	35.0	37.6	40.5	44.3	49.1	54.9	—	—
		Back Metal, Site 1	27.3	27.3	27.7	28.7	30.1	31.6	33.9	36.6	40.1	44.4	49.2	55.1	—	—
		Back Metal, Site 2	27.3	27.3	27.7	28.2	30.1	32.0	33.9	36.3	40	43.9	49.2	55.6	—	—
WBottom, Site 1	Yes	WTop, Site 1	26.7	27.0	27.6	29.2	30.7	33.1	36.0	40.0	44.7	50.0	56.9	64.8	—	—
		WTop, Site 2	26.8	27.1	27.3	28.1	29.0	30.4	31.9	34.0	36.4	39.7	43.2	46.9	—	—
		WBottom, Site 1	27.8	28.0	29.2	31.6	34.5	38.8	43.9	50.3	58.6	68.4	80.4	94.5	—	—
		WBottom, Site 2	27.9	28.4	28.6	29.5	30.7	32.0	33.7	36.0	38.5	41.7	45.1	49.4	—	—
		Back Metal, Site 1	27.2	27.4	27.7	28.6	29.5	31.2	33.2	35.6	38.5	41.8	46.0	51.1	—	—
		Back Metal, Site 2	27.0	27.4	28.0	28.5	29.8	31.0	33.0	35.7	38.4	41.7	45.9	50.6	—	—
WTop, Site 1	No	WTop, Site 1	27.0	27.6	28.6	30.2	31.3	33.5	36.6	39.8	44.4	49.4	54.9	61.6	—	—
		WTop, Site 2	26.8	27.5	28.1	28.8	30.0	31.1	32.7	35.4	37.9	41.0	44.9	49.1	—	—
		WBottom, Site 1	27.5	27.8	28.4	30.0	30.8	33.1	36.1	39.2	43.3	48.1	53.9	60.9	—	—
		WBottom, Site 2	27.8	28.7	29.1	30.4	30.8	32.5	34.4	36.5	39.2	42.6	46.3	50.6	—	—
		Back Metal, Site 1	27.1	27.3	27.6	28.2	29.0	30.4	32.4	35.1	38.0	41.2	45.7	50.3	—	—
		Back Metal, Site 2	27.2	27.3	27.8	28.5	30.1	31.9	33.2	36.5	39.3	42.2	46.5	51.6	—	—
WTop, Site 2	No	WTop, Site 1	26.5	26.9	27.6	28.8	30.7	33.1	35.6	38.4	42.4	47.0	52.8	59.0	—	—
		WTop, Site 2	26.7	27.3	27.9	29.8	32.1	35.0	38.9	42.2	48.5	55.4	62.8	71.8	—	—
		WBottom, Site 1	27.5	27.6	28.0	29.0	30.4	32.3	35.3	38.4	41.6	46.4	52.0	58.1	—	—
		WBottom, Site 2	27.4	28.3	29.1	30.6	32.7	35.4	39.5	43.5	49.5	57.0	64.7	72.8	—	—
		Back Metal, Site 1	27.1	27.3	27.9	28.9	30.4	32.6	35.6	38.7	43.2	48.0	54.3	61.4	—	—
		Back Metal, Site 2	26.9	27.5	27.8	29.1	30.8	32.9	36.4	40.7	45.8	51.7	58.1	65.9	—	—
WBottom, Site 1 WTop, Site 1	No	WTop, Site 1	27.1	28.0	30.2	32.5	36.4	41.8	48.4	57.3	68.3	82.1	100.7	124.8	—	—
		WTop, Site 2	27.3	28.1	29.8	31.9	34.0	36.9	40.1	45.1	52.2	60.0	70.8	81.4	—	—
		WBottom, Site 1	27.9	28.6	30.0	33.7	38.4	46.8	54.8	66.9	82.4	101.4	126.1	161.0	—	—
		WBottom, Site 2	28.0	28.5	29.4	33.1	35.7	38.4	43.1	48.2	54.2	63.1	74.2	86.5	—	—
		Back Metal, Site 1	27.2	28.5	29.9	31.7	34.1	38.2	42.1	48.4	55.3	64.9	76.5	91.9	—	—
		Back Metal, Site 2	27.6	28.7	29.7	30.9	32.7	36.4	40.8	46.6	55.7	64.5	76.6	89.9	—	—
WBottom, Site 1 WTop, Site 2	No	WTop, Site 1	27.2	27.8	29.6	31.7	35.6	40.6	47.0	56.1	67.5	81.9	103	137.2	—	—
		WTop, Site 2	27.0	27.1	28.5	30.6	34.2	38.9	44.9	52.8	63.7	77.7	96.1	125.6	—	—
		WBottom, Site 1	27.8	28.2	30.0	33.7	38.6	46.0	55.0	67.1	81.5	101.4	132.9	179.9	—	—
		WBottom, Site 2	28.0	28.5	30.2	32.5	36.3	41.2	47.6	56.4	66.9	80.4	99.3	130.6	—	—
		Back Metal, Site 1	27.3	27.5	28.3	30.3	33.6	38.5	44.6	52.1	60.7	74.1	91.0	121.0	—	—
		Back Metal, Site 2	27.2	27.3	28.6	30.9	34.6	39.3	45.7	54.3	64.0	78.1	96.1	128.4	—	—
WBottom, Site 1 WTop, Site 1	Yes	WTop, Site 1	26.9	27.2	28.6	31.1	34.7	39.6	45.6	53.0	62.7	74.8	90.8	112.0	—	—
		WTop, Site 2	26.8	27.1	28.3	29.8	31.5	33.8	37.5	41.8	47.3	53.6	62	72.6	—	—
		WBottom, Site 1	27.9	29.0	31.0	33.9	38.8	44.3	52.4	63.0	76.7	94.3	117.3	148.6	—	—
		WBottom, Site 2	28.1	28.7	29.6	31.0	33.1	36.1	39.7	44.6	49.7	56.6	65.3	76.2	—	—
		Back Metal, Site 1	27.1	27.2	28.1	30.1	32.2	35.6	39.7	44.9	51.0	58.7	68.9	81.0	—	—
		Back Metal, Site 2	27.4	28.5	29.5	31.2	33.5	36.6	40.6	45.8	51.9	59.5	69.2	80.9	—	—
Back metal, Site 1	No	WTop, Site 1	26.6	26.7	27.2	28.0	29.2	30.5	32.5	34.9	38.6	42.4	47.6	54.1	64.1	79.3
		WTop, Site 2	27.1	27.3	27.5	28.1	29.0	30.4	32.5	34.6	37.3	41.4	46.1	52.1	61.4	75.9
		WBottom, Site 1	27.5	27.6	28.0	28.6	29.8	31.2	32.9	35.7	38.6	42.7	47.2	54.5	65.2	81.7
		WBottom, Site 2	28.0	28.3	28.7	29.4	30.0	31.5	33.8	35.9	39.0	42.9	47.8	54.0	63.4	81.1
		Back Metal, Site 1	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		Back Metal, Site 2	26.9	27.3	27.3	28.7	29.6	31.0	32.9	35.3	38.6	43.6	49.0	55.1	67.0	85.2
Back metal, Site 1	Yes	WTop, Site 1	27.0	26.9	27.0	27.8	28.6	29.8	31.5	33.3	35.8	39.0	43.4	48.6	55.1	63.5
		WTop, Site 2	27.1	26.9	27.4	28.0	28.7	29.9	31.2	33.2	35.3	38.4	42.0	46.2	52.5	60.3
		WBottom, Site 1	27.4	27.6	28.0	28.8	29.5	30.8	32.3	34.3	36.5	40.0	43.9	49.1	56.2	65.4
		WBottom, Site 2	27.9	28.1	28.3	28.7	29.7	30.8	32.4	34.2	36.7	39.7	43.5	48.3	54.9	63.8
		Back Metal, Site 1	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		Back Metal, Site 2	27.1	27.5	27.8	28.4	29.2	30.6	32.4	34.3	36.9	40.1	44.3	49.7	56.9	66.7

This result confirms the claim that additional TSVs form thermal paths from the on-chip hot spots to the heat sink. An interesting finding is that the decrease in temperature is not constant. This behavior is due to the parallel thermal resistors with a concomitant increase in the density of TSVs (similar to electrical resistors placed in parallel).

VII. CONCLUSION

The performance and reliability of a 3-D IC are greatly affected by large heat gradients. Thermal effects can potentially alter the performance of the clock and power networks due to hot-spot formation. Proper block placement and active and passive heat removal techniques are critical to ensure that a 3-D IC operates within the specified thermal design power envelope.

A 3-D test circuit examining thermal propagation within a 3-D stack has been designed, fabricated, and tested. Five test conditions are examined to characterize thermal propagation in 3-D ICs. The five conditions are as follows: 1) the location of the active circuit; 2) the impact of intraplane thermal

spreading; 3) the relative vertical alignment of the two active circuits; 4) heat flow from a thermal source at the back side of the silicon; and 5) convective cooling of the 3-D IC. Design suggestions are provided to better manage hot-spot formation while reducing the effects on neighboring circuit blocks. The experimental data are confirmed by the simulations conducted on a model of the fabricated 3-D test circuit. The position of a block relative to a heat sink significantly affects the thermal resistance and therefore the flow of heat from the hot spots. The effective design of both the interplane and intraplane thermal conduits provides an important means for removing heat. This test circuit provides enhanced understanding of thermal hot-spot formation, propagation, and modeling of 3-D ICs.

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APPENDIX A

CALIBRATION OF THE FOUR-POINT THERMAL SENSORS

Resistance data for calibrating the on-chip and back metal four-point thermal sensors are shown in Table VII. A temperature-controlled hot plate is used to measure resistance as a function of temperature for the thermal sensors on WTop, WBottom, and the back metal at sites 1 and 2. The data are fitted to a second-order polynomial expression to determine the temperature from the resistance measurements.

APPENDIX B

TEMPERATURE DATA FROM THERMAL SENSORS

Temperature data for all test conditions are determined from the four on-chip and two back metal resistive thermal sensors. The location of the resistive heaters determines the specific test condition. The temperature at the six thermal sensors as a result of activity from the single heater, double heaters, and active cooling is listed in Table VIII. The data are derived from converted measured resistances.

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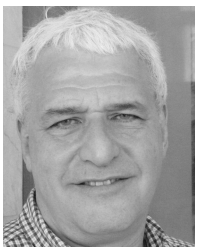
Ioannis Savidis received the B.S.E. degree in electrical and computer engineering and biomedical engineering from Duke University, Durham, NC, USA, in 2005, and the M.Sc. and Ph.D. degrees in electrical and computer engineering from the University of Rochester, Rochester, NY, USA, in 2007 and 2013, respectively.

He was with the 3-D Integration Group, Freescale Semiconductor, Inc., Austin, TX, USA, in 2007, and the System on Package and 3-D Integration Group, IBM Thomas J. Watson Research Center, Yorktown Heights, NY, USA, from 2008 to 2011. He is currently an Assistant Professor with the Department of Electrical and Computer Engineering, Drexel University, Philadelphia, PA, USA, where he directs the Integrated Circuits and Electronics Design Laboratory. His current research interests include analysis, modeling, and design methodologies for high-performance digital and mixed-signal integrated circuits, power management for system-on-a-chip and microprocessor circuits (including on-chip dc–dc converters), emerging integrated circuit technologies, IC design for trust (hardware security), and interconnect-related issues in 2-D and 3-D ICs, with a specific emphasis on electrical and thermal modeling and characterization, signal and power integrity, and power and clock delivery for heterogeneous 2-D and 3-D circuits.

Dr. Savidis is an Editorial Board Member of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION SYSTEMS, the *Microelectronics Journal*, and the *Journal of Circuits, Systems and Computers*.

Boris Vaisband (S'12) received the B.Sc. degree in computer engineering from the Technion-Israel Institute of Technology, Haifa, Israel, in 2011, and the M.S. degree in electrical engineering from the University of Rochester, Rochester, NY, in 2012, where he is currently pursuing the Ph.D. degree.

He was a Hardware Design Engineer with Intel Corporation, Haifa, from 2008 to 2011. In 2013, he interned with the Optical and RF Research Group, Cisco Systems, Inc., San Jose, CA, USA. His current research interests include thermal-aware design and floorplanning, and power delivery in 3-D integrated circuits.



Eby G. Friedman received the B.S. degree from Lafayette College, Easton, PA, USA, in 1979, and the M.S. and Ph.D. degrees from the University of California at Irvine, Irvine, CA, USA, in 1981 and 1989, respectively, all in electrical engineering.

He was the Manager of the Department of Signal Processing Design and Test with Hughes Aircraft Company, Culver City, CA, USA, from 1979 to 1991, where he was responsible for the design and test of high-performance digital and analog IC's. He has been with the Department of Electrical and Computer Engineering, University of Rochester, Rochester, NY, USA, since 1991, where he is currently a Distinguished Professor, and the Director of the High Performance VLSI/IC Design and Analysis Laboratory. He is also a Visiting Professor with the Technion-Israel Institute of Technology, Haifa, Israel. He has authored over 400 papers and book chapters and holds 12 patents, and authored and edited 16 books in high-speed and low-power CMOS design techniques, 3-D design methodologies, high-speed interconnect, and the theory and application of synchronous clock and power distribution networks. His current research interests include high-performance synchronous digital and mixed-signal microelectronic design and analysis with an application to high-speed portable processors and low-power wireless communications.

Dr. Friedman is a Senior Fulbright Fellow. He is the Editor-in-Chief of the *Microelectronics Journal*, an Editorial Board Member of the *Analog Integrated Circuits and Signal Processing*, the *Journal of Low Power Electronics*, and the *Journal of Low Power Electronics and Applications*, the Chair of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION SYSTEMS Steering Committee, and a member of the Technical Program Committee of numerous conferences. He was the Editor-in-Chief of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION SYSTEMS, a Regional Editor of the *Journal of Circuits, Systems and Computers*, an Editorial Board Member of the PROCEEDINGS OF THE IEEE, the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II: ANALOG AND DIGITAL SIGNAL PROCESSING, the IEEE JOURNAL ON EMERGING AND SELECTED TOPICS IN CIRCUITS AND SYSTEMS, and the *Journal of Signal Processing Systems*, a member of the Circuits and Systems Society Board of Governors, the Program and Technical Chair of several IEEE conferences. He was a recipient of the IEEE Circuits and Systems 2013 Charles A. Desoer Technical Achievement Award, the University of Rochester Graduate Teaching Award, and the College of Engineering Teaching Excellence Award.