Bitline Techniques With Dual Dynamic Nodes for Low-Power Register Files

Rahul Singh, Gi-Moon Hong, and Suhwan Kim, *Senior Member, IEEE*

***Abstract*—Wide fan-in dynamic multiplexers are one of the critical circuits of read-out paths in high-speed register files. However, these dynamic gates have poor noise immunity, which is aggravated by their wide fan-in structure, and their high switching activity consumes significant power. We present new footer voltage feedforward domino (FVFD) and static-switching pulse domino (SSPD) designs for dynamic multiplexers. Both improve noise tolerance, and both reduce the switching power by limiting the voltage swing on the large bitline capacitance through the introduction of dual dynamic nodes. The FVFD technique is based on charge sharing, while SSPD employs a conditional pulse generator to achieve a limited-switching behavior. Adopting these dual dynamic node techniques, we implemented 32-word × 16-bits/word (0.5-Kb) 1-read, 1-write ported register files in a 1.2-V, 65-nm low-V_T CMOS process. Although the SSPD and FVFD techniques respectively require 2.4 and 1.4 times more area than the established single-keeper domino technique, comparative analysis through simulations and measurement results suggests that they can be advantageous in terms of both read power and noise immunity.**

***Index Terms*—Domino logic circuits, dynamic gates, high-speed integrated circuits, low-power design, noise immunity, register files, switching activity.**

I. Introduction

HIGH-PERFORMANCE register files are critical components of modern microprocessors [1], [2]. The architecture of fast register files includes wide fan-in dynamic multiplexers in its read path to achieve single-cycle latency [3]. Similar wide-OR structures are also used in L0 caches, the match lines of content-addressable memories, rotator circuits, and programmable logic arrays [4]–[7].

A simplified representation of a single-port, single-ended read path in a register file (RF) is shown in Fig. 1. To perform a bitline (BL) read operation on a register file with 2^N registers, it requires a dynamic multiplexer structure with 2^N parallel inputs. Since the pull-down network and the output inverter must be preferentially skewed to achieve high speed, the noise margin of these dynamic structures, which is small even without skewing, is further degraded. These dynamic multiplexers also require a strong keeper to compensate for the cumulative leakage from the parallel evaluation paths, which increases the read access time. Therefore the bitlines typically have a hierarchical organization, in which they are partitioned into local and global bitlines (LBLs and GBLs), with the latter driving the output [3], [8]. But both the LBLs and GBLs remain susceptible to the noise problem intrinsic to the exponential increase in subthreshold leakage that occurs with technology scaling; this leakage reaches significant levels below 90-nm.

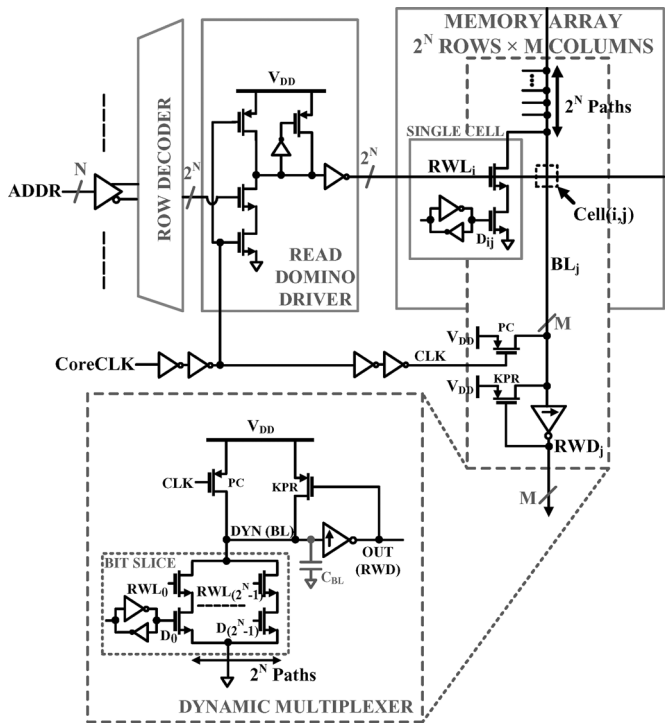

Fig. 1. Single-ended read path with precharged domino logic in a 2^N-word × M-bits/word register file (RF). PC and KPR are respectively the precharge and keeper transistors. BL, RWL and RWD stand for bitline, read word line and read word respectively. C_{BL} is the bitline capacitance, which is the sum of the interconnect loading and the parasitic diffusion capacitances.

Increasing the size of the keeper is no longer considered a viable option for improving bitline noise immunity [9], and so several alternative ways of dealing with noise have been proposed [3], [10]–[16]. Their common goal is to achieve high noise immunity, but some recent techniques also include process-tracking capabilities to reduce variability across process corners [2], [14]–[16]. To resolve the trade-off between performance and noise immunity, an innovative delayed keeper design is proposed in [10], [11] where a strong keeper is conditionally turned-on after a delay to avoid contention at the start of the evaluation cycle. A similar principle is employed in the conditional keeper technique, proposed in [12], where

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R. Singh was with the Department of Electrical Engineering, Seoul National University, Seoul, 151-744, Korea. He is now with Samsung Electronics, Yongin, 446-711, Korea.

G.-M. Hong and S. Kim are with the Department of Electrical Engineering, Seoul National University, Seoul, 151-744, Korea (e-mail: suhwan@snu.ac.kr).

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the keeper circuit is now split into a weak and a strong keeper. The weak keeper is always on during an evaluation phase and, if the dynamic node is not discharged by the pull-down network, the strong keeper is also turned on after a delay. This improves tolerance of sub-threshold leakage noise, but the conditional keeper and the delayed keeper schemes remain susceptible to external input noise in the switching time window, during which the dynamic node is not adequately protected [17]. An alternative is the pseudostatic bitline [3], in which the pull-down network is modified so as to create a negative gate-source underdrive on the top transistors in the pull-down network when the read word lines are deselected. This topology weakens the bitline leakage paths but increases the fan-in capacitive load on the read word lines and the delay due to the use of static NOR gates. The diode-footed domino technique [13] uses the stacking effect to achieve high noise immunity. But the overdrive of the transistors in the mirror network is limited, due to the reduced swing on the mirror node, significantly degrading the evaluation speed [18]. In summary, existing techniques aiming at increasing noise tolerance either remain susceptible to external noise or incur a significant speed penalty.

In addition to low noise immunity, bitline charging and discharging with wide fan-in dynamic multiplexers also dissipates a significant portion of the power used by a register file: this makes it a good target for new low-power designs. While a static gate only consumes switching power when a toggling event occurs at its output, the switching power of a dynamic gate depends on its output state [20]. If the probability of a rising transition at the input is high, which it usually is for a high fan-in structure like a dynamic multiplexer in an RF read port, the intensity of switching activity approaches that of the clock. Due to the large capacitance (C_{BL} in Fig. 1) on the dynamic node caused by the bitline interconnect loading, together with parasitic diffusion capacitances from the pull-down network, high switching activity significantly increases the switching power. In addition, as shown in Fig. 1, dynamic operation requires all the RWL inputs to be driven by clocked drivers, which use more energy than static buffers.

Recently, so-called switching-aware design techniques [6], [20] have been proposed to tackle this excessive switching and the related overheads of wide fan-in dynamic multiplexers. Limited switch dynamic logic (LSDL) [6], [19] adds a latch structure at the gate output [Fig. 2(a)]. This eliminates redundant switching, but only at the output; the dynamic node with its large capacitive loading still has a high switching rate. Thus LSDL fails to produce a truly static switching behavior. The single-phase SP-Domino technique [20] [Fig. 2(b)] aims to achieve static input and output characteristics. With static input characteristics, the clocked wordline drivers can be replaced by static buffers thereby making them more energy efficient. It has a clock-delayed [21] single-phase mode of operation, in which both pull-up and pull-down of the dynamic node occur during the evaluation phase. The reduction in switching at the dynamic and output nodes resulting from this static-like behavior saves a lot of power [20]. However, SP-Domino design uses the same transistor M1 to perform pull-up and keeper operations. To equalize the rise and fall delays of the gate requires M1 to have a particular width, which fixes the delay and noise design points, precluding any tuning of performance [22].

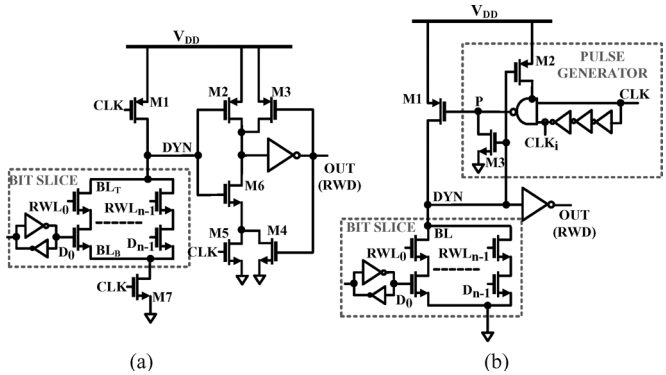


Fig. 2. Switching-aware techniques—(a) limited switch domino [4], [5], and (b) single-phase SP-Domino [6].

To overcome these various drawbacks, we recently proposed two different dynamic logic styles in [18], [22], [23] and verified their correct operations through transistor-level schematic simulations of individual logic gates. In this work, however, we make the following unpublished contributions:

1) In Section II, through discussions on the common principles of operation of the new techniques, we describe how adopting dual dynamic nodes helps to simultaneously overcome the problems of high power dissipation, subthreshold leakage and poor noise immunity.
2) In Section III, we compare and contrast the two techniques with each other through performance and variability simulations and also establish their relative advantages over a conventional single-dynamic-node structure in terms of delay, power, and noise immunity.
3) In Section IV, adopting these two techniques that were carefully analyzed in Section III, we validate the benefits and effectiveness of ours through silicon-proven results of non-trivial functional units: 0.5-Kb register files. The prototype chip was designed and fabricated in a 1.2-V, 65-nm low-V_{T} CMOS technology. Through detailed measurement results and their analysis, we demonstrate that the proposed approaches and structures can offer several advantages in deep submicrometer technologies compared to a register file based on the conventional domino technique.

II. Proposed Bitline Techniques

High sensitivity to noise and a large switching power are the two main limitations of the wide fan-in dynamic multiplexers employed in the read ports of register files. The existing bitline techniques that we reviewed in Section I address these two problems separately: thus the techniques with good noise immunity largely fail to curb power dissipation, and vice versa. We will now describe two dual dynamic node bitline techniques which simultaneously achieve high noise immunity and reduced switching power, while maintaining high performance. The essence of both our techniques is the introduction of an extra dynamic node into the bitline read port topology. This reduces the switching power by restricting the voltage swing on the primary dynamic node with its large bitline capacitance;

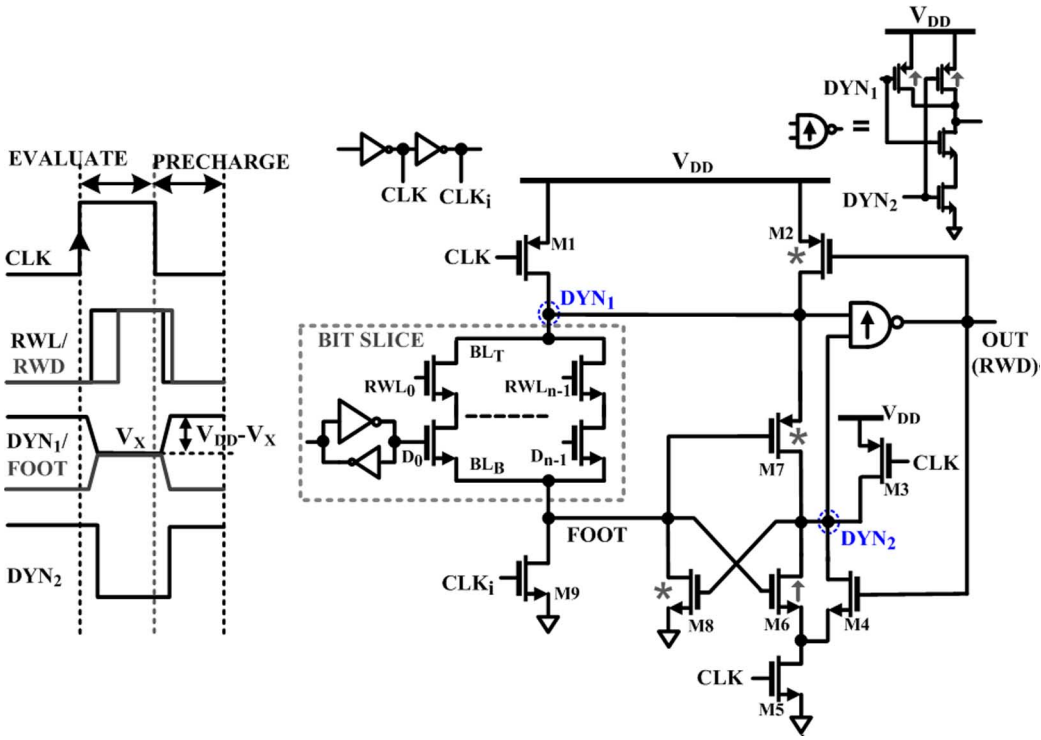


Fig. 3. FVFD technique applied to the dynamic multiplexer in an RF bitline read-out circuit (the symbol ↑ indicates an upsized transistor and * indicates a weak transistor) and the timing diagram.

at the same time it avoids a significant increase in delay by allowing a full rail-to-rail swing on a lightly loaded second dynamic node with a small parasitic capacitance and which is inversely coupled to the output. We will now describe the two techniques in more detail.

A. Footer Voltage Feedforward Domino (FVFD)

Fig. 3 is a schematic diagram showing the application of the FVFD technique [18] to a dynamic multiplexer in an RF read port. As shown in the timing diagram, when a read word line (RWL) goes high during the evaluation phase and a pull-down path is activated, the charge initially stored on C_{DYN1} which is the bitline capacitance of the main dynamic node DYN_1, is redistributed between DYN_1 and FOOT. This sharing of charge during evaluation activates two parallel paths: (1) a slow path utilizing the drop in the voltage at DYN_1 to evaluate the output through a high-skewed NAND gate; and (2) a fast feedforward path that uses the voltage developed on FOOT (V_{X}) to turn on M6 which rapidly pulls down a second dynamic node, DYN_2, which, unlike DYN_1, has a low parasitic capacitance and is also coupled to the output through the skewed NAND gate. The fast feedforward path assists the primary evaluation path and offsets the reduction in evaluation speed that would otherwise be caused by an incomplete discharge of the main dynamic node. Also note that, although M6 is not strongly turned on during evaluation, it will still have enough overdrive to discharge the small capacitance of the second dynamic node quickly. After the clock signal goes low, the dynamic nodes are precharged high while FOOT is discharged to ground by M9 to prepare for the next evaluation cycle. The clocked transistor M5 serves to cut off the short-circuit path through M3 and M6 which exists at the start of the precharge phase. M1 and M3 are the precharge transistors, while M2 and M7 are the keeper transistors (of minimum size) for the two dynamic nodes, DYN_1 and DYN_2. Another minimum-sized keeper transistor, M8, is added to prevent charge building up on the FOOT node in a noisy environment.

The primary dynamic node, DYN_1, which has a large capacitance, now experiences a limited voltage swing $(V_{\mathrm{DD}} - V_{\mathrm{X}})$ during the evaluation and precharge phases, while the second dynamic node, DYN_2, which is separated from the pull-down network, undergoes a complete rail-to-rail swing. The way in which this arrangement reduces the switching power overhead can be better understood by first considering the switching power $P_{\mathrm{Dyn,Conv}}$ of a dynamic multiplexer in an RF read port [20]:

$$\begin{aligned} P_{\mathrm{Dyn,Conv}} &= P_{\mathrm{Switching}} + P_{\mathrm{SC}} + P_{\mathrm{CLK}} \\ &= \Pr\{1\}(C_{\mathrm{DYN}} + C_{\mathrm{SW}})V_{\mathrm{DD}}^2 f_{\mathrm{CLK}} \\ &\quad + \Pr\{1\} I_{\mathrm{SC,AVG}} V_{\mathrm{DD}} f_{\mathrm{CLK}} + P_{\mathrm{CLK}}, \end{aligned} \quad (1)$$

where $P_{\mathrm{Switching}}$ is the power dissipated due to the charging and discharging of two capacitances: C_{DYN}, the main bitline capacitance, and C_{SW}, the effective switched capacitance due to transition at other nodes. P_{SC} is due to the average short-circuit current (contention current due to keeper action) $I_{\mathrm{SC,AVG}}$ that flows in every cycle in which the output is at logic state "1" (an event which occurs with probability $\Pr\{1\}$). P_{CLK} is the clocking power. Since C_{DYN} is much larger than the other capacitances $(C_{\mathrm{DYN}} + C_{\mathrm{SW}} \approx C_{\mathrm{DYN}})$, $P_{\mathrm{Switching}}$ is effectively only influenced by the voltage swing at C_{DYN}. Thus, the

switching power $P_{\mathrm{Dyn,FVFD}}$ of a FVFD multiplexer can now be written as follows:

$$\begin{aligned} P_{\mathrm{Dyn,FVFD}} &= \Pr\{1\} C_{\mathrm{DYN_1}} V_{\mathrm{DD}} (V_{\mathrm{DD}} - V_{\mathrm{X}}) f_{\mathrm{CLK}} \\ &\quad + \Pr\{1\} C_{\mathrm{DYN_2}} V_{\mathrm{DD}}^2 f_{\mathrm{CLK}} \\ &\quad + \Pr\{1\} I_{\mathrm{SC,AVG}} V_{\mathrm{DD}} f_{\mathrm{CLK}} + P_{\mathrm{CLK}} \\ &\approx \Pr\{1\} \left(\frac{C_{\mathrm{DYN_1}}}{2} + C_{\mathrm{DYN_2}} \right) V_{\mathrm{DD}}^2 f_{\mathrm{CLK}} \\ &\quad + \Pr\{1\} I_{\mathrm{SC,AVG}} V_{\mathrm{DD}} f_{\mathrm{CLK}} + P_{\mathrm{CLK}} \end{aligned} \quad (2)$$

where C_{DYN1} and C_{DYN2} respectively are the capacitances of the two dynamic nodes 1 and 2, and $V_{\mathrm{DD}} - V_{\mathrm{X}}$ is the voltage swing at $\mathrm{DYN_1}$. The voltage developed on FOOT, V_{X}, is approximately $V_{\mathrm{DD}}/2 - \Delta$, since both $\mathrm{DYN_1}$ and FOOT run along the entire length of the bitslice and have similar interconnect capacitances. Comparing (2) with (1), we see that the switching power contribution of the main dynamic node is reduced by nearly a half. Of course the additional dynamic node makes its own contribution to the switching power and the increase in the number of clocked transistors also increases P_{CLK}: but since C_{DYN2} is small and switching contribution from C_{DYN1} is nearly halved, we can still expect significant power savings despite the clock and switching power overheads of the second dynamic node. We later show this to be the case in Sections III, IV.

The new design also improves leakage tolerance and noise immunity due to the self-reverse bias effect [4], [24]. The worst-case noise condition during evaluation [9] occurs when all the RWL signals are deselected and $\mathrm{D}_0 \ldots \mathrm{D}_{n-1} = 1$. Any sub-threshold leakage in the nMOS transistors or crosstalk noise on the RWL inputs, which can trigger a false evaluation, contributes to the development of a positive potential at FOOT. This reduces the gate-source overdrive of the transistors connected to the data inputs. Due to the stacking (self-reverse bias) effect, the leakage current through the nMOS access transistors connected to the read word lines is also reduced. This increase robustness against noise and obviates the need for strong keepers [13]. Thus the short-circuit power P_{SC} is also reduced. In Section III, we show that even with a minimum-sized keeper (small P_{SC}), the FVFD technique achieves much better noise tolerance than the conventional technique with a strong keeper (large P_{SC}).

B. Static-Switching Pulse Domino (SSPD)

One approach to remove the limitation on dynamic multiplexers imposed by switching power is to reduce voltage swing at the main dynamic node. This is applied in our FVFD design, but we retain the dynamic input and output characteristics of a conventional footless domino gate, which leads to high switching activity and requires energy-expensive clocked input buffers. The single-phase SP-domino technique [20], in which the dynamic circuit topology is modified so that it has static input and output characteristics, is an alternative way of minimizing the switching power of both the dynamic multiplexers and the wordline drivers. The level of switching activity then becomes similar to that of a static gate. However, as we discussed in Section I, the SP-Domino multiplexer is an inflexible design because using the same transistor for pull-up as a keeper precludes tuning to achieve a specific noise or delay characteristic. We propose a static-switching pulse domino (SSPD) technique [22] with a similar clock-delayed footless operation and static switching behavior to SP-Domino, but with a more flexible design. We also use the concept of dual dynamic nodes, seen earlier in the FVFD technique, to reduce the voltage swing on the bitline capacitance.

The schematic diagram and timing diagram in Fig. 4 show how the SSPD technique can be applied to a dynamic multiplexer. The pull-up and keeper action are now provided by two separate transistors—M1 and M2 respectively. A clocked isolation transistor, M4, separates the main dynamic node $\mathrm{DYN_1}$, with its large bitline capacitance, from the second dynamic node $\mathrm{DYN_2}$, which is inversely coupled to the output. This arrangement reduces the swing at $\mathrm{DYN_1}$ by the nMOS threshold voltage $V_{\mathrm{TH,N}}$ and eases the sizing requirement on M1. The SSPD technique requires a conditional pulse generator (CPG), which generates a pulse to turn on M1 at the start of a clock cycle, but only when the dynamic node has been discharged or held low in the previous cycle, as shown in Fig. 4(b). Then, if all the RWL inputs are low, the turned-on M1 charges up the dynamic node and the output transitions to logic-low eventually. If the pull-down network is also on, then there is a short period equal to the delay path of the CPG [the sum of the delays of the NOR gate and the two inverters in Fig. 4(a)] during which contention between M1 and the turned-on pull-down path occurs. During this contention period, a short-circuit current flows; however, because the pull-down path is sized to be stronger than M1, the dynamic nodes and the output do not change their states. On the other hand, if the dynamic node has not been discharged in the previous cycle, M1 is not turned on by the CPG; and so, when and the pull-down network is on, it only faces contention from the keeper transistor. As a result, the SSPD technique allows independent tuning of the rise and fall delays - it is easy to see that M1 affects only the high-to-low transition delay of the output while M2 affects only the low-to-high delay. Consequently, dynamic multiplexers with a wide spread of keeper ratios can be easily designed using the SSPD technique [23].

The CPG plays two important roles in the SSPD scheme: (1) it monitors the dynamic node $\mathrm{DYN_2}$ and generates a pulse only when $\mathrm{DYN_2}$has been discharged or held low during the previous cycle; and (2) it extends the pulse width to the clock's on-period during a pull-up operation. In performing these two functions, the CPG generates two internal signals $\mathrm{CCLK_d}$ and $\mathrm{CCLK_i}$. Their behavior in relation to the clock and the voltage at $\mathrm{DYN_2}$ is shown in Fig. 4(b). $\mathrm{CCLK_d}$ and $\mathrm{CCLK_i}$ only behave as the delayed and inverse phases of the clock when $\mathrm{DYN_2}$ is low, whereas they are held low if $\mathrm{DYN_2}$ is evaluated high. Instead of generating the internal signal $\mathrm{CCLK_d}$, a synchronous latch can also be used to realize a signal X which is the inverse of $\mathrm{DYN_2}$ sampled at every negative clock edge. This alternative implementation of CPG is also shown in Fig. 4(a). The output of the CPG is the conditional pulse CP, which is generated by a

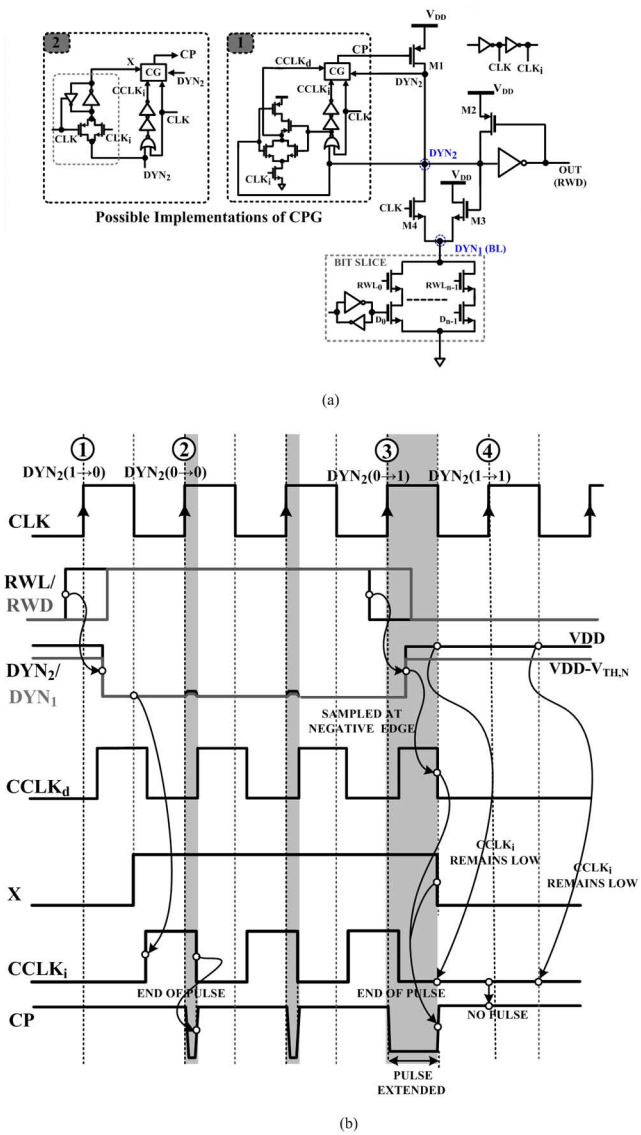


Fig. 4. (a) SSPD technique applied to a dynamic multiplexer in a RF bitline read-out circuit. Possible implementations of the conditional pulse generator (CPG) are also shown. (b) Timing diagram of a SSPD dynamic multiplexer showing the different modes of operation.

complex CMOS gate CG from the two internal signals $\mathrm{CCLK_d}$ (or X) and $\mathrm{CCLK_i}$. The logical expressions for the two signals and gate G can be written as follows:

$$CCLK_d = \overline{\overline{CLK} + DYN_2}, \tag{3}$$

$$X = \overline{CLK} \cdot \overline{DYN_2} + CLK \cdot X \tag{4}$$

$$CCLK_i = \overline{CLK + DYN_2}. \tag{5}$$

$$CP = \overline{CLK \cdot CCLK_i + DYN_2 \cdot CCLK_d}. \tag{6}$$

During a pull-up operation, CPG spans the on-period of the clock: this extended pulse width relaxes the sizing requirement on M1. Usually, in designs with explicit pulse generators, the delay path controlling the pulse width should be very long to ensure functionality across all corners and to cover the effects of random variations [25]. In the case of SSPD, we need only ensure that the pulse window is wide enough for $\mathrm{DYN_1}$ to be charged up sufficiently by M1 to turn-on gate G's pull down path before $\mathrm{CCLK_i}$ falls. Further details on SSPD's operation and sizing methodology are provided in [23].

The switching power of the SSPD multiplexer can be expressed as follows:

$$\begin{aligned} P_{\mathrm{Dyn,SSPD}} &= P_{\mathrm{Mux}} + P_{\mathrm{CPG}} + P_{\mathrm{SC}} + P_{\mathrm{CLK}} \\ &= \left[\frac{1}{2}\alpha C_{\mathrm{DYN2}} V_{\mathrm{DD}}^2 f_{\mathrm{CLK}} \right. \\ &\quad \left. + \frac{1}{2}\alpha C_{\mathrm{DYN1}} (V_{\mathrm{DD}} - V_{\mathrm{TH,N}}) V_{\mathrm{DD}} f_{\mathrm{CLK}}\right] \\ &\quad + P_{\mathrm{CPG}} + \Pr\{1\} I_{\mathrm{SC,AVG}} V_{\mathrm{DD}} f_{\mathrm{CLK}} + P_{\mathrm{CLK}}, \end{aligned} \tag{7}$$

where P_{Mux} and P_{CPG} respectively are the power dissipated in the dynamic multiplexer (excluding the CPG) and the pulse generator; and α is the switching probability of the input and output terminals. From this expression, we can see that the contribution of the main dynamic node to the switching power is output-switching dependent because $\Pr\{1\}$ is replaced by α, and that the power is further reduced due to the smaller voltage swing $V_{\mathrm{DD}} - V_{\mathrm{TH,N}}$. These factors contribute significant power savings, despite the overhead of the conditional pulse generator. Additionally, we can also expect the reduced voltage across the pull-down network to be beneficial in terms of sub-threshold leakage as it has an exponential dependence on the drain-to-source voltage [24].

It must be further noted that a large M1 increases the average short-circuit current $(I_{\mathrm{SC,AVG}})$ and the power dissipation which may negate the benefits of a reduced switching factor. A large M1 will be required in an SSPD multiplexer with a large fan-in. For example, the large bitline capacitance (large C_{DYN1}) of a 32-bit SSPD multiplexer means that the pull-up action from M1 has to be strong enough to avoid increasing the high-to-low transition delay. To avoid making M1 too large, it then becomes necessary to split the multiplexer into two separate 16-bit SSPD sections each with their own pull-up transistor and pulse generator. This two-section arrangement increases the layout area but, vitally, limits the size of the pull-up transistor and preserves the power advantage.

III. Performance Comparisons of Dynamic Multiplexers

Using the conventional domino, FVFD, and SSPD circuit techniques, we designed and simulated 16-bit and 32-bit dynamic multiplexers in a 1.2-V, low-$\mathrm{V_T}$, 65-nm CMOS process. The conventional domino multiplexers were simulated with two different keeper ratios: a small keeper (1% keeper ratio) provides a reference for high performance, and a large keeper (7% keeper ratio) provides a reference for good noise tolerance. We found that a 2% keeper can be used with the SSPD multiplexer to achieve similar robustness (the same UNG) against noise as a conventional multiplexer with a 7% keeper, which demonstrates the improved noise tolerance of the SSPD topology. Since the FVFD technique only requires keeper transistors of minimum size, it has a very small keeper ratio of about 0.07%. The transistors in the pull-down network were of

TABLE I
SIMULATED DELAY, UNG AND AVERAGE POWER VALUES OF 16-BIT AND 32-BIT CONVENTIONAL, FVFD AND SSPD MULTIPLEXERS AT THE NOMINAL PROCESS CORNER

	16-bit Delay [ps]	32-bit Delay [ps]	16-bit UNG [V]	32-bit UNG [V]	16-bit Power [mW]	32-bit Power [mW]
					Pr{1} = 0.5	
Conventional (1% Keeper)	60.1	94.5	0.36	0.34	0.085	0.175
Conventional (7% Keeper)	99.8	152.9	0.44	0.40	0.128	0.234
FVFD	106.1	148.6	0.54	0.50	0.080	0.148
SSPD (2% Keeper)	78.6	85.5	0.39	0.40	0.107	0.176

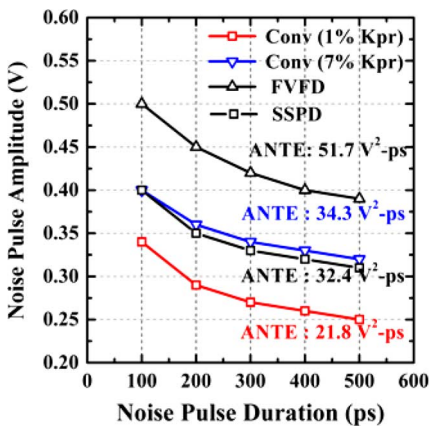


Fig. 5. Noise Immunity curves of 32-bit conventional, FVFD and SSPD multiplexers.

the same size in each of the three designs. Power measurements include the local clock buffer. The average power consumption was measured for an output state probability Pr{1} of 0.5 with a fanout-of-4 (or 1FO4) inverter load. The delay, UNG and average power results are shown in Table I. The noise signature can also be characterized by an additional noise metric called the average noise threshold energy (ANTE) [26]. The ANTE can be measured from the noise immunity curve (NIC) [27] which is the locus of points $(A_{\text{noise}}, W_{\text{noise}})$ at which a logic error first occurs. The noise immunity curves of 32-bit multiplexers are shown in Fig. 5.

The FVFD multiplexer has nearly the same delay as a conventional domino with a 7% keeper, which can be seen as a minor reduction in performance inherent in the charge-sharing topology. However, the FVFD multiplexer has a vastly improved noise performance: averaged across 16-bit and 32-bit cases, its UNG is 24% better than that of a conventional domino with an upsized 7% keeper. Also, a 32-bit FVFD multiplexer has an ANTE value 51% larger than a conventional domino with 7% keeper. The SSPD multiplexers, designed to equal the noise performance of a conventional domino with 7% keepers (same UNG), exhibit less delay than the FVFD multiplexers. Both the 16-bit and 32-bit SSPD multiplexers have a similar evaluation delay because the latter uses the two 16-bit sections that we have already mentioned. It must however be noted that the 16-bit SSPD multiplexer is much faster than both 16-bit

TABLE II
MINIMUM, NOMINAL CORNER (NN AT 27 °C), AND MAXIMUM VALUES OF EVALUATION DELAY FOR 32-BIT CONVENTIONAL, FVFD AND SSPD MULTIPLEXERS AT DIFFERENT PROCESS AND TEMPERATURE CORNERS

	32-bit Delay (Corner Simulations)			32-bit Delay (Monte Carlo Simulations)		
	Min. [ps]	NN 27°C [ps]	Max. [ps]	μ [ps]	σ [ps]	σ/ μ [in %]
Conventional (1% Keeper)	82.0	94.5	118.2	94.7	5.9	6.2
Conventional (7% Keeper)	134.4	152.9	209.7	156.3	14.5	9.2
FVFD	110.6	148.6	186.2	150.1	19.3	12.9
SSPD (2% Keeper)	71.9	85.5	111.7	85.9	5.5	6.4

FVFD and conventional domino with 7% keeper. We therefore see that while SSPD multiplexers are fast with good noise robustness, FVFD multiplexers have excellent noise immunity while being relatively slower. Further, for an output state probability of 0.5, 16-bit SSPD and FVFD multiplexers respectively consume 37.5% and 16.4% less power than the conventional domino with a 7% keeper. For 32-bit multiplexers, the equivalent figures are respectively 36.8% and 24.8%. The relative power advantage of the SSPD multiplexers over conventional domino is even more pronounced for biased output states [23].

We also tested the robustness of the proposed techniques against process variations by performing simulations at the five process corners (NN, FF, SS, FS and SF) for three different temperatures (27 °C, 55 °C, and 110 °C), and against random variations by performing 1000-point Monte Carlo (MC) simulations using industrial-hardware calibrated transistor statistical models. Table II gives the minimum, nominal and maximum evaluation delay of the three techniques obtained from corner simulations, and the mean (μ) and the standard deviation (σ) of the delay obtained from MC simulations. The delays given for the SSPD multiplexer are the average of the rise and fall delays, which were equalized at the NN corner. Compared to conventional domino with 1% keeper, using a 7% keeper results in a larger delay standard variation (14.5 ps) and higher delay variability (σ/μ) of 9.2%. This is expected as a strong keeper increases the feedback loop gain associated with the keeper transistor which also increases the delay variability [28]. The FVFD multiplexer uses a minimum-sized keeper but still has the worst delay standard variation of 19.3 ps. This might be explained by the presence of transistors operating with a limited overdrive which are more susceptible to process, voltage, and temperature (PVT) variations [29]. The SSPD multiplexer, using a small 2% keeper, has delay variability similar to the conventional domino technique with 1% keeper. The SSPD multiplexer's pulse generator has a 3-gates long delay path creating a pulse window which is sufficiently wide to limit the impact of process variations on the pull-up operation.

In summary, the FVFD technique significantly increases the noise immunity of a dynamic multiplexer and reduces its dynamic power dissipation, at the cost of an increase in the evaluation delay. The SSPD technique also uses less dynamic power, even though it is faster than FVFD. However, these improvements in performance come at a cost in terms of complexity:

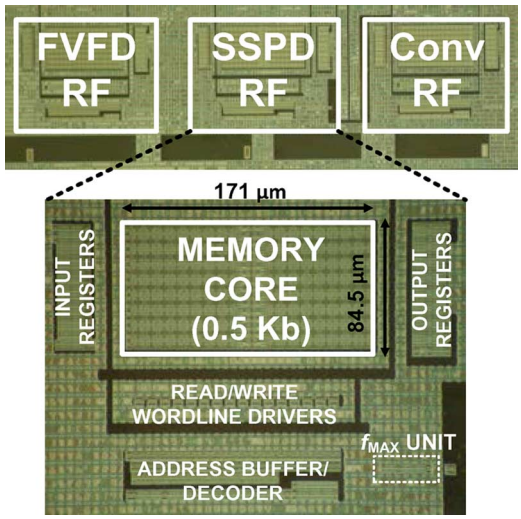


Fig. 6. Die photo of the register file test-chip.

both the SSPD and FVFD require more area than the conventional technique.

IV. Register File

A. Architecture and Circuit Design

Using a 65-nm CMOS technology, we implemented three different 32-word × 16-bits/word (0.5-Kb) 1-read, 1-write ported register files. These RFs severally used the conventional domino, FVFD and SSPD techniques to implement the bitline read-out multiplexers. Fig. 6 shows a micrograph of the chip. Both the read and write ports are single-ended, and the RF storage cell comprises two cross-coupled asymmetrically sized inverters. The block diagram of the register file is shown in Fig. 7(a). The bitline read-out circuits are 32-input dynamic multiplexers to test the performance of the proposed techniques with very wide fan-in structures. As discussed previously, the bitline is split into two sections for the SSPD technique.

In general, read is the critical operation which determines the noise robustness of the different bitline techniques as well as the cycle period. Therefore, we restrict our attention to the read operation. As shown in the timing diagram of Fig. 7(b), a complete read operation is performed in a single clock cycle. When the read enable (RE) signal goes high, the 5-bit read address is latched at the negative edge of the core clock CCLK and decoded by a static decoding stage during the low state. At the very next positive edge, the corresponding domino read word line driver is launched. The main memory core uses CLK_3, which is a delayed version of CCLK, to enable the read select signals (referred to as the read word lines RWL) to arrive during the evaluation phase. Finally, at the negative clock edge of CLK_3, the read word RWD is latched by the output registers. If the read access time T_{AC} is defined as the delay from the positive edge of CLK_3 until the rising transition on the read word RWD, then T_{AC} is the sum of the CLK_3 to RWL delay and the RWL to RWD delay. Only the RWL to RWD portion of the T_{AC} is affected by the bitline technique employed by the register file. The SSPD RF differs from the conventional and FVFD RFs in two ways: first, it uses static word line drivers whereas FVFD and conventional RFs use domino word line drivers; second,

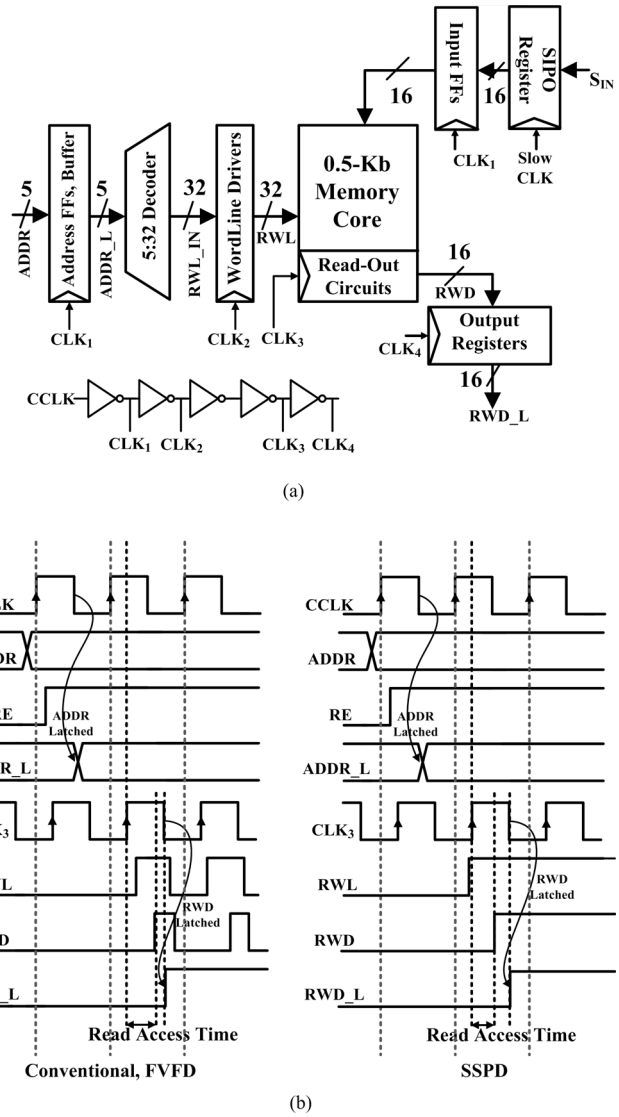


Fig. 7. (a) Block diagram of a register file, (b) the timing diagram of a single-cycle read operation.

since the SSPD RF requires clock-delayed operation, the decoder-driver and CLK_3 paths are adjusted to deliver the read select signals before the rising edge of CLK_3.

To compare the performance of the proposed techniques against the conventional domino read-out circuit for different keeper strengths, the latter was implemented using an externally controllable 2-bit keeper [14]. Compared to the conventional read-out circuit with a 7% keeper, the programmable keeper requires 35% more area. The 32-bit SSPD and FVFD multiplexers respectively required 2.4 and 1.4 times more area than the conventional domino multiplexer with an upsized 7% keeper. For relatively large structures like register files, the multiplexer area overheads do not have a significant impact on the overall core area (Table III). Like those discussed in Section III, the SSPD and FVFD multiplexers respectively use a 2% and a 0.07% keeper.

B. Maximum Frequency Measurement

To measure the read performance, 16-bit data word FFFF is first written into a particular location and then a single-shot read

TABLE III
PERFORMANCE SUMMARY OF 0.5-KBIT CONVENTIONAL, FVFD AND SSPD REGISTER FILES IN 1.2-V 65-NM LOW-V_t CMOS TECHNOLOGY

	Keeper Ratio	Measurement Results			
		Maximum Frequency at 1.2 V [GHz]	Average Read Power at 1.2 V [mW/GHz]	Area (Bitline Read-Out Circuit) [W μm × H μm]	Area (Memory Core) [W μm × H μm]
Conventional	1%	1.99	1.73	6.2 × 5.9 ($36.6\mu m^2$)	153.9 × 84.5 ($0.013mm^2$)
	3%	1.87	2.16		
	5%	1.86	2.50		
	7%	1.67	2.94		
FVFD	0.07%	1.84	0.84	6 × 6.2 ($37.2\mu m^2$)	153.4 × 84.5 ($0.013mm^2$)
SSPD	2%	2.46	1.94	6.2 × 10.3 ($63.8\mu m^2$)	171 × 84.5 ($0.015mm^2$)

is performed from the same location. Reading FFFF ensures that all the bitlines in the memory core switch during the read operation. Fig. 8 shows the schematic diagram of the f_{MAX} test unit used with each of the three register files to measure the maximum frequency of operation, together with timing diagrams illustrating the detection of a correct and an erroneous read operation. The externally-provided asynchronous read enable signal RE is first aligned with CCLK by a synchronization unit comprising a cascade of three flip-flops. The synchronized read enable signal SYNC_RE, which enables the decoders in the read path, is also the input to a flip-flop FF1 of the f_{MAX} test unit clocked by CLK_3. At the next CLK_3 positive clock edge after the rising transition of SYNC_RE, A rises, marking the beginning of the read operation in the memory core. After exactly one clock cycle, C transitions high, and FF3 latches the value at the output of one of the latched read word lines (RWD_L) on to NO_ERR, which we monitor externally. If the read operation of the data word FFFF is performed correctly, RWD_L will transition before C, and the NO_ERR signal will go high, signaling a successful read. However, when the clock frequency is faster than the inertial delay of the read-out circuit (the time taken to completely charge and discharge all capacitances in the circuit), the dynamic and the output nodes of the read-out dynamic multiplexer do not reach a steady state at the end of their precharge and evaluation phases. The read operation now takes more than one cycle to complete, and RWD_L arrives after C has transitioned high. NO_ERR remains low and an unsuccessful read is thus detected.

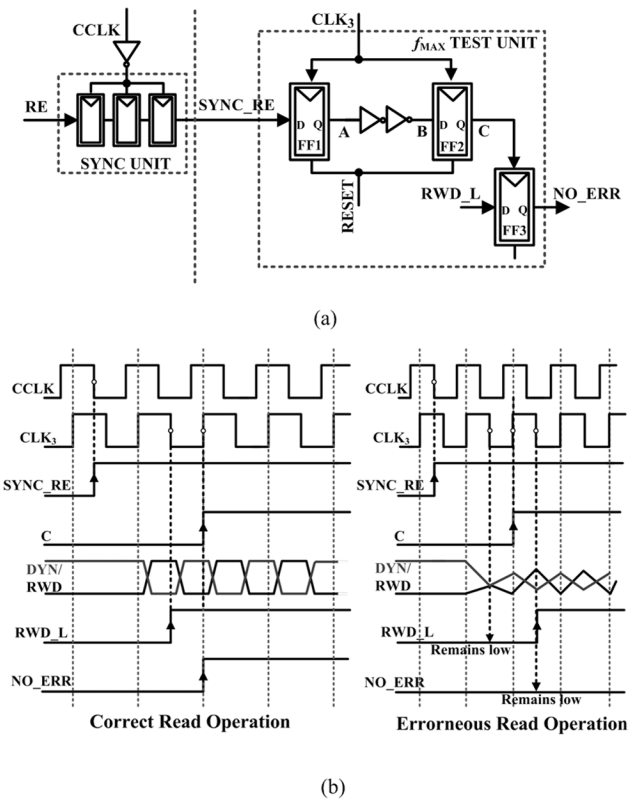
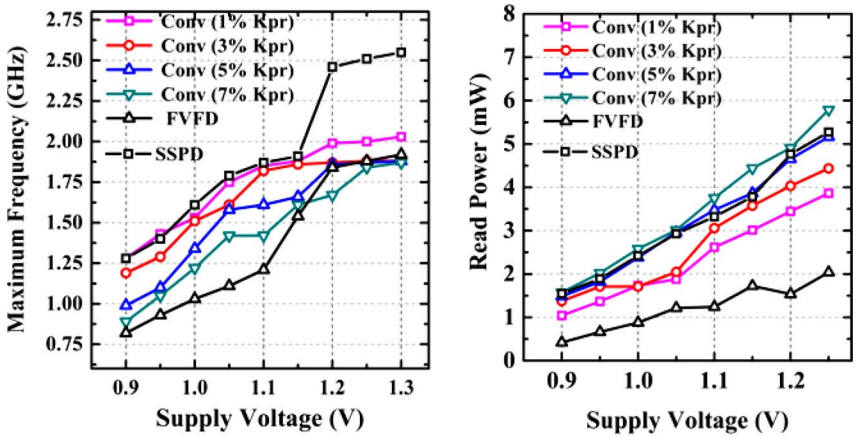


Fig. 8. (a) Setup for measurement of maximum frequency of operation (f_{MAX}), and (b) timing diagrams explaining correct and erroneous read operations.

C. Measurement Results

The read performance measurement results for the three register files are summarized in Table III. The shmoo plot of the variation of maximum frequency of operation with supply voltage and power dissipation for the three register files is shown in Fig. 9. As expected from the results for the dynamic multiplexers in Section III, the FVFD register files have significantly reduced read power, but they can only match the read speeds of conventional register files with upsized 5%–7% keepers. Compared to a conventional register file employing an upsized keeper (7% keeper ratio) which has a memory core read power dissipation of 2.94 mW/GHz at 1.2 V, the FVFD register file's memory core uses 71% lesser read power. Additionally, the measured maximum frequency of operation of the FVFD register, operating at 1.2 V, improves by 10%. The shmoo plot in Fig. 9(a) shows that the FVFD register file has comparable speed with a conventional register file with 5% keeper for nominal and overdrive voltages but at lower voltages, the FVFD register file becomes predictably slower due to its charge-sharing topology.

The SSPD register file, on the other hand, is comparatively faster. SSPD register file's high speed confirms the results in Section III where we saw that while a 16-bit SSPD multiplexer was slightly slower than a conventional multiplexer with 1% keeper, a 32-bit SSPD multiplexer was faster due to the split bitline. Further, since we measure power over several read cycles in which the same data word is read from the same location,



(a) (b)

Fig. 9. (a) Shmoo Plot of the register files for maximum frequency of operation with supply voltage. (b) Variation in memory core read power, expressed in mW, with supply voltage.

the measured average power of the SSPD memory core is dominated by the contention currents that flows through during every read cycle. It must be noted that this scenario does not capture the power savings resulting from limiting the swing on the bitlines. At the nominal supply of 1.2 V, the average read power is 1.94 mW/GHz (or 0.121 mW/GHz/bitline), which is smaller than the equivalent values of switching power for conventional memory cores with 3%–7% keepers. Compared to conventional memory core with a 7% keeper, the SSPD register file's memory core uses 34% lesser read power. We therefore see that for frequent read operations, when the power dissipation of the SSPD core is dominated by contention currents, the SSPD register file is faster and more energy efficient than the conventional register file. We expect the power advantage will remain for lower values of switching activity as well due to the reduced swing on the bitlines. Additionally, the power signature of the SSPD register file can be reduced even further by trading off some of its high performance, in which case a smaller pull-up transistor (M1) will be required in the SSPD multiplexers, reducing further the contention currents and hence the read power.

V. Conclusion

We began this paper by examining the related issues of simultaneously improving the noise immunity and reducing the switching power for wide fan-in dynamic multiplexers employed in the bitline read-out circuits of register file memory arrays. We stated that conventional designs are not viable in very deep submicrometer technologies because they are not robust against noise and use too much power. Conventional register file designs employ a single keeper in their read-out multiplexers with a single dynamic node, and the large bitline capacitance at this dynamic node has then to undergo a full rail-to-rail swing during a read operation. To reduce this switching power, we have introduced dual dynamic nodes into the register file bitline read-out circuits. The voltage swing on the primary dynamic node with a large bitline capacitance is thus restricted, while a second low-capacitance dynamic node still goes through a complete swing. These dual dynamic node techniques achieve high noise immunity, leakage tolerance and reduced switching power, but performance is not significantly affected. Measurement results from 0.5-Kb register files implemented in a 65-nm CMOS technology suggest that these techniques can be a promising choice for register files in very deep submicrometer technologies.

References

[1] W. Hwang, R. V. Joshi, and W. H. Henkels, "A 500-MHz, 32-word × 64-bit, eight-port self-resetting CMOS register file," *IEEE J. Solid-State Circuits*, vol. 34, no. 1, pp. 56–67, Jan. 1999.

[2] H. F. Dadgour and K. Banerjee, "A novel variation-tolerant keeper architecture for high-performance low-power wide fan-in dynamic OR gates," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 18, no. 11, pp. 1567–1577, Nov. 2010.

[3] R. K. Krishnamurthy, A. Alvandpour, G. Balamurugan, N. Shanbhag, K. Soumyanath, and S. Y. Borkar, "A 130-nm 6-GHz 256 × 32 bit leakage-tolerant register file," *IEEE J. Solid-State Circuits*, vol. 37, no. 5, pp. 624–632, May 2002.

[4] S. Hsu *et al.*, "A 4.5-GHz 130-nm 32-kB L0 cache with a leakage-tolerant self reverse-bias bitline scheme," *IEEE J. Solid-State Circuits*, vol. 38, no. 5, pp. 755–761, May 2003.

[5] K. Pagiamtzis and A. Sheikholeslami, "Content-addressable memory (CAM) circuits and architectures: A tutorial survey," *IEEE J. Solid-State Circuits*, vol. 41, no. 3, pp. 712–727, Mar. 2006.

[6] J. Sivagnaname, H. C. Ngo, K. J. Nowka, R. K. Montoye, and R. B. Brown, "Wide limited switch dynamic logic implementations," in *Proc. IEEE Int. Conf. VLSI Design*, 2006.

[7] J.-S. Wang, "Analysis and design of high-speed and low-power CMOS PLAs," *IEEE J. Solid-State Circuits*, vol. 36, no. 8, pp. 1250–1262, Aug. 2001.

[8] S. Hsu *et al.*, "A 90 nm 6.5 GHz 256 × 64 b dual supply register file with split decoder scheme," in *Symp. VLSI Circuits Dig. Tech. Papers*, 2003, pp. 237–238.

[9] M. Anders, R. Krishnamurthy, R. Spotten, and K. Soumyanath, "Robustness of sub-70 nm dynamic circuits: Analytical techniques and scaling trends," in *Proc. Symp. VLSI Circuits*, 2001, pp. 23–24.

[10] M. W. Allam, M. H. Anis, and M. I. Elmasry, "High-speed dynamic logic styles for scaled-down CMOS and MTCMOS technologies," in *Proc. Int. Symp. Low Power Electron. Des. (ISLPED)*, 2000, pp. 155–160.

[11] M. H. Anis, M. W. Allam, and M. I. Elmasry, "Energy-efficient noise-tolerant dynamic styles for scaled-down CMOS and MTCMOS technologies," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 10, no. 2, pp. 71–78, Apr. 2002.

[12] A. Alvandpour, R. K. Krishnamurthy, K. Soumyanath, and S. Y. Borkar, "A sub-130-nm conditional keeper technique," *IEEE J. Solid-State Circuits*, vol. 37, no. 5, pp. 633–638, May 2002.

[13] H. Mahmoodi-Meimand and K. Roy, "Diode-footed domino: A leakage-tolerant high fan-in dynamic circuit design," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 51, no. 3, pp. 495–503, Mar. 2004.

[14] C. H. Kim, K. Roy, S. Hsu, R. Krishnamurthy, and S. Borkar, "A process variation compensating technique with an on-die leakage current sensor for nanometer scale dynamic circuits," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 14, no. 6, pp. 646–649, June 2006.
[15] Y. Lih, N. Tzartzanis, and W. W. Walker, "A leakage current replica keeper for dynamic circuits," *IEEE J. Solid-State Circuits*, vol. 42, no. 1, pp. 48–55, Jan. 2007.
[16] R. G. D. Jeyasingh, N. Bhat, and B. Amrutur, "Adaptive keeper design for dynamic logic circuit using rate sensing technique," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 19, no. 2, pp. 295–304, Feb. 2011.
[17] D. Li and P. Mazumder, "On circuit techniques to improve noise immunity of CMOS dynamic logic," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 12, no. 9, pp. 910–925, Sept. 2004.
[18] R. Singh, A.-R. Kim, and S. Kim, "Footer voltage feedforward technique for wide fan-in dynamic logic," in *Proc. IEEE Int. SOC Conf.*, 2010, pp. 224–229.
[19] R. Montoye *et al.*, "A double precision floating point multiply," in *Proc. IEEE Int. Solid-State Circuits Conf.*, 2003, pp. 336–337.
[20] C. J. Akl and M. A. Bayoumi, "Single-phase SP domino: A limited-switching dynamic circuit technique for low-power wide fan-in logic gates," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 55, no. 2, pp. 141–145, Feb. 2008.
[21] G. Yee and C. Sechen, "Clock-delayed domino for dynamic circuit design," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 8, no. 4, pp. 425–430, Aug. 2000.
[22] R. Singh, J.-C. Son, U. Cho, G. Jung, M.-S. Kim, H. Lee, and S. Kim, "A static-switching pulse domino technique for statistical power reduction of wide fan-in dynamic gates," in *Proc. Great Lakes Symp. VLSI*, 2011, pp. 127–132.
[23] R. Singh, G. M. Hong, M. Kim, J. Park, W.-Y. Shin, and S. Kim, "Static-switching pulse domino: A switching-aware design technique for wide fan-in dynamic multiplexers," *Integration, the VLSI J.*, vol. 45, no. 3, pp. 253–262, Jun. 2012.
[24] K. Roy, S. Mukhopadhyay, and H. Mahmoodi, "Leakage current mechanisms and leakage reduction techniques in deep-submicrometer CMOS circuits," *Proc. IEEE*, vol. 91, no. 2, pp. 305–327, Feb. 2003.
[25] J. Tschanz *et al.*, "Comparative delay and energy of single edge-triggered and dual edge-triggered pulsed flip-flops for high-performance microprocessors," in *Proc. Int. Symp. Low Power Electron. Design*, 2001, pp. 147–152.
[26] L. Wang and N. Shanbhag, "An energy-efficient noise-tolerant dynamic circuit design," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 47, pp. 1300–1306, Nov. 2000.
[27] G. A. Katopis, "Delta-I noise specification for a high-performance computing machine," *Proc. IEEE*, vol. 73, no. 9, pp. 1405–1415, Sep. 1985.
[28] G. Palumbo, M. Pennisi, and M. Alioto, "A simple circuit approach to reduce delay variations in domino logic gates," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 59, no. 10, pp. 2292–2300, Oct. 2012.
[29] R. G. Dreslinski *et al.*, "Near-threshold computing: Reclaiming Moore's law through energy efficient integrated circuits," *Proc. IEEE*, vol. 98, no. 2, pp. 253–266, Feb. 2010.

Rahul Singh received the B.Tech. degree in electronics engineering from Indian Institute of Technology (Banaras Hindu University), Varanasi (formerly IT-BHU), India, in 2008, and the M.S. degree in electrical engineering from Seoul National University, Seoul, Korea, in 2011. He is currently working for Samsung Electronics, Korea, in the Processor Development Team. His research interests include clocking circuits and, variability and noise issues in the design of deep-submicrometer circuits.

Gi-Moon Hong received the B.S. and M.S. degrees in electrical engineering from Seoul National University, Seoul, Korea, in 2009 and 2011. Since 2011, he is working toward the Ph.D. degree at the same university. His research interests include low-power and high-speed serial link circuits and memory interface.

Suhwan Kim (M'01–SM'08) received the B.S. and M.S. degrees in electrical engineering and computer science from Korea University, Seoul, Korea, in 1990 and 1992, respectively, and the Ph.D. degree in electrical engineering and computer science from the University of Michigan, Ann Arbor, in 2001.

From 1993 to 1999, he was with LG Electronics, Seoul. From 2001 to 2004, he was a research staff member at the IBM T. J. Watson Research Center, Yorktown Heights, NY. In 2004, he joined Seoul National University, Seoul, where he is currently an Associate Professor of electrical engineering. His research interests encompass high-performance and low-power analog and mixed-signal integrated circuits, high-speed I/O circuits, and power electronics.

Dr. Kim served as a Guest Editor for IEEE JOURNAL OF SOLID-STATE CIRCUITS special issue on IEEE Asian Solid-State Circuits Conference. He has also served as the General Co-Chair and Technical Program Chair for the IEEE International SOC Conference. He has participated on the Technical Program Committee of the IEEE International SOC Conference, the International Symposium on Low-Power Electronics and Design, the IEEE Asian Solid-State Circuits Conference, and the IEEE International Solid-State Circuits Conference.