Pattern Grading for Testing Critical Paths Considering Power Supply Noise and Crosstalk Using a Layout-Aware Quality Metric *

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Abstract

Power supply noise and crosstalk are considered as the two major noise sources that negatively impact signal integrity in digital integrated circuits. In this paper, we propose a novel quality metric to evaluate path-delay fault test patterns in terms of their ability to cause excess delay on targeted critical paths. The proposed procedure quickly selects the best set of patterns for testing the critical paths under power supply noise and crosstalk effects. It also offers the design engineers a quick approach to evaluate the critical paths in static timing analysis (STA) and silicon to improve timing margin strategies. Simulation results demonstrate that the patterns selected by the proposed methodology generate the worst-case supply noise and crosstalk effects on target paths.

Categories and Subject Descriptors:
B.7.3 [Reliability and Testing]: Test generation
J.6 [Computer-Aided Engineering]: Computer-aided design

General Terms: Design, Reliability, Verification.

Keywords: Path Delay Test, Pattern Grading, Power Supply Noise, Crosstalk, Signal Integrity

1. INTRODUCTION

As technology scales, feature size of devices and interconnects shrink and silicon chip behavior becomes more sensitive to on-chip noise, process and environmental variations, and uncertainties. As reported by ITRS [1], the power supply noise and crosstalk effects significantly increase as technology scales to 65nm and below. The number of silicon failures and escapes caused by signal integrity is on the rise, because existing design tools and test methodologies cannot fully address these issues effectively. Commercial tools perform a vector-less estimation of the impact on circuit timing caused by such effects which seem inaccurate. Therefore, it is important to generate patterns that can be used to evaluate the noise impact on signal integrity before tape out and to excite the noise events during silicon validation and production test to capture the potential chip failures. However, it is not possible to take into account these noise sources/uncertainties by running current ATPG tools because of the pattern dependent characteristics (e.g. switching location and arrival time) of these noise sources. Considering the interactions and inter-dependencies between these noise effects, it is extremely difficult to develop an efficient SI-aware ATPG flow.

In this work we focus on path delay faults (PDFs) for efficient critical path delay testing and reducing test escapes. In general, it is easy to randomly fill the unspecified bits in a PDF pattern first, and then select the most effective ones by grading the resulting patterns based on their noise effects. In other words, we would be able to select the pattern that increases "multiple" noise effects. This is the main motivation of this work. We believe that the pattern grading technique proposed in this paper can also be used for other applications, such as diagnosis of any timing marginality and correlation between STA and silicon.

Several works have addressed power supply noise during pattern generation in [2]-[5]. There are also some approaches proposed to deal with crosstalk issues during verification and test in [6]-[9]. Many of the techniques mentioned above target maximizing power supply noise in a circuit (not path delay) to identify worst-case noise. Others target each effect individually, which are not able to provide a realistic insight to their cumulative impact on circuit and path delay. In this paper, a novel layout-aware pattern quality metric is developed to estimate the power supply noise and crosstalk effects together on the path under test for each pattern by taking into account the power distribution network structure, parasitic information, and switching information (location, direction, and arrival time) on the physical layout.

This paper is organized as follows. Section 2 describes our analysis of power supply noise and crosstalk effects and discusses the victims and aggressors for each noise. Section 3 introduces the proposed integrated methodology for pattern grading and selection considering both noises. In Section 4, experimental results and analysis are presented. Finally, the concluding remarks are given in Section 5.

2. ANALYZING PATTERN-DEPENDENT NOISE SOURCES: POWER SUPPLY NOISE AND CROSSTALK

A path delay consists of two parts: gates delay and interconnects delay. The gate delay is mainly impacted by voltage drop and the interconnect delay is mostly impacted

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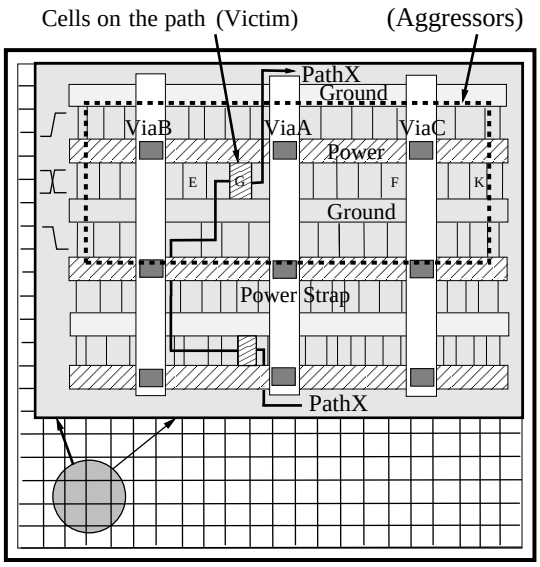

Figure 1: Critical path cell (victim) and neighboring cells (aggressors) identification.

by both. The increase in gate and interconnect delay has a direct impact on the path delay. In this section we present a new layout-aware analysis for these two effects.

2.1 Layout-Aware Power Supply Noise Analysis

Power supply noise (PSN) includes two major components: inductive ($L\frac{dI}{dt}$) and resistive power/ground voltage noise (IR). Although the proposed method can be expanded to include inductance noise impact, but in this paper, we only focus on the resistive noise increase, i.e. total voltage drop on both power and ground networks.

Figure 1 illustrates a typical standard cell layout consisting of cells placed in rows and power/ground rails tied horizontally to the cells. Rows are placed back-to-back and share a common power/ground rail. Figure 1 also shows part of a critical path (Path X) going through this region. Cell G of this critical path is placed in between the power and ground rails as shown in the figure. Simulations have been performed to analyze localized IR-drop effects caused by switching cells that are in close proximity to one another in [5], which shows the closer the neighboring cell is to the switching cell, the larger the voltage drop created by the switching cell and experienced by the neighboring cell.

As shown in the figure, cells E, F, and K are placed in the same row as cell G. After applying a PDF pattern a transition on cell E will cause more voltage drop on G than that on cell K. We refer to cell G as "victim" cell and the neighboring cells as "aggressors" because their switching activity can impact the voltage drop and performance of the victim cell. If there are m gates on a critical path, we consider all of them to be victim cells; some may be in the same row and others in different rows.

As shown in the dashed box in Figure 1, cells directly adjacent to G and those that extend beyond the right and left of *ViaC* and *ViaB*, respectively, are classified as aggressor cells. The block with dashed lines in Figure 1 shows all the aggressor cells for victim cell G. Identifying the effective aggressor cells, whose switching will impact the delay of victim cell (e.g. cell G), would help evaluate the IR-drop impact on path delay more accurately and efficiently.

2.2 Layout-Aware Crosstalk Analysis

As technology feature size scales, interconnect spacing and width are also being reduced. However, in order to keep the resistance low, the thickness of the wires is not scaled at the same rate. This produces tall sidewalls between long parallel interconnects separated by very little space, which creates a parasitic coupling capacitance between wires. Due to this fact, crosstalk has become a significant contributor to signal integrity problems in modern designs.

To evaluate the impact of crosstalk effects from the aggressors, we need to identify the aggressor nets for the critical paths, and this requires knowledge of the physical design. We use the extracted coupling capacitance of each of the nets to identify those that will have a significant effect. A distributed RC model is used as the interconnect model during parasitic extraction. We use a *minimum coupling threshold* during 3D extraction of the layout to prune aggressors with coupling capacitance smaller than the threshold. Using the coupling threshold will reduce the complexity of our analysis by filtering some of the neighboring nets that have almost no effect on the victim path. This will eliminate nets that may be near each other but are routed perpendicularly. The coupling threshold is defined as the minimum amount of capacitance between aggressor and victim that can impact the delay of transition traveling along the victim net.

3. PDF PATTERN GRADING PROCEDURE

In this paper, we model the power supply and crosstalk noise for each pattern with a quality metric according to the way they impact the path delay. The metric represents the amount of noise the pattern introduces and can be calculated quickly and efficiently. Using this metric the method we propose eliminates the extremely time-consuming SPICE simulation process and can grade the pattern accurately.

The quality value calculation procedure involves three major steps together with a pre-processing step as shown in the flow diagram in Figure 2. In the pre-processing step, we extract the physical parasitic effects of the layout using a commercial tool and acquire wire resistances, capacitances to ground, and coupling capacitances. Then, the critical paths are identified using static timing analysis considering these parasitic parameters. The three steps consist of (i) Effective Aggressor Identification, (ii) Pattern Quality Value (Q) Calculation for each effect, and (iii) Final Q Value Calculation for each pattern. Each of these steps are briefly described in the following.

• **Step 1: PSN and Crosstalk Aggressors Identification:** Design Exchange Format (DEF) file is used to identify the cells on the path under consideration in the layout. DEF file is generated from the layout design and contains the physical placement and routing information of the elements in the circuit. To identify the power supply noise aggressor cells, we developed a DEF file parser; using it we extracted a gate list which contains all the aggressor cells that are required for path delay analysis for the targeted critical path as described in Section 2.1.

To identify the crosstalk aggressor nets, since the timing analysis tool stores the parasitic coupling information, custom scripts have been developed to report this for each net of the critical path to assist in identifying the effective neighboring nets. If a net is coupled to a neighboring net in several locations, the tool will add the coupling capacitances into a single value. Only those segments with a coupling ca-

pacitance above a user-defined threshold will be identified as an aggressor net.

• **Step 2: Pattern Quality Value Calculator:** To monitor the transition of all the aggressors, we use a verilog programming language interface (VPI) routine during gate-level verilog simulation, which is done by the Synopsys VCS.

The metric named layout-aware weighted switching activity (*WSA*) [11] is used to calculate the pattern quality value in the presence of power supply noise. *WSA* for gate k in a circuit is calculated by:

$$WSA_k = d_k(\tau_k + \phi_k f_k), \text{ where}$$
$$d_k = \begin{cases} 1, & \text{Transition in required direction occurs} \\ 0, & \text{No transition} \end{cases} \tag{1}$$

For gate k, the WSA_k will be dependent on the gate weight, τ_k, the number of fan-out of this gate, f_k, and the fan-out load weight, ϕ_k. We assign different weight to each gate based on its area size and cell type. The pattern quality value (Q) for power supply noise is the sum of the *WSA* value of all N_{aggr_cell} aggressor cells, which can be expressed by the following equation:

$$Q_{PSN} = \sum_{k=0}^{N_{aggr\_cell}} WSA_k \tag{2}$$

If IR-drop analysis is available, average IR-drop of the path can be used instead of the *WSA* metric and acts as a more accurate quality value of the pattern. In this case, the quality value of power supply noise can be expressed as Equation 3.

$$Q_{PSN} = \sum_{j=0}^{N_{cell\_crit}} IR_j / N_{cell\_crit} \tag{3}$$

where N_{cell_crit} is the total number of cells on the critical path and IR_j is the IR-drop value of cell j on the path. In a similar way, we calculate Q for crosstalk noise using Equation 4.

$$Q_{Xtalk} = \sum_{i=0}^{N_{aggr\_net}} d_i \cdot C_i \cdot f(\Delta t), \text{ where}$$
$$d_i = \begin{cases} 1, & \text{Opposite transition} \\ 0, & \text{No transition} \\ -1, & \text{Same transition} \end{cases} \tag{4}$$
$$f(\Delta t) = \begin{cases} 1, & t_1 < \Delta t < t_2 \text{ and } \Delta t = t_a - t_v \\ 0, & \text{otherwise} \end{cases}$$

For all N_{aggr_net} aggressor nets the equation considers the direction of the transition with respect to associated nets of the targeted critical path, d, the amount of coupling between the two nets, C_i, and a timing window $f(\Delta t)$ to take into account the arrival time difference (Δt) of the transitions on aggressors (t_a) and victims (t_v). A positive value of Q_{Xtalk} indicates that the targeted path will experience slow-down due to induced crosstalk effects from the switching aggressors. Similarly, a negative Q_{Xtalk} indicates that the targeted path will experience speed-up.

• **Step 3: Final *Q* Calculation:** The total Q can be calculated using Equation 5.

$$Q = W_P * Q^{nom}_{PSN} + W_X * Q^{nom}_{Xtalk} \tag{5}$$

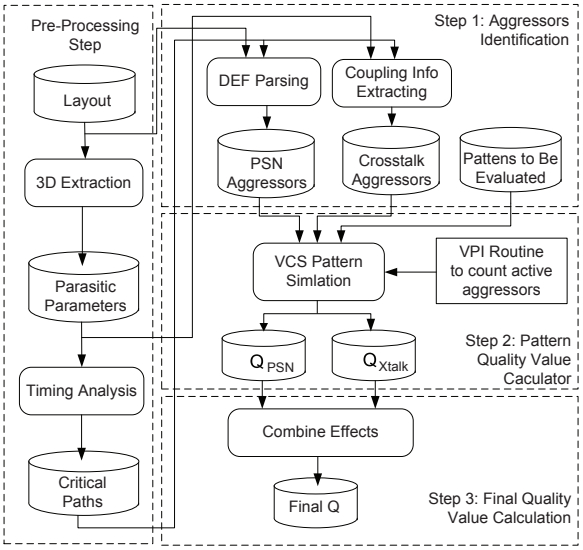

Figure 2: Flow diagram of the pattern quality value calculation procedure.

where Q^{nom}_{PSN} and Q^{nom}_{Xtalk} are normalized pattern quality values for power supply noise and crosstalk. Weights W_P and W_X are used to account for the different impacts that power supply noise and crosstalk have on path delay. Different technologies may have different combinations of weights. Empirical W_P:W_X value is suggested to be used for each technology. If no such value exists, a learning process is needed to generate the W_P:W_X values. A small number of fast-SPICE simulations can be done on small circuits to simulate the path delay for few patterns, and after calculating the patterns quality value Q, we could try different W_P:W_X ratios to calculate the correlation coefficients between Q and path delay and pick the one with best correlation. This step needs to be done only once for each technology node.

There are two main applications for the pattern quality value (Q): (1) to select the best pattern for PDF test; (2) to grade a pattern set in terms of their noise-induced delay for a given set of critical paths.

To perform pattern selection, we rank the patterns according to their *Final Q* values and then select the one with the largest Q value as the best pattern.

For a single pattern, by comparing its Q value with the lower bound and higher bound (if available), we obtain an estimate about how effective the pattern is in activating power supply noise and crosstalk to increase the path delay. The higher the Q value of a pattern, the better the pattern is in exciting the noise.

4. EXPERIMENTAL RESULTS

We implemented the pattern grading and selection procedures on ISCAS benchmark *s38417*. The physical layout was designed using the 180 *nm* Cadence Generic Standard Cell Library [12] with 1.8 V as its typical supply voltage. The program for parsing the DEF file to extract the victim and aggressor cells/nets list was developed in C. To validate and analyze the accuracy and complexity of our proposed method, we perform our method over a number of patterns and compare its pattern grading results with that from the fast-SPICE simulation.

First, we generated an unfilled path delay fault pattern for a target critical path. Launch-off-Capture (LOC) method is

Table 1: Analysis of *IR-Xtalk*/ *WSA-Xtalk* methods for *s38417* benchmark.

Method	Best Pattern		Worst Pattern		Corr. Coef.
	Pattern Index	Path Delay	Pattern Index	Path Delay	
Golden	542	6.97ns	923	6.26ns	N/A
IR-Xtalk	487	6.87ns	923	6.26ns	0.9
WSA-Xtalk	294	6.77ns	917	6.26ns	0.7

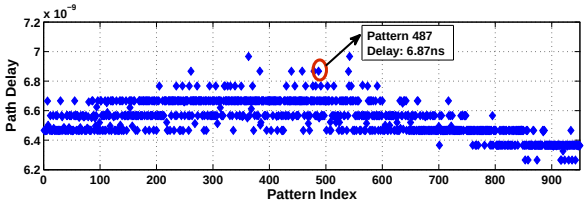

Figure 3: Path delay based on fast-SPICE simulation for 950 random-filled patterns.

used to generate PDF patterns, since there is a good chance that our pattern is functionally valid [10]. In this work for the purpose of demonstration, in order to create a pattern set with random switching activity to induce noise effects at different levels, we fill the pattern in the following way. We use our program to fill the don't-care bits 950 times randomly with bit '0' probabilities increasing by 5% every 50 patterns from 5% to 95% to generate 950 PDF patterns for the path under test. For example, patterns 100 to 150 are filled with around 15% don't-care bits as '0' and the remaining don't-care bits as '1'.

A transistor level fast-SPICE simulation using the SPICE model of the layout with Synopsys NanoSim is used to verify the accuracy of our pattern grading and selection procedure. During the fast-SPICE simulation, to account for the power supply noise effect, we annotate the SPICE netlist with new power/ground supply voltages for each gate/cell using IR-drop analysis results obtained using Cadence SOC Encounter. The ranking of patterns based on fast-SPICE simulation results are treated as "*golden*" values in the following analysis.

Here we implement two methods: (1) *IR-Xtalk*: using IR-drop based Q_{PSN}^{nom} metric for PSN and Q_{Xtalk}^{nom} for crosstalk noise; and (2) *WSA-Xtalk*: using *WSA* based Q_{PSN}^{nom} metric for PSN and Q_{Xtalk}^{nom} for crosstalk noise. According to Equation 5 and using $W_P : W_X = 8$, we calculate the final Q for each pattern and rank the 950 patterns.

Table 1 summarizes the best and worst pattern reported by both methods and compares their path delays with the golden ones obtained from fast-SPICE. As can be seen from Table 1, the *IR-Xtalk* method shows a higher correlation value and provides the best pattern with longer path delay. This is because IR-drop is a more accurate model for power supply noise than the *WSA* values. For this reason, if IR-drop analysis is available we recommend using the *IR-Xtalk* method; while if only a rough estimation provides enough accuracy and speed is preferred, the *WSA-Xtalk* method provides a satisfactory solution. The performance of the *WSA-Xtalk* method could be improved if we adopt a more elaborate *WSA* model in the future.

Figure 3 shows the path delays of these patterns obtained by running fast-SPICE simulation. From it we can see only 2 patterns have path delay longer than pattern 487, which is the best pattern selected through *IR-Xtalk* method.

Table 2: CPU Run-Time Comparison for *s38417* benchmark.

Number of Patterns	Our method		Fast-SPICE simulation
	WSA-Xtalk	*IR-Xtalk*	
1	0.43 s	0.8 s	18 $mins$
100	50 s	60 s	29.5 hrs
1000	13 $mins$	20 $mins$	$\simeq$300 hrs

The CPU run-time comparison between our pattern grading method and selecting patterns by running the fast-SPICE simulation is shown in Table 2. The simulations were performed on an x86 server architecture, running a Linux OS, 8 CPU cores clocked at 2.826 GHz, and 32GB of RAM. From this result, we can see that our proposed method has great advantage in terms of CPU run-time.

5. CONCLUSION

In this paper, we proposed a novel pattern grading and pattern selection procedure to quickly and efficiently evaluate the patterns in terms of their ability to increase path delay. The procedure is based on a novel quality metric for power supply and crosstalk noises. By evaluating the patterns with a quality metric to represent the impact of the active aggressors on path delay, the proposed procedure characterizes the patterns very quickly. The simulation results demonstrate (i) the effectiveness of the pattern evaluation and pattern selection process and (ii) significant reduction (about 1000X) on CPU run-time.

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