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The Major Physical Layer Constraints of Fiber Optical fiber Packet Switch Architectures

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Abstract — Many optical packet switch (OPS) architectures are proposed and demonstrated. In the design of these architectures, most of the attention is paid on the network layer parameters like high through put (low packet loss probability) and low latency, etc. and to achieve these goals. The structure of the architectures becomes very complex. In real scenarios, these architectures may not work efficiently because of physical layer constraints. Hence, cross layer optimization needs to be considered. This paper addresses the major physical layer constraints, and it has been found that the optical packet switch architecture can work efficiently within the bounded regimes which can be called as an operation window.

Index Terms — Tunable Wavelength Converter (TWC), Optical Packet Switch, Multi-Wavelength Buffer, Loop Buffer

I. Introduction

The important functionalities of photonic packet switching [1] are packet synchronization, clock recovery, packet routing, control, contention resolution and packet header replacement. In OPS, buffering is required when more packets arrive for the same destination than there are output ports available leading to that destination. One of the contending packets will be directed to the output port that will lead the packet towards destination, and rests of them have to be stored in random access memory (RAM). True all-optical RAM for photonic packet switching is still very challenging [2], and current proposed OPS switch architectures and proof-of-concept implementations still rely on fiber delay lines (FDL). To realize the buffering using FDL, some additional components are also required and thus give rise to the birth of many optical packet switch architectures. The overviews of some of the existing optical packet switch architectures are well described in [1]. In broad sense, optical packet switch architecture can be classified into three categories:

1. Wavelength routed photonic packet switch, [3] - [6].
2. Broad-cast and select type switch, [7] - [14].
3. (AWG)/Space switch based packet switch [15] - [21].

Overall, the design of the optical packet switch architecture is a complex problem and in most of the architectures, one problem is suppressed at the expense of other. In few architectures, physical layer problems have been mitigated with a complex control structure. Generally the performance of the switches is measured in terms of packet loss probability and average delay; these parameters can only provide behavior of the switch at the network layer. But parameters related to physical layer have not been discussed, which also plays an important role in the performance of the switch architectures. In this paper, impact of physical layer parameters is investigated on the switch and operation window is derived in which switch can work effectively. We have also shown the effect of physical layer impairments on the packet loss probability. The concept of the operation window is elaborated by considering two multi-wavelength optical packet switch architectures. The list of all the parameters considered in this paper is presented in Table 3.

The paper is organized as follows. In section II, The Major Physical Layer Constraints with Operating Window is discussed. Design parameters, design Constraints and motivation are discussed in section III of the paper. Section IV concludes the paper.

Table 1: Critical Attributes and their Effect

Attribute	Effect	Reference
Attenuation	Scaling become Critical	[22]
Dispersion	Bit Rate gets limited	[22]
ASE Noise	Number of re-circulation gets reduced	[22]
FWM	Number of re-circulation gets reduced	[22]

Table 2: Performance Evaluation under Various Attributes

Performance Measure	Refer -ence
Loss, power, noise and BER analysis	[22]
Affect of FWM	[22]
Placement of Regenerators	[25]
Packet Loss Probability (Without Re-circulation Limits)	[26]
Packet Loss Probability (With Re-circulation Limits)	[27]
Packet Loss Probability (In presence of Regeneration)	[12]

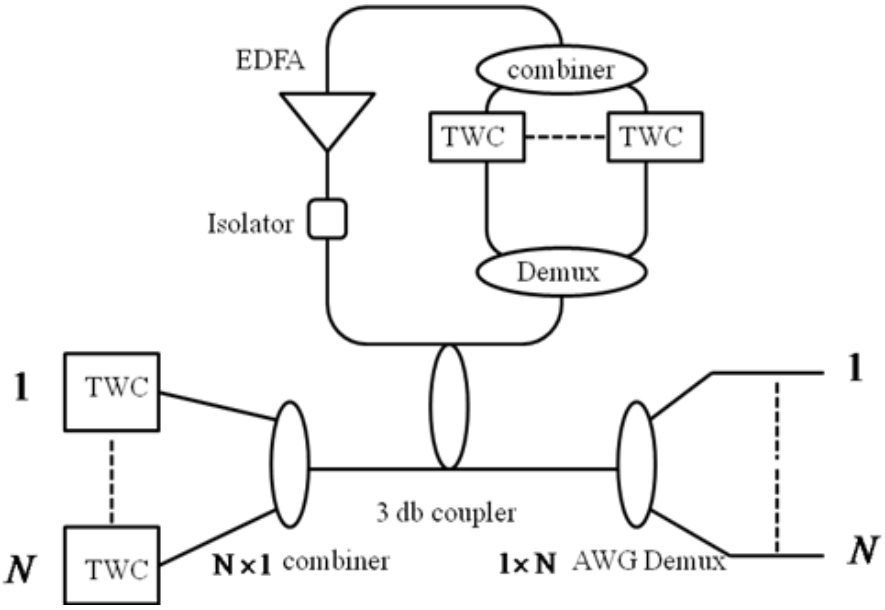

Fig. 1: Description of architecture A1

II. The Major Physical Layer Constraints with Operating Window

In past many loop buffer based architectures have been proposed and demonstrated, and comparative study of some of the loop buffer based architectures is performed in [14] and it was found that the architecture (A1) shown in Figure 1, performs better than other compared architectures in terms of packet loss probability and other functionalities (control points, buffer usage, loss analysis). Here, in this paper we have celebrated the concept of operation window by considering architecture A1.

2.1 Operation Window

In optical packet switched system, the various attributes like attenuation, dispersion, bit-rate, buffering capacity are interdependent. Hence, the overall design of OPS architecture is very complex and proper design guidelines cannot be fixed easily. Here, we have made an attempt to provide fundamental guidelines in terms of `operation window'. The size of the operation window of the optical communication depends on large number of attributes (nearly countless) and most important one are shown in Figure 2. These constraints push the switch operation in narrow region. The operation window start to shrink as any one of the above mentioned effects starts to dominate. For example, as the number of input channels increases (N) the total power propagating through the fiber increases $(\sum_{i=1}^{N} NP_i$ here P_i is the power of $'i^{th}'$ channel) and due to the non-linear effect, the size of the operation window starts to shrink (Figure 2). The physical layer constraints that critically effect the performance of the architectures are: attenuation, dispersion and noises of the various components. Dispersion limits the maximum possible bit rate; minimum possible loop length limits minimum possible storage in the buffer. Buffer depth (maximum number of possible wavelengths in the buffer) is limited by the insertion loss. The length of the unit slot which is equal to the length of the fiber loop (L_{Loop}) is evaluated using [17].

$$L_{Loop} = \frac{cb_n}{nB_R} \tag{1}$$

Here, c is the speed of light, b_n is number of bits stored in the fiber loop, n is the refractive index and B_R is the bit rate. Figure 3, shows the operating window of the OPS architectures which is divided into five separate regions. The lines drawn (on logarithmic scale) in Figure 3, are not to scale; they only represent the boundary of different regimes.

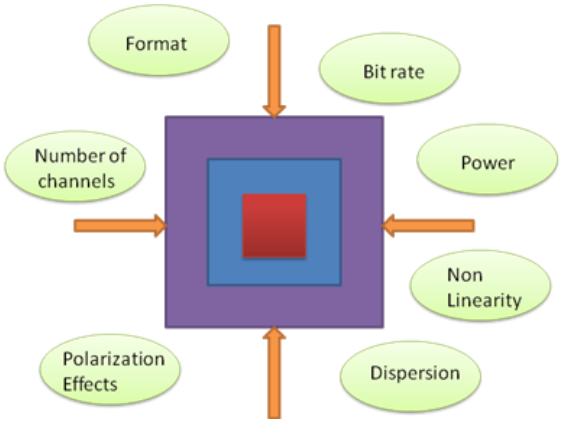

Fig. 2: Schematic of the operation window

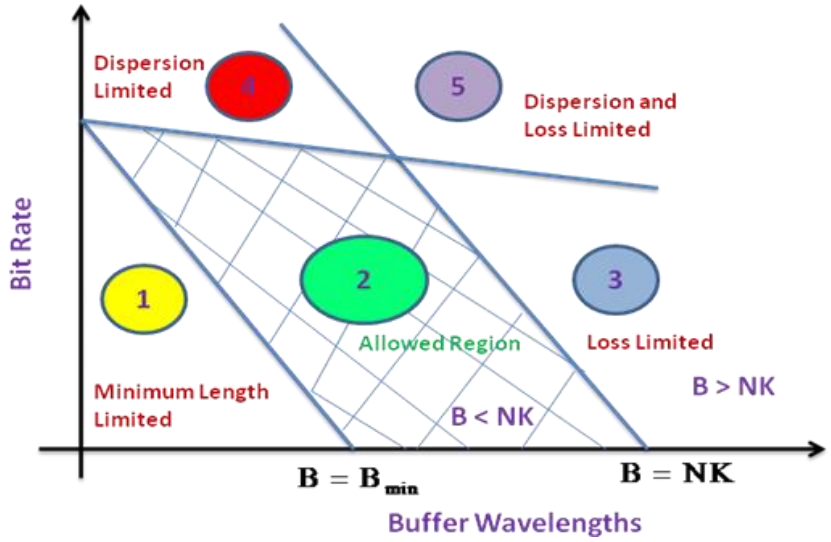

Fig. 3: Schematic of the bounded regions

Table 3: List of Symbols

Symbol	Parameter
N	Size of the Switch
B	Hardware Buffer Space (size of buffer demux/splitter)
ρ	Load
BL	Average Burst Length
B_R	Bit Rate
σ^2	Variance
Q	Error Function
L_{EDFA}	EDFA Length
I	Photo-current
h,t	Head, tail fiber length
n	Refractive Index
v	Frequency
b_n	Number of Bits
B_e	Electrical Bandwidth
B_o	Optical Bandwidth
R	Responsivity
P_{in}	Input Power
$\triangle\lambda$	Source Spectral Width
h	Planck Constant

2.2 Region-1

The region-1 of the figure shows the practical size limitations due to the minimum length constraints of the loop that cannot be less than the summation of head and tail fiber length of the devices used to create buffer i.e.,

$$L_{\min} = \sum_{q=1}^{z} \left(h_q + t_q \right) \tag{2}$$

Here, '*h*' and 't' represent the head and tail fiber lengths of the devices, while assuming '*z*' devices in the buffer. If EDFA is used then minimum length of the buffer will be given by

$$L^T{}_{\min} = \sum_{q=1}^{z} (h_q + t_q) + L^{\min}{}_{EDFA} \tag{3}$$

Where $L^{\min}{}_{EDFA}$ is the minimum length of EDFA to provide sufficient gain. Therefore,

$$L_{Loop} \geq L^T{}_{\min} \tag{4}$$

Which in turn limits the ratio $\frac{b_n}{B_R}$. Therefore, at a given bit rate the minimum length of the loop decide the minimum possible storage. Moreover, minimum buffer length is also depends on the number of packets that need to be stored in the buffer using WDM technique.

Table 4: Length of the EDFA to provide the sufficient gain [17]

Buffer Capacity (B)	Gain (G)	Length of EDFA
4	16.85 dB	10 m
8	21.75 dB	11m
16	26.65 dB	14 m

As the number and size of the buffer components increase in a number of wavelengths that need to be

accommodated. Hence, to compensate comparatively larger loop loss the length of the EDFA has to be increased (refer Table 4) and in-turn increases loop length. Therefore, in case of fixed length packets comparatively smaller bit-rate can be supported.

2.3 Region-3

In most of the OPS architectures, each packet placed inside the buffer need to be controlled separately and for this separation, generally demux are used. In architecture A1, each port of the demux allows only one wavelength to pass through it. Hence, apparently the size of the buffer demux $(1\times B)$ decides the number of buffer wavelengths that can be accommodated in the buffer $(\lambda_1....\lambda_B).$ hence, in the buffer single wavelength corresponds to single packet storage. Therefore, as the number of buffer wavelengths increases, loss of the loop increases. The loss of the loop is compensate by EDFA to restore signal level and increases the maximum number of allowed re-circulations. But the allowed re-circulations cannot be arbitrarily large as it is now limited by the ASE noise of the amplifier. Hence, effectively as the buffer space (decided by the port of the demux, hence *B*) increases, maximum number of allowed re-circulations (*K*) decreases. Here, a relation between *B* and *K* is obtained. In the optical communication, for Intensity modulated/Direct detection (IM/DD) system, under Gaussian noise approximation the expression for BER is given by [26].

$$BER = Q\left[\frac{I(1)-I(0)}{\sigma(1)+\sigma(0)}\right] \tag{5}$$

Where, $Q(x)$ is error function which denote the probability that a zero mean unit variance Gaussian random variable exceeds the value *x*. Thus,

$$Q(x) = \frac{1}{\sqrt{2\pi}}\int_x^{\infty} e^{-\frac{y^2}{2}}dy \tag{6}$$

In the expression 5, $I(1)$, $\sigma(1)$ and $I(0)$, $\sigma(0)$ are the photocurrent and noise variances for bit '1' and '0' respectively.

Or,

$$Q^{-1}\left[BER\right] = R\left[\frac{P(1)-P(0)}{\sigma(1)+\sigma(0)}\right] \tag{7}$$

In loop buffer based architecture, the dominant noise is sig-ASE beat noise [17] hence the expression can be written as,

$$Q^{-1}\left[BER\right] = \left[\frac{P(K)}{2\sqrt{P(K)P_{sp}(K)\frac{B_e}{B_o}}}\right] \tag{8}$$

while assuming extinction ratio $\frac{P(1)}{P(0)}$ as infinity and where $P(K)$ and $P_{sp} = K_{nsp}(G-1)h\nu B_o$ is the signal and noise power respectively, after K re-circulations. Referring to Figure 1, A_{in} is loss of the input unit consist of TWC and combiner, A_{out} is loss of the output unit consist of demux only. Considering A is the loss of loop and G is the gain of the EDFA whereas, P_{in} is the input signal power. The above equation can be modified as,

$$4(Q^{-1}[BER])^2 = \left[\frac{P_{in}A_{in}(AG)^K A_{out}}{Kn_{sp}(G-1)h\nu B_e A_{out}}\right] \tag{9}$$

In the loop buffer, the condition $AG = 1$, maximize the allowed re-circulations of the packet [17]. Thus,

$$K(G-1) = \left[\frac{P_{in}A_{in}}{4n_{sp}h\nu B_e(Q^{-1}[BER])^2}\right] \tag{10}$$

The bandwidth and bit rate of a digital signal are related but not equivalent. The relation between the two depends on the type of modulation scheme. The ratio of bit rate to the available bandwidth is referred to as the spectral efficiency. However, under an approximation for IM/DD system the $B_e \sim B_R$ and at a constant input power and for a particular wavelength the term at the right hand side of the equation becomes a constant i.e.,

$$K(G-1)B_R = Const \tag{11}$$

For larger gain,

$$K \approx \frac{Const}{GB_R} \tag{12}$$

The gain of the amplifier placed in the buffer, is also depends on the buffer size, because buffer size depends on the size of components used to realize the buffer structure and thus gain (G) of the amplifier needs to be changed to maintain the condition $AG = 1$. Hence,

$$G = f(B) \tag{13}$$

Where, $f(B)$ is a polynomial of *B*, Therefore,

$$K \approx \frac{Const}{f(B)_R} \tag{14}$$

Hence, *K* and *B* holds inverse relation. Thus, in the buffer once the condition *B=NK* is achieved then there will be no advantage of increasing the buffer space beyond *B* say B_{opt}. As the additional buffer space $B_{opt} - NK$ will remain effectively unused. The maximum number of allowed circulations can be increased by raising the power level of the signals, but at higher power levels, non-linear effects adversely affect the re-circulation count. Hence, selection of switch size (*N*) and buffering capacity (*B*) is not straight forward and, the buffering conditions (*B, K*) should be selected in such a way that minimum packet loss probability can be achieved as *B* and *K* are inversely related. Using, *K = B/N* the above expression can be written as,

$$\frac{B}{N} \approx \frac{Const}{f(B)B_R} \tag{15}$$

$$\frac{Bf(B)B_R}{Const} \approx N \tag{16}$$

One should note that as bit rate increases, thus the *const* cause's reduction of *B*. This explains the line separating region 2 and region 3.

2.4 Region-4

Region - 4 of the figure is dispersion limited region. The maximum bit rate is limited by the dispersion and in the mathematical from for IM/DD system can be written as [27].

$$B_R L_t |D| \Delta\lambda \le 1 \tag{17}$$

Here, L_t is the total length traversed by the data in the buffer, $|D|$ is the second order dispersion coefficient and $\Delta\lambda$,is the source spectral width. In terms of loop length (L_{Loop}), the total traversed length (L_t) can be written as $L_t = KL_{Loop}$. Here, *K* is the number of re-circulations that data takes in the buffer with $K_{\max} = B$ as the maximum possible allowed re-circulations can grew up to *B* re-circulations. By combining Equation 1 and 17 it can be deduced that the maximum possible storage in terms of number of bits is:

$$b_n \le \frac{n}{B_R |D| \Delta\lambda} \tag{18}$$

One can observed that for a given $|D|$ with increasing *B*, number of bits which can be stored are less. Once we increase B the B_R has to be reduced to satisfy Equation 17 as the traverse length (L_t) may increases due to the larger buffer space. This explains the negative slope as the line separating region 2 and 4.

2.5 Region-5

Region-5 of the figure is both dispersion and loss limited.

2.6 Region-2

The Region-2 of the Figure is allowed region which decide the size of the operating window. Therefore, switch architecture must be design in such a way that the operating conditions remain within the region 2.

III. Design Parameters and Motivation

3.1 Design Constraints

Finally the boundaries equation for the different zones can be summarized as,

$$\text{Zone 1-2 boundary} = L_{Loop} \ge L^T_{\min} \tag{19}$$

The above equation state that the length of the loop cannot be less than certain minimum length, and depends on the length of the EDFA that can provide sufficient gain.

$$\text{Zone 2-3 boundary} = \frac{Bf(B)B_R}{Const} \approx N \tag{20}$$

This equation state that the scaling of the buffer is not straight forward, and there is a limit on the maximum possible buffering space at a given bit rate.

$$\text{Zone 2-4 boundary} = B_R L_t |D| \Delta\lambda \le 1 \tag{21}$$

These equations define the constraints due to the dispersion on the buffering capacity.

3.2 Motivation

The above equations define the fundamental guidelines for the design of loop buffer based optical packet switch architectures. The above equations are proof-of-concept that OPS architectures cannot be scaled arbitrarily. Overall, buffer hardware size is not

easily scalable due to the physical layer constraints. These constraints motivate us to design OPS architectures in such a way that within limited hardware space a large number of packets can be stored. One of the possible solution is that the different port of devices used in the buffer, must be capable of handling more than one wavelengths or in other words ports of the device are insensitive to the wavelengths.

IV. Conclusions

In this paper, various major physical layer constraints (attenuation, dispersion, ASE noise and minimum length) are discussed, which may affect the performance of the fiber optical packet switch architectures, and it is shown that architectures can perform better in the bounded region only. And it is clearly explained that the multi-wavelength OPS architecture where the large number of packets (*NB*) can store and efficiently within the bounded region only.

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