Low Power Fir Filter Design Using Truncated Multiplier

A.Deepika[#1], A.Bhuvaneswari[*2]

[#]*PG student(Applied Electronics)&Electronics and communication engineering &Jayaram college of Engineering and Technology, Trichy, India.*

Assistant professor& Electronics and communication engineering &Jayaram college of Engineering and Technology, Trichy, India.

Abstract--- **In this paper Low-cost finite impulse response(FIR) design are presented using the concept of faithfully rounded truncated multipliers. We jointly consider the effective of bit width and hardware resources without sacrificing the frequency response and output signal accuracy. Non-uniform coefficient quantization with proper filter order to minimize the cost of total area. Multiple constant multiplication/accumulation in a pipelined direct FIR structure is implemented using an improved version of truncated multipliers. Comparisons with previous FIR filter design approaches show that the proposed design achieve the best area and power results.**

***Index Terms*—Digital signal processing (DSP), faithful rounding, truncated multipliers, FIR filter design.**

I. Introduction

Linear phase finite impulse response (FIR) filters are widely used in digital signal applications such as speech coding, image processing, sampling of multiple systems, etc. Although the stability and linear phase is guaranteed, the complexity and power consumption of the linear phase FIR filter are usually much higher than that of the infinite impulse response (IIR) filter which meets the same magnitude response specifications. Therefore, many efforts have been dedicated to the design of low complexity and low-power linear phase FIR filters.

Multiplication of two numbers generate a product With twice the original bit width. It is usually desirable to truncate the product bits to the required precision to reduce area cost, leading to the design of truncated multipliers or fixed-width multipliers. Fixed-width multipliers, a subset of truncated multipliers, compute only n most significant bits (MSBs) of the $2n$-bit product for $n \times n$ multiplication and use extra correction/compensation circuits to reduce truncation errors.

There are two basic FIR structures, direct form and transposed form for a linear-phase even-order FIR filter. In the direct form in the multiple constant multiplication (MCM)/accumulation (MCMA) module performs the concurrent multiplications of individual delayed signals and respective filter coefficients, followed by accumulation of all the products. Thus, the operands of the multipliers in MCMA are delayed input signals $x[n-i]$ and coefficients a_i.

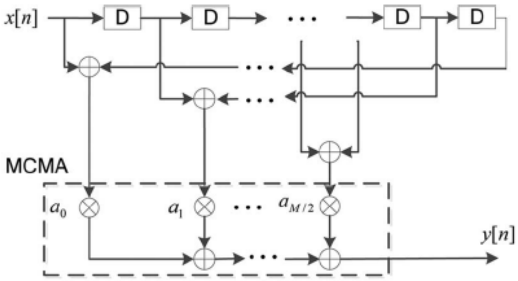

Fig-1 Direct form linear phase FIR filter

The basic FIR filter is expressed as in the form of

$$Y[n]=\sum_{i=0}^{m-1} a_i\ x[n-i].$$

In an M-level pipelined system, the number of delay elements in any path from input to output is (M-1) greater than that in the same path in the original sequential circuit. Pipelining reduces the critical path, but lead to a penalty in terms of an increased latency. Latency is the difference in the availability of the first output data in the pipelined system and the sequential system. Two main drawbacks: increase in the number of latches and in system.

An important design issue of FIR filter implementation is the optimization of the bit widths for filter coefficients, which has direct collision on the area cost of arithmetic units and registers. In addition, since the bit widths after multiplications grow, many DSP applications do not require full-precision outputs. Instead, it is desirable to produce faithfully rounded outputs where the total error introduced in quantization and rounding is no more than one unit of the last place (ulp) defined as the weighting of the least significant bit (LSB) of the outputs. In this brief, we present low-cost implementations of FIR filters based on the direct structure in Fig. 1 with faithfully rounded truncated multipliers. The MCMA module is realize by accumulating all the partial products (PPs) where unnecessary PP bits (PPBs) are uninvolved without affecting the final precision of the output. The bit widths of all the filter coefficients are minimized using non uniform quantization with unequal word lengths in order to reduce the hardware cost while still satisfying the specification of the frequency response.

II. QUANTIZATION AND OPTIMIZATION

A generic flow of FIR filter design and implementation can be divided into three stages: finding filter order, coefficient quantization, and hardware optimization. In the first stage, the filter order and the corresponding coefficients of infinite precision are determined to satisfy the specification of the frequency response. Then, the coefficients are quantized to finite bit accuracy. lastly, various optimization approaches such as CSE are used to minimize the area cost of hardware implementations. Most prior FIR filter implementations focus on the hardware optimization stage. Behind FIR filter operations, the output signals have larger bit width due to bit width expansion after multiplications. In several practical situations, only partial bit of the full-precision outputs are needed.

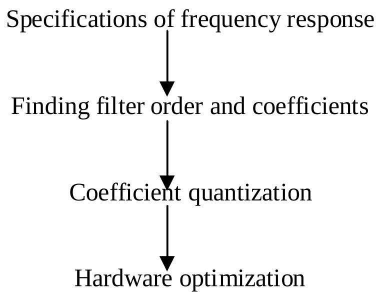
Specifications of frequency response
Finding filter order and coefficients
Coefficient quantization
Hardware optimization

Fig-2 Stages of digital FIR filter design and implementation

For example, assuming that the input signals of the FIR filter have 12 bits and the filter coefficients are quantized to 10 bits, the bit width of the resultant FIR filter output signals is at least 22 bits, but we might need only the 12 most significant bits for subsequent processing. In this brief, we adopt the direct FIR structure with MCMA because the area cost of the flip-flops in the delay elements is smaller compared with that of the transposed form. Furthermore, we jointly consider the three design stages in order to achieve more efficient hardware design with faithfully rounded output signals. Unlike conventional uniform quantization of filter coefficients with equal bit width, the non uniform quantization technique with possibly different bit widths is adopted in this brief.

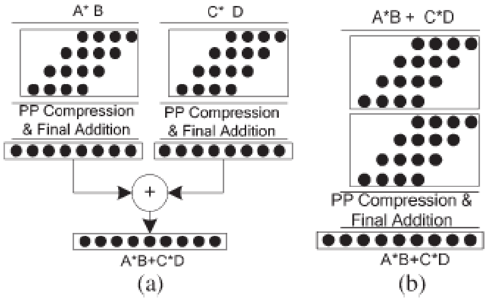
A* B
C* D
A*B + C*D
PP Compression & Final Addition
PP Compression & Final Addition
+
A*B+C*D
(a)
PP Compression & Final Addition
A*B+C*D
(b)

Fig-3:Multiplication/Accumulation using(a)individual PP compression (b) combined PP compression

After coefficient quantization, we perform recoding to minimize the number of nonzero digits. In this brief, we consider CSD recoding with digit set of {0, 1,−1} and radix-4 modified. Booth recoding with digit set of {0, 1,−1, 2,−2} and select the one that results in smaller area cost.

While most FIR filter designs use minimum filter order, we observe that it is possible to minimize the total area by slightly increasing the filter order. Therefore, the total area of the FIR filter is estimated using the subroutine area_ cost_ estimate using this approach. Indeed, the total number of PPBs in the MCMA is directly proportional to the number of FA cells required in the PPB compression because a FA reduces one PPB. After Step 1 of uniform quantization and filter order optimization, the non uniform quantization in Step 2 gradually reduces the bit width of each coefficient until the frequency response is no longer satisfied. Finally, we fine-tune the non uniformly quantized coefficients by adding or subtracting the weighting of LSB of each coefficient and check if further bit width reduction is possible. Using the algorithm we can find the filter order M and the non uniformly quantized coefficients that lead to minimized area cost in the FIR filter implementation.

III. TRUNCATED MULTIPLIER

Parallel multipliers are normally implemented as either carry-save array or tree multipliers. In many computer systems, the (n+m)-bit products produced by parallel multipliers are rounded to *r* bits to avoid growth in word size. As presented in truncated multiplication provides an efficient method for reducing the hardware requirements of rounded equivalent multipliers. With truncated multiplication, only the r+k most-significant columns of the multiplication matrix are used to compute the product. The error produced by omitting the m+n−r−k least-significant columns and rounding the final result to *r* bits is estimated, and this estimate is added the length of with the r + k most-significant columns to produce the rounded product. Although this lead to additional error in the rounded product, various technique have been developed to help limit this error.

One method to give back for truncation is Constant Correction Truncated (CCT) Multipliers. In this method constant is added to columns n+m−r−1 to n+m−r−k of the multiplication matrix. The stable help compensate for the error introduced by omitting the n +m− r – k least-significant columns (called reduction error), and the error due to rounding the product to r bits (called rounding error). The expected value of the sum of these error Etotal is computed by assuming that each bit in A, B and P has an equal chance of being one or zero. Consequently, the expected value of the total error is the sum of expected reduction error and the expected rounding error as

$$E_{total} = E_{reduction} + E_{rounding}$$

The constant Ctotal is obtained by rounding Etotal to r + k fractional bit, such that

$$\text{Ctotal} = \frac{-\text{round}(2r+k \cdot \text{Etotal})}{2r+k}$$

Where round(x) indicates that *x* is rounded to the nearby integer. Although the value of *k* can be chosen to limit the maximum absolute error to a specific correctness, this paper assumes the maximum total error is limited to one unit in the last place (i.e., 2−*r*).In constant correction method design the lower N columns of a parallel multiplier are truncated and a correction is then added to the remaining most significant columns. The Constant Correction Methods (CCM) uses a constant value, independent on the actual values of the inputs, in order to estimate the LSP minor. The multiplier output can be written as:

$$\text{PCCM} = \text{trun}(\text{SMSP} + \text{SLSP major} + \text{constant})$$

where SLSP major is the weighted sum of the elements of the LSP major. In this technique the LSP is eliminated and is substituted by a constant term, calculated considering only the misplace carries. This approach reduces up to 50% the area of the full-width multiplier, but introduces a rather large error, which rapidly increases with n, resulting impractical in most applications.

Another method to compensate for the truncation is using the Variable Correction Truncated (VCT) Multiplier. With this type of multiplier, the values of the partial product bits in column m+n−r−k−1 are used to estimate the error due to leaving off the m+n−r−k least-significant columns. This is skilful by adding the partial products bits in column m + n − r − k − 1 to column m + n − r − k. To compensate for the rounding error, a stable is added to columns m+n−r−2 to m+n−r−k of the multiplication matrix. The value for this constant is

$$\text{Ctotal} = 2^{-S-1}(1 - 2^{-k+1})$$

which correspond to the expected value of the rounding error truncated to *r* + *k* bits. The basic design of the multiplier is the same as that of a constant correction fixed width multiplier. The least significant N-2 partial product columns of a full width multiplier are truncated. The partial product terms in the N- 1 column are then added to the partial product terms in the Nth column using full-adders. This is done in order to balance the error introduced due to truncation of least significant N-2columns. The correction term that is generated is based on the following arguments, 1) The biggest column in the entire partial product array of a full-width multiplier is the Nth column. 2) The Nth column contributes more information to the most significant N-1 columns than the rest of the least significant N-1 columns. The information presented could be made more accurate if the carry from the N- 1th column is preserved and passed onto the Nth column. 3) Adding the elements in N- 1th column to the Nth column provides a variable correction as the information presented is dependent on input bit. When all the partial product terms in the N-1th column are zero, the modification added is zero. When all the conditions are one, a different correction value is added. The accuracy of truncated multipliers can be significantly improved using variable correction truncated multipliers that compensate the effect of the dropped terms with a non constant return function. The multiplier output is computed as:

$$\text{PVCM} = \text{trun}\ (\text{SMSP} + \text{SLSP major} + f\ (\text{IC}) + \text{Kround})$$

where f (IC) is a suitable compensation function.

Another method, called a Hybrid Correction Truncated (HCT) Multiplier uses both constant and variable correction Techniques to reduce the overall error [14]. In order to implement a HCT multiplier a new parameter is introduced, p, that represents the percentage of variable correction to use for the correction. This percentage is utilized to choose the number of partial products from column m + n − r − k – 1 to be used to add into column m + n − r − k. The calculation of the number of variable correction bit is the following utilizing the number of bit used in the variable correction method, NHCT

$$\text{NHCT} = \text{floor}(N_{V\,CT} \times p)$$

Similar to both CCT and VCT multipliers but a HCT multiplier uses a modification constant to compensate for the error. However, since the correction constant will be based on a smaller number bit than a VCT multiplier to the correction constant is modified as follows

$$C_{VCT} = 2^{-r-k-2} \cdot \text{NHCT}$$

This produces a new improvement constant based on the difference between the new inconsistent correction constant and the constant correction constant.

$$\text{Ctotal} = \frac{\text{round}((C_{CCT} - C_{V\,CT}) \cdot 2_{r+k})}{2_{r+k}}$$

Most DSP and embedded systems engage the use of signed and unsigned binary numbers. Therefore, multiplication requires some mechanism to compute two's complement multiplication. A common implementation for two's complement multipliers is to use the basic mathematical equation for multiplication and use algebra to formalize a structure. The most popular of these implementation are called Baugh- Wooley multipliers. Each structure utilizes the same tree structure, however, several columns require complementation as well as adding compensation constants for sign extension.

IV. PRIORWORK

A. FIR Filter Design Using MCMAT

The FIR filter design in this brief adopts the direct form in Fig. 1 where the MCMA module sums up all the products $\hat{a}_i \times x[n - i]$.Instead of accumulating individual multiplication for each product, it is more efficient to collect all the PPs into a single PPB matrix with carry-save addition to reduce the height of the matrix to two, followed by a final carry propagation adder. Fig. 3 illustrates the difference of individual multiplications and combined multiplication for
A × B + C × D.

In order to avoid the sign extension bits, we complement the sign bit of each PP row and add some bias constant using the property $\bar{s} = 1 - s$, where *s* is the sign bit of a PP row, as shown in Fig. 5. All the bias constants are collected into the last row in the PPB matrix. The complements of PPBs are denoted by white circles with over bars.

In the faithfully rounded FIR filter realization and it is required that the total error introduce during the arithmetic operations are no larger than one ulp. We modify a recent truncated multiplier design in so that more PPBs can be deleted, leading to smaller area cost. Fig. 4 compares the two approaches. In the removal of unnecessary PPBs is composed of three processes: deletion, truncation, and rounding. Two rows of PPBs are set undeletable because they will be removed at the subsequent truncation and rounding. The fault ranges of deletion, truncation, and rounding before and after adding the offset constants. The gray circles, crossed green circles, and crossed red circles represent respectively the deleted bits, truncated bits, and rounded bits.

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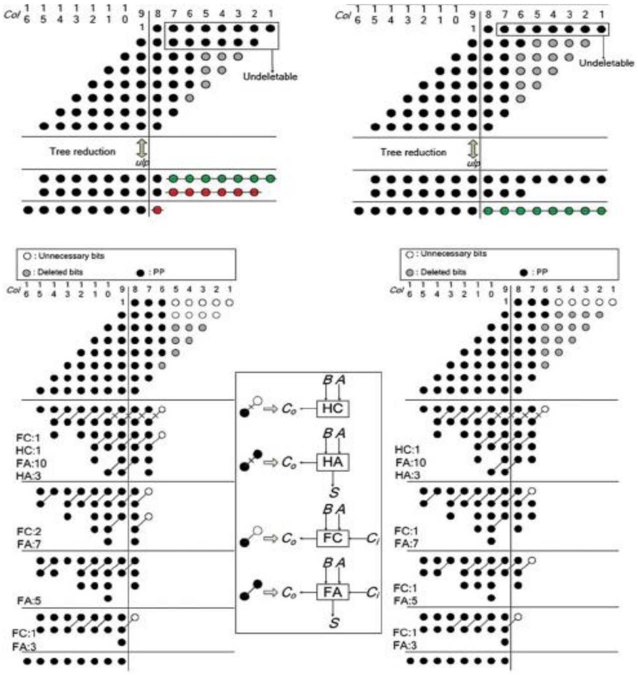
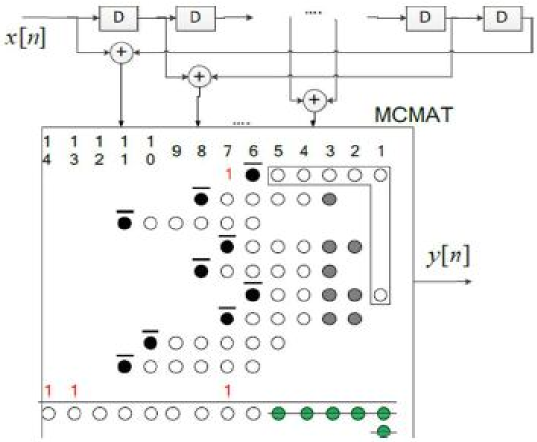


Fig 4:Steps of design in Truncated multipliers

In this brief, we propose an improved version of the faithfully rounded truncated multiplier design as shown in Fig.4. Only a single row of PPB is through undeletable (for the subsequent rounding), and the PPB elimination consists of only deletion and rounding. The error range of deletion and rounding in the improved version. Since the range of the deletion error in the improved version is twice larger than that in more PPBs can be deleted leading to smaller area in the successive PPB compression.

While most FIR filter designs use minimum filter order, we observe that it is possible to minimize the total area by slightly increasing the filter order. Therefore, the total area of the FIR filter is estimated using the subroutine area_cost_estimate using the approach in . Indeed, the total number of PPBs in the MCMA is directly proportional to the number of FA cells required in the PPB compression because a FA reduces one PPB. After the uniform quantization and filter order optimization the non uniform quantization in gradually reduces the bit width of each coefficient until the frequency response is no longer satisfied. Finally, we fine-tune the non uniformly quantized coefficients by adding or subtracting the weighting of LSB of each coefficient and check if further bit width reduction is possible. Using the algorithm , we can find the filter order M and the non uniformly quantized coefficients that lead to minimized area cost in the FIR filter implementation.



.Fig 5:FIR filter architecture using MCMAT

Fig. 5 shows the illustrative architecture of MCMA with Truncation (MCMAT[Multiple constant multiplication/ Accumulation with faithfully rounded truncated multipliers]). that removes unnecessary PPB. The white circles in the L-shape block represent the undeletable PPB. The deletion of the PPB is represented by gray circles. After PP compressions the rounding of the resultant bits is denoted by cross circles. The last row of the PPB matrix represents all the offset and bias constants required including the sign bit modifications.

V. PRESENT WORK

A. *Pipelined Fir Filter Using MCMAT*

Pipelining leads to reduce the critical path. Either increases the clock speed (or sampling speed) or reduces the power consumption at same speed in a DSP system. Pipelining is reduce the effective critical path by introducing pipelining latches along the critical data path. The pipelined implementation by introducing 2 additional latches in the critical path is reduced from TM+2TA to TM+TA. The schedule of events for this pipelined system. You can see that, at any time, 2 consecutive outputs are computed in an interleaved manner.

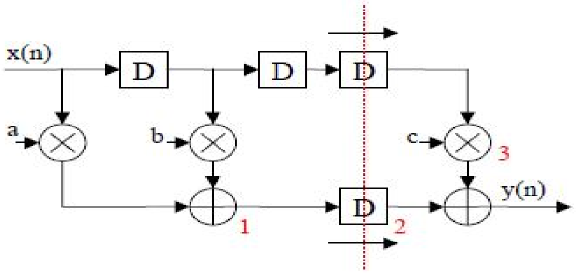


Fig 5:Block Diagram of pipelined FIR filter

In an M-level pipelined system, the number of delay elements in any path from input to output is (M-1) greater than that in the same path in the original sequential circuit. Pipelining reduces the critical path but leads to a penalty in terms of an increased latency. Latency is the difference in the availability of the first output data in the pipelined system and the sequential system. Drawbacks of pipelined filter is increase in the number of latches and in system latency. The speed of a DSP architecture (or the clock period) is limited by the longest path between any 2 latches or between an input and a output, or between a input and an latch, or between the latch and the output. This longest path or the “critical path” can be reduced by suitably placing the pipelining latches in the DSP architecture. The pipelining latches can only be placed across any feed-forward cutest of the graph.

Two important definitions:
Cutset: A cutset is a set of edges of a graph such that if these edges are removed from the graph becomes disjoint.
Feed-forward cutset: A feed-forward cutset is the data move in the forward direction on all the edge of the cutset.

According to the below flow diagram a software routine is developed and accordingly the simulation is carried out using Quaratus II software. The target device selected is Stratix III. The functional and timing analyses were carried out. The maximum frequency obtain is 247.65MHz.

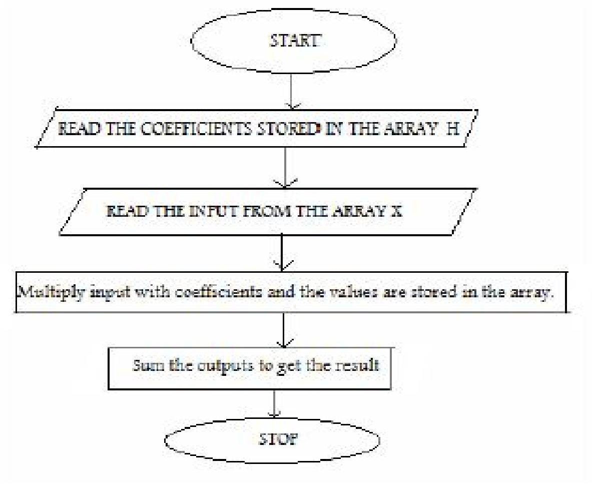

START
READ THE COEFFICIENTS STORED IN THE ARRAY H
READ THE INPUT FROM THE ARRAY X
Multiply input with coefficients and the values are stored in the array.
Sum the outputs to get the result
STOP

Fig-6 Flow graph diagram of pipelined FIR filter

Compare FIR filter and pipelined FIR filter the power has to be reduced. The delay elements are added in combinational block the speed is increase, the overall FIR filter speed is reduced using the delay elements the power has to be reduced. Single level pipelined used in multiplier structure. The functional outputs are not changed the power only reduced.

Our proposed FIR filter design has four versions. MCMA is the baseline implementation using combined PP compression with uniformly quantized coefficients. MCMA_opt is an improved version by adopting the non uniform quantization in for coefficient optimization .MCMAT_I and MCMAT_II faithfully truncate PPBs using the approaches in Fig.4 respectively. The total numbers of PPBs before compression in MCMA, MCMA_opt, MCMAT_I, and MCMAT_II are 3407, 3175, 2124, and 1946,respectively. We observe that MCMA_opt, MCMAT_I, and MCMAT_II have area reduction rates of 3%, 24%, and 27%, respectively, compared with the baseline MCMA designs that are already smaller than prior designs of similar TP.

Although the area costs of the proposed designs are significantly reduced, the critical path delay is increased because all the operations in the MCMA are executed within one clock cycle. It is possible to reduce the delay by adding pipeline registers in the PP compression as suggested in the major goal is to minimize the number of FAs, HAs, and registers (including algorithmic registers and pipelined registers) using integer linear programming. In this brief, we focus on low-cost FIR filter designs with moderate speed performance for mobile applications where area and power are important design considerations.

VI. SIMULATION RESULTS

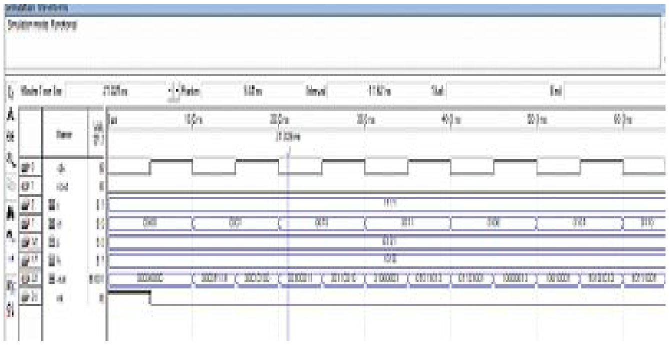


Fig-7 Simulation results obtained from Quaratus II 9.1

A. Results Evaluvation

Table-1Comparision of FIR filter and pipelined FIR filter using MCMAT-II

S. N O	COMPARI SION	28-TAP FILTER		64-TAP FILTER	
		FIR filter	Pipelined FIR filter	FIR filter	Pipelined FIR filter
1	Thermal power dissipation	1,804 mw	736.31 mw	1,868 mw	855.32 mw
2	Dynamic power dissipation	604 mw	263.88 mw	1,293 mw	307.70 mw
3	Static power dissipation	27.90 mw	27.07 mw	86.51 mw	82.52 mw
4	I/O power dissipation	452 mw	445.36 mw	488 mw	465.10 mw

VII. CONCLUSION

This paper has presented low-cost FIR filter designs by jointly considering the optimization of coefficient bit width and hardware resources in implementations. By using a new truncated multiplier design by jointly considering the reduction, deletion, truncation, and rounding of the PP bits. The faithfully truncated multiplier has a total error of no more than 1 ulp and can be used in applications that require accurate results. Moreover, the proposed method can be easily extended to designs are based on the direct form; we observe that the direct pipelined FIR structure with faithfully rounded MCMAT leads to the smallest area cost and power consumption.

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I am very thankful for the support she extended to me and the freedom to express my views. Words are inadequate to express the gratitude to my beloved parents and friends for their excellent and never ending co-operation.

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AUTHORS PROFILE

DEEPIKA.A received the **B.E.** degree in Electronics and Communication Engineering from Vivekanandha College of Engineering and Technology for Women, Anna University, Chennai, India, in 2012, the **M.E** degree in Applied Electronics from the Jayaram College of Engineering & Technology, Trichy, Anna University, Chennai, India, in 2014

A.Bhuvaneswari received the **B.E.** degree in Electronics and Communication Engineering from Annai Mathammal Sheela Engineering College, Namakkal, Madras University, in 2001, the **M.E** degree in Communication Systems from Jayaram College of Engineering and Technology, Anna University, Trichy in 2011. Currently working as assistant professor in Jayaram College of Engineering and Technology, Trichy, India.