Dual Modulation Technique for High Efficiency in High-Switching Buck Converters Over a Wide Load Range

Jen-Chieh Tsai, Tsung-Ying Huang, Wang-Wei Lai, and Ke-Horng Chen, *Senior Member, IEEE*

***Abstract*—A dual modulation technique to improve power conversion efficiency with minimal increase in output voltage ripple is presented. The worsening switching noise caused by parasitic resistance and inductance due to high-switching operation can also be alleviated by the proposed ac ripple detector. Furthermore, the dual modulation method can speed up the load transient response since the switching frequency can increase to 5 MHz during the transient period. At very light loads, the switching frequency is always kept higher than the acoustic frequency to avoid noisy sound. Experiment results show that the converter operates at 5 MHz using a small inductor of 1 μH. The load transient response time is shorter than 3 μs when load current changes from 150 to 450 mA or *vice versa*. Power efficiency is kept higher than 85% over a wide load current range. Specifically, light efficiency can be raised to about 45% above that of the conventional design.**

***Index Terms*— DC-DC buck converter, dual modulation technique, hopping frequency modulator (HFM), loading potential detector (LPD) .**

I. Introduction

RECENTLY, switching power converters use a high-switching controller to reduce the size of the output filter for compact solution in portable devices, such as cellular phones, wireless devices, and Bluetooth applications. However, the design of a high-switching controller needs to consider carefully the power conversion efficiency and high-switching noise caused by parasitic components. In general, the efficiency of a converter is defined as the ratio of output power, $P_{\rm out}$, to input power, $P_{\rm in}$, as expressed in (1)

$$\eta = \frac{P_{\rm out}}{P_{\rm in}} = \frac{P_{\rm out}}{P_{\rm out} + P_{\rm loss}} \quad \text{where } P_{\rm in} = P_{\rm out} + P_{\rm loss}. \quad (1)$$

$P_{\rm loss}$ is the sum of power loss in switching converters and expressed as (2). $P_{\rm con}$ and $P_{\rm sw}$ are the conduction and switching losses, respectively. $P_{\rm sys}$ is the power loss in the controller composed of analog and digital circuits [1]

$$P_{\rm loss} = P_{\rm con} + P_{\rm sw} + P_{\rm sys}. \quad (2)$$

Manuscript received September 21, 2010; revised January 25, 2011; accepted March 21, 2011. Date of publication May 16, 2011; date of current version June 29, 2011. This paper was recommended by Associate Editor C. Piguet.

The authors are with the Institute of Electrical Control Engineering, National Chiao Tung University, Hsinchu, Taiwan (e-mail: khchen@cn.nctu.edu.tw).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TCSI.2011.2142970

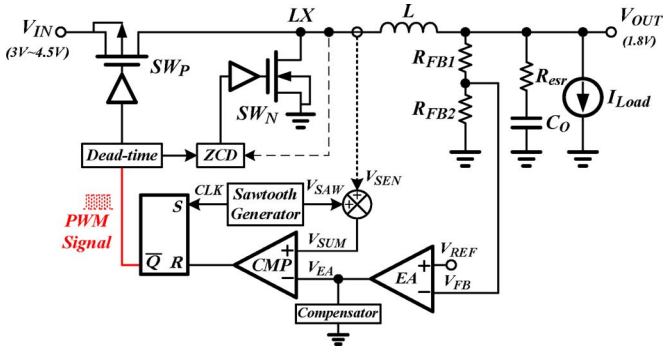


Fig. 1. The conventional current mode buck converter.

The conventional pulse width modulation (PWM) of the current mode control (Fig. 1) becomes limited as switching frequency increases. The control system can have high efficiency at heavy loads as the $P_{\rm con}$ is kept low by using low on-resistance of power switches. Incidentally, efficiency decreases drastically when the load gradually decreases to no load condition since the increasing value of $P_{\rm sw}$ dominates it. Specifically, the high-switching operation resulting from the use of a small inductor could deteriorate efficiency. Thus, it is important to keep high efficiency over a wide load range.

The power converter system generally undergoes multiple operation modes in order to extend the battery life of present-day portable devices. Essentially, these include standby mode regulated by the pulse frequency modulation (PFM), burst mode to save on power, and normal PWM operation mode to sustain system operation [2]–[5]. However, the circuit complexity, output ripple, and noise issue are not effectively treated at the same time [6]–[9]. For high-switching operation, it is important to carefully consider the specifications at the same time since the performance of the power converter will be deteriorated and the load current range will be limited [10], [11]. Furthermore, in the current-mode control, high-switching frequency decreases system accuracy due to limited response time of the inductor current sensor [12]–[14]. In addition, the switching noise drastically increases to deteriorate the accuracy of current sensor to decrease the system stability.

Thus, it is important to improve the estimation accuracy of the inductor current for high-switching operation. In prior arts, the equivalent series resistance (ESR) on the output capacitor can be used to generate the current ripple to achieve fast load transient response through the two voltage feedback loops. However, it suffers from large output voltage ripple and low efficiency [15]–[20]. Besides, using large ESR for system stability

TABLE I
A COMPARISON OF THE CONVERTER WITH DIFFERENT CONTROL METHODS

	PFM mode [2]	*Burst mode* [24]	*Dual modulation mode* [25]
Efficiency	Good	Good	Good
Circuit Complexity	Large	Medium	Small
Output Ripple	Large	Medium	Small
Audio Noise	Small	Larger	Small
Load Range	Medium	Small	Wide

limits the selection of output capacitor. Specifically, the large ripple reduces the performance of the sequent stage that needs small transient voltage dip [21]–[23]. Therefore, the proposed dual modulation technique with the ac ripple detector needs to improve power conversion and remove high-switching noise to increase system stability simultaneously.

The dual modulation technique can separate the inductor current into the ac ripple signal and the loading potential signal. It can accurately acquire the inductor current information to decide the duty cycle without the need of large ESR. The loading potential signal not only can determine the optimum switching numbers for each power switch at different loads, it also can generate a hopping switching frequency at light loads for high-conversion efficiency. Furthermore, the hopping switching frequency should be higher than the acoustic frequency to avoid noisy sound. Compared with conventional PWM switching converters, the dual modulation technique can achieve faster transient response and higher power conversion efficiency simultaneously with an acceptable output ripple. In addition, multilayer ceramic capacitors (MLCC) can be selected as the output capacitor for low cost. The low-cost MLCC becomes more popular due to its low ESR. Thus, the proposed ac ripple detector can sense the low inductor current ripple. It is superior to those designs without using MLCC.

Table I compares the converter with different control methods. The dual modulation mode not only has good efficiency but also reduces the output ripple and chip area compared with other methods. Specially, the audio noise, which is important issue for communication applications, can be effectively reduced.

The organization of this paper is shown as follows. Section II introduces the design concept of the proposed dual modulation technique and the ac ripple detector. The circuit implementation is shown in Section III. The close-loop analysis is described in Section IV to demonstrate the system stability. Experimental results shown in Section V can prove the correction and advantages of the dual modulation technique. Finally, conclusions are given in Section VI.

II. DESIGN CONCEPT DESCRIPTION

For high-switching operation, power conversion efficiency decreases drastically when load current changes from heavy to light. The dual modulation technique needs to hop switching frequency to find a trade-off between power conversion efficiency and output voltage ripple when load current decreases [25].

The timing diagram of the dual modulation technique is illustrated in Fig. 2. The original PWM control uses a high-switching

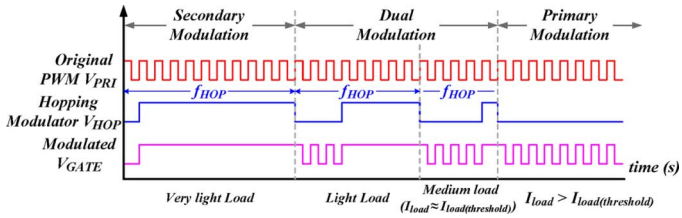


Fig. 2. Waveforms of the buck converter with the dual modulation technique.

signal V_{PRI} to regulate the output voltage to achieve a reduced ripple. Since the conduction loss dominates the whole power consumption at heavy loads, the high-switching signal would not result in a great decrease in efficiency. However, the switching loss drastically deteriorates efficiency from medium- to light-load condition due to the high-switching operation. Therefore, the secondary modulator becomes necessary to reduce the switching numbers as shown by the modulated signal V_{GATE} used to control the power switches. At this time, dual modulation operates to raise efficiency within an allowable output ripple.

The architecture of the proposed dual modulation technique is shown in Fig. 3. The controller is separated into two parts. The primary modulator makes the system operate normally under high-switching frequency, and the secondary modulator can raise power conversion efficiency at light loads. Thus, high power conversion efficiency and a fast transient response under high-switching operations can be achieved. The dual modulation technique should detect the load condition using the proposed loading potential detector (LPD) circuit. In addition, the combination of the LPD circuit and the error signal received by the error amplifier can be viewed as the control signal in the hopping frequency modulator (HFM) circuit. As a result, the hopping signal generated by the secondary modulator can regulate the original PWM signal to find the trade-off between efficiency and output voltage ripple.

The flow diagram of the dual modulation technique is shown in Fig. 4. Basically, the operation of primary modulator is similar to that of the buck converter. When the load current is smaller than the threshold current $I_{\mathrm{load(threshold)}}$, the dual modulation is started. That is, the PWM signal generated by the primary modulator will be modulated by the secondary modulator to reduce the switching power loss. As the I_{LOAD} current is smaller than 10 mA, the system will automatically switch to secondary modulation. The secondary modulator contributes to the decrease in the switching frequency and the increase in the hopping period. Light-load conditions require reduced switching frequency in order to save power. The HFM circuit can determine a suitable switching frequency to reduce substantially the switching power loss at the power switches. Meanwhile, dual modulation starts to decrease the switching frequency from the constant $f_{\mathrm{SW(constant)}}$ to $f_{\mathrm{SW(dynamic)}}$ through the hopping frequency, f_{HOP}, in the secondary modulator. As depicted in Fig. 5, the value of f_{HOP} varies with load current.

In addition, the hopping frequency not only reduces switching loss but also always keeps the output ripple within the allowable range.

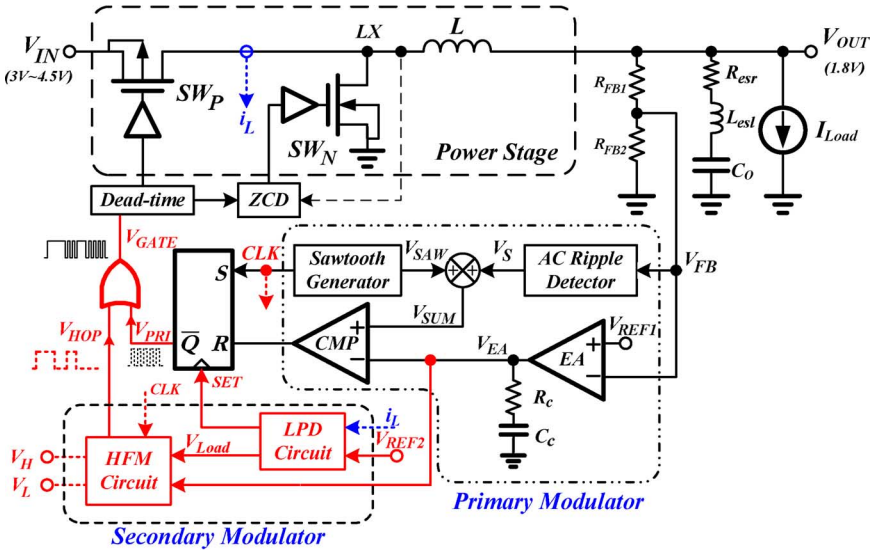


Fig. 3. The proposed buck converter with the dual modulation technique.

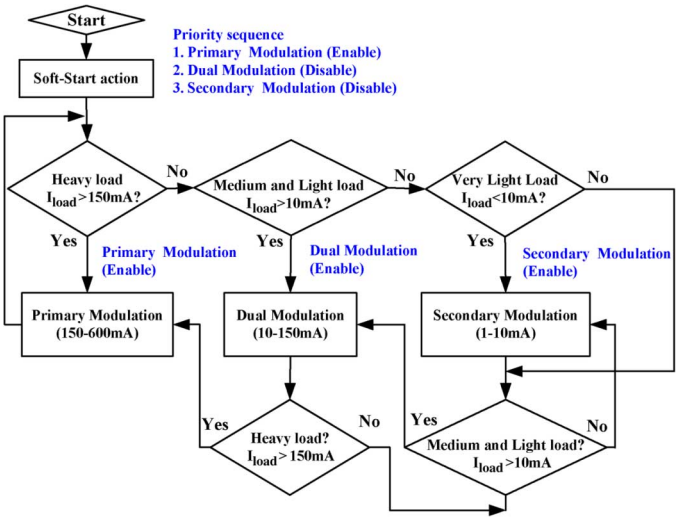


Fig. 4. The flow chart of the dual modulation system.

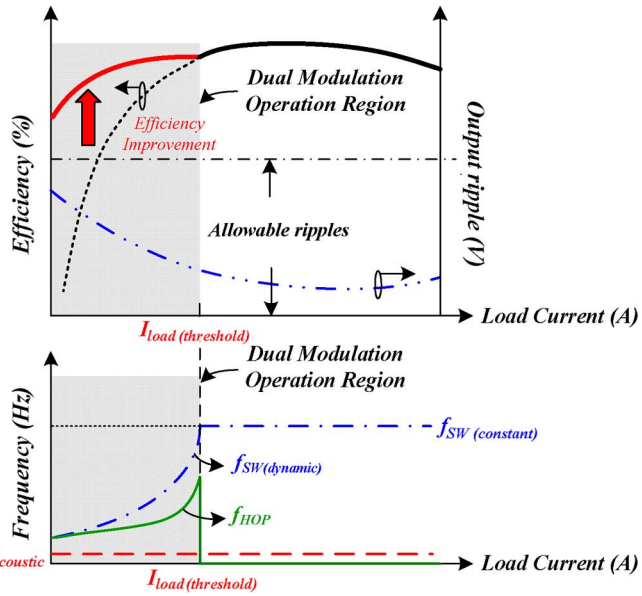


Fig. 5. Efficiency and hopping frequency versus load current in the proposed converter system.

The decrease in the switching frequency is accompanied with an increase in the hopping period as load current declines continuously. The decrease in switching frequency results in increased efficiency from a medium- to light-load condition. Much power is retrenched due to the switching loss reduction at the power MOSFETs. To further raise efficiency at very light loads, the primary modulator is shut down automatically and only the secondary modulator is employed to regulate the output voltage and to save much power in the quiescent operation loss. Furthermore, to avoid operation in the acoustic region, the hopping frequency is always kept higher than the acoustic frequency, f_{acoustic}, even at no load condition.

For high-switching converters, the conventional current sensing method may fail to provide accurate sensing load current due to limited bandwidth. Thus, it is better to find a suitable current sensing method for the high-switching converter. Fig. 6 shows the concept of the proposed ac ripple control. In time domain, the output LC stage of the converter can be considered as a low-pass filter and work as an integrator.

However, the existence of ESR and ESL may deteriorate the accuracy of current sensing signal and the steady state duty cycle. Considering the ESR, R_{esr}, and the equivalent series inductor (ESL), L_{esl}, on the output capacitor, C_O, the output voltage ripple can be evaluated as the summation expressed in (3)

$$\begin{aligned} v_{\text{out}} &= v_{out|esr} + v_{out|esl} + v_{out|Co} \\ &= R_{\text{esr}} i_L + L_{\text{esl}} \frac{di_L}{dt} + \frac{1}{C_O} \int i_L dt. \end{aligned} \tag{3}$$

Briefly, (3) is composed of overshoot voltage, $v_{\text{out|esr}}$, across the ESR; induced voltage, $v_{\text{out|esl}}$, which is the differentiation of the inductor current with ESL; and voltage ripple, $v_{\text{out|Co}}$, which is the integration of the inductor current on the C_O [26],

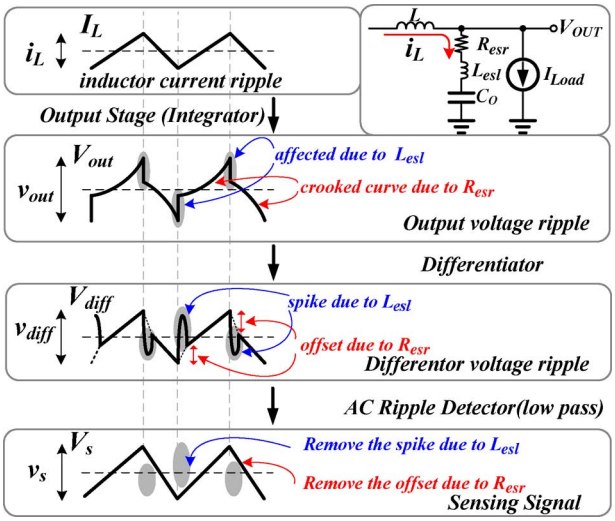


Fig. 6. The concept of current sensing flow as it utilizes the ac ripple detector.

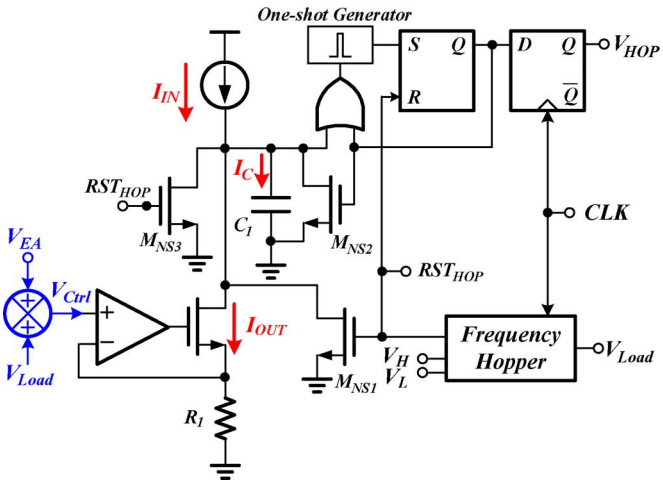


Fig. 7. Schematic of the HFM circuit.

[27]. Thus, it is convenient to differentiate $v_{\rm out}(t)$ in order to obtain the ac signal of the inductor current. This can be expressed as

$$v_s = \frac{dv_{\rm out}}{dt} = R_{\rm esr}\frac{di_L}{dt} + L_{\rm esl}\frac{d^2 i_L}{dt^2} + \frac{i_L}{C_O}. \qquad (4)$$

At the right side of (4), the first and second terms represent the effect of the ESR and ESL, respectively. Owing to high-switching operation, the ESR and ESL seriously affect system stability and result in a large output ripple. The inductor current information can be accurately derived through the operation of the proposed ac ripple detector. The ac ripple detector behaves as a differentiator and inserts one low-frequency zero to increase system stability. One low-pass filter is utilized to filter out the high-frequency components contributed by the ESR and ESL. Consequently, the accurate inductor current can be derived as the PWM ramp since the effect of the ESR and ESL can be efficiently removed. In other words, the cheap MLCC can be selected as the output for low cost.

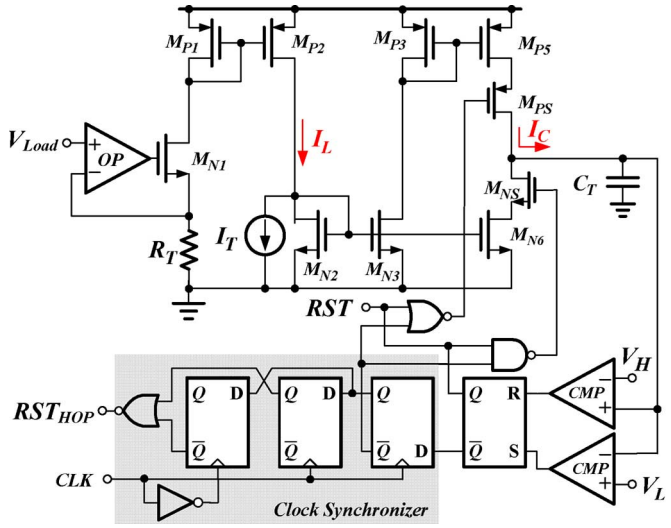


Fig. 8. Schematic of the frequency hopper.

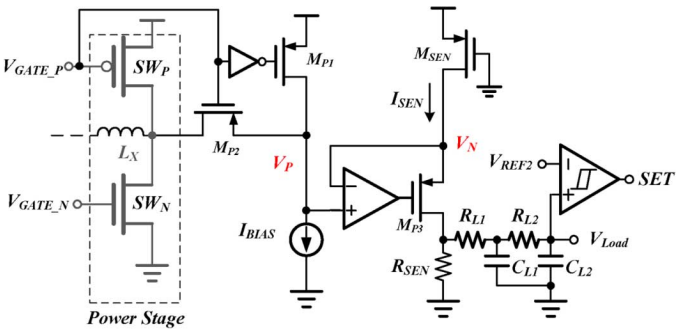


Fig. 9. Schematic of LPD circuit.

III. Circuit Implementation

A. Hopping Frequency Modulator Circuit

The HFM circuit, as shown in Fig. 7, can generate a load-dependent pulse, $V_{\rm HOP}$, to modulate the primary PWM signal in order to reduce further the switching loss [28]. Besides, the hopping frequency technique is used to power-level tracking power amplifier with reduced spurious emission by utilizing a dc-dc converter. The frequency-hopping technique is implemented by varying the switching frequency of the dc-dc converter, which supplies the power of an RF PA. Ideally, if two switching frequencies are used and each frequency is used half of the time, the magnitude of the resulting spurs can be reduced by 6 dB [29]. In our design, the signal $V_{\rm Ctrl}$, is controlled by two variables, which are the error signal, $V_{\rm EA}$, from the error amplifier and the dc load current signal, $V_{\rm Load}$, from the LPD circuit. It can decide an adequate duty cycle in the HFM circuit once the dual modulation technique is triggered. The output voltage may have a large drop voltage caused by the small value of $V_{\rm Load}$, which induces a large number of switches skipped. The drop voltage at the output raises the value of $V_{\rm EA}$ to constitute a negative feedback loop for increased system stability.

The charging current for the capacitor, C_1, is determined by the current signal I_C decided by the values of $I_{\rm IN}$ and $I_{\rm OUT}$ and expressed as (5)

$$I_C = I_{\rm IN} - I_{\rm OUT} = I_{\rm IN} - \frac{V_{\rm Ctrl}}{R_1} = \frac{C_1 \cdot \Delta V}{\Delta T}. \qquad (5)$$

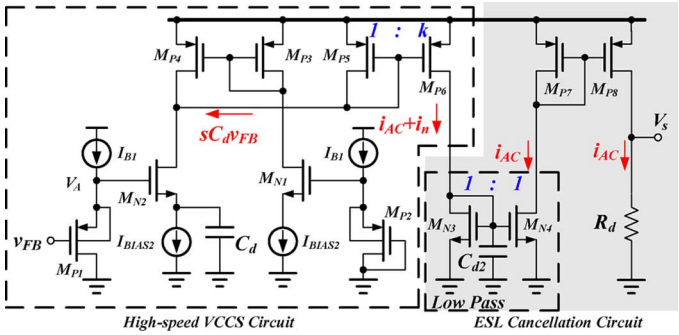


Fig. 10. Schematic of the ac ripple detector.

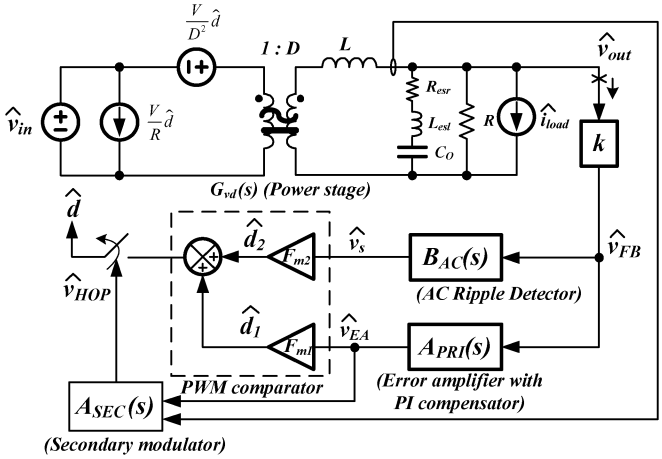


Fig. 11. Small-signal model of the ac ripple control buck converter.

$I_{\rm IN}$ defines the threshold current that switches the operation from the primary PWM to dual modulation. As load current decreases continuously, the system switches automatically to dual modulation; that is, load current is smaller than $I_{\rm load(threshold)}$. The current $I_{\rm OUT}$ is converted from the signal $V_{\rm Ctrl}$ by the voltage-to-current (V-to-I) converter. The minimum value of $V_{\rm Ctrl}$ corresponds to the largest charging current for the C_1 that result in the shortest charging time. As a result, the duty of the HFM pulse can contain the longest duration at very light loads to reduce the switching frequency at the power switches.

The charge on the capacitor C_1 is reset by a hopping frequency signal, $\rm RST_{HOP}$, generated by the frequency hopper in order to vary the hopping frequency, $f_{\rm HOP}$, based on load current. Consequently, the $f_{\rm HOP}$ decreases and the duty cycle increases to reduce the switching numbers at the power MOSFETs when load current becomes light. Thus, efficiency can be improved. On the other hand, the HFM pulse is greatly decreased, and small enough to have no effect on the high-switching PWM pulse during the primary PWM operation. Only the primary PWM operates to suppress output ripple.

B. Frequency Hopper

The frequency hopper is used to generate a load-dependent hopping switching frequency for the HFM circuit. The load-dependent hopping switching frequency varies over a wide load range if the secondary starts to work from medium to very light-load condition.

TABLE II
DESIGN PARAMETERS OF THE PROPOSED CONVERTER

EA's G_m	*62.5 μA/V*		
Resistor	*R_o=90 MΩ*	*R_c=150 kΩ (internal)*	*R_d=5MΩ (internal equivalent)*
Capacitor	*C_c=30 pF (internal)*	*C_d=2 pF (internal)*	
Three Poles	*f_{P1_p}=59 Hz*	*f_{O1}=f_{O2}=73 kHz*	
Two Zeros	*f_{zcom1}=57.7 kHz*	*f_{zcom2}=91.5 kHz*	

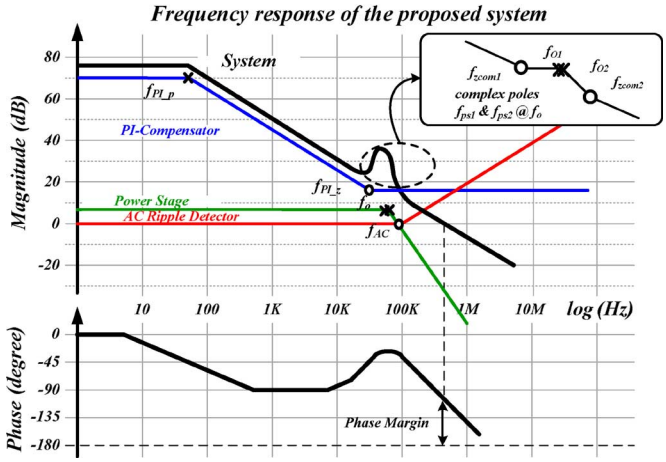


Fig. 12. Bode plot of the proposed converter system.

As shown in Fig. 8, the $V_{\rm Load}$ is generated by the LPD circuit to determine the dc load current condition. The current signal I_L converted from the $V_{\rm Load}$ by the V-to-I converter is nearly equal to the charging current I_C, which is expressed as (6) and can determine the hopping frequency as shown in (7) due to the small current I_T. The frequency hopper can let the user design the desired frequency by adjusting of R_T and I_T

$$I_C = I_L - I_T = \frac{V_{\rm Load}}{R_T} - I_T \tag{6}$$

$$f_{\rm HOP} = \frac{\frac{V_{\rm Load}}{R_T} - I_T}{C_T \cdot (V_H - V_L)} \approx \frac{I_C}{C_T \cdot (V_H - V_L)}. \tag{7}$$

Since the system has a primary high-switching frequency, $f_{\rm SW}$, the clock synchronizer is used to synchronize the output signal $\rm RST_{HOP}$ with high-switching clock, CLK. It also can fix the pulse width of the signal $\rm RST_{HOP}$ for regular operation in the dual modulation technique compared with using the signal RST.

When load current changes from 1 mA to 150 mA, the $f_{\rm HOP}$ varies from 70 kHz to 1 MHz. Meanwhile, the $f_{\rm SW(dynamic)}$ can range from 70 kHz to 3 MHz. As a result, a lot of switching loss can be reduced to improve power conversion efficiency. In this design, the switching frequency reverts to high-switching operation of 5 MHz when load current is larger than $I_{\rm load(threshold)}$, which is designed as 150 mA. The selection of 5 MHz is to suppress the output ripple smaller than 50 mV at medium to heavy loads.

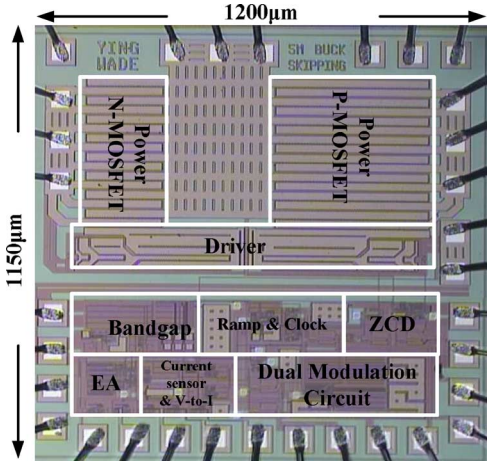


Fig. 13. Chip micrograph.

C. Loading Potential Detector Circuit

The LPD circuit (Fig. 9) is used to generate the loading potential signal, $V_{\rm Load}$, which is proportional to the dc load current [30], [31].

The sensing transistor, $M_{\rm SEN}$, with the aspect ratio much smaller than the power PMOSFET, SW$_P$, at the power stage, the virtual short-circuit characteristic of the operational amplifier can mirror the inductor current in the power P-type MOSFET to the sensing transistor. The sensing current can be scaled down to the transistor M_{P3} during the rising period. The sensing current $I_{\rm SEN}$ flows through the internal resistor $R_{\rm SEN}$ and is filtered by the low-pass filter to suppress the switching ripple in generating the loading potential signal $V_{\rm Load}$.

The design of the compensator contains two low pass filters composed of $R_{\rm L1}$, $R_{\rm L2}$, $C_{\rm L1}$, and $C_{\rm L2}$ to get a smooth control signal to generate a dual modulation signal to find out the trade-off between the output ripples and the efficiency. Besides, the low pass filters will stable the secondary modulation and it will be analyzed in Section IV.

The hysteretic comparator compares the output signal $V_{\rm Load}$ with the predefined threshold voltage $V_{\rm REF2}$. When $V_{\rm Load}$ is smaller than $V_{\rm REF2}$ (i.e., the system is at very light loads), the hysteretic comparator triggers the signal, SET, from high to low. Specifically, to promote additional power saving, the primary modulator shuts down and the output voltage of the system is regulated only by the secondary modulator at very light loads.

Since the LPD circuit extracts the dc value of the load current, the bandwidth of the operational amplifier should not be too large to save power; that is, the selection of the operational amplifier can only be a simple one-stage structure with low quiescent current in order to save chip area and power consumption. Furthermore, the biasing current induces a minimum output sensing current even at no load condition, indicating a minimum value at the signal $V_{\rm Load}$. As a result, the hopping frequency can be always kept higher than the acoustic frequency to address the noise issue.

D. AC Ripple Detector

The schematic of the ac ripple detector is shown in Fig. 10. Apart from its ability to determine the ac value of the inductor current, the ac ripple detector can also eliminate high-frequency noise due to ESL [26], [27].

In time-domain, the high-speed voltage-controlled current-source (VCCS) circuit is used to differentiate the output feedback signal, $V_{\rm FB}$, to generate a low-frequency zero without the need of large compensation capacitor for reducing silicon area. Owing to the simple circuit structure, the bandwidth can be extended beyond that of conventional current sensing circuit using an operational amplifier. Thus, the $v_{\rm FB}$ is converted to a small-signal current $sC_dv_{\rm FB}$ to charge and discharge the capacitor. Before generating the sensing signal V_s, the small-signal current is delivered to the ESL cancellation circuit to eliminate the ESL effect using a low-pass filter.

The signal of $sC_dv_{\rm FB}$ contains the ac inductor current, $i_{\rm ac}$, and the high-switching noise generated by the ESL, i_n. After the operation of ESL cancellation circuit, the pure ac inductor current can be derived to modulate the primary modulator. Thus, the value of $i_{\rm ac}$ approximately equals to (8). $v_{\rm FB(low-pass)}$ represents the value of $v_{\rm FB}$ after the low-pass filter

$$i_{\rm ac}(s) \approx skC_dv_{\rm FB(low-pass)}. \tag{8}$$

The sensing ac signal, V_s, can be received as shown in (9) by the sensing resistor R_d

$$V_s(s) = skC_dR_dv_{\rm FB(low-pass)}. \tag{9}$$

Thus, the sensing signal can be produced correctly and rapidly under high-switching operation.

TABLE III
DESIGN SPECIFICATIONS

Technology	TSMC 0.25μm CMOS
Proposed die area (with test pads)	1150 μm × 1200 μm
Supply variation (V_{IN})	3–4.5 V
Output voltage (V_{OUT})	1.8 V
Switching frequency (f_{SW})	5 MHz
Maximum output voltage ripple	50 mV
Undershoot/Overshoot (150mA to 450mA)/(450mA to 150mA)	20 mV/15 mV
Undershoot/Overshoot (1mA to 500mA)/(500mA to 1mA)	60 mV/60 mV
Recovery time 150mA to 450mA/450mA to 150mA	2.5 μs/3 μs
Recovery time 1mA to 500mA/500mA to 1mA	14 μs/15 μs
Inductor (L)	1 μH
Output capacitor (C_O)	4.7 μF
Secondary modulation range	1–10 mA
Dual modulation range	10–150 mA
Primary modulation range	150–600 mA

IV. SMALL-SIGNAL ANALYSIS OF THE PROPOSED SYSTEM

Fig. 11 shows the small-signal model of the dual modulation buck converter with the ac ripple detector [26]. The loop gain can be divided into two parts. The first part, which is the power stage, contributes duty-to-output transfer function and contains

TABLE IV
THE COMPARISONS ARE BETWEEN THE PROPOSED METHOD AND THE PRIOR ARTS

		This work	[2]	[3]	[5]	[10]	[13]
Inductor		1 μH	10 μH	4.7 μH	10 μH	4.7 μH	4.7 μH
Capacitor		4.7 μF	47 μF	4.7 μF	10 μF	10 μF	10 μF
Input voltage		3.0-4.5 V	2.8-5.5 V	3.3 V	2.7-5 V	3.6 V	3.0-5.2 V
Output voltage		1.8 V	1.0-1.8 V	1.65 V	1 V	1.8 V	< input voltage – 0.2V
Switching frequency (PWM max frequency)		5 MHz	1.5 MHz	1 MHz	600 KHz	1 MHz	1 MHz
Circuit Complexity		Medium	Large	Large	Medium	Medium	Medium
Control mechanism		Dual Modulation	PWM/PFM	PWM/PFM/DSM	PWM/PFM	PWM/PFM	PWM
Load transient response	Load transient	1 mA – 600 mA	20 mA – 400 mA	0.1 mA – 500 mA	3 mA – 460 mA	50 mA – 450 mA	50 mA – 450 mA
	Max output voltage ripple	50 mV	25 mV	35 mV	36 mV	20 mV	20 mV
	Recovery time	20 μs	100 μs	N/A	28 μs	N/A	N/A

dual poles due to the output LC filter as expressed in (10) with a dc gain of G_{vd0}

$$G_{vd}(s) = \frac{\hat{v}_{\text{out}}}{\hat{d}} = G_{vd0} \cdot \frac{1 + \frac{s}{\omega_{\text{esr}}}}{1 + \frac{2\zeta}{\omega_O} s + \left(\frac{s}{\omega_O}\right)^2}$$
$$\text{where} \quad \omega_{\text{esr}} = \frac{1}{R_{\text{esr}} C_O},\ \omega_O = \frac{1}{\sqrt{LC_O}},$$
$$\text{and } \zeta = \frac{1}{2}\left(\frac{1}{R_L\sqrt{\frac{C_O}{L}}}\right). \tag{10}$$

The zero, ω_{esr}, generated by R_{esr} is pushed to high frequencies by using small ESR. R_L is the loading resistor and R_s is the series resistor of the LC resonant loop, which is the sum of MOSFET on resistance, inductor resistance, and R_{esr}.

The second part, composed of the controller, contributes the output-to-duty transfer function. In dual modulation, the control path contains two feedback loops, namely, the primary loop and the secondary feedback loops. The primary feedback loop is determined by the ac ripple detector and the error amplifier. Thus, the primary duty cycle can be decided through the signals, v_s and v_{EA}, by the PWM comparator. On the other hand, the secondary feedback loop is determined by the error amplifier and the secondary modulator.

The loop selection is determined by the LPD circuit. At very light loads, only the secondary modulator loop is selected as the feedback path. The feedback signal directly passes through the secondary modulator loop, $A_{\text{SEC}}(s)$, to generate the duty cycle. As load current increases continuously, the feedback signal passes through both primary and secondary loops. Thus, dual modulation combines the primary and the secondary modulators at medium to light loads. At heavy loads, the feedback path is decided by the primary modulator when load current is larger than $I_{\text{load(threshold)}}$. The feedback signal only passes through the primary loop since the secondary loop $A_{\text{SEC}}(s)$ is disabled and the switch is always connected to the primary path.

The transfer function, $A_{\text{PRI}}(\text{s})$, of the error amplifier with the PI compensator can be derived as (11)

$$A_{\text{PRI}}(s) = G_m R_o \frac{1 + \frac{s}{\omega_{\text{PI\_}z}}}{1 + \frac{s}{\omega_{\text{PI\_}p}}}. \tag{11}$$

The dc gain is constituted by the error amplifier's transconductance, G_m, and the output resistance, R_o. The PI compensator introduces one pole, $\omega_{\text{PI\_}p}$ composed of R_o and compensation capacitor C_c, and one zero, $\omega_{\text{PI\_}z}$ composed of the compensation network, R_c and C_c.

Similarly, the transfer function, $A_{\text{SEC}}(\text{s})$ as shown in (12) contributed by the secondary modulator, is used to provide a low-bandwidth response to filter out the high-switching PWM signal according to the load current. Thus, the dc gain of the $A_{\text{SEC}}(\text{s})$ is inversely proportional to the load current and controlled by $I_{\text{load(threshold)}}$

$$A_{\text{SEC}}(s) = A_{\text{SEC0}} \cdot \left(\frac{I_{\text{load(threshold)}} - I_{\text{load}}}{I_{\text{load(threshold)}}}\right) \cdot \frac{1}{\left(1 + \frac{s}{\omega_{\text{SEC\_}p1}}\right)\left(1 + \frac{s}{\omega_{\text{SEC\_}p2}}\right)} \tag{12}$$

where $\omega_{\text{SEC\_}p1} = 1/R_{L1}C_{L1}$, $\omega_{\text{SEC\_}p2} = 1/R_{L2}C_{L2}$, and A_{SEC0} is the low-frequency gain.

The close-loop transfer function in the secondary modulator can be expressed as (13)

$$T_{\text{SEC}}(s) = k \cdot G_{vd}(s) \cdot A_{\text{PRI}}(s) \cdot A_{\text{SEC}}(s). \tag{13}$$

Therefore, the close-loop transfer function in dual modulation can be expressed as (14)

$$T_{(dual)}(s) = \left(\frac{I_{\text{load}}}{I_{\text{load(threshold)}}}\right) T_{\text{PRI}}(s) + T_{\text{SEC}}(s). \tag{14}$$

As the load decreases continuously, the contribution of the primary modulation becomes smaller than that of the secondary modulation. At very light loads, the secondary modulator can take over the control authority.

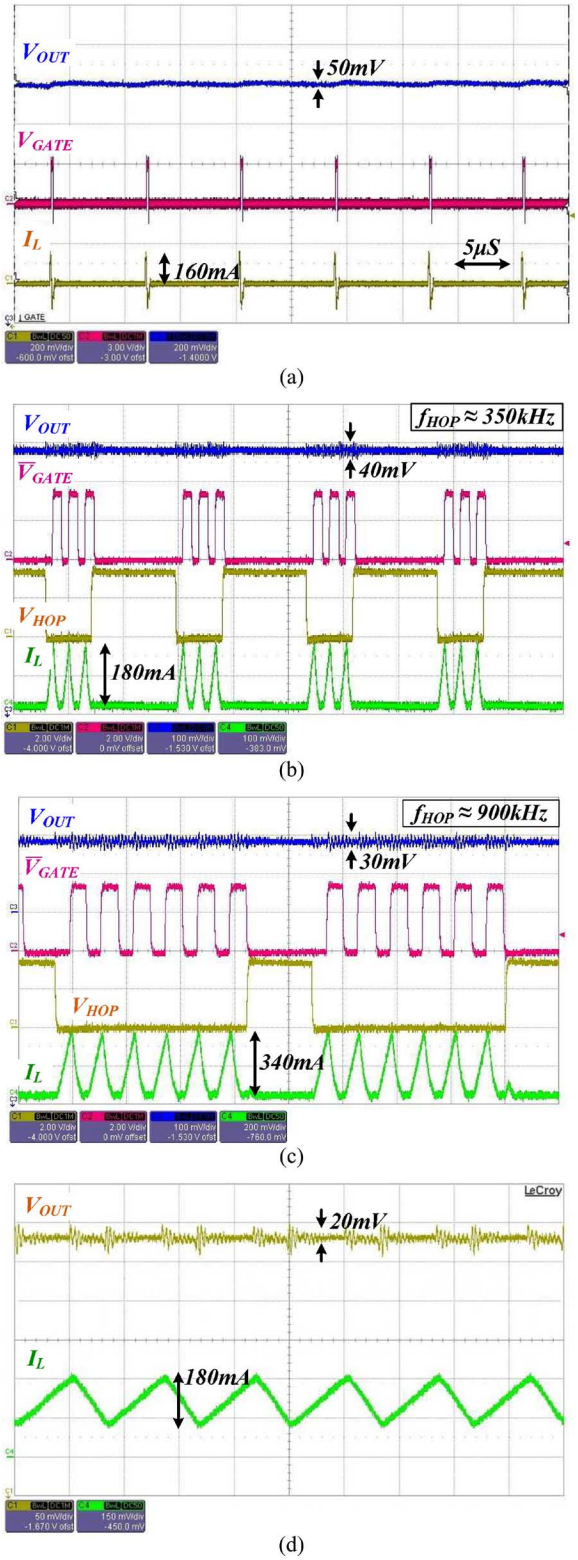


Fig. 14. Waveforms of the output voltage and inductor current at different load current conditions. (a) $I_{\mathrm{Load}} = 5$ mA. (b) $I_{\mathrm{Load}} = 20$ mA. (c) $I_{\mathrm{Load}} = 110$ mA (d) $I_{\mathrm{Load}} = 220$ mA.

In this study, the primary modulation is demonstrated as follows: The control duty can be expressed as (15) to include the results from the ac ripple detector and the error amplifier

$$\hat{d} = \hat{d}_1 + \hat{d}_2 = (F_{m1}A_{\mathrm{PI}} + F_{m2}B_{\mathrm{ac}}) \cdot k \cdot \hat{v}_{\mathrm{out}}$$

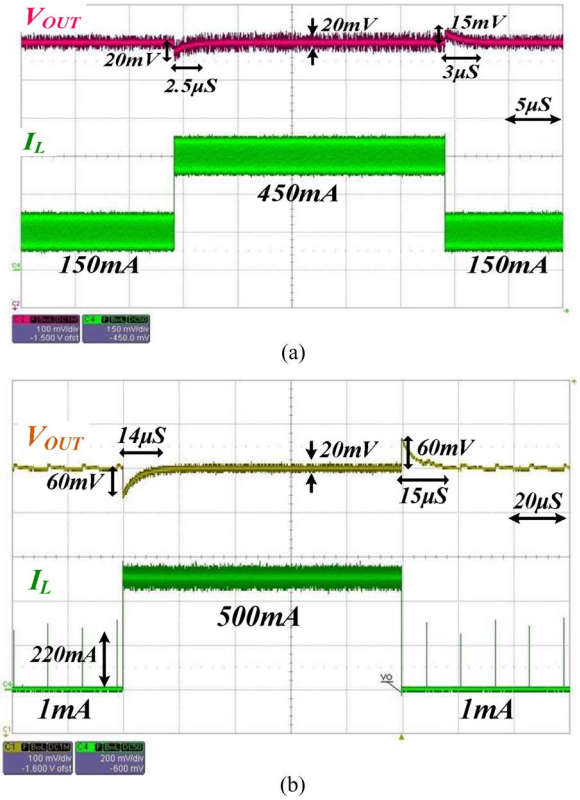


Fig. 15. Load transient response. (a) Load current steps from 150 mA to 450 mA or *vice versa*. (b) Load current steps from 1 mA to 500 mA or *vice versa*. The modulation rapidly switches between the secondary and the primary modulation techniques.

where k is the sensor gain. (15)

Owing to the LC double poles, the ac ripple detector as a differentiator can introduce a low-frequency zero, ω_{ac}, with a time constant, C_dR_d, to increase the system stability. Thus, the transfer function, $B_{\mathrm{ac}}(s)$, is shown in (16)

$$B_{\mathrm{ac}}(s) \approx \frac{s}{\omega_{\mathrm{ac}}} = sC_dR_d. \tag{16}$$

In a steady state, the PWM comparator transfer functions F_{m1} and F_{m2} have the same value of F_m as defined in (17)

$$F_m = F_{m1} = F_{m2}. \tag{17}$$

Thus, the output-to-duty transfer function can be derived as shown in (18). As expressed in (19), the system contains one single, low-frequency dominant pole, ω_{PI_p}, and two compensated zeros, $\omega_{\mathrm{zcomp1,2}}$

$$\begin{aligned}\frac{\hat{d}}{\hat{v}_{\mathrm{out}}} &= k \cdot F_m \left[A_{\mathrm{PRI}}(s) + B_{\mathrm{ac}}(s)\right] \\ &= kF_mG_mR_o \frac{\left(1+\frac{s}{\omega_{\mathrm{zcom1}}}\right)\left(1+\frac{s}{\omega_{\mathrm{zcom2}}}\right)}{\left(1+\frac{s}{\omega_{\mathrm{PI}\_p}}\right)}\end{aligned} \tag{18}$$

$$\text{where } \omega_{\mathrm{PI}\_p} = \frac{1}{R_oC_c}$$

$$\text{and } \omega_{\mathrm{zcom1,2}} = \frac{G_mR_c}{2C_dR_d}\left(1 \pm \sqrt{1 - \frac{4C_dR_d}{G_mC_cR_c^2}}\right). \tag{19}$$

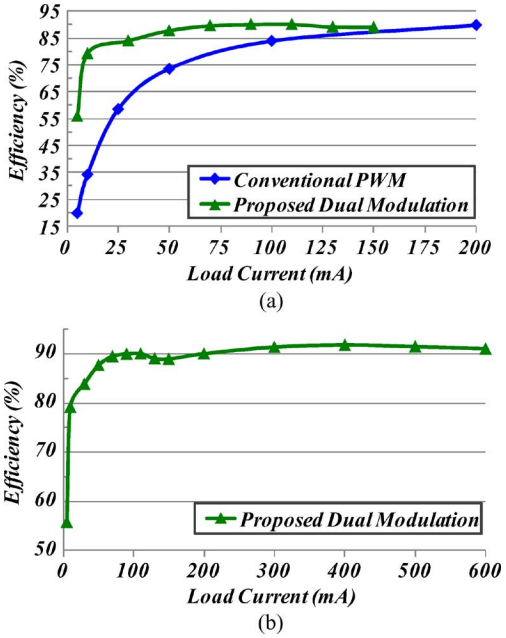


Fig. 16. (a) Efficiency comparison between the original PWM operation and the proposed dual modulation technique. (b) Efficiency of the proposed converter over a wide range of load current.

As a result, the close-loop transfer function can be expressed in (20), which contains two zeros and three poles. According to design parameters shown in Table II, the position of the three poles and the two zeros can guarantee system stability during the primary PWM operation

$$\begin{aligned} T_{\mathrm{PRI}}(s) &= kF_m G_{vd}(s)\left[A_{\mathrm{PRI}}(s) + B_{\mathrm{ac}}(s)\right] \\ &\approx kF_m G_{vd0} G_m R_o \\ &\quad \times \frac{\left(1+\frac{s}{\omega_{\mathrm{zcom1}}}\right)\left(1+\frac{s}{\omega_{\mathrm{zcom2}}}\right)}{\left[1+\frac{2\zeta}{\omega_O}s+\left(\frac{s}{\omega_O}\right)^2\right]\left(1+\frac{s}{\omega_{\mathrm{P1\_}p}}\right)}. \end{aligned} \quad (20)$$

Fig. 12 depicts the analytic Bode plot of the primary modulator with the ac ripple detector. Expectedly, the phase margin is larger than 45 degrees since the pole-zero cancellation of the proposed ac ripple detection technique is achieved without using a large ESR.

V. Experimental Results

The circuit was implemented by the TSMC 0.25 μm CMOS process. The chip micrograph is shown in Fig. 13. The specifications of the converter are listed in Table III and the comparison list of the dcdc buck converter is shown in Table IV.

Fig. 14 shows the output waveforms at different load current conditions when the converter enables the dual modulation technique. Fig. 14(a)–(c) reveals how the HFM circuit can adjust the switching frequency dynamically according to load current. Fig. 14(d) shows the system correctly reverts to the PWM mode when load current is raised higher than $I_{\mathrm{load(threshold)}}$.

The waveforms of the output voltage and the inductor current during load transient response are shown in Fig. 15. Fig. 15(a) shows the recovery times are about 2.5 μs and 3 μs when load current changes from 150 mA to 450 mA and *vice versa*, respectively. And the load current changes from 1 mA to 500 mA and *vice versa* as shown in Fig. 15(b). This demonstrates the system stability is controlled by the dual modulation system with the ac ripple detector.

Fig. 16(a) shows the comparison in efficiency between the conventional PWM operation and the proposed dual modulation technique. The number of switching signal at the gate of the power MOSFETs can be effectively reduced. As a result, the maximum efficiency improvement is about 45% at load current $=$ 10 mA. The efficiency of the proposed converter over a wide load range is shown in Fig. 16(b). The level of efficiency dropped slightly at the mode transition within allowable specification. However, this demonstrates that efficiency can be always kept high by using the dual modulation technique.

VI. Conclusion

The proposed dual modulation technique can enhance power conversion efficiency within the allowable output voltage ripple for the supply of system-on-a-chip applications. The proposed ac ripple detector can alleviate the worsening switching noise caused by parasitic resistance and inductance due to high-switching operation. In addition, the switching frequency can be kept higher than the acoustic frequency to avoid noisy sound in the LPD circuit. Experiment results show that the inductor size can be reduced to about 1 μH with the switching of 5 MHz. The load transient response time is smaller than 3 μs when load current changes from 150 to 450 mA or *vice versa*. Furthermore, the power efficiency can be always kept higher than 85% over a wide load current range. It ensures light efficiency can be raised about 45% above that of the conventional design.

References

[1] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics, 2nd Ed.*. Norwell, MA: Kluwer, 2001, pp. 92–101.

[2] J. Xiao, A. V. Peterchev, J. Zhang, and S. R. Sanders, "A 4- μA quiescent-current dual-mode digitally controlled buck converter IC for cellular phone applications," *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2342–2348, Dec. 2004.

[3] H.-W. Huang, K.-H. Chen, and S.-Y. Kuo, "Dithering skip modulation, width and dead time controllers in highly efficient DC-DC converters for system-on-chip applications," *IEEE J. Solid-State Circuits*, pp. 2451–2465, Nov. 2007.

[4] C.-Y. Hsieh and K.-H. Chen, "Adaptive Pole-Zero Position (APZP) technique of regulated power supply for improving SNR," *IEEE Trans. Power Electron.*, vol. 23, no. 6, pp. 2949–2963, Nov. 2008.

[5] W.-R. Liou, M.-L. Yeh, and Y. L. Kuo, "A high efficiency dual-mode buck converter IC for portable applications," *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 667–677, Mar. 2008.

[6] P.-J. Liu, Y.-K. Lo, H.-J. Chiu, and Y.-J. E. Chen, "Dual-current pump module for transient improvement of step-down DC-DC converters," *IEEE Trans. Power Electron.*, vol. 24, no. 4, pp. 985–990, Apr. 2009.

[7] R. P. Singh and A. M. Khambadkone, "A buck-derived topology with improved step-down transient performance," *IEEE Trans. Power Electron.*, vol. 23, no. 6, pp. 2855–2866, Nov. 2008.

[8] J. Choi, D. Huh, and Y. Kim, "The improved burst mode in the stand-by operation of power supply," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2004, pp. 426–432.

[9] S. Kapat, S. Banerjee, and A. Patra, "Voltage controlled pulse skipping modulation for efficiency improvement in light load," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 2009, pp. 2649–2652.

[10] C.-L. Chen, W.-L. Hsieh, W.-J. Lai, K.-H. Chen, and C.-S. Wang, "A new PWM/PFM control technique for improving efficiency over wide load range," in *Proc. IEEE Int. Conf. Electron., Circuits, Syst.*, Sep. 2008, pp. 962–965.

[11] H.-W. Huang, H.-H. Ho, C.-C. Chien, K.-H. Chen, G.-K. Ma, and S.-Y. Kuo, "Fast transient DC-DC converter with on-chip compensated error amplifier," in *Proc. IEEE ESSCIRC*, 2006, pp. 324–327.

[12] K.-H. Chen, C.-J. Chang, and T.-H. Liu, "Bidirectional current-mode capacitor multipliers for on-chip compensation," *IEEE Trans. Power Electron.*, pp. 180–188, Jan. 2008.

[13] C. F. Lee and P. K. T. Mok, "A monolithic current-mode CMOS converter with on-chip current-sensing technique," *IEEE J. Solid-State Circuits*, vol. 39, no. 1, Jan. 2004.

[14] F.-F. Ma, W.-Z. Chen, and J.-C. Wu, "A monolithic current-mode buck converter with advanced control and protection circuits," *IEEE Trans. Power Electron.*, vol. 22, no. 5, pp. 1836–1846, Sep. 2007.

[15] J. Sun, "Characterization and performance comparison of ripple-based control for voltage regulator modules," *IEEE Trans. Power Electron.*, vol. 21, no. 2, pp. 346–353, Mar. 2006.

[16] F. Wang, J. Xu, and B. Wang, "Comparison study of switching DC-DC converter control techniques," in *Proc. IEEE Int. Conf. Commun. Circuits Syst.*, Jun. 2006, vol. 4, pp. 2713–2717.

[17] S. Qu, "Modeling and design considerations of V^2 controlled buck regulator," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Mar. 2001, pp. 507–513.

[18] F. Wang, J. Xu, and J. Xu, "Small-signal model of V^2 control technique with compensation," in *Proc. IEEE Int. Conf. Commun. Circuits Syst.*, Jun. 2004, vol. 2, pp. 27–29.

[19] G. Schuellein, "Current sharing of redundant synchronous buck regulators powering high performance microprocessors using the V^2 control method," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Feb. 1998, pp. 853–859.

[20] S.-J. Wang, Y.-H. Lee, Y.-C. Lai, and K.-H. Chen, "Quadratic differential and integration technique in V^2 control buck converter with small ESR capacitor," in *Proc. IEEE Custom Integr. Circuits Conf.*, Sep. 2009, pp. 211–214.

[21] H. P. Forghani-zadeh and G. A. Rincon-Mora, "Current-sensing techniques for DC-DC converters," in *Proc. IEEE Midwest Symp. Circuits Syst.*, Aug. 2002, vol. 2, pp. 4–7.

[22] S. Ziegler, R. C. Woodward, H. H. C. Iu, and L. J. Borle, "Lossless inductor current sensing method with improved frequency response," *IEEE Trans. Power Electron.*, vol. 24, no. 5, pp. 1128–1222, May 2009.

[23] Y. Wu, S. Y. S. Tsui, and P. K. T. Mok, "An area- and power-efficient monolithic buck converter with fast transient response," in *Proc. IEEE Custom Integr. Circuits Conf.*, Sep. 2009, pp. 307–310.

[24] J. M. Esteves and R. G. Flatness, "Adjustable Minimum Peak Inductor Current Level for Burst Mode in Current-Mode DC/DC Regulators," U.S. Patent 6,724,174, Apr. 20, 2004.

[25] J.-C. Tsai, T.-Y. Huang, W.-W. Lai, and K.-H. Chen, "Dual modulation technique for high efficiency in high switching buck converters over a wide load range," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 2010, pp. 3709–3712.

[26] Y.-H. Lee, S.-J. Wang, and K.-H. Chen, "Quadratic differential and integration technique in V^2 control buck converter with small ESR capacitor," *IEEE Trans. Power Electron.*, vol. 25, no. 4, pp. 829–838, Apr. 2010.

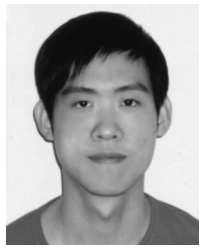
[27] J. Li and F. C. Lee, "Modeling of V^2 current-mode control," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Feb. 2009, pp. 298–304.

[28] A. M. Wu and S. M. Piekiewiez, "Switched Converter With Variable Peak Current and Variable Off-Time Control," U.S. Patent 7528587, May 2009.

[29] J.-H. Chen, P.-J. Liu, Y.-L. Hung, H.-S. Yang, and Y.-J. E. Chen, "A spur-reduced multimode power-level tracking power amplifier using a frequency-hopping DC-DC converter," *IEEE Trans. Microw. Theory Tech.*, vol. 58, no. 5, pp. 1333–1338, May 2010.

[30] H. Y. H. Lam, W.-H. Ki, and D. Ma, "Loop gain analysis and development of high-speed high-accuracy current sensors for switching converters," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 2004, pp. 828–831.

[31] C. Y. Leung, P. K. T. Mok, K. N. Leung, and M. Chan, "An integrated CMOS current-sensing circuit for low-voltage current-mode buck regulator," *IEEE Trans. Circuits and Systems II, Exp. Briefs*, vol. 52, no. 7, pp. 394–397, Jul. 2005.



Jen-Chieh Tsai was born in Kaohsiung, Taiwan. He received the B.S. degree in electrical engineering from National Yunlin University of Science and Technology, Yunlin, Taiwan, in 2003 and the M.S. degree in electrical engineering from Tamkang University, Taipei, Taiwan, in 2005. He is currently working toward the Ph. D. degree in electrical and control engineering, National Chiao Tung University, Hsinchu, Taiwan.

His research area contains many projects of high resolution ADC, low power DAC, and power management ICs at the Low Power Mixed Signal Lab. His interests include power management circuit designs, PFC ICs, and analog integrated circuit designs.

Tsung-Ying Huang was born in Taoyuan, Taiwan, who received the B.S. and M.S. degree from Electrical Control Engineering in National Chiao Tung University, Taiwan, in 2008 and 2010. He has participated in contains many projects of power management ICs at Low Power Mixed Signal Lab in National Chiao Tung University, Taiwan. Also he is presently an advanced engineer of analog IC design in Novatek Microelectronics Corporation in Hsinchu Science Park, Taiwan. His interests include power management circuit designs and analog integrated circuit designs.

Wang-Wei Lai was born in Taoyuan, Taiwan, on July 22, 1986. He received the M.S. degree in electrical control engineering from National Chiao Tung University, Taiwan, in 2010.

His research area contains many projects of power management ICs in Low Power Mixed Signal Lab in National Chiao Tung University, Taiwan. Currently, he is an Advanced Engineer of analog IC design at Novatek Microelectronics Corporation in Hsinchu Science Park, Taiwan. His interests include power management circuit designs and analog IC designs.

Ke-Horng Chen (M'04–SM'09) received the B.S., M.S., and Ph.D. degrees in electrical engineering from National Taiwan University, Taipei, in 1994, 1996, and 2003, respectively.

From 1996 to 1998, he was a part-time IC Designer at Philips, Taipei. From 1998 to 2000, he was an Application Engineer at Avanti, Ltd., Taiwan. From 2000 to 2003, he was a Project Manager at ACARD, Ltd., where he was engaged in designing power management ICs. He is currently an Associate Professor in the Department of Electrical Engineering, National Chiao Tung University, Hsinchu, Taiwan, where he organized a Mixed-Signal and Power Management IC Laboratory. He is the author or coauthor of more than 100 papers published in journals and conferences, and also holds several patents. His current research interests include power management ICs, mixed-signal circuit designs, display algorithm and driver designs of liquid crystal display (LCD) TV, red, green, and blue (RGB) color sequential backlight designs for optically compensated bend (OCB) panels, and low-voltage circuit designs.