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Antenna-in-Package Design for Wirebond Interconnection to Highly Integrated 60-GHz Radios

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***Abstract*—This paper first presents a quasi-cavity-backed, guard-ring-directed, substrate-material-modulated slot antenna. The antenna, intended for use in highly integrated 60-GHz radios, is deliberately designed to exhibit capacitive input impedance to suit low-cost wire-bonding packaging and assembly technique. The antenna implemented in a thin cavity-down ceramic ball grid array (CBGA) package in low-temperature cofired ceramic (LTCC) technology has achieved an acceptable impedance bandwidth from 59 to 65 GHz with an estimated efficiency of 94%. At millimeter-wave (mm-wave) frequency 60 GHz, one of key challenges is how to realize low-loss interconnection between a radio chip and an antenna using wire-bonding technique. This paper then addresses this issue in the framework of antenna-in-package (AiP) design at 60 GHz and proposes a new solution to the challenge. Detailed wirebond design method and results are given. A major concern with AiP is the risk of the antenna coupling to the radio chip. This paper also evaluates this unwanted coupling and shows that the coupling from the in-package antenna to the on-chip inductor is lower than 30 dB for the worst case. These results clearly demonstrate the feasibility and promise of the elegant AiP technology for emerging high-speed short-range 60-GHz wireless communications.**

***Index Terms*—Antenna in package (AiP), low-temperature cofired ceramic (LTCC), 60-GHz radio.**

I. Introduction

An IEEE standards group, 802.15.3c, is defining specifications for 60-GHz radios to use a few gigahertz of unlicensed spectrum to enable very high-data-rate applications such as high-speed Internet access, streaming content downloads, and wireless data bus for cable replacement. The targeted data rate for these applications is greater than 2 Gb/s [1].

The 60-GHz radios have been typically designed as an assembly of several microwave monolithic integrated circuits (MMICs) in gallium arsenide (GaAs) semiconductor technology. They have been used for Gigabit Ethernet (1.25 Gb/s) bridges between local area networks [2]. A recent work has pushed up the data rate to 1.5 Gb/s with simple amplitude shift-keying (ASK) modulation using single-chip transmitter (Tx) and receiver (Rx) MMICs in a 0.15-μm GaAs process [3]. It should be mentioned that the data rate of 1.5 Gb/s is limited by the measurement system and the same MMICs are especially well suited for transmission and reception of 60-GHz signals at data rates of several Gb/s [3]. However, it is generally believed that the 60-GHz radios in GaAs MMICs are rather bulky [2] and expensive [2], [3]. In order for 60-GHz radios to have mass deployment and meet consumer marketplace requirements, the cost and size of any solution thus have to be cheap and compact. That means Si (silicon), not the GaAs used today [1]. In fact, designs towards low-cost highly integrated 60-GHz radios have been carried out in Si technologies. Floyd *et al.* have demonstrated the first 60-GHz fully integrated radio transmitter and receiver chipset in a 0.13-μm silicon-germanium (SiGe) technology [4]. However, CMOS is the lowest cost and highest integration option. Today, bulk CMOS at nodes 130, 90, and 65 nm are capable of power gain at 60 GHz. Razavi has demonstrated a 60-GHz radio transceiver chip in a 130-nm CMOS [5] and Toshiya *et al.* a 60-GHz receiver chip in a 90-nm CMOS [6]. Building-block circuits in a 65-nm CMOS have also been designed and characterized [7]. As CMOS scales, it is expected that future bulk CMOS at nodes 45 and 22 nm will provide higher power gain at 60 GHz with lower power consumption.

An antenna plays a key role in a radio as it has independent properties that affect the radio as a whole. Antenna designs for highly integrated radios operating at 60 GHz or above are shifting from conventional discrete designs to antenna-on-chip (AoC) and antenna-in-package (AiP) solutions [8]–[20]. This is because the antenna form factor at 60 GHz is on the order of millimeters or less, which opens up new integration options on a chip or in a package. Zhang *et al.* evaluated the AoC solution for 60-GHz radio on a silicon substrate and found that both inverted-F and quasi-Yagi on-chip antennas have very poor radiation efficiency, about 5% due to the low resistivity and high permittivity of the silicon substrate [8]. Micromachining techniques and proton implantation process have been proposed to reduce silicon substrate loss so as to improve the AoC radiation efficiency [9], [10]. However, use of them has deviated from mainstream silicon technology, which undoubtedly increases the cost of the total solution. Nevertheless, the realization of a truly single-chip 60-GHz radio and avoidance of transmission loss due to interconnect are yet encouraging particularly circuit designers to explore the integration of an antenna (or antennas) with other circuits on a single chip [6], [12], [13]. The AiP solution was originally proposed and demonstrated at frequencies below 6 GHz [14], [15]. Recently, it has

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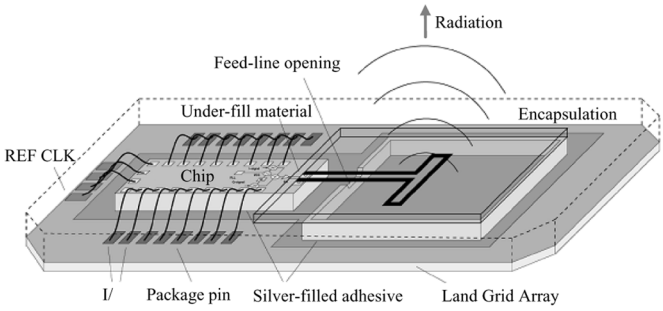

Fig. 1. Conceptional drawing of AiP by IBM.

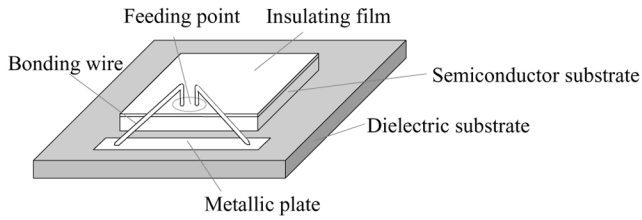

Fig. 2. Conceptional drawing of AiP by Toshiba.

begun to receive great attention among 60-GHz radio developers, for example, the IBM researchers have demonstrated a complete AiP solution for 60-GHz radios in a land grid array package using plastic mould injection technology, and showed that a folded dipole antenna suspended in a metal cavity has very good radiation efficiency of about 90% [16]–[18]. The Toshiba engineers have demonstrated another AiP solution, which connects the chip 60-GHz input and output pads to the metal plate on the chip mounting substrate with bonding wires to form a three-dimensional triangular loop. The three-dimensional triangular loop creates distance between the chip and the strong electric current, thereby minimizing deterioration of efficiency [19]. The low-temperature cofired ceramic (LTCC) and liquid crystal polymer (LCP) processes have been added to the short list of technologies capable of realizing mm-wave wireless systems [20]. In this paper, we present a novel wirebond AiP in LTCC technology for highly integrated 60-GHz radios. The design, fabrication, and test of the AiP with an emphasis on the antenna part are described in Section II. Detailed wirebond design method and results are discussed in Section III. Unwanted coupling of the antenna to the radio chip in the AiP is evaluated in Section IV. Finally, we conclude the paper in Section V with an outline of future developments.

II. Antenna-in-Package

Driven by the great potential of the high-speed short-range wireless communications in the 60-GHz band, several AiP designs based on different packaging materials and technologies have been demonstrated. In this section, we first review them and then focus on our wirebond AiP in LTCC. Given that the AiP should be a chip-scale package, we are required to achieve such specifications as wider impedance bandwidth from 59 to 64 GHz, broader beamwidth with peak gain equal to or larger than 6 dBi, and radiation efficiency equal to or better than 80% at the central frequency 61.5 GHz.

A. Mini-Review of 60-GHz AiP Designs

Fig. 1 shows the conceptional drawing of the AiP in a land grid array (LGA) by IBM [16]–[18]. As shown, standard wire bonding is used, except for the 60-GHz signal between the chip and the antenna. The antenna is constructed from a fused silica (SiO_2) substrate, which is bonded to a covar metal frame using a thermosetting adhesive. A chemical etching and photolithography process was used for frame fabrication. The antenna is flipped to the chip using a thermal compression flip-chip bonding technique. Simultaneously, the antenna frame is attached to the package base using a silver-filled adhesive. This way, the antenna is suspended in air below the silica superstrate and the metallic base plate of the package acts as a reflecting ground. The spacing between the radiating element and the ground influences the bandwidth of the antenna and is defined by the thickness of the cover frame, which serves two purposes. First, it provides the mechanical support for the antenna, and second, it provides a well-controlled electromagnetic (EM) environment, making the antenna performance less sensitive to the surrounding package- and PCB-level dielectric and metal layers. In this configuration, the folded-dipole antenna achieves 7-dBi gain (in package) at 60 GHz and over 10% impedance bandwidth. Review of this AiP shows that use of the frame decouples the design of the antenna from the exact physical properties of the package, simplifies simulation and modeling complexity, and avoids any unknown shapes or encapsulants in close proximity to the radiating element. Special care, however, is required for the antenna feed line and flip-chip bonding that interface the chip to the antenna. A dedicated opening, an encapsulation prior to the mounting of the antenna, and a ball height of 30 μm (100 μm for mass production) make it difficult to fabricate and assemble this AiP.

Fig. 2 shows the conceptional drawing of the AiP by Toshiba [19]. It is seen that the feeding point on the chip is connected to the metal plate on the package substrate with bonding wires to form a three-dimensional triangular loop. As the antenna element is directly connected to the feeding point on the high-loss silicon chip, there is no feeder loss. The three-dimensional triangular loop creates distance between the semiconductor chip and the strong electric current, thereby minimizing deterioration of efficiency. Moreover, by widening the metal plate on the package substrate there is greater tolerance of wire displacement occurring during the manufacturing process. Furthermore, since no special process is required for connecting the bonding wires, extra work in the manufacturing process due to changes in the structure of the antenna is minimal. Although this AiP solution is cheap, the antenna gain -0.3 dBi is quite low and needs to be improved by adding a parasitic element on the package substrate. It is also difficult, if not impossible, for 60-GHz radios where more antennas are required.

Fig. 3 shows the conceptional drawing of the AiP by the Micro Radio Group at Nanyang Technological University

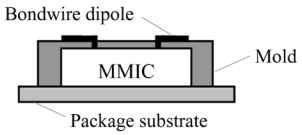

Fig. 3. Conceptional drawing of AiP by NTU.

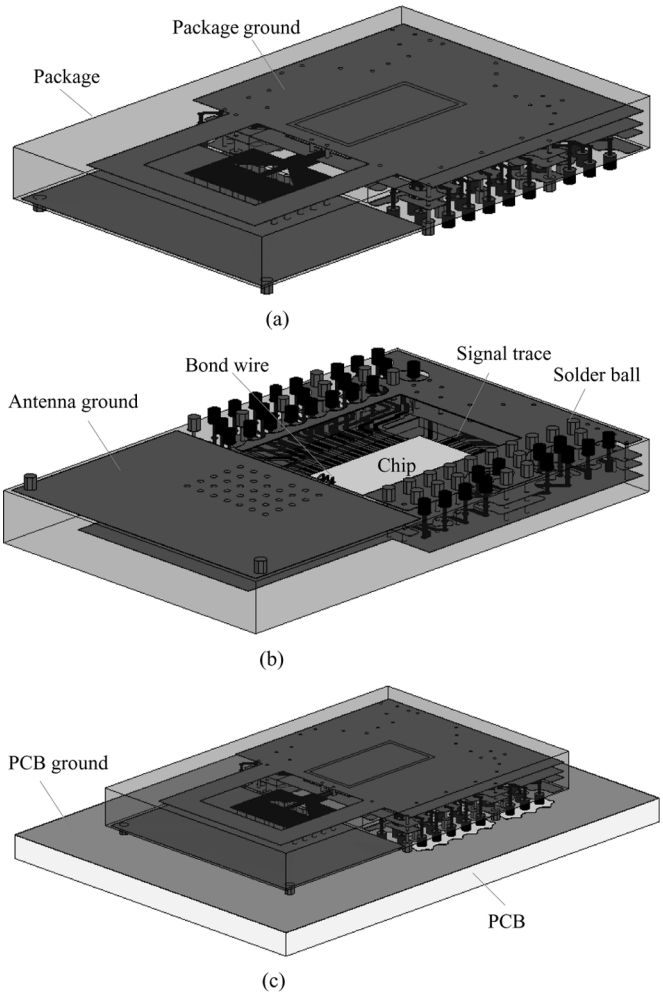

Fig. 4. Partially transparent views of the AiP: (a) top, (b) bottom, and (c) landing on the PCB.

(NTU), Singapore. It has the same advantages and disadvantages as the AiP solution by Toshiba.

In addition, it should be mentioned that there have been some important works similar to AiP for system-on-package or multichip solutions of 60-GHz radios in ceramic and plastic (Teflon and LCP) packages [20]–[27].

B. An AiP Design in LTCC

An international team consisting of researchers from NTU, Singapore Institute of Manufacturing Technology (SIMTech), and IBM has been working closely over the last three years to develop the AiP solutions in LTCC targeted to the IBM 60-GHz radio chip set with mass production capability [28], [29]. Fig. 4 shows the top and bottom partially transparent views of the AiP for the Rx chip of size $3.55 \times 1.75 \times 0.46$ mm^3. As shown, the AiP features standard wire bonding. A three-tier cavity facilitates chip mounting and efficient utilization of available space

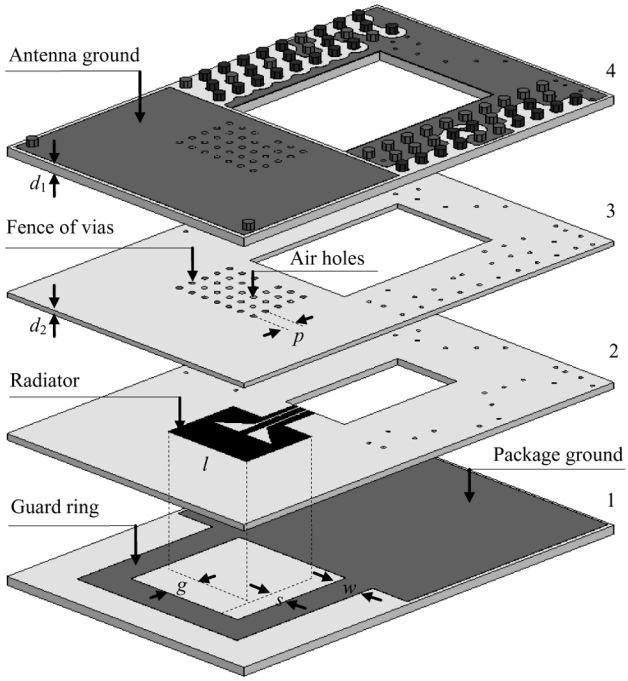

Fig. 5. Exploded view and dimensions of the AiP. The outer ring of vias is the fence of vias and the inner rings of vias are air holes.

for signal routing and also to enable reduced parasitic from wire bonding. The radio chip is adhered to the cavity base of the package ground plane. This configuration will contribute to the shielding of the chip from the antenna. The signals from the chip are connected to the antenna through bondwires in a ground–signal–ground (G-S-G) configuration. The other signals from the chip are connected to the outside PCB by the bondwires, signal traces, vias, and solder balls. The ground planes in five layers are all connected by vias and they are also connected to the outside PCB by solder balls. The AiP has 58 input/outputs with a JEDEC (Joint Electronic Device Engineering Council) standard solder ball pitch of 0.65 mm. Two dummy solder balls are attached to the two corners of the AiP, respectively, for the finishing touch on the system PCB.

Fig. 5 shows the dimensions of the AiP in FERRO A6 LTCC ($\varepsilon_r = 5.9$ and $\delta = 0.002$). Note there are four cofired laminated ceramic layers for the package. The first ceramic layer is 0.385 mm thick, the second ceramic layer is 0.285 mm thick with an opening 3.8×2 mm^2, the third layer is 0.21 mm thick with an opening 5×3.2 mm^2, and the fourth layer is 0.385 mm thick with an opening 5×3.8 mm^2. These openings form the three-tier cavity that can house the 60-GHz radio Rx chip. There are also four metallic layers for the AiP. The top buried layer provides the metallization for the package ground plane and antenna guard ring, the second buried layer the metallization for the slot radiator and signal traces, the third buried layer the metallization for the signal traces, and the bottom exposed layer the metallization for the antenna ground plane and solder ball pads. The size of the whole AiP is $12.5 \times 8 \times 1.265$ mm^3. It is interesting to note that the antenna uses a triangular slot radiator to avoid warpage in LTCC fabrication. The l of the triangular slot is chosen to be one guided wavelength λg to have broader bandwidth. A ground-plane reflector and a fence of vias

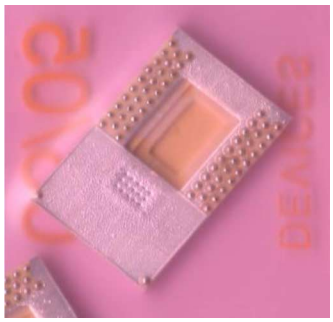

Fig. 6. Photo of the AiP.

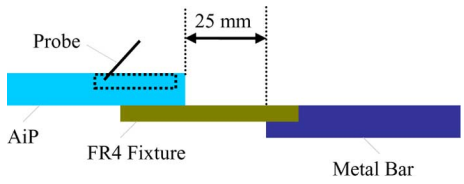

Fig. 7. Illustration of the AiP on the fixture for testing.

are introduced. The fence of vias shorts the outer metal edge of the slot radiator to the reflector to form a quasi-cavity to create a well-controlled EM environment for the radiator of the AiP. The quasi-cavity is similar to the metal cavity used in [16], [24] and makes the antenna performance less sensitive to the carried radio chip, PCB dielectric and metallic structures, which is an important design feature for system integration. The depth d of the quasi-cavity is chosen to be $\lambda g/4$ so that the radiation of the slot in free space can be enhanced by the reflector. The guard ring chosen to be $\lambda g/2$ wide serves two purposes: one, it helps to suppress the surface wave ($\lambda g/2$ opened guard ring as an open circuit to the surface wave) and two, to focus the radiation as a director. The pitch p of vias should ideally be zero to form a wall rather than a fence. Realistically, it should be chosen to satisfy $\lambda g/10$ [30]. The coplanar waveguide (CPW) feed line is designed to be 50 Ω with a pitch of 0.25 mm and a line width of 0.1 mm. The ceramic material under the slot radiator is modulated with air holes also to reduce surface wave. Thus, we have realized a novel CPW-fed quasi-cavity-backed, guard-ring-directed, substrate-material-modulated slot antenna with the following optimum values: $l = 2.064$ mm $\approx \lambda g$, $d = d_1 + d_2 = 0.595$ mm $\approx \lambda g/4$, $w = 0.925$ mm $\approx \lambda g/2$, $s = 0.442$ mm, $g = 0.8156$ mm, $p = 0.2$ mm $\approx \lambda g/10$.

The AiP was fabricated with nine green types, silver and gold metals in a panel size of 100×100 mm^2 by LTCC Boutique Foundry in SIMTech on the NTU campus. Fig. 6 shows the photo of the fabricated AiP. The antenna function of the AiP was tested with a probe-based measurement setup at IBM Thomas J. Watson Research Center, NY. Fig. 7 illustrates the test fixture to hold the AiP for testing.

Fig. 8 shows the simulated and measured reflection and impedance of the AiP with the distances of 0.13 and 0.15 mm to account for the difference between the wave-port excitation in the simulation and the probe excitation in the measurement. The distances of 0.13 and 0.15 mm were estimated by inspection using the probe pitch of 0.25 mm as reference. It

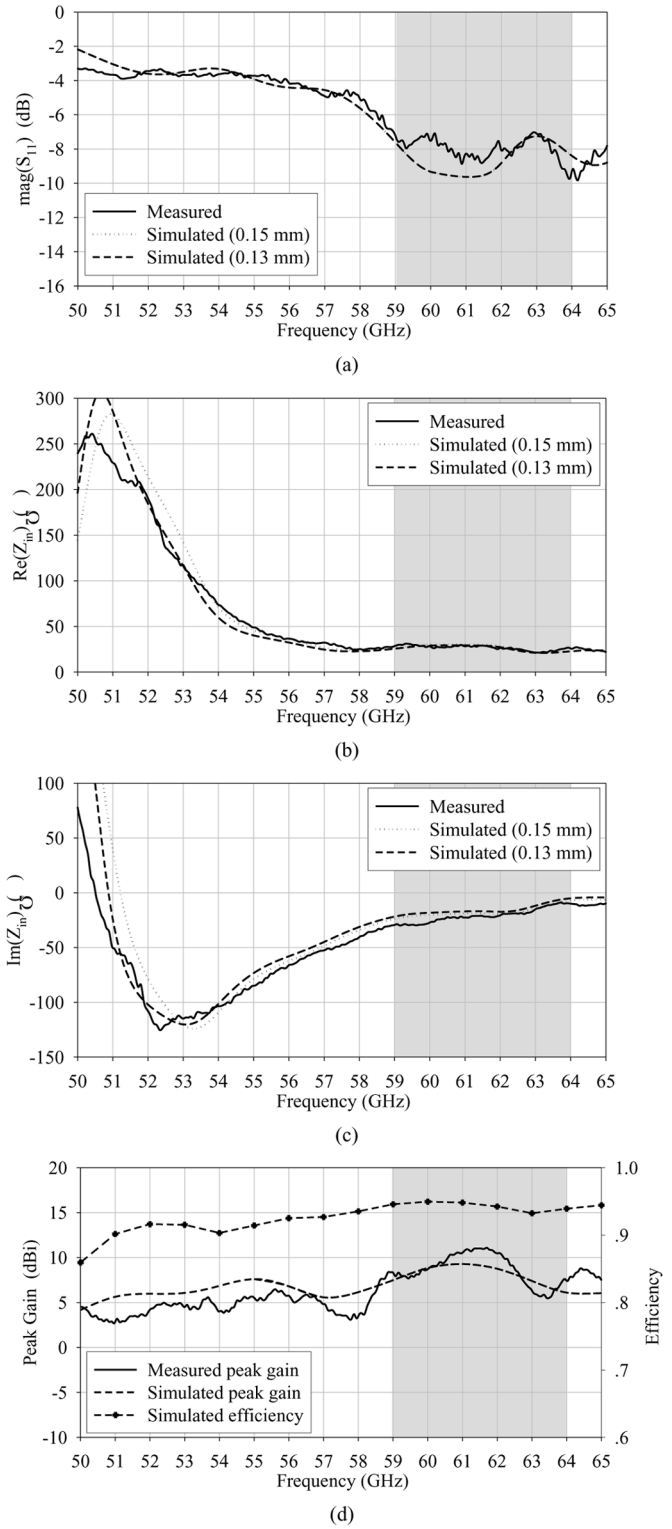

Fig. 8. Simulated and measured reflection and impedances of the AiP: (a) magnitude of S_{11}, (b) real part of the input impedance, (c) imaginary part of the input impedance, and (d) peak gain and efficiency as a function of frequency.

is seen from Fig. 8(a) that the magnitude values of S_{11} are in good agreement and are lower than -7 dB from 59 to 65 GHz indicating an acceptable matching to a 50-Ω source at these frequencies. Fig. 8(b) and (c) shows the simulated and measured impedance values from 50 to 65 GHz. They are also in

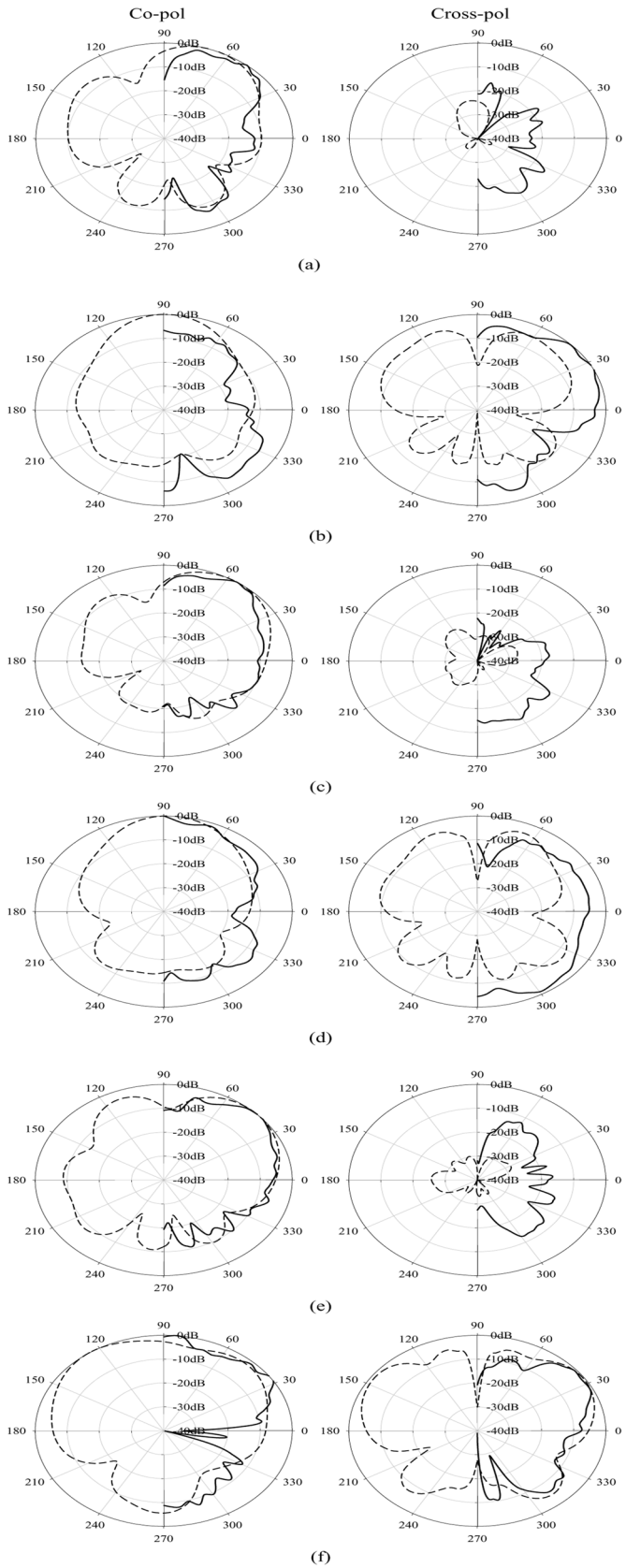

Fig. 9. Simulated (dash line) and measured (solid line) radiation patterns of the AiP: (a) E-plane patterns at 59 GHz; (b) H-plane patterns at 59 GHz; (c) E-plane patterns at 61.5 GHz; (d) H-plane patterns at 61.5 GHz; (e) E-plane patterns at 65 GHz; and (f) H-plane patterns at 65 GHz.

good agreement. As expected, the antenna exhibits capacitive reactance. The matching to the 50-Ω output impedance of the

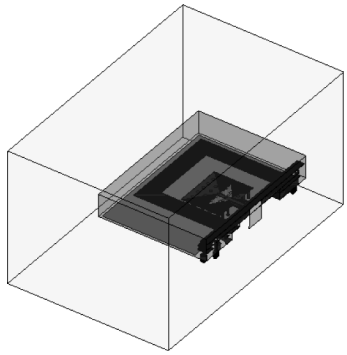

Fig. 10. HFSS model of the antenna part of the AiP.

carried 60-GHz radio Rx chip will be improved if the inductive reactance from the bondwire is properly exploited. We will discuss this issue in Section III. The measured and calculated peak gain values for the AiP in the main beam direction are 11 and 9.5 dBi at 61.5 GHz, respectively, with an estimated efficiency of 94%, as shown in Fig. 8(d).

Fig. 9 shows the simulated and measured radiation patterns of the AiP. Due to a limitation of the measurement setup, the measured radiation patterns only extend from 90° to 270°. The simulation was done for only the antenna portion due to compute memory issues. This will not affect the antenna impedance, but it will have some effect on antenna radiation patterns. The simulated and measured radiation patterns of the AiP at 61.5 GHz reveal that the H-plane patterns are similar to, but the E-plane patterns are different from, those of a conventional cavity-backed slot antenna. A shaped-beam pattern can be seen in the co-polar E-plane with the main beam in the directions from 45° to 60°. The shaped-beam pattern in the co-polar E-plane is mainly caused by the package ground, which weakens the radiation of the antenna towards the chip.

The simulation was done in HFSS from Ansoft, Pittsburgh, PA, USA [31]. Fig. 10 shows the HFSS model for the impedance calculation of the antenna part with the wave-port excitation. The measurement of the antenna impedance of the AiP has validated the model, which should be expected as the excellent EM environment has been created in the AiP for the antenna. The design of the antenna from the exact physical properties of the package greatly simplifies simulation and modeling complexity.

III. Wirebond Design for the AiP

At mm-wave frequency 60 GHz, the interconnection between the chip and the package using the wire-bonding technique has been identified as one of key challenges because the discontinuity introduced by the bondwire can significantly affect the performance of the entire radio at mm-wave frequency. Nonetheless, the wire-bonding technique, well established in consumer electronics, remains a very attractive solution since it is robust and inexpensive. In addition, it has the advantage of being tolerant of chip thermal expansion, an important requirement for many applications.

A number of studies on the electrical performance of wire-bonding interconnection have been reported for microstrip and coplanar configurations, indicating that a bondwire

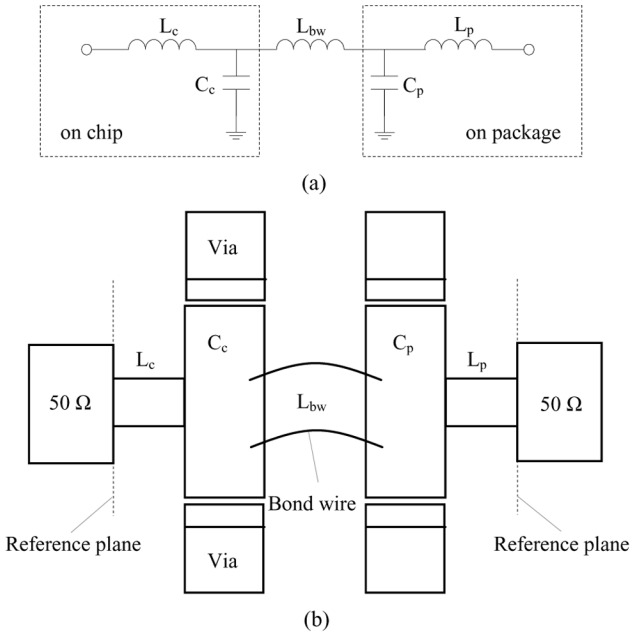

Fig. 11. Budka's bondwire compensation scheme: (a) circuit model and (b) layout.

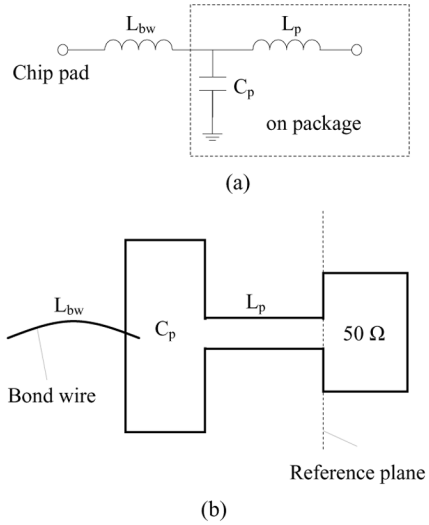

Fig. 12. Bondwire compensation scheme used in [36] and [23]: (a) circuit model and (b) layout.

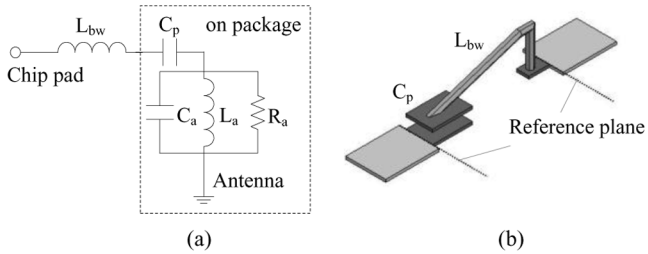

Fig. 13. New compensation scheme: (a) circuit model and (b) layout.

as a series inductor will increase the loss drastically as the frequency or the length is increased [32]–[34]. In order to improve the high-frequency performance of a bondwire interconnect, efforts have usually focused on reducing the length of the bondwire and also reducing the chip-to-package spacing. However, limitations in manufacturing require longer bondwire lengths and wider chip-to-package spacing to improve the yields of mm-wave chip-package assemblies. Therefore, the goal for mm-wave interconnect design is to maximize bondwire length to improve manufacturability and maximize bond-pad size so that mechanical tolerances are eased. Budka has demonstrated that this is possible with a filter theory approach to interconnect design as shown in Fig. 11 [35]. He has considered the conventional bondwire design as a single-stage low-pass filter while his novel design as a five-stage low-pass filter. Thus, for the same cutoff frequency of the single- and five-stage filter, the center inductor in the five-stage design can have a 3.6 times higher inductance than a single inductor design. This directly translates into a 3.6 times longer bondwire for the same cutoff frequency.

Budka's wirebond design technique enables the use of significantly longer bondwires but the chip must have filter-like compensation on the mm-wave bonding pads. This is usually impossible unless the codesign of the chip and package can be done. Also, Budka's method is not suitable for connecting the radio chip to the antenna because it is difficult to implement the DC blocking capacitor between them.

Sun *et al.* have demonstrated a T-network to compensate for the series inductance introduced by the bondwire as shown in Fig. 12 [36]. The inductor $L_{\rm bw}$ models the bondwire inductance. Inductor $L_{\rm p}$ and capacitor $C_{\rm p}$ are realized on package. This compensation network has also been used in [24], but it has two drawbacks. One is the large on-package area required to implement $L_{\rm p}$ and $C_{\rm p}$, and the other is that it is not suitable for on-package CPW design. Also, Sun's method for connecting the radio chip to the antenna needs to implement the DC blocking capacitor on chip.

Fig. 13 shows the novel bondwire compensation scheme with the suggested structure proposed by Sun and Zhang [37]. As can be seen, a series capacitor is used to tune the inductance of the bondwire to a resonant condition, thus compensating the high inductance of bondwire at the resonant frequency. In the mm-wave frequency range, the form factor of the capacitor for compensation is on the order of tens of femtofarads, making the structure very compact. In addition, the compensation structure enjoys the properties of manufacturing reliability and cost effectiveness. It could be used successfully for the commonly used chip-to-package connections at mm-wave frequencies. This will be very desirable for highly integrated mm-wave wireless devices which call for the properties of miniaturization, manufacturing reliability, and mass-production cost effectiveness.

The compensation design involves the following steps [37]:

1) Identify the bondwire to be compensated.
2) Identify an operation frequency and bandwidth.
3) Model the bondwire to be compensated in the highly integrated device environment first and then simulate the electrical performance of the established model at the operating frequency band. Based on this simulation, the bondwire inductance to be compensated is obtained.
4) Construct a bondwire compensation structure as shown in Fig. 13 in the highly integrated device environment. Based

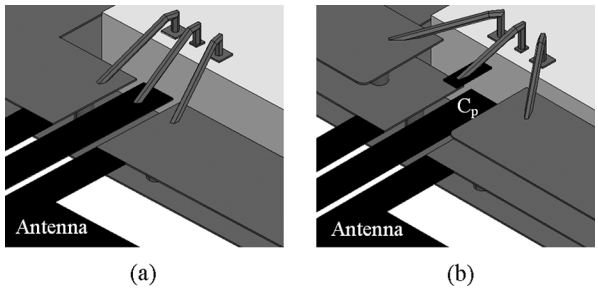

Fig. 14. Wire-bonding configurations: (a) without the compensation capacitor and (b) with the compensation capacitor.

on this structure the capacitor dimensions are estimated to compensate the inductance value calculated at the last step. Model this capacitive compensation structure to combine with the bondwire in the highly integrated device environment first and then optimize the frequency response of the established model to the optimal by just adjusting the bondwire compensation structure.

Fig. 14(a) illustrates the wire-bonding configuration of the highly integrated 60-GHz radio Rx chip with the antenna in the AiP. As shown in Fig. 15(a) and (b), the connection of the 400-μm-long 25.4-μm bondwire will not introduce significant resistance but $\sim$ 120 ohm inductive reactance at the frequency band of interest, 55–65 GHz. Accordingly, the return loss of the antenna degrades greatly as seen in Fig. 15(c). A significant degradation in the magnitude of S_{11} to 1.9 dB at 61 GHz is observed. It is obvious that the antenna cannot work with the bondwire connected directly. Based on our compensation scheme, a capacitor in series with the signal bondwire as illustrated in Fig. 14(b) is implemented. Following the above steps, the inductive reactance at the 60-GHz band from 55 to 65 GHz has been compensated successfully as shown in Fig. 15(b). It is also seen from Fig. 15(c) that the magnitude of S_{11} of the AiP is now lower than -10 dB from 58.5–64.5 GHz, indicating a good matching to the 50-Ω chip. The other parameters of the antenna performance, such as gain, efficiency, and patterns, are also acceptable after compensation as shown in Figs. 16 and 17. The peak gain is found to be 7 dBi. These results clearly demonstrate that the antenna can work well using the bondwires with our novel bondwire compensation scheme. In addition, as shown in Fig. 8, the measurement and simulation results agree well without bondwires. Therefore, the simulation tool can be trusted to estimate the bondwire connection and compensation scheme as analyzed above. It can be seen that, using our bondwire compensation scheme, the designed AiP provides an extremely compact and elegant solution for communication systems operating at mm-wave frequencies. The scheme is easy to realize by only adding the capacitive coupling part. The compensation structure can be designed separately. Once it is designed well, it can be easily modified for other designs as well.

When the AiP is placed on the system PCB as shown in Fig. 4(c), the PCB board affects the antenna performance. This is confirmed by the simulation of landing the above bondwire-compensated AiP on a $15.7 \times 10 \times 0.8$ mm^3 FR4 PCB. It is seen from Fig. 15 that the PCB changes the magnitude of S_{11} but the 10-dB impedance bandwidth still can cover the 59–64 GHz

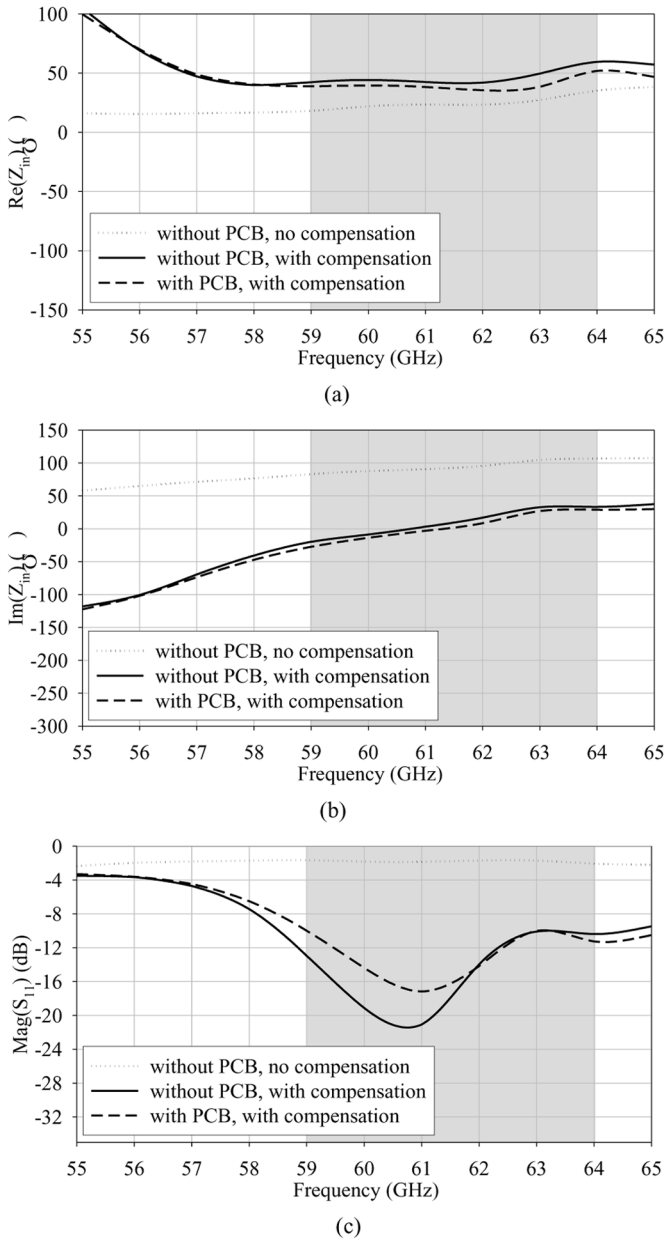

Fig. 15. Simulated impedance and magnitude of S_{11} of the AiP with bondwires as a function of frequency.

band. It is also seen from Fig. 16 that the PCB improves the AiP radiation in the upper hemisphere and reduces the AiP radiation in the lower semi-sphere. This leads to a high peak gain of 8.7 dBi as shown in Fig. 17, though the radiation efficiency degrades. In simulation, it is also found that the matching performance is insensitive to the further extended PCB, while the gain could be further improved.

Table I lists key data of this work with other AiP designs as well as related antenna solutions for highly integrated 60-GHz radios. We have no intention to compare them because it is difficult to make a fair comparison between the different solutions since they are fabricated in different technologies and meant for different purposes. Nevertheless, we can see from Table I that basic radiating elements such as dipole, slot, and patch are popular in AiP designs and excellent radiation efficiency can be

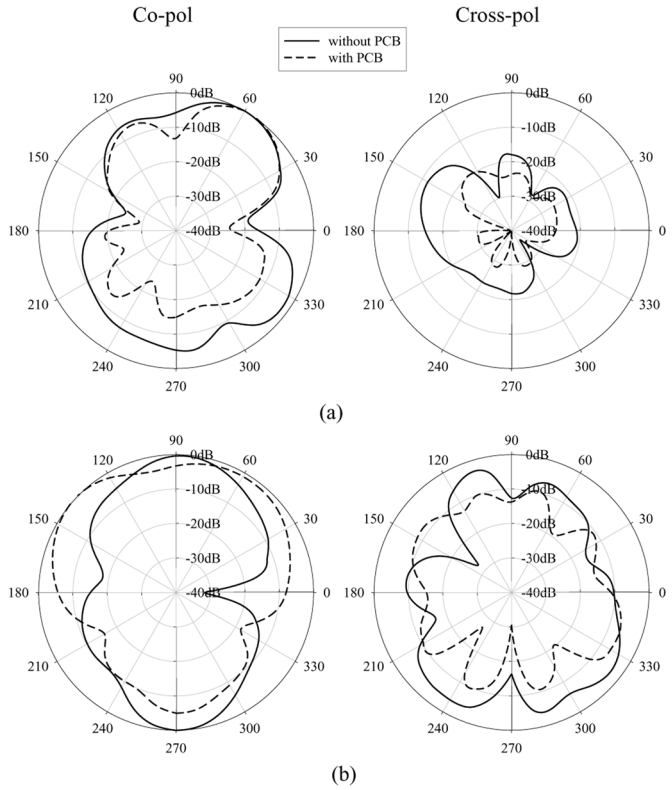

Fig. 16. Simulated patterns of the AiP with bondwires and compensation: (a) E-plane patterns at 61.5 GHz; (b) H-plane patterns at 61.5 GHz.

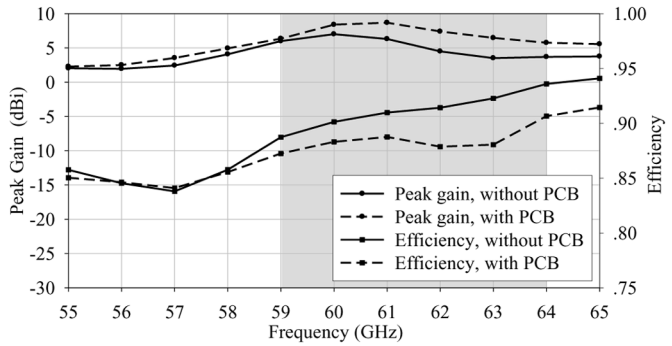

Fig. 17. Simulated gain and efficiency of the AiP with bondwires and compensation.

achieved in LTCC. Both wire-bonding and flip-chip techniques are used for interconnecting the antenna to the radio chip. The wirebond needs compensating, while the flip-chip does not. The compensation is usually made in the package not on the chip.

IV. Evaluation of Unwanted Coupling

A major concern with AiP is the risk of the antenna coupling to the radio chip. On-chip passive components such as inductors and capacitors occupy substantial die area and thus are susceptible to the antenna coupling. Here, taking an on-chip inductor as an example, we simulate the coupling from the in-package antenna to the on-chip inductor in terms of the magnitude of the transmission coefficient S_{21}.

Fig. 18 shows the configuration of the on-chip spiral inductor. It is is implemented using two metal layers, M5 and M6 ($\sigma =$

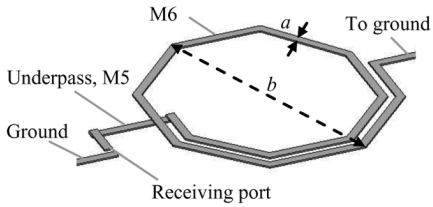

Fig. 18. Inductor configuration in the coupling simulation.

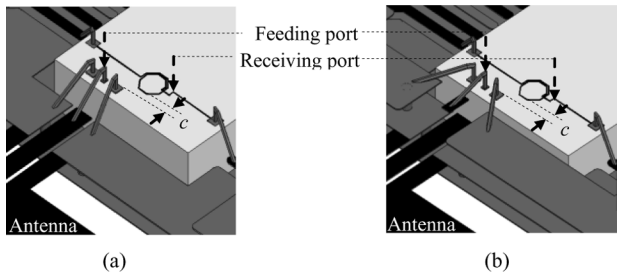

Fig. 19. Coupling simulation setups: (a) without the compensation capacitor and (b) with the compensation capacitor.

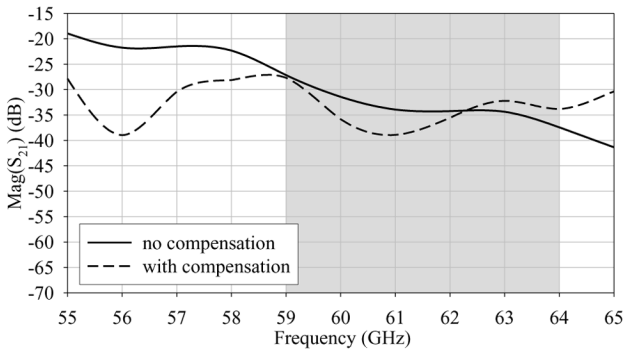

Fig. 20. Simulated $|S_{21}|$ with $c = 0.1$ mm.

$2.8e + 7$ S/m), in a 9-μm-thick SiO_2 ($\varepsilon_r = 4$) layer on a 451-μm-thick Si ($\varepsilon_r = 11.9$ and $\sigma = 10$ S/m) substrate. It has dimensions $a = 10$ μm and $b = 311$ μm. Fig. 19(a) and (b) shows the coupling simulation setups without and with the compensation capacitor, respectively. The on-chip inductor has one terminal connected to the package ground by a bondwire and the other terminal together with another grounded bondwire used as the receiving port. The feeding port to the antenna is located on the chip and excites the antenna through the G-S-G bondwires. Fig. 20 shows the simulated $|S_{21}|$ as a function of frequency from 55 to 65 GHz under the worst condition. Here, we define the worst case as no guard ring and pattern grounded shield are used for the inductor and the distance between the inductor and antenna is the shortest allowed by the on-chip layout rule. Note that the coupling levels are both lower than 27.5 dB over the 60-GHz band for the cases with and without the compensation capacitor, respectively. The lower coupling is the result of good grounding and shielding design in the AiP. It is more interesting to note that the coupling fluctuates with frequency indicating multiple-coupling mechanisms. It is conjectured that there are inductive coupling from the G-S-G bondwires to the inductor, radiative coupling from the antenna to the inductor, and resistive coupling from the antenna feeding port to the in-

TABLE I
PERFORMANCE SUMMARY OF THE ANTENNA SOLUTIONS FOR HIGHLY INTEGRATED 60-GHZ RADIOS

Antennas	Technology	Radiator	Dimension (mm)	Bandwidth (GHz)	Peak Gain (dBi)	Efficiency	Beamwidth	Interconnection
This work	LTCC	Slot	12.5×8×1.265	59-65 ($\|S_{11}\|$<=-7 dB)	11	94%	~30°	Wirebond
[16]	Plastic	Dipole	13×13×2	52-68 ($\|S_{11}\|$<=-10dB)	7	90%	60°	Flip chip
[19]	Plastic	Loop	<4×4	-	-0.4	-	>90°	Wirebond
[20]	Teflon	Patch array	10×10×1.1	60.9-61.8($\|S_{11}\|$<=-10dB)	8.5	>91%	~40°	Flip chip
	LTCC	Patch array	10×10×0.45	59.3-61.3($\|S_{11}\|$<=-10dB)	7.17	-	~40°	Flip chip
[21]	LTCC	Patch array	10×10×0.3	-	7	-	36°	Wirebond
[22]	LTCC	Slot	5×4×0.32	62-64 ($\|S_{11}\|$<=-10dB)	4	-	~100°	Flip chip
[23]	HTCC	Patch array	1×12×0.127	59.2-60.7($\|S_{11}\|$<=-10dB)	12	-	20°	Wirebond
			5×10×0.127	59.6-60.5($\|S_{11}\|$<=-10dB)	13	-	33°	Wirebond
[24]	MEMS	Dipole	~13×6×0.7	56-65 ($\|S_{11}\|$<=-10dB)	8	90%	~60°	Flip chip
[25]	LTCC	Slot array	-	59-63 ($\|S_{11}\|$<=-10dB)	19	-	~10°	-
[26]	LTCC	Patch array	<9.6×1.5×0.32	55.4-66.8($\|S_{11}\|$<=-10dB)	12.6	-	~20°	-
[27]	LCP	Patch array	17.4×2.1×0.15	56-65 (VSWR 2:1)	12	-	~20°	-

ductor receiving port over the low-resistivity chip substrate. To further reduce the coupling, for the on-chip components an understanding of the impact of the process technology, grounding, guarding, shielding, and decoupling is necessary as suggested in [38], while for the in-package antenna, better radiation nulling toward the chip or new AiP structures needs to be devised.

V. CONCLUSION

A CPW-fed quasi-cavity-backed, guard-ring-directed, and substrate-material-modulated slot antenna has been designed, fabricated as an AiP in LTCC, and experimentally verified for highly integrated 60-GHz radios. The novel design concept and sophisticated LTCC process have guaranteed excellent performance of the antenna with an estimated efficiency of 94% at 61.5 GHz.

A mini-review of existing AiP designs for highly integrated 60-GHz radios has been given. Low-loss interconnection between the radio chip and the antenna was identified as one of key issues for the AiP designs. Interconnection using wire-bonding technique was particularly challenging as compared with the flip-chip technique and a new wirebond compensation scheme was proposed to overcome the challenge. It was shown from extensive simulations that a bondwire of 350-μm length could be used. The length of 350 μm was almost a doubled length of the shortest bondwire supported by the current technology and would thus greatly improve the yield of assembly of the chip with the AiP. It was also shown that the AiP gain was reduced by the bondwire but the matching was improved. Furthermore, the risk of the antenna coupling to the radio chip in the AiP was evaluated and found that the coupling from the in-package antenna to the on-chip inductor was lower than 27.5 dB for the worst case.

We are currently working on the other issues such as integration of the AiP with the chipset and realization of an antenna-array-in-package in LTCC. We believe that the antenna design, AiP solution, and wirebond compensation scheme can be used in other technologies such as LCP or at even higher frequency, say, 100 GHz. It is therefore anticipated that the works presented in this paper are useful and inspiring for those interested in the development of highly integrated mm-wave radios for emerging high-speed short-range wireless communications.

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