CONSIDERATIONS FOR COST-EFFICIENT CALIBRATION OF SCALED ADCS

Marian Verhelst, Erkan Alpman, Hasnain Lakdawala
Intel Labs – Radio Integration Research
2111 NW 25th Ave, Hillsboro, Oregon, USA
marian.verhelst@intel.com

Abstract

Observed ADC area and power scaling do not seem to follow the trends predicted using pure technology scaling arguments. A cubic improvement in area and power with gate length is observed in literature, which has been enabled by migration towards more and more capacitor-based ADC architectures, and the introduction of digitally-assisted performance enhancement strategies to overcome component mismatch. This paper assesses these trends, and discusses the most relevant enhancement strategies for mismatch-limited ADCs. Trade-off analysis between mismatch compensation in the analog domain (digitally assisted trimming, possibly in combination with up-scaling) vs. the digital domain (digital post-distortion) is required. The increasing use of digitally enhanced ADC architectures proves to be the main driver for the observed improvement in area and power with scaling.

1. Introduction

The need for increased mobility and portability of computing devices and ever increasing data rate requirements puts more and more stress on the ADC's performance. At the same time cost and battery life issues demand continuous scaling of the ADC area and power consumption and require designs in smaller and smaller (CMOS) technologies. Furthermore increased dynamic range required for modern communication standards also pushes the required dynamic range of the ADCs with scaling. This causes significant noise and matching issues in several key ADC building blocks, as traditional scaling studies predict a power and area flattening or even increase. Nevertheless, a survey of published data indicates that ADC performance does improve significantly over technology. This contradiction is explained by new architecture and design innovations in ADC design that exploit the inherent improvements provided by CMOS technology scaling. These improvements include:

1. Metal finger capacitor (MFC) density as well as MFC matching per pF improved significantly over the last technology generations.
2. The speed of digital gates increases, while their power and area reduce.

Analysis of performance enhancement techniques that exploit these advantages of scaling is necessary to understand the improved performance of ADC implementations and to extrapolate these learnings towards future scaled ADC designs.
This paper starts by deriving the expected ADC area and power consumption trends from pure technology scaling in Section 2. Section 3 makes the comparison with observed trends from survey data on state-of-the-art ADCs of the last decade. Next, Section 4 focuses on several digital enhancement techniques to explain the inconsistency between the theoretical and observed trends. Section 5 finally derives the strategies to incorporate these calibrations in a cost-aware way into ADC design and illustrates this with a design example.

2. Theoretical performance trends in scaled ADCs

2.1 ADC performance limiters

Noise and distortion impose fundamental limits on ADC performance. Their impact on ADC area and power consumption has been covered extensively in literature [1,2,3,4]. This section summarizes these dependencies, which will be used in Section 2.2 to evaluate the impact of scaling.

The conversion accuracy of ADCs is typically expressed in ENOB (effective number of bits), or SNDR (signal-to-noise-and-distortion power ratio):

$$ENOB = \frac{SNDR(dB) - 1.76}{6.02}, \tag{1}$$

$$SNDR = \frac{S}{N_{noise} + N_{mismatch} + N_{non-lin}} \tag{2}$$

Where:

S: signal power at the ADC input, or $V_{sig,rms}^{2}$.

N_{noise}: input referred noise power. Noise appearing in the ADC output signal is caused by a combination of quantization noise, thermal noise, flicker noise and input sampling jitter. Quantization noise, caused by the finite resolution quantization intervals, sets the limit for the maximum achievable SNDR. Practical ADC designs are also limited by thermal noise, which can be characterized by the total integrated noise:

$$N_{noise} = \frac{k_B.T}{C}, \tag{3}$$

With k_B the Boltzmann constant, temperature T and effective input referred noise capacitance C.

$N_{mismatch}$: distortion due to mismatch. As shown in [2,5] matching rather than thermal noise dictates the performance of low resolution ADCs. Mismatch of critical circuit elements has different effects depending on the ADC architecture. In Flash converters the random mismatch among the comparators' (or pre-amplifiers') offset degrades performance, while in a SAR ADCs, the comparator offset is un-important, but the sensitivity to capacitor (and hence radix) mismatch is large. Pipelined ADCs need carefully matched opamps and capacitors to maintain good ENOB, while finally time-interleaved ADCs heavily suffer from mismatch among gain, offset, skew or bandwidth of the time interleaved channels.
This mismatch causes non-linear distortion, affecting dynamic and static ADC metrics, like SNDR, INL and DNL. The latter have to be reduced to a fraction of the LSB to avoid ADC performance degradation. One way to reduce circuit mismatch, is by increasing circuit area. This linear relationship is demonstrated in Eq. (4) and (5) for amplifier differential offset voltage matching (ΔV_{gs}) [5,6,7], as well as capacitor matching (ΔC):

$$\sigma^2(\Delta V_{gs}) = \frac{1}{W.L}\left[A_{V_T}^2 + \frac{A_\beta^2}{4}\left(V_{gs} - V_T\right)^2\right] \tag{4}$$

$$\sigma^2\left(\frac{\Delta C}{C}\right) = \frac{A_C^2}{N.C_{unit}} \tag{5}$$

with $A_{V_{Tl}}$, A_β and A_C technology constants, $W.L$ the transistor area and N the unit capacitor multiplier.
However, due to the deterministic nature of mismatch (unlike thermal noise), opportunities for smarter correction exist. They are the primary focus of this paper and will be covered extensively in Section 4.

$N_{non\text{-}lin}$: device non-linearity. The linearity of an ADC is further degraded by device non-linearity. A well know example of this is the input sampling stage, which is affected due to charge injection and a varying input resistance [8]. The input resistance R_{on} heavily depends on the sampled input voltage V_{in}:

$$R_{on} = dV_{in}/dI = \frac{1}{2\frac{W}{L}C_{ox}(V_{in} - V_T)} \tag{6}$$

To limit the non-linear distortion, the difference in Ron over the signal swing (ΔRon) has to be kept small. Assuming a transmission gate:

$$\max \Delta Ron = \frac{Ron_{\max}}{Ron_{\min}} = \frac{V_{dd} - V_T}{(\frac{V_{dd}}{2} - V_T)/2} = \frac{2k-2}{k/2-1} \tag{7}$$

This parameter however significantly degrades with process scaling, as the ratio $k = Vdd/Vth$ decreases rapidly with technology (trending < 2.5 for some low leakage <45nm CMOS). Luckily, gain boosting and bootstrapping

resolve most of this signal dependency, but at the cost of input bandwidth, area and power [9]. Again, due to the deterministic nature of the impairment, post-distortion techniques have proven to provide additional improvement [8].

Amplifying stages can also be a source of non-linear distortion. Although even order harmonics are typically cancelled out by employing differential circuits, odd order distortion does affect the ADC performance.

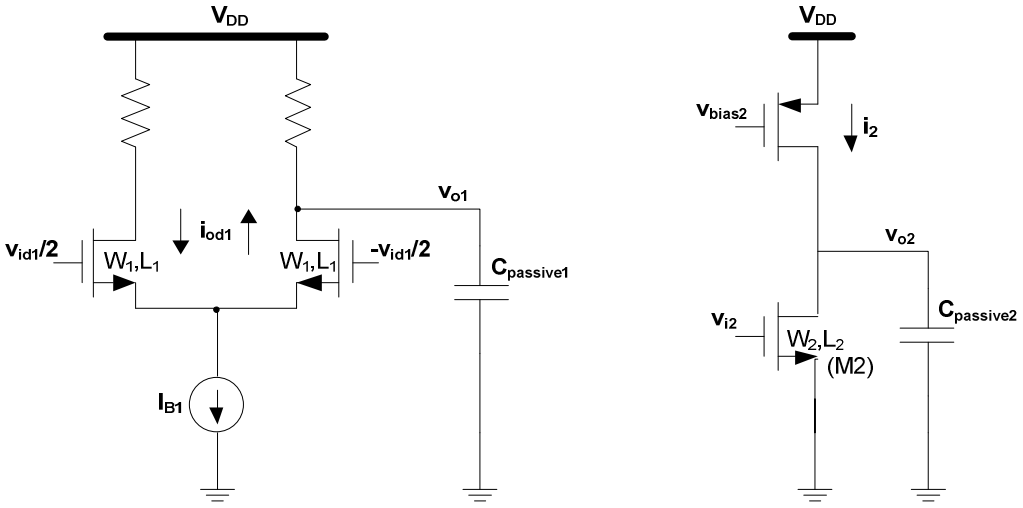
For the differential pair of Figure 1(a), and assuming ideal square law devices, it can be shown that [10]:

$$\frac{i_{od}}{I_B} = x.\sqrt{1-\frac{x^2}{4}}, \quad with\ x = \frac{v_{id}}{(V_{gs1}-V_T)} \tag{8}$$

and hence by approximation:

$$\frac{gm}{gm3} \cong 8.\frac{I_B}{2.K_n.W_1/L_1} = 8.(V_{gs1}-V_T)^2 . \tag{9}$$

with gm being the transconductance, $gm3 = \delta^3 i_{od} / \delta V_{gs}^3$ (third harmonic of the transconductance) and $K_n = \frac{\mu_n}{2} C_{ox}$.



(a) (b)

Figure 1: Representative circuit model of ADC input stage(a) and output stage(b)

2.2 Fixed performance ADC scaling

The noise and distortion formulae of previous section allow assessing the impact of scaling on ADC performance. More specifically this section derives trends in ADC area and power consumption with iso-performance technology scaling. Broader studies of scaling effects in analog and mixed signal circuits can be found in [6,7,11,12,13,14].

The circuits shown in Figure 1 will be used as a representative circuit for an ADC input stage (Figure 1(a)), respectively output stage (Figure 1(b)), driving a

passive capacitor $C_{passive}$. These circuits are relevant for a multitude of recent ADCs based on open loop amplifiers and passive capacitors, like pipelined, sigma-delta or SAR ADCs. While noise and matching constraints mainly impact the input stage, device linearity has to be addressed for both input- and output stage.

Throughout this study, following assumptions are made:

- The square law MOSFET model is used, with the understanding that short channel effects limit the accuracy of this model in scaled technologies. However this assumption allows a first order calculation to reveal trends.
- L scales with technology. Design rules of deep submicron technologies do not allow long channel devices without severe area and leakage penalties. The scaling factor of L per technology generation will be denoted s_L(≈0.7).
- Voltage scaling is pursued less aggressively in latest technology generations. Leakage concerns cause the threshold voltage to be almost flat. As a result V_{DD} scales at a slower pace to keep sufficient voltage overdrive. Therefore, a voltage scaling factor s_V, different from s_L, is used. Recently this factor has been trending towards $\sqrt{s_L}$ or even less when different supply voltages are used for analog and digital blocks.
- Gate t_{ox}, and as a result C_{ox} has not been keeping up with feature scaling due to gate leakage concerns. Survey data [15] shows C_{ox} scaling of $\sim 1/\sqrt{s_L}$ (towards $1/s_L$ for high-k gate). Interconnect t_{ox} scales with $1/s_L$.
- Absolute matching coefficients A_{VT} and A_C (Eq. (4) and (5)) improve with every new technology generation. Lately this improvement rate has been trending around $\sqrt{s_L}$ [15,16]. A_β, which does not see similar improvements, has not been taken into account in this study, resulting in a slightly optimistic (smaller area, power) outcome.
- A passive metal finger capacitor (MFC) capacitor is assumed. MFC capacitor density scales with technology as $\sim 1/s_L$ [16].
- The input stage operates in Class A, or $I_{B1}/i_{od1} = \text{constant}$. This implies that $(V_{gs} - V_T)$ cannot scale faster than the input signal swing, or s_V.
- Iso-bandwidth (conversion rate) scaling is pursued in all scenarios (unless other iso-performance requirements force the bandwidth to be larger). This poses the following constraints for the representative circuits:

  Input stage (linear settling): $$\frac{gm_1}{C_{load1}} = \text{constant} \quad (10)$$

  Output stage: (slew rate limited): $$\frac{C_{load2}.\Delta(v_o)_{\max}}{i_2} = \text{constant} \quad (11)$$

Table 1 shows the effect on the most important circuit parameters when scaling device length (~s_L) and supply voltage (~s_V) under different scenarios.

Iso-(device-)linearity scaling

In a first scenario, an iso-linearity scaling of the input stage is pursued, assuming a constant load capacitor $C_{passive1}$. Only the intrinsic non-linearity of the transistor device is considered. Non-linearity due to mismatch will be covered later (iso-matching). As can be derived from Eq. (9), this linearity is maintained as long as the overdrive voltage $V_{ov} = (V_{gs1} - V_T)$ scales proportional to v_{id}. This is realized by scaling both voltages with s_V, resulting in a device width scaling:

$$W \sim \frac{I.L}{C_{ox}.(V_{gs} - V_T)^2} \sim \frac{s_I.s_L.\sqrt{s_L}}{s_V^2}. \qquad (12)$$

Iso-(device-)linearity scaling of the output driver stage (Figure 1(b)) requires both $(V_{gs} - V_T)$ of M2, as well as the voltage drop over the output stage bias transistor to scale with s_V. Assuming constant bandwidth, bias current can be decreased according to Eq. (11). As a result, iso-linearity enforces similar scaling to the output driver stages as derived for the input stage (Eq. (12)).

As can be seen from Table 1, iso-(device-)linearity scaling (without other noise or matching requirements) results in an almost perfect scaling with technology, where both area and power scale down with a factor s_L to s_L^2 (using $s_V \sim \sqrt{s_L}$).

From this observation, linearity does not seem to be affected by scaling if the input swing range is allowed to be reduced with the input supply, predicting ever decreasing area and power numbers for scaled technologies. However, system, noise and matching requirements will make it harder and harder to scale the input swing with s_V, which will be reflected in an area and power penalty as seen in the following scenarios.

Table 1: Effect on design parameters, area and power consumption of the input stage reference circuit of Figure 1(a) under iso-performance scaling.

Parameter	Iso-linearity	Iso-noise	Iso-matching	Iso-SNDR
L	s_L	s_L	s_L	s_L
V_{dd}	s_V	s_V	s_V	s_V
$(v_o), (v_i)_{max}$	s_V	s_V	s_V	s_V
$C_{passive}$	1	s_V^{-2}	s_L	s_V^{-2} (noise)
I	s_V	s_V^{-1}	$s_L^{-3/2}$ (passive load)	$s_L^{-3/2}$ (linearity)
W	$s_L^{3/2}.s_V^{-1}$	$s_L^{3/2}.s_V^{-3}$	s_V^{-2} (offset)	s_V^{-2} (matching)
Power	s_V^2 ~s_L	1	$s_L^{-3/2}.s_V$ ~s_L^{-1}	$s_L^{-3/2}.s_V$ ~s_L^{-1}
Area (active)	$s_L^{5/2}.s_V^{-1}$ ~s_L^2	$s_L^{5/2}.s_V^{-3}$ ~s_L	$s_L.s_V^{-2}$ ~1	$s_L.s_V^{-2}$ ~1
Area (passives)	s_L	$s_L.s_V^{-2}$ ~1	s_L^2	$s_L.s_V^{-2}$ ~1

Green formulae assuming $s_V \sim \sqrt{s_L}$.

Iso-thermal noise scaling:
To keep the signal-to-thermal-noise-ratio constant in a scaled technology, assuming the input swing scales proportional to the supply, circuit noise has to be suppressed with ~s_V^2. As a result, the passive capacitive load $C_{passive}$ has to be scaled up with the same factor. To account for the larger *gm* requirement due to this load under iso-bandwidth constraints and only allowing limited overdrive voltage scaling to maintain Class-A operation, this requires approximately flat device width scaling. Table 1 shows the impact on area and power consumption.
It has to be noted that flicker noise, important for low frequency ADC designs has been neglected here. Flicker noise limited designs can use architectural solutions like correlated double sampling or need to keep input device sizes large to limit the flicker noise.

Iso-matching scaling
In an iso-matching scenario the amount with which active and passive circuits can scale is limited, and directly tied to the improvement over technology of A_{VT} and A_C (Eq. (4) and (5)). Additionally, the scaled supply voltage and input swing increases the threshold voltage matching requirement for the active devices with s_V. The decrease in required *gm* (smaller load) does however not allow significant power savings due to the Class A operating requirement. The design is no longer iso-bandwidth, but is forced to increase bandwidth with 's_L^3' at a larger power cost. As shown in Table 1, area is flat for active devices, passive area decreases due to improved capacitor density and matching.
Note that a purely passive load is assumed. An active load (with matching requirements, like in current steering DACs, or CT ΣΔ ADCs) scales slower, resulting in a ~$1/s_L^{3/2}$ times higher power consumption.

Iso-SNDR
A good ADC implementation will always use all excess margin in terms of every performance limiter: device non-linearity, noise and matching. As result, when such a design has to scale down, performance across all three has to be improved simultaneously. The last column in Table 1 shows the result on the circuit's area and power consumption for such an iso-SNDR scaling (iso-linearity + iso-noise + iso-matching). The size of the passives will typically be determined by noise, and of the actives in many designs (e.g. flash) by threshold voltage matching, while the current is set based on the linearity constraint of Eq. (9), taking the increased *W* due to matching into account. Assuming $s_V \sim \sqrt{s_L}$, this scenario results in iso-bandwidth scaling as well.

Conclusion
An interesting observation from Table 1 is the difference in scaling between active and passive devices. While active devices seem to suffer less from scaling in a noise-limited scenario, passive devices scale better under matching constraints. This relates to the ongoing shift of ADC designs towards

oversampling implementations (relying more on active devices) for noise limited designs, while more passive capacitor based designs (like SAR ADCs) gain popularity for low SNDR requirements (matching limited [17]). However, as can be concluded from Table 1, no significant overall area or power improvements can be expected from pure technology scaling alone under fixed performance constraints. *The ADC area and power seems solely dependent on and tied to its SNDR requirement.* Due to the slowed down voltage scaling $s_V \leq \sqrt{s_L}$ both are more or less flat, or slightly increasing over generations. If s_V would have maintained his old trend $\sim s_L$, power would have scaled better at the cost of additional area. The increasingly common trend of using of dual supplies for the ADC, with the analog supply being higher and scaling slower than the digital supply helps in terms of area scaling. Next section will compare these trends with survey data from recent ADC implementations.

3. ADC area and power survey

Based on the survey data from [18] an assessment can be made about the actual trend of area and power consumption of iso-SNDR ADC implementations over the past decade. The power consumption scaling per calendar year is studied extensively in [17]. The study reveals a significant scaling divergence between high SNDR ADCs (>75dB SNDR), limited by thermal noise (technology), and lower SNDR ADCs, which are mismatch limited.

The remainder of this paper will focus on trends for mismatch limited ADCs, as they contain the majority of recent ADC designs. This section will investigate the trend in area scaling, as well as quantify the area and power scaling over technology generations.

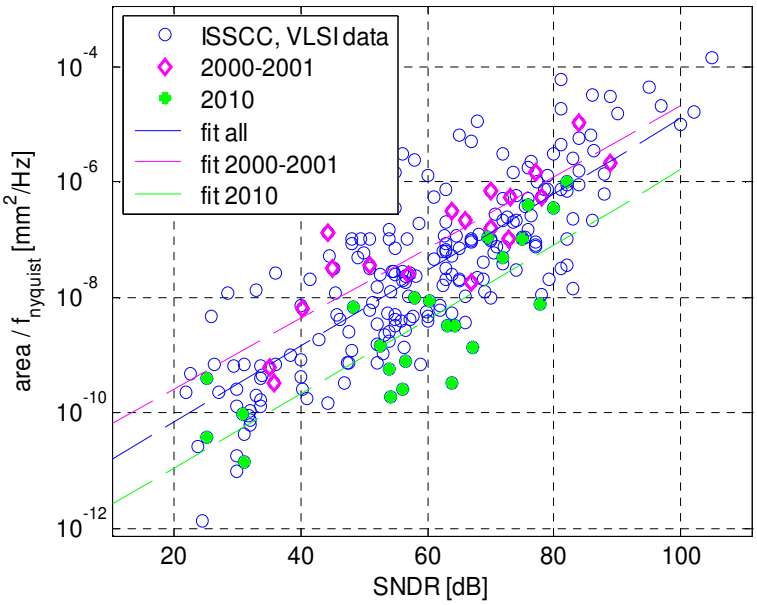


Figure 2: ADC performance data (ISSCC 2000-2010, VLSI Circuit Symposium 2000-2010). Area efficiency plotted in function of SNDR.

Figure 2 shows an analysis of all ADC implementations presented at the IEEE International Solid-State Circuits Conference (ISSCC) and the VLSI Circuit Symposium during the last decade [18]. In this plot, the area efficiency (area divided by the Nyquist sampling rate $f_{nyquist}$) is plotted in function of the achieved SNDR. The oldest (2000-2001) and most recent (2010) implementations are highlighted. A first observation is the large spread of the data around their best linear fit, which can be explained by different performance metrics targeted by the various ADC designs, not all reflected in this drawing: area, power, bandwidth, or a combination of them.
However, due to the abundance of data, interesting conclusions can still be drawn from averaged data through linear regression models. Figure 2 shows linear fits constructed based on all mismatch limited ADCs (SNDR<75dB) of different publication years. Based on these lines, a clear improvement of area efficiency from 2000 to 2010 can be identified. This trend is also observed in three generations of similar sigma-delta ADCs at Intel in scaled technologies (Figure 3) [19].

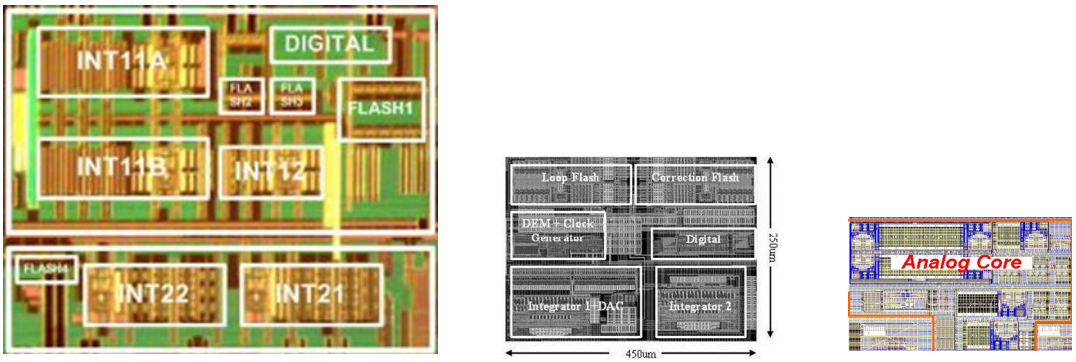


Figure 3: Three generations of similar delta-sigma ADC implementations, demonstrating the ongoing area improvement over technology generations.

This observation is contradictory to the theoretical area scaling effect derived in previous section. One partial explanation is a shift toward passive capacitor-based ADC designs, which rely on passive, rather than active device matching. As shown in Table 1, these devices still scale quite well over technology.
Figure 4 confirms this trend: The fraction of SAR ADC implementations significantly increased over the past years. Also, sigma-delta (SD) and pipeline ADCs, relying heavily on passive capacitors as well, remain popular.
However, as derived in Table 1, this design shift can only (partially) explain an improvement in area efficiency. Improvements in power efficiency (power consumption divided by the Nyquist sampling rate $f_{nyquist}$) are not expected from

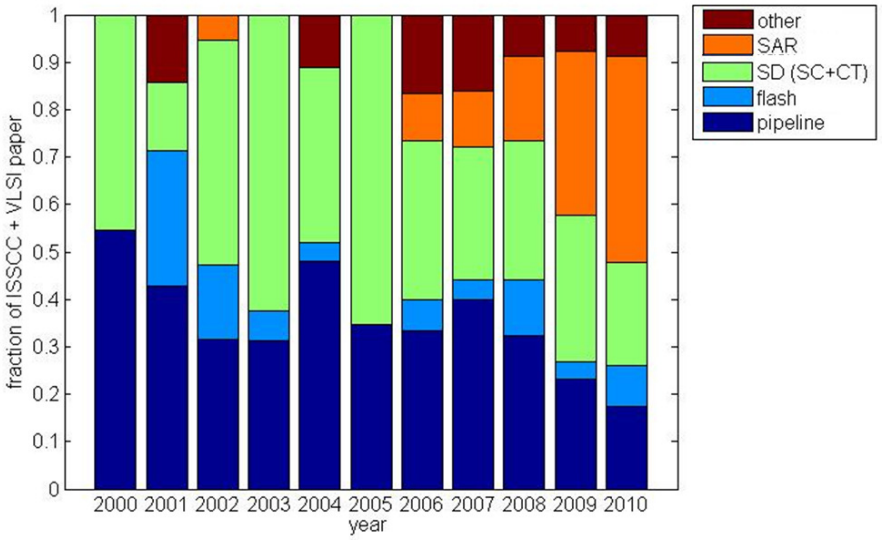


Figure 4: Fraction of ADC architectures published in ISSCC and VLSI in different calendar years.

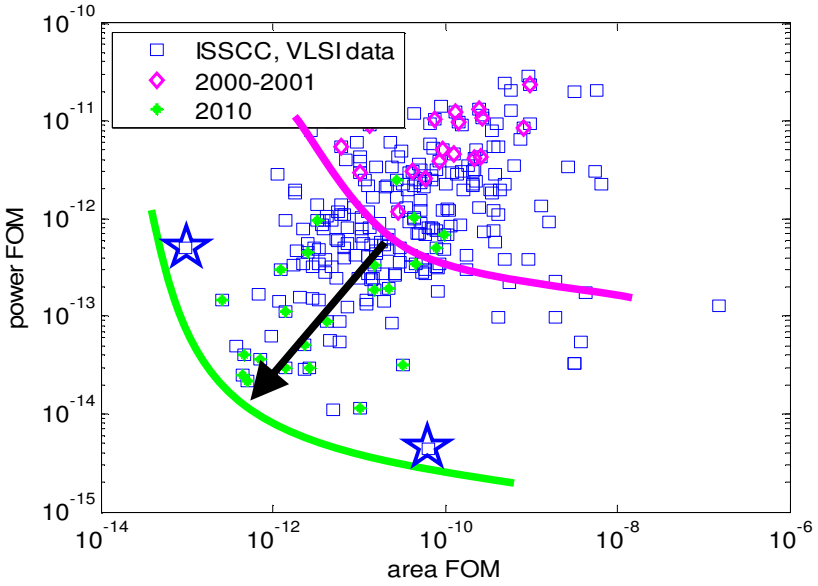


Figure 5: Power figure-of-merit vs. area figure-of-merit (FOM).

the scaling study of Section 2. Figure 5 however shows that the power efficiency of ADC designs demonstrates a similar decrease over the last decade. This scatter plot visualizes the power versus area FOM (figure-of-merit):

$$power\ FOM = \frac{P}{f_{nyquist}.2^{ENOB}}, \quad area\ FOM = \frac{A}{f_{nyquist}.2^{ENOB}} \tag{13}$$

The scattered data can again be attributed to different design optimization metrics pursued. A clear power-area trade-off locus can be observed, which steadily improves over the years for both area and power.

A similar trend can be observed when computing the expected area and power consumption of a iso-SNDR ADC in different technology generations: Based on a linear fit of both area and power in function of SNDR over the ISSCC/VLSI survey data for every different CMOS technology generation between 600nm and 65 nm (not enough data points available for 45nm), the area and power consumption of a typical comms ADC, targeting 60dB SNDR, is predicted. Figure 6 plots the result: a perfect scaling with s_L^2 for both metrics…

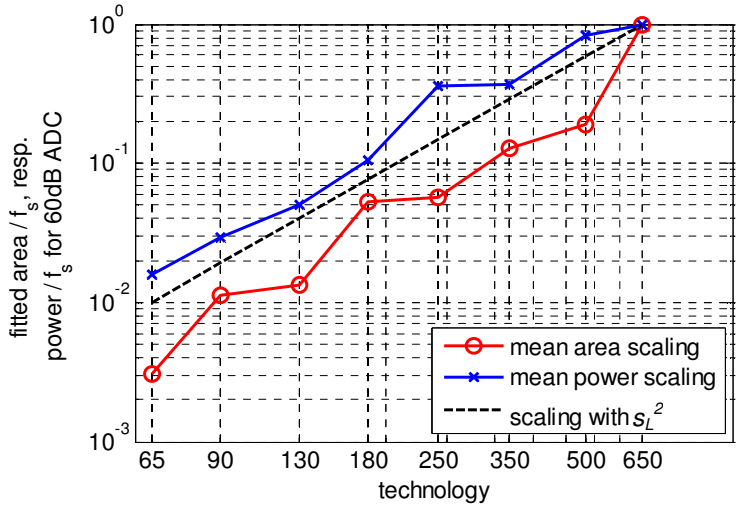


Figure 6: Predicted power consumption and area for 60dB SNDR ADC over technology generation (normalized to the 650nm data point (1um²/Hz, 9.5nW/Hz)).

To understand why this perfect scaling with technology is possible, despite the contradictory theoretical derivation of Table 1, let's look at two interesting data points in Figure 5: the most power efficient and most area efficient design up to date, indicated with the 'stars':

The most power efficient ADC design, described in [20] is a *4.4fJ*/conversion step charge redistribution (SAR) ADC, heavily relying on metal-plate capacitor matching.

The most area efficient ADC design, described in [21] is a *0.01mm²* flash ADC using minimum-size input devices in 65nm. To compensate for resulting non-linearities and offsets in the comparator and track-and-hold, the ADC employs digital compensation techniques, both calibrated during startup.

These two examples beautifully illustrate the two most important strategies followed in many of the ISSCC / VLSI survey designs to overcome mismatch limitations and maintain aggressive area and power scaling over technology:

1. Rely on metal-plate capacitor matching instead of device matching whenever possible (see also Figure 4).
2. Add digital enhancements to the ADC to boost performance.

Although a majority of the recent ISSCC / VLSI ADC implementations heavily relied on digital enhancements, only few of them demonstrated these in actual silicon. As a result, their true power and area cost is often not taken into account

in the reported performance metrics. The remainder of this paper will focus on various digital enhancement strategies for ADCs, as well as quantify their benefits and penalties. This information helps the ADC designer to make smart design choices to optimize *overall* area and power of analog *plus* digital.

4. ADC performance through digital enhancements

Designers have been using digital enhancements for many decades to boost the ADC performance at a reduced power / area cost compared to traditional up-scaling [22,23]. Analog power / area is saved, at the expense of more digital gates. Finding the best trade-off between the two is not straightforward and requires thorough understanding of the impact of these enhancements.

This section will revise different digital enhancement techniques and their influence on both analog and digital performance metrics. This data can be used to understand the s_L^2 scaling trends seen for ADC area and power consumption, and to investigate whether this trends is expected to continue in the future.

A well-known and thoroughly studied digital enhancement technique for overcoming SNDR limitations for thermal noise limited ADCs is oversampling [24]. This section will therefore solely focus on enhancements for mismatch limited ADCs.

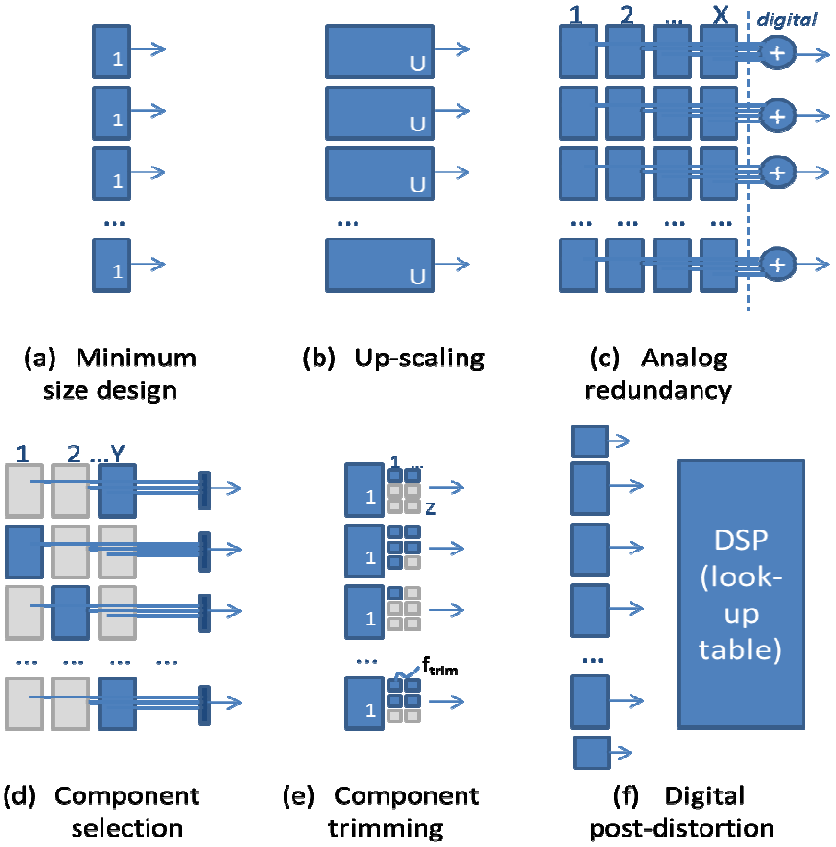


Figure 7: (b) – (f): Enhancement techniques to improve matching performance over the minimum size, thermal noise-limited, baseline design (a)

4.1 Non-digital enhancements

Figure 7 gives a classification of various strategies to improve matching performance of circuit components, and by extension of ADCs.

The baseline, reference design which has to be improved is drawn in Figure 7(a). It consists of a set of *N* mismatched circuit components, which can be either active or passive devices, depending on the ADC under study. E.g. in a Flash ADC, these could be *N* pre-amplifiers which require careful voltage offset matching; While in a SAR ADC these could be *N* capacitors. In this reference design of Figure 7(a) these *N* components have the minimal size required to meet the signal-to-thermal-noise-ratio constraint (~ target SNDR). We denote this size as *'1'*. As shown in Table 2, such an ADC would consume a reference (=*'1'*) analog area A_{analog} and power P_{analog}, and does not need any digital area $A_{digital}$, power $P_{digital}$ or calibration time T_{cal}. Its performance is limited by mismatch, having a component variation of $\sigma_{(a)}$ and the resulting *SNDR* is again normalized to *'1'*.

A first way to improve matching between the fundamental circuit components of the reference design of Figure 7(a) in a fixed silicon technology is by up-sizing the individual circuit components. Up-scaling every device area with a factor *U*, as shown in Figure 7(b) improves the component matching and reduces their variance with *U* (Eq. (4) and (5)). As a result, the 'voltage accuracy' improves by $\sqrt{U}$, or an SNDR (power ratio) improvement of a factor *'U'* is achieved at the cost of a *'U'* times analog area and power increase (See Table 2).

From the discussions earlier in this paper, it is clear that this is not the way mismatch and non-linearity are overcome in modern ADCs. The oldest calibration techniques to improve ADC matching and linearity are based on analog feedback (eg. Opamps). Drawback of these analog feedback loops are however the requirement for the circuit to remain active during the whole circuit operation, as well as the very stringent gain-bandwidth (*GBW*) and linearity requirements for the feedback opamps and reproducibility and yield concerns. Designing under these requirements becomes problematic in scaled technologies and has a detrimental impact on system power consumption and area. This trend, together with the ever decreasing cost of digital gates over technology [2], pushes designers towards digital performance enhancements to improve performance will a smaller area / power penalty. Three techniques will be described: *digitally assisted analog selection (including analog redundancy)*, *digitally assisted analog trimming* and *digital post-distortion*.

Table 2: Costs and SNDR improvement of enhancement techniques. Last column shows the effect of technology scaling on every enhanced ADC (assuming $s_V \sim \sqrt{s_L}$)

	A_{analog}	$A_{digital}$	P_{analog}	$P_{digital}$	T_{cal}	**SNDR** *(defined by Eq. (2))*	**Technology effect on (P ; A)**
Min size design	*1*	*/*	*1*	*/*	*0*	*1*	s_L^{-1} ; *1* *(Table1)*
Upscaled design	*U*	*/*	*U*	*/*	*0*	*U*	s_L^{-1} ; *1* *(Table1)*
Analog redundancy	*X*	*small, ~log2(X)*	*X*	*small, ~log2(X)*	*0*	*X*	s_L^{-1} ; *1* *(Table1)*
Component selection	*Y*	*minimal (at startup)*	*>1*	*minimal*	*~Y*	$\frac{\text{erfcinv}(\text{erfc}(3)^{1/Y})}{3}$	s_L^{-1} ; *1* *(Table1)*
Component trimming	$1+Z/2.f_{trim}$ $(\cong 1+3.\sigma_a)$	*minimal (at startup)*	*~1* $<<1+6.\sigma_a$	*minimal*	*~log2(Z)*	$\sim 6.\sigma_a / f_{trim}$ *(=Z)*	s_L^2 ; s_L^2 *(Eq. (16))*
Digital post-distortion	*>>1 (e.g. 1.2)*	*significant (e.g LUT)*	*>>1 (e.g. 1.2)*	*significant (e.g LUT)*	0 (if ran in background)	↑↑ *,depends on impairment, f(an. redund., LUT size)*	$s_L^{3/2}$; s_L^2 *(digital scaling)*

4.2 Analog redundancy and digitally assisted analog selection

A straightforward approach to avoid designing accurate analog components is to create analog redundancy, and average the outcome of the redundant, inaccurate (min-size) elements in the *digital* domain (shown in Figure 7(c)) to enhance performance. This is e.g. used in Flash convertors to reduce sensitivity to offset voltage, by having several comparators evaluate the same input voltage and use their output in a voting mechanism [25]. By statistically averaging, the designer can get away with small devices.
As shown in Table 2, increasing the number of redundant devices by a factor of *X*, will only reduce equivalent device mismatch standard deviation by $\sqrt{X}$, hence improving *SNDR* by *X*. A small area and power penalty in the digital domain is paid, to implement the averaging. As a result, analog redundancy shows a similar, or even slightly worse performance cost compared to classical up-scaling. Similarly, Figure 8, which plots the SNDR improvement in function of area increase, shows an identical SNDR-area relationship for device up-scaling and analog redundancy, which both linearly reduce the component variation with increasing area (see distribution histograms in Figure 8).

Pure analog redundancy is hence not a good strategy to enhance ADC performance. It can however be extended with digitally assisted analog component selection, which is much more interesting [26].
This technique (Figure 7(d)) aims at digitally selecting the best devices out of the pool of redundant analog components. It has been applied to Flash converters to reduce input offset voltages, where for an *N*- bit converter, all 2^N

comparator (+preamplifier) stages are replaced by *Y* identical copies of the same component. During a training phase, the best matching comparator (smallest offset) is selected out of every pool of *Y* comparators [26,27].
This "selection step" reduces the variation of the remaining components much more effectively than adding redundancy. It can be derived that the $3.\sigma_{(d)}$ spread (determining *SNDR*) after component selection in scheme (d) is reduced from the spread $3.\sigma_{(a)}$ of the reference design of scheme (a) as:

$$3.\sigma_{(d)} = \text{erfcinv}(\text{erfc}(3)^{1/Y}).\sigma_{(a)} \quad (14)$$

with erfc and erfcinv the (inverse) error function. The resulting "peaking" distribution is depicted in Figure 8.
Power savings are more significant, than area savings, since power is saved due to smartly shutting down the non-selected components. However, depending on how the non-selected components are gated, they might still load the input stage, resulting in some additional power consumption compared to the baseline design. The overhead of the off-line calibration required to implement this approach can have significant impact on the system and should not be neglected. Contrary to previous solutions (Figure 7(a)-(c)), calibration time (*Tcal*) will have to be foreseen in the manufacturing environment or when powering up the device to run the selection procedure. Depending on the configuration stability, this could however be a one-time tune-and-store process.

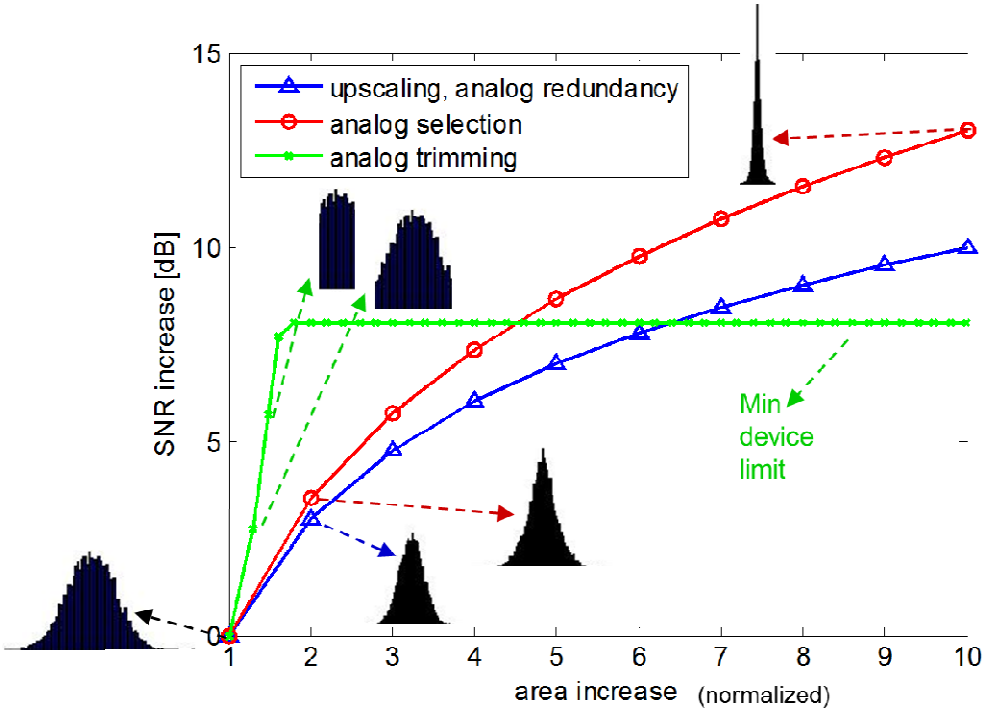


Figure 8: Area and SNR impact of different performance enhancement techniques, normalized to the thermal noise-sized design (1,0). Assumptions for baseline design: 7% mismatch, $f_{trim,min}$ = 1/10, trimming overhead = 1/10.

4.3 Digitally assisted analog trimming

While analog component selection allows reducing ADC power consumption for a fixed SNDR drastically, it does not come with a significant area breakthrough. Even more importantly though, as shown in the last column of Table 2: *it does not allow to break with the traditional scaling laws* presented in Table 1 and hence does not explain the observed scaling of Figure 6. The enhanced designs (b)-(d) don't scale any better than the reference case (a)! More interesting it is however to trim, instead of selecting components [28,29,30].

In component trimming (Figure 7(e)), component variation is reduced by post-manufacturing inserting or removing small fractions of the component. A well-known example is trimming capacitor values by connecting or disconnecting small capacitor to the main capacitor [30]. Similar trimming can be done to match current sources, *gm*, etc. [28,29]. As shown in Figure 8, this kind of trimming reduces the spread of the component drastically, since it cuts the tails of the component variation distribution. Both the amount of trimming steps *Z*, as well as the size of every trim step required depends on the original variation of the baseline device ($\sigma_{(a)}^2$) and the target *SNDR*. All trim steps together should cover the $6.\sigma_{(a)}$ spread of the original component. Or, defining f_{trim} as the fraction of the trim step size to the original component size:

$$(Z+1).f_{trim} = 6.\sigma_{(a)} \tag{15}$$

The resulting SNDR will then show an improvement with approximately a factor *Z* ($\approx 6.\sigma_{(a)} / f_{trim}$) over the baseline design. This of course comes at a small area cost due to the component selection switches and interconnect overhead. The power cost is often negligible, since the extra load of the switches can be incorporated in the design.

Certainly the most important observation is that digitally controlled trimming decouples device sizing from the target *SNDR,* since it is tuned post-manufacturing to the required *SNDR*. As a result the area and power cost is nearly independent of *SNDR*, as seen in Figure 8 by the steep increase in *SNDR* at almost no area cost. This would lead to the conclusion that minimum sized components (thermal noise limited) can in theory be used as trimmable devices. This however does not hold in practice due to two reasons:

1. The size of a trim component cannot be made arbitrarily small. Technology limits the trim step f_{trim}. As a result, the maximally achievable SNDR improvement for a design depends on the original mismatch $6.\sigma_{(a)}$ and the best achievable trim ratio f_{trim}.
2. The component selection area and power overhead is not negligible for close to minimum size devices. To assess this, let's look into a representative circuit, which can be used as a*"fundamental unit of digital trimming"*: a digitally controlled switch, plus a passive element (R_{trim} or C_{trim}) (Figure 9). The overhead of using this passive element as a trim

component are the parasitics of the switch, which load the component under trim, consume area and power and diminish the effect of the trim impact. In order to keep the overhead marginal and ensure a predictable impact of the trim, the value of the passive trim component should be significantly (e.g. 5X) larger than the parasitic of the switch.

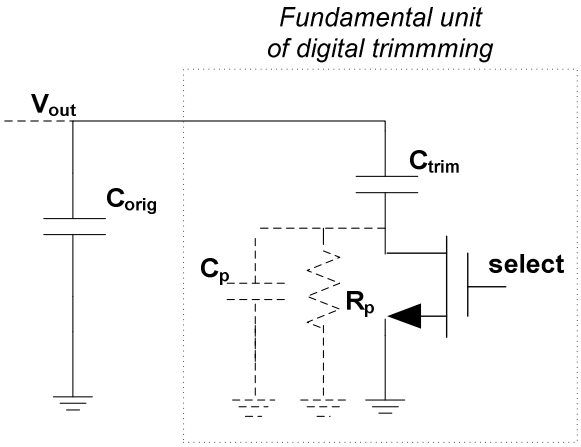


Figure 9: Fundamental unit of digital trimming

As a result, these switch parasitics (C_p or R_p) determine the maximal achievable SNDR improvement and hence the sizing and power consumption of the original component under trim. Since switch parasitics, and hence $f_{trim,\min} \sim C_p, R_p$, heavily depend on technology, this directly links the design cost to achieve a certain *SNDR* to the silicon technology used. Parasitics are moreover characterized by following scaling rules [31]:

$$C_{p,switch} \sim W.L \sim s_L^{\,2} \tag{16}$$

$$R_{p,switch} \sim L/W \sim 1 \tag{17}$$

Interconnect parasitics follow different scaling rules [31]:

$$\begin{aligned} C_{p,interc} &\sim \frac{W.L}{t_{ox}} \sim s_L && \text{(local interconnect)} \\ &\sim 1 && \text{(constant length interconnect)} \end{aligned} \tag{18}$$

$$\begin{aligned} R_{p,interc} &\sim L/(W.H) \sim 1/s_L^{\,1/2} && \text{(local interconnect)} \\ &\sim 1/s_L^{\,3/2} && \text{(constant length interconnect)} \end{aligned} \tag{19}$$

The relationship between $f_{trim,\min}$ and C_p together with Eq. (16) justifies a scaling of the ADC design cost (area and power) with $s_L^{\,2}$ over technology: The intrinsic accuracy with which components can be trimmed in a certain technology improves by $s_L^{\,2}$, which *does* explain the observed trends of Section 3. This conclusion holds for C-based trimming, and as long as interconnect parasitics do not dominate. Since interconnect parasitics start to become more and more relevant relative to device parasitics, a slowdown of this area and power scaling

trend is to be expected. It is also clear that R-based trimming is not favorable in advanced silicon technologies.
Once the trimming accuracy limit of a certain technology is reached, the only way to increase *SNDR* further in the analog domain is to increase original device sizes. This up-scaling results in a relative decrease of f_{trim}. It however again has a linear effect on area and power consumption. An alternative to stick with minimal size devices is to increase SNDR in the digital domain by using digital post-distortion when technology prevents further trimming.

4.4 Digital post-processing

Due to the decreasing cost of digital gates over technology generations, digital post-distortion (Figure 7(f)) to boost ADC performance becomes less and less costly [2]. A multitude of digital post-distortion techniques for ADCs have been developed and published over the past decade and are all very diverse in nature. The two most common, but very distinct, classes of digital post-processing are "*look-up-table (LUT)"-based* [32] and *filter-based* [8]. The former corrects analog impairments by using the bare ADC output as the index to a table look-up containing the corrected sample data. This approach is very straightforward and easy to implement, but only suitable for low SNDR (small number of bits) ADCs. It is also not well suited for on-line calibration.
Filter based correction eliminates impairments by sending the bare ADC output data through a digital filter. The filter coefficients are adapted (on-line or off-line) based on the detected actual ADC impairments. The type of filter required (linear vs. non-linear, order, length, etc.) is heavily dependent on the nature of the impairment(s) under correction. E.g. offset and gain mismatches between channels in a time interleaved ADC can simply be corrected with a linear, single-tap 'filter', while skew or non-linearity correction of the same ADC needs complex higher order implementations [8,33]. These types of adaptive filters are especially attractive in medium to high SNDR ADCs, where LUT approaches become infeasible and where the cost of extra digital gates is relatively low compared to the analog power. Moreover, these filters lend themselves perfectly to on-line training and background adaptation, hence eliminating the need for (and cost of) startup calibration time T_{cal}, but only if initial settling transients are acceptable before achieving full performance. While very distinct in nature, digital post-distortion techniques have several key characteristics in common: They are all able of achieving very large SNDR improvements, and allow close-to-minimum size ADC front-end designs. Like in the case of digitally assisted trimming, this partly decouples component sizing, area and power requirements from the target SNDR, explaining the observed improvement over technology.
However, unlike in the case of digitally assisted trimming, this comes at a significant (digital) area and power penalty. Additionally, a penalty in the analog domain has to be paid as well: Almost all forms of digital post-distortion require analog overhead to allow correction in the digital domain. This overhead is

necessary to ensure that no unrecoverable information gets lost when digitizing the data. Table 3 lists the required overhead for common digitally corrected ADC impairments. The amount of analog overhead area and power consumption due to this depends on the (3-σ value of the) expected impairment, but can typically be estimated to be between 10 and 20%.
It finally has to be noted that sometimes digital power and area are non-existent if leveraged from other DSP blocks already present in the system [34].

Table 3: Analog overhead required for digital impairment correction

Impairment type	Required analog overhead
Offset	ADC dynamic range + max offset
Gain error	ADC dynamic range * max gain error
Radix mismatch (e.g. in SAR)	Use nominal radix <2, to ensure max radix ≤2. Typically radix ≅1.7
Linearity correction	Ensure worst case DNL still within spec (smaller nominal DNL)

5. Cost-aware calibration design

5.1 Cost-aware enhancement selection

Previous section gave an overview of strategies for digital ADC enhancement. The effect of every strategy on the area, power consumption, the calibration time, as well as the SNDR was discussed. As shown, the various strategies improve component matching, which in its turn allows to scale down analog component sizes, and hence area and power consumption. However, often a penalty on either the digital area, power or the calibration time has to be paid. As a result, the selection of the optimal strategy for a particular ADC design is not straightforward. It requires a careful analysis of the expected analog savings due to the enhancement compared to its cost. Depending on the relative importance α_i of area vs. power vs. calibration time in the overall cost factor K of the particular design a different solution will be preferred.

$$K = \alpha_1.(A_{analog} + A_{digital}) + \alpha_2.(P_{analog} + P_{digital}) + \alpha_3.T_{cal} \quad (20)$$

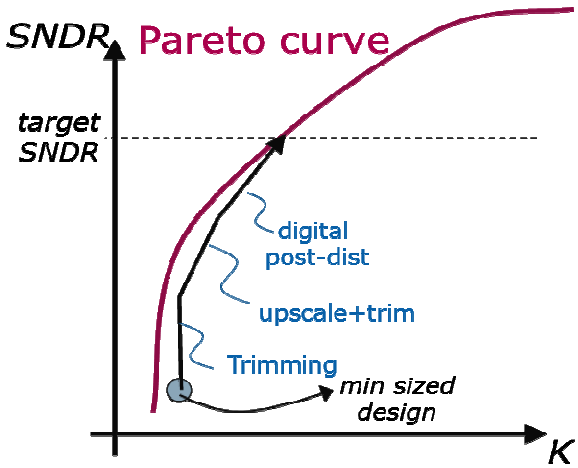


Figure 10: Optimizing K under SNDR constraint by successively applying performance enhancement with largest sensitivity.

Often a combination of different strategies offers the best trade-off. This "strategy selection / combination" problem can be treated as an optimization problem. Starting from a minimum sized design, without any enhancements, the overall cost factor *K* has to be minimized under an *SNDR* constraint by successively applying several enhancement strategies (Figure 10). At every point in this optimization process, the enhancement strategy *x* with the highest SNDR vs. cost sensitivity $S_{SNDR,K,x}$ should be applied first until the target SNDR is achieved:

$$S_{SNDR,K,x} = \frac{\Delta SNDR / \Delta x}{\Delta K / \Delta x}, \text{applying enhancement strategy } \Delta x \tag{21}$$

This sensitivity is a measure of the expected cost investment to achieve SNDR improvement with this strategy.

As can be seen from Figure 8 and Table 2, up-scaling and analog redundancy have and equal SNDR-cost sensitivity of '1'. Analog selection demonstrates a larger sensitivity, which is however still far off from the sensitivity of digitally assisted trimming, being ~2/f_{trim} considering area cost and even larger when taking power cost into account. However, the benefit of this large SNDR sensitivity to trimming is only limited, since technology restricts achievable f_{trim}. When more SNDR improvement is needed, additional up-scaling can however be combined with trimming, resulting in a joint SNDR-cost sensitivity of:

$$S_{up-scale+trim} = \frac{6.\sigma_{(a)} / \sqrt{U} / f_{trim}.U}{(U-1) + 3\sigma_{(a)} / \sqrt{U}} \sim 6.\sigma_{(a)} / \sqrt{U} / f_{trim} \quad (\text{for large } U) \tag{22}$$

with $\sigma_{(a)}$ and f_{trim}, resp. the component standard deviation and trim-ratio of the minimum size baseline design. This sensitivity decreases when *U* gets larger.

The SNDR-cost sensitivity of digital post-distortion cannot be put into formulae that easily, as it heavily depends on the type (LUT vs. filter) and complexity of the implemented enhancement. Moreover, the sensitivity will in general be larger for complex, high resolution ADCs, since the area and cost adder will be relatively smaller compared to the overall ADC area and power consumption [2]. This sensitivity should be compared to the (decreasing) $S_{up-scale+trim}$, to determine at what point in the design it no longer makes sense to add additional trimming (in combination with up-scaling) and post-distortion should be deployed instead due to its larger sensitivity.

5.2 Practical example: TI SAR ADC calibrations

In this section, the cost *K* of a time interleaved (TI) successive approximation (SAR) ADC will be optimized by applying different enhancement strategies. The performance of the *7-bit, 2.5GHz 45nm* TI SAR ADC [35] (architecture in Figure 11), is severely impacted by mismatch of the following parameters:

- *Capacitor values* within every ADC: The linearity of a SAR ADC depends on the ADC's capacitor ratios, which have to be equal to 2.

- *Offset and gain* mismatch: Different (comparator) offset voltages and gains for the different TI channels also cause spurious tones.
- *Sampling skew* mismatch between the different TI channels.

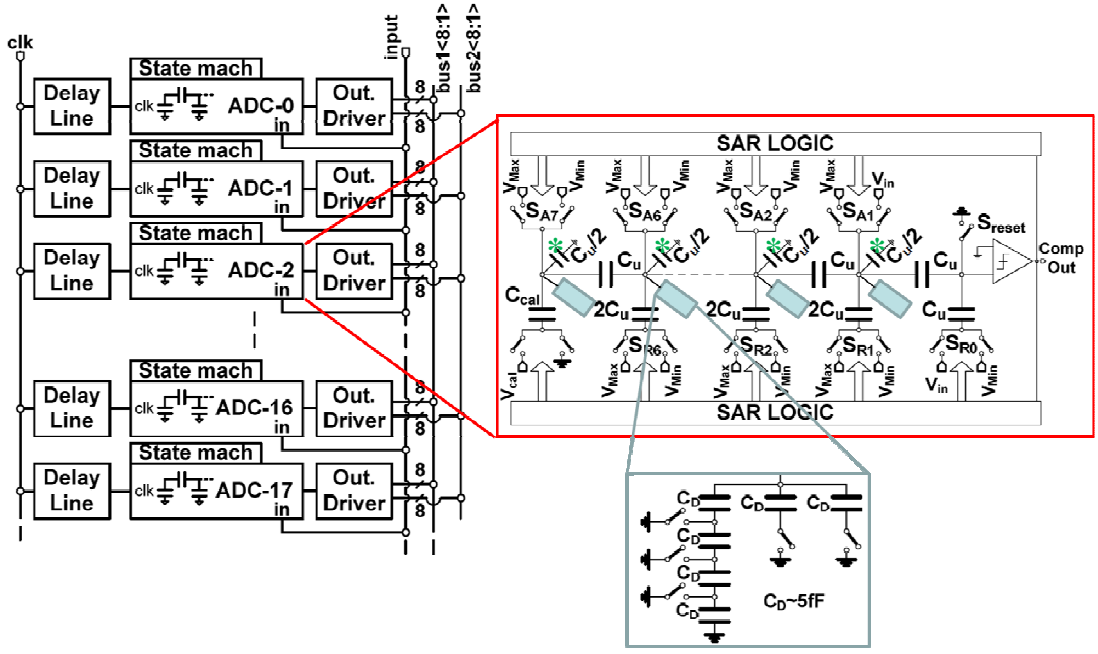


Figure 11: Architecture of the TI SAR ADC (= parasitic capacitor)*

Capacitor value mismatch:

As depicted in Figure 11, the SAR ADC under study does not rely on a binary weighted DAC, but uses a C-2C DAC instead [36]. This has the advantage that the DAC size only increases linearly with the resolution and small, fixed capacitor sizes can be used. However, a C-2C DAC suffers heavily from the parasitic capacitances at the intermediated nodes, which distort the capacitor ratios and can serve as a resolution limit [36]. The proposed SAR however incorporates these parasitic capacitors into the design: The '$C_u/2$' capacitors in this design (Figure 11) represent the total parasitic capacitances at the intermediate nodes but are also included as an integral part of the DAC [35]. Their nominal (parasitic) value is around *40fF*, which sets the limit of the minimum size design of this ADC, which is hence not thermal noise limited.

The values of these parasitic capacitors will be severely mismatched and have to be corrected by calibration. When assessing the SNDR-cost sensitivity of both capacitor trimming and digital post-distortion, capacitor trimming is to be preferred here due to the achievable f_{trim} being:

$$f_{trim} = \frac{C_{trim}}{40\,fF} = 0.125, \qquad (23)$$

$$\text{with } C_{trim} = 5.C_{p,switch} = 5\,fF \text{ in 45nm CMOS design}$$

As shown in Figure 11, a slightly (2.2X) smaller effective f_{trim} can even be achieved by placing several trim capacitors in series. The trimming structure is

able to compensate the range of 6.σ mismatch with a Z=6, assuming a mismatch of σ=5% on the nominally 40fF parasitic capacitors. The resulting measured performance improvement can be seen in Figure 12.
The remaining capacitors 'C_u' and '$2C_u$' are formed by metal finger capacitors (MFC). In the technology (*45nm LPCMOS*) used, their matching is more than sufficient to achieve *7-bit* resolution without the need for additional calibration.

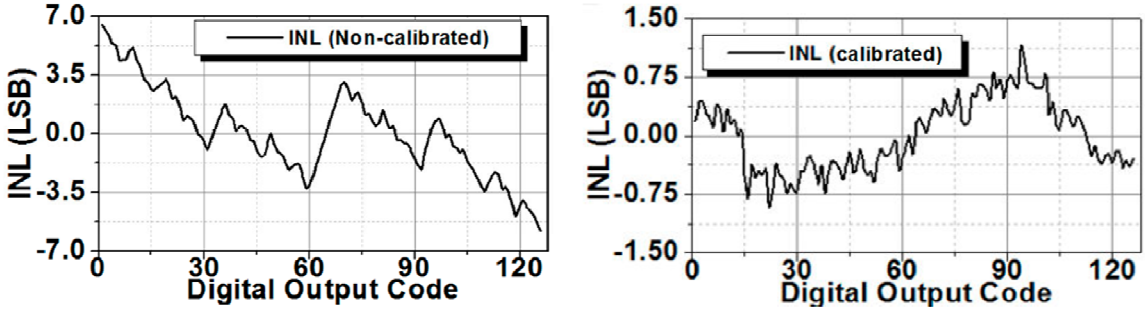


Figure 12: INL improvement after capacitor trimming of individual SAR ADC.

Offset and gain mismatch:
Once mismatch within the individual ADCs is calibrated, the mismatch across ADCs has to be addressed. In this design, an un-calibrated offset mismatch up to ±*85mV* is expected, while un-calibrated gain mismatch is typically limited to less than 5%. Both offset, as well as gain mismatches can easily be detected in the digital domain. Also the circuitry to correct for them does not require a lot of digital gates. However, due to the large offset mismatch (3-σ spread typically equals ±*85mV =34%* of comparator input range) the analog cost adder of the required extra analog redundancy to allow digital post-distortion is very large. As a result, the SNDR-cost sensitivity of digital post-distortion will be poor for offset mismatch correction, while it is good for gain mismatch correction. As a result, the ADC gain is calibrated in the digital domain using a multiplier, while an automated offset calibration loop is implemented in the analog domain (Figure 13).

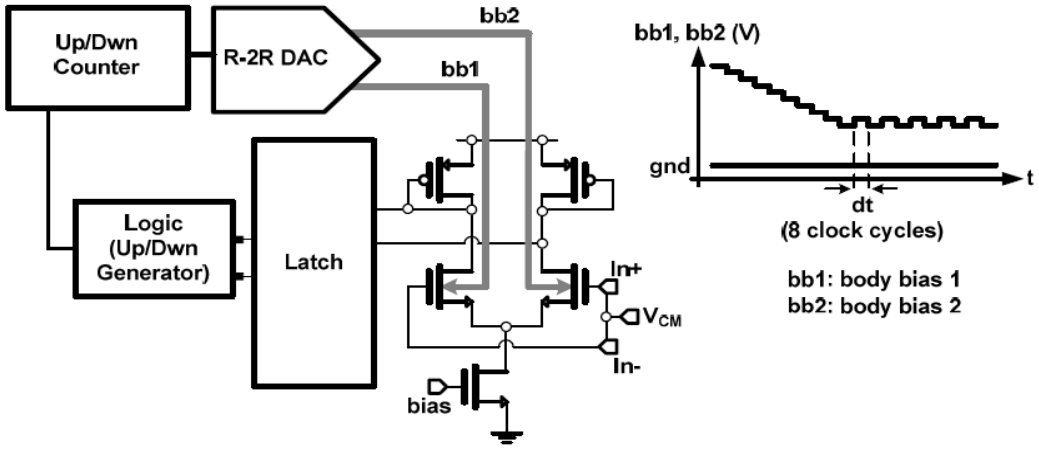


Figure 13: Automated offset calibration loop in TI SAR ADCs [35].

Sampling skew mismatch:

Sampling skew mismatch affects the maximum ADC performance by [37]:

$$SNR_{max} = 20\log(\frac{1}{\sigma_{skew} f_{signal} / f_{sample}}) - 10\log(\frac{(M-1)}{M} 4\pi^2) dB \quad (24)$$

with σ_{skew} the sampling error standard deviation and M the number of time interleaved ADC channels. The original sampling skew mismatch in our design is estimated have a $\sigma_{skew} \approx 1.5\%$ of the sampling period. This sampling skew mismatch between different ADCs is much harder to detect than gain or offset mismatch, and has attracted a lot of attention from the research community. The most common estimation approach is a digitally implemented LMS optimization loop [33]. While implemented in the digital domain, the correction can both be executed digitally (digital post-distortion) or in the analog domain by using digitally assisted trimming. The required compensation step resolution is found from Eq. (24) to be about *0.2%* of the total ADC sampling period, or *1psec*.

Digital post-distortion involves the implementation of a time-varying fractional delay filter, often realized with a (poly-phase) Farrow filter [38]. The instantiation of this, typically at least 30-tap [33], digital filter comes with a large area and power penalty, as it is always on and runs at the full rate.

The digitally assisted trimming counterpart consists of a digitally tuned delay line. This can be realized by cascaded inverters, loaded by a programmable capacitor bank (16 *2.5fF* capacitors). Both the area (*45um*^{2}/channel) and power cost (*50uW*/channel) of this are negligible on the total ADC design.

The realized performance enhancement of the full TI SAR ADC under the described channel mismatch correction (offset, gain, timing) can be derived from Figure 14.

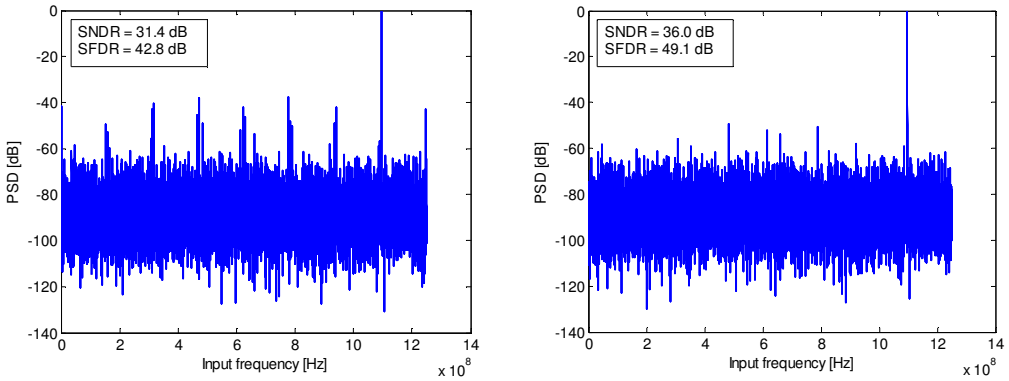


Figure 14: Performance of full ADC before (left) and after (right) TI channel mismatch correction

6. Conclusions

Theoretical analysis of ADC scaling over technology predicts a flat to increasing trend on the ADC's area and power consumption. A study over survey data of all published state-of-the-art ADC designs over the last decade however shows a cubic area and power improvement with technology gate length. The same survey data seems to indicate that this improvement is realized by heavily relying on capacitor-based ADC architectures, as well as by exploiting digitally assisted performance enhancement techniques.

Several digitally assisted techniques to improve performance of mismatch-limited ADCs are evaluated. Digitally assisted trimming, as well as digital post-distortion do not only show the largest SNDR-cost sensitivity, but also demonstrate the same cubic improvement relationship with the technology gate length, which explains the observed ADC scaling. A practical design example is used to describe the ADC enhancement selection for different mismatch parameters. More work is required on system level techniques for fast, but low complexity background mismatch estimation techniques, to limit the calibration time penalty of both digitally assisted trimming and post-distortion.

References

[1] P. Scholtens, D. Smola, and M. Vertregt, "Systematic Power Reduction and Performance Analysis of Mismatch Limited ADC Designs", Proceedings of ISPED, August 2005, pp. 78-83.

[2] B. Murmann , "Limits on ADC Power Dissipation", Analog Circuit Design, 2006, pp. 351–367.

[3] Y. Chiu, B. Nikolic, and P. R. Gray, "Scaling of Analog-to-Digital Converters into Ultra-Deep-Submicron CMOS", Proceedings of IEEE CICC, 2005, pp. 375-382.

[4] K. Uyttenhove and M. Steyaert, "Speed–Power–Accuracy Tradeoff in High-Speed CMOS ADCs", IEEE TCAS-II, Vol.. 49, No.. 4, April 2002, pp. 280-287.

[5] P. Kinget and M. Steyaert, "Impact of transistor mismatch on the speed-accuracy-power trade-off of analog CMOS circuits", Proceedings of IEEE CICC, 1988, pp. 333-336.

M. Pelgrom, A. Duinmaijer, and A. Welbers, "Matching Properties of MOS Transistors", IEEE JSSC, Vol. 24, No. 5, October 1989, pp. 1433-1440.

[7] P. Kinget, "Device mismatch and tradeoffs in the design of analog circuits", IEEE JSSC, Vol. 40, No. 6, June 2005, pp. 1212 - 1224.

[8] P. Nikaeen, B. Murmann, "Digital Compensation of Dynamic Acquisition Errors at the Front-End of High-Performance A/D

Converters", IEEE Journal of Selected Topics in Signal Processing, June 2009, Vol. 3, No. 3, pp. 499-508.

[9] A. Abo and P. Gray, "A 1.5-V, 10-bit, 14.3-MS/s CMOS pipeline analog-to-digital converter", IEEE JSSC, Vol. 34, No. 4, April 1999, pp. 599 - 606.

[10] K. Laker and W. Sansen, "Design of Analog Integrated Circuits and Systems", McGraw-Hill, 1994.

[11] P.Woerlee, M. Knitel, R. van Langevelde, D. Klaassen, L. Tiemeijer, A. Scholten, and A. Zegers-van Duijnhoven, "RF-CMOS Performance Trends", IEEE Transactions on Electron Devices, Vol. 48, No. 8, August 2001, pp. 1776-1782.

[12] C. Diaz, D. Tang, and J. Sun, "CMOS Technology for MS/RF SoC", IEEE Transactions on Electron Devices, Vol. 50, No. 3, March 2003, pp. 557-566.

[13] Q. Huang, F. Piazza, P. Orsatti, and T. Ohguro, "The Impact of Scaling Down to Deep Submicron on CMOS RF Circuits", IEEE JSSC, Vol. 33, No. 7, July 1998, pp. 1023-.1036

[14] M. Vertregt and P. Scholtens, "Scalable high-speed analog circuit design", Analog Circuit Design, 2003, pp. 3-21.

[15] C.-H. Jan et al, " RF CMOS Technology Scaling in High-k/Metal Gate Era for RF SoC (System-on-Chip) Applications", Proceedings of IEEE IEDM, 2010, pp. 27.2.1.

[16] International Technology Roadmap for Semiconductors, 2009 Edition: www.16.net/Links/200916/Home2009.htm

[17] B. Murmann, "A/D Converter Trends: Power Dissipation, Scaling and Digitally Assisted Architectures", Proceedings of IEEE CICC, 2008, pp. 105-112.

[18] B. Murmann, "ADC Performance Survey 1997-2010," [Online]. Available: www.stanford.edu/~murmann/adcsurvey.html

[19] P. Malla, H. Lakdawala, K. Kornegay, K. Soumyanath, "A 28mW Spectrum-Sensing Reconfigurable 20MHz 72dB-SNR 70dB-SNDR DT ΔΣ ADC for 802.11n/WiMAX Receivers", Proceedings of IEEE ISSCC, 2008, pp. 496-497.

[20] M. van Elzakker, E. van Tuijl, P. Geraedts, D. Schinkel, E. Klumperink, and B. Nauta, "A 1.9μW 4.4fJ/Conversion-step 10b 1MS/s Charge-Redistribution ADC", IEEE ISSCC, 2008, pp. 244-245.

[21] H. Chung, A. Rylyakov, Z. Toprak Deniz, J. Bulzacchelli, G.-Y. Wei, D. Friedman, "A 7.5-GS/s 3.8-ENOB 52-mW flash ADC with clock duty cycle control in 65nm CMOS", Proceedings of Symposium on VLSI Circuits, 2009, pp. 268-269.

[22] B. Murmann, "Digitally Assisted Analog Circuits", IEEE MICRO, March-April 2006, pp38-47.

[23] B. Murmann, C. Vogel, and H. Koeppl, "Digitally Enhanced Analog

Circuits: System Aspects", Proceedings of ISCAS, 2008, pp. 560 – 563.
[24] R. van de Plassche, "A sigma-delta modulator as an A/D converter" IEEE TCAS, Vol. 25, No. 7, July 1978, pp. 510-514.
[25] S. Weaver, B. Hershberg, D. Knierim, and U. Moon, "A 6b Stochastic Flash Analog-to-Digital Converter Without Calibration or Reference Ladder," IEEE ASSCC, 2008, pp. 373-376.
[26] L. Pileggi, G. Keskin, X. Li, K. Mai and J. Proesel, "Mismatch Analysis and Statistical Design at 65 nm and Below", IEEE CICC 2008, pp. 9-12.
[27] M. Flynn, C. Donovan, and L. Sattler, "Digital Calibration Incorporating Redundancy of Flash ADCs", IEEE TCAS-II, Vol. 50, No. 5, May 2003, pp. 205-213.
[28] B. Verbruggen, J. Craninckx, M. Kuijk, P. Wambacq, and G. V. der Plas, "A 2.2 mW 1.75 GS/s 5 Bit Folding Flash ADC in 90 nm Digital CMOS," IEEE JSSC, Vol. 44, No. 3, March 2009, pp. 874-882.
[29] D. C. Daly and A. P. Chandrakasan, "A 6-bit, 0.2 V to 0.9 V Highly Digital Flash ADC With Comparator Redundancy," IEEE JSSC, Vol. 44, No. 11, November 2009, pp. 3030-3038.
[30] G. V. der Plas, S. Decoutere, and S. Donnay, "A 0.16pJ/Conversion-Step 2.5mW 1.25GS/s 4b ADC in a 90nm Digital CMOS Process", IEEE ISSCC, 2006, pp. 2310.
[31] J. Rabaey, A. Chandrakasan, B. Nikolic, "Digital Integrated Circuits", Prentice Hall
[32] C. Grace, P. Hurst, S. Lewis, "A 12b 80MS/s Pipelined ADC with Bootstrapped Digital Calibration", IEEE ISSCC, 2004, pp. 460.
[33] C. Vogel, S. Saleem and S. Mendel, "Adaptive blind compensation of gain and timing mismatches in M-channel time-interleaved ADCs" Proceedings of IEEE ICECS, September 2008, pp. 49 – 52.
[34] Y. Oh; B. Murmann , "System embedded ADC calibration for OFDM receivers", IEEE TCAS-I, August 2006, Vol. 53, No. 8, pp. 1693 – 1703.
[35] E. Alpman, H. Lakdawala, R. Carley, and K. Soumyanath1, "A 1.1V 50mW 2.5GS/s 7b Time-Interleaved C-2C SAR ADC in 45nm LP Digital CMOS", IEEE ISSCC, 2009, pp. 76-77.
[36] S. Iyer et al., "A 0.5mm2 Integrated Capacitive Vibration Sensor with Sub-10 zF/rt-Hz Noise Floor," IEEE CICC, 2005, pp. 93-96,
[37] Y-C. Jenq, "Digital Spectra of Nonuniformly Sampled Signals: A Robust Sampling Time Offset Estimation Algorithm for Ultra High-speed Waveform Interleaving", IEEE Transactions on Instrumentation and Measurement, Vol. 39, No. 1, February 1990.
[38] C. Farrow, "A Continuously Variable Digital Delay Element", Proceedings of IEEE ISCAS, 1988, pp. 2641 - 2645.