Remote Labs for Industrial IC Testing

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Abstract—This paper deals with the remote access to an Integrated Circuits (ICs) Automated Test Equipment (ATE) for both educational and engineering purposes. This experience was initiated in 1998 in the context of a French network (CNFM) in order to provide a distant control to industrial equipment to academic and industrial people. The actual shared resource is a Verigy V93K System-on-Chip (SoC) tester platform. The cost of such equipment is close to 1 million dollar, without taking into account the maintenance and attached human resources expenses to make it work properly daily. Although the sharing of such equipments seems to be obvious for education, the French experience is quite a unique example in the world. The paper introduces the context of industrial IC testing and justifies the introduction of labs in Electrical Engineering curricula. Practical information regarding IC testing and network setup for remote access are detailed, together with lab contents.

Index Terms—Test, testability, remote labs, ATE programming.

1 Introduction

This paper details the French experience of distant learning in the field of Integrated Circuit (IC) testing. This work is supported by the Comité National pour la Formation en Microélectronique (CNFM), which is a public organization that federates academic and industrial partners for the purpose of education in Micro and Nanoelectronics [1]. CNFM focuses on making heavy educational resources such as professional CAD tools, clean rooms, or industrial test equipments available for common use, by all French universities.

In the past, early attempts to spread low-cost test equipments among several universities failed to obtain good results. First, low-cost testers do not represent the industry reality so that getting experienced on those machines does not provide strong added value to the student curriculum. Second, developing training modules and labs in the field of IC testing requires good technical support and teachers with high degree of expertise, which is not easy to find. Finally, the maintenance constraint was too high and equipments were switched off, one after one.

The National Test Resource Center of CNFM (so-called CRTC) has been created to respond to the industrial demand in engineering curriculum with Design and Test competences. Considering the huge cost of up-to-date IC testers, the policy of CNFM was to set up a single test center for all the French academic centers. So in 1998, the University of Montpellier was chosen to implement the CRTC. The technical platform benefits from the competence of more than 25 people (researchers and professors) from a research laboratory (LIRMM [2]) internationally renowned in the field of design and test of integrated circuits and systems. Research projects include *Design-for-Test* (DfT) and *Built-in Self-Test* (BIST) for digital, analog, and mixed-signal circuits, and design and test of integrated *Microelectromechanical Systems* (MEMS).

To avoid any excessive travel expense for students from their university to CRTC in Montpellier, the implementation has been designed to make the CRTC equipment reachable from any remote center [3], [4]. Other similar experiences are reported in [5] for a variety of engineering fields.

For about 10 years, CRTC has provided support for labs in IC testing, based on the remote control of industrial test equipment. On a national level, more than 100 students per year have been trained using this support from 1998 till now. In 2003, after a two-year long European Information Society Technology (IST) project was completed, students from Germany, Spain, Italy, and Slovenia were able to take control of the tester for remote labs [6].

The paper is organized as follows: Section 2 describes the industrial context of IC testing and the subsequent requirements in terms of education for the students in the Electrical Engineering field. Especially, the need to bridge the gap between regular academic courses and industrial testing considerations is addressed. Section 3 recaps the fundamentals of IC testing according to the actual procedures. Section 4 presents the CRTC setup to allow simple remote access to users, and ways to improve interaction between trainers and students in the case of distant learning. Section 5 provides details on few training modules that we have experienced with students at various educational levels. Finally, Section 6 concludes the paper.

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2 Motivations for IC Testing Labs in Initial and Continuing Education

2.1 Industrial Context

Manufacturing test consists in verifying the quality of a product with respect to its specifications. For most of the manufactured products, the cost of the final verification represents only a small part of the production costs. This is due to the fact that these products are either of high cost (e.g., automotive industry) or enough reliable to authorize randomly applied verification (e.g., food industry). This scheme doesn't apply in the microelectronics industry, where low-cost products may be produced with a significant number of out-of-specifications or nonfunctioning parts [7]. Manufacturing tests are then required to verify the physical integrity and the correct behavior of any produced parts at a reasonable cost. The problem is that manufacturing test introduces a breakage in the batch fabrication concept. Indeed, speaking about malfunctions leads to singularities that cannot be dealt in a batch-based model. Even if test is undertaken at the wafer level and if parallelism is still possible, each produced device must be tested independently to discard the few percent of defective circuits.

The cost of the production test for integrated circuits is a very strategic challenge for the competitiveness of the microelectronics industry. State-of-the-art integrated circuits are complex silicon systems that combine both digital and analogue blocks. They may be either high added value Application-Specific Integrated Circuit (ASIC) or composite multichip Module (MCM) with mixed technologies, up-to-date System in Package (SiP), or new-age System-on-Chip (SoC) made from Intellectual Property (IP) modules including High-Density Memories or FPGAs [8]. These circuits constitute the major part of modern electronic appliances and their fabrication is strongly boosted by the tremendous growth of the multimedia and telecom market. In some cases, the test of a multimedia circuit may constitute up to 50 percent of its total cost [9], [10]. Moreover, due to the growing complexity of IP-based SoC devices, this high percentage is planned to increase significantly in the close future. The global test cost for a given circuit mainly includes the cost for test development, the cost for implementing the full characterization test on high-tech engineering testers, and the cost for using highly efficient production testers.

Assuming a testing equipment running continuously and a typical global cost of one hundred thousand dollars per year, the cost of a single minute of test time rises to 20 cents. It is obvious that test time must be reduced as much as possible for large volume production, where low gross margins are expected [11]. This economical context has two main consequences on test engineering. First, to reduce costs, the microelectronics industry is dealing with test time and test complexity in the early phases of the design of a new product. This is known as design for testability. Second, industry needs highly trained engineers to save seconds of test time on their equipment, and thus, to reduce the number of test equipments running in parallel. As a result, there is a strong demand from the microelectronics industry in engineers having knowledge ranging from the simple awareness of testing problems to the full skill and competence in IC testing [12]. Four main levels of test competence are required for future microelectronics engineers, depending on their role in the production process as follows:

- *Design-for-Test Engineers*: Due to the increasing cost of production tests for multimedia/telecom circuits, it is mandatory that test engineers have a full knowledge of up-to-date high-tech Automatic Test Equipment.
- *Test Engineers*: The major role played by time-to-market in the economical strategy of circuit manufacturers implies that the time needed for test development has become of critical importance. Thus, it is now mandatory for test program engineers to have a good knowledge of characterization and production test in addition to their traditional software skills.
- *Product Engineers*: By definition, product engineers must have adequate knowledge in both circuit design and circuit testing.
- *Design Engineers*: In the context of a modern Design-for-Test approach, design engineers are nowadays required to be aware of testing issues and to have notions of engineering testing implementation.

For all these profiles, the microelectronic industry suffers from an important shortage in microelectronics engineers having sufficient skills in test development.

2.2 Academic Context

The issue of improving the quality of engineering testing education of Electronics Engineers in the US was raised in the early 90s by R. Absher's paper *IEEE Design and Test of Computers* [13] and a Round Table at the 1991 International Test Conference [14]. At that time, it was noticed that engineers had to cope with complicated testing issues of modern microelectronic devices. Moreover, the very limited number of strong research centers capable of spanning the entire spectrum of testing know-how was pointed out. As a result, there was no testing unit in the undergraduate curricula and a significant missing element was the educational link to the realities of manufacturing engineering. Later on, the situation improved a little with the introduction of some theoretical test topics such as: *fault modeling*, *fault simulation*, *test generation*, DfT, etc. Nowadays, the situation of test education is still under concern as discussed in the round table at the 16th Asian Test Symposium in 2007 [15].

On one hand, we witness the amazing event of the SoC revolution, which permits any electronic designer to create a complex system on a single chip by using sophisticated Intellectual Property cores from various design providers. On the other hand, manufacturing test is strongly advancing due to research in new testing techniques such as *scan path*, *boundary scan*, *delay testing*, *mixed-signal testing*, etc.

At the same time, there is a strong demand from consumers for low-cost complex circuits with high level of quality or reliability and reduced time-to-market. Test equipments have thus undergone a strong technological mutation so as to be able to integrate these new techniques and requirements.

As a result of this combined evolution of design and test contexts, the test of new generation mixed-signal SoCs,

through the use of sophisticated test tools, becomes a very critical economical problem.

Under these conditions, the engineering test education in undergraduate and graduate curricula has to be reconsidered. The idea of making ATE accessible to Academic Institutions to make manufacturing testing a part of Electrical Engineers curriculum becomes an issue [16]. This will undoubtedly help microelectronic students to be aware of modern testing problems.

Our main idea when initiating a nationwide program in 1997 was to bridge the gap between academic test teaching and effective industrial test needs. Indeed, we observed that during their job interview, students often encounter problems when discussing IC testing issues. The reason is a certain ambiguity about the exact meaning of the word test. When educated in academic IC testing, a microelectronic student is aware of theoretical topics such as *fault modeling*, *fault simulation*, *test generation*, *DfT*, *BIST*, etc. When speaking about industrial test, the employer essentially refers to topics such as: *characterization test*, *production test*, *wafer sort*, *Average Quality Level*, *ATE*, *testflow*, *multisite testing*, *yield*, etc. Of course, not only the vocabularies are different but also the underlying concepts. So, we found it was mandatory to give our microelectronic graduates a better electronic education by including engineering testing in their curriculum.

From the 10-year experience of CRTC, we have verified that students with knowledge in engineering test indubitably have a good added value when competing to get a job in microelectronics industry. Other initiatives in the same field [17], [18], and [19] have led to the similar observations and confirmed the pertinence of the idea.

3 Fundamentals of Industrial IC Testing

Manufacturing of ICs is performed in the well-controlled environment of high-class clean rooms. However, it still occurs that isolated particles (dust) accidentally land onto wafers or masks creating so-called "spot defects." Electrically, this typically generates open or short circuits faults. Other physical phenomena, such as electro migration, diffusion, or ionic contamination contribute to the production of defective devices. Production equipment also suffers from deviation in their settings leading to spreading in electrical parameters of fabricated circuits. It increases the chance to manufacture out-of-specification products. Finally, the packaging step may also introduce defects such as bonding opens or shorts. The all-purpose of industrial testing is to guaranty that commercialized circuits meet their expected specifications.

Test is performed at several levels that depend on the product itself, and on the reliability level required in the final application. A standard test approach during the product life is illustrated in Fig. 1. Basically, a test is performed between each integration step in order to minimize the cost of defective devices. This paper focuses on fabrication tests, which occur at the foundry level (i.e., *Wafer Sort* and *Final Test*).

3.1 Characterization and Production Test

Commonly, testing a circuit consists in verifying its behavior (its function) for all possible input situations. For

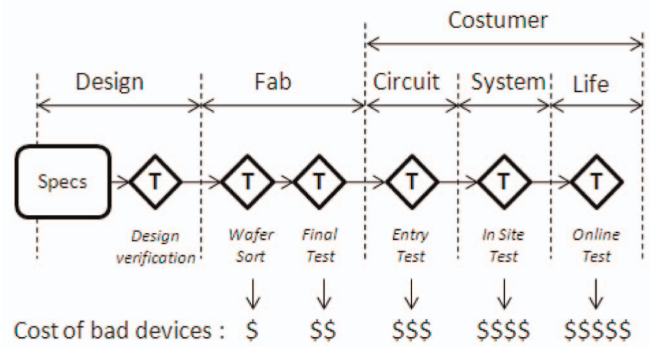

Fig. 1. A test is performed at every integration step. The latter a bad device is detected, the higher it costs, especially after selling to the costumer.

digital circuits, this is called *exhaustive functional testing*. Practically, the functional test of digital circuits having few tens of inputs is not possible because it would take too much time, even with state-of-the-art ATE. For this reason, the functional test is replaced by something called *structural testing,* which consists in applying a reduced number of input combinations in order to verify the integrity of the component according to a predetermined list of potential faults (*fault list*).

In the industrial context, two distinct kinds of tests are performed: *characterization test* and *production test*. The *characterization test* is performed first, after early dies are produced. The objective is of course to verify the device functionality but more especially to measure the circuit performance in order to determine all the specification that will appear in the component *datasheet.* It concerns static (*DC*) parameters such as output voltages, current capability, input levels, leakage, and dynamic (*AC*) parameters such as propagation delays, setup and hold times, operating frequency, etc. The *characterization test* is not under strong timing constraint (few minutes is acceptable). It must provide accurate information and statistical data in order to determine, for each parameter of the *datasheet*, a range of acceptable values. Note that the *datasheet* is a contractual document which states the guarantied performances.

The *production test* has no other purpose than verifying that manufactured circuits meet the datasheet information. Because *production test* is performed on every single product, it has to be very fast (few seconds). Basically, a production test consists in a flowchart implementation of elementary tests, each having a simple *Pass/Fail* output. Doing so, it is possible to distinguish the failure origin and to perform a sorting (*binning*) for both good and bad circuits. The *production test* is considered right after foundry at the wafer level (*wafer sort*) and after packaging (*final test*).

The training modules developed at CRTC focus on both characterization and production tests.

3.2 Implementation on ATE

Getting into the details of the tester, programming is impossible here. Therefore, the purpose of this section is only to give an overview of a test implementation as it is done during remote labs, taking, for example, the test of a simple digital device.

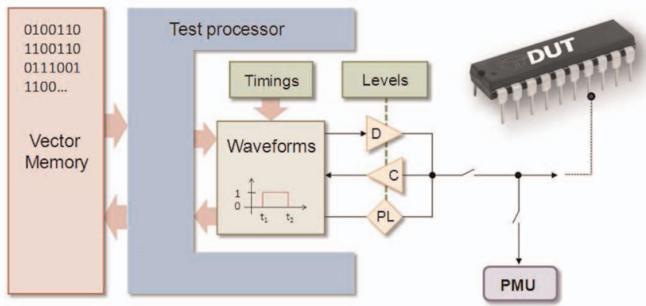

Fig. 2. Internal structure of an ATE digital channel (Pin Electronics).

Basically, testing a device consists in applying electrical signals to its inputs and measuring response from its outputs. Practically, many parameters have to be defined such as the voltage levels, the timings, the sequence of input vectors, the nature of the measurements, etc. Fig. 2 illustrates the electronic architecture of a tester channel for a digital pin, which can be an input, an output, or a bidirectional input/output.

The settings for each digital channel concern the following:

- The levels: Signals are applied to the device under test (DUT) using the *driver* D, which converts logic "0" and "1" into real voltages. In return, signals coming from the DUT are converted into logic states by the *comparator* C based on programmable detection thresholds. In addition, current load can be applied to the DUT using the *parametric load* (PL).
- The timings: Driver and comparator events are first defined as *waveforms* with no timing information and stored in the *wavetable*. The timing generator then locates each event in time. This separation allows using the same set of waveforms with different timings.
- The vectors: The vector memory contains a column of pointers to the wavetable, and so determines the sequence of signal to be applied to the DUT by calling waveforms one after one, for each tester period.

Each parameter of these settings can have different values, each being applied at the right time in the test procedure. Also parameters can be linked together by equations. The first testing procedure to develop is a functional test. For a logic device, it generally consists in verifying the truth table with relaxed constraints on timing and levels. This functional test is very important since most of the *DC* and *AC* parameters are next measured "on the fly" during the execution of this functional test.

The last step in the programming process concerns the *testflow*. Fig. 3 shows a hypothetical *testflow*, where a continuity check is performed first. This is common in practice. The continuity check simply measures the voltage across the protection diodes of the DUT pins, by forcing a small current, in order to make sure that the DUT is well connected to the tester. The *testflow* then determines the succession of test function to be applied to the DUT and routes the flow depending on the result (*Pass* or *Fail*) of each test. Both good and bad dies are sorted into *bins* (this is called *binning*). Good dies can therefore be sorted depending on their performance. More generally, monitoring the way bins are filled up helps detecting potential problems

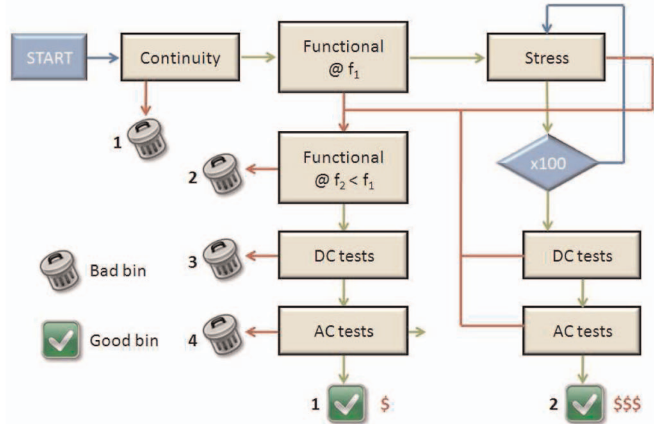

Fig. 3. Example of testflow.

with the fabrication process or the test application. With today's aggressive fabrication technologies, this monitoring plays an essential role [8].

4 CRTC Hardware and Software Setup

4.1 Test Resources

The CRTC tester is a V93K from Verigy. Verigy is one of the four major test equipment manufacturers in the world and is well represented in the European microelectronic industry [20]. This is an important point that people get trained on trendy machines. The V93K platform targets SoC testing. It is made of a test head that can host various resources such as digital channels, mixed-signal, supply, or RF boards. The user is, therefore, able to optimize the testhead contents to meet the DUT requirements.

Fig. 4 illustrates the basic elements that compose the ATE. The main part is the testhead. This testhead is a compact model dedicated to engineering. It can host up to 18 boards (*Pin Electronics*) for a maximum number of 512 digital pins based on commercialized 32 channels boards. Programming is performed using a regular computer running dedicated software under Linux. The communication between the testhead and the computer is an optical GPIB link.

At that time, the testhead is equipped with supply, digital, and mixed-signal resources as summarized in Table 1. This

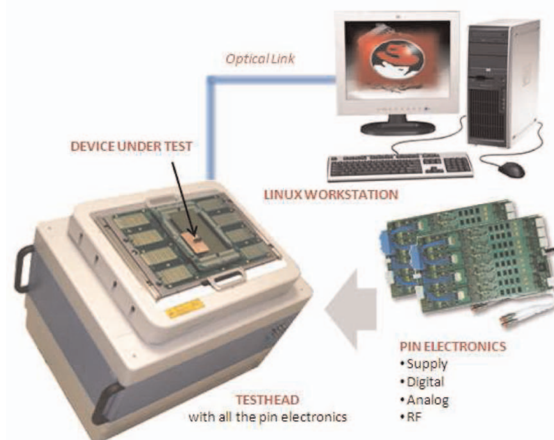

Fig. 4. Elements of the ATE.

TABLE 1
CRTC Tester Hardware Resources

Board	Ressource Type	Qty	Channels / board	Specifications
PS3600	Digital	1	32	3.6GSps / 64Mvec memory
PS800	Digital	1	32	800MSps / 64Mvec memory
AV8	Mixed-Signal	1	8	24bits / 200kSps for Audio 14bits / 65MSps for Video
MSDPS	Supply	2	8	-8V to 8V / 2A

setup allows CRTC to address both digital and mixed-signal trainings. Memory testing is also possible without additional resources. In most cases, the devices under test during training are not too complex for obvious educational reasons. Regarding the performances of the boards, the PS3600 features digital channel with sampling rates up to 3.6 GSps, which are suitable to test state-of-the-art very high speed digital circuits. The AV8 board is designed for current multimedia circuits with both audio/video resolution and bandwidth. Finally, 16 independent supplies are available, which is more than enough in most training situations.

4.2 Software Setup

The test program is developed into a complex environment called *SmarTest*, which is based on the open platform *Eclipse*. Detailing this environment would be out of the scope of this paper. Basically, the application manages the various setup files (pins, levels, timing, and vectors) and is used to build testflows. *SmartTest* comes with a library of preprogrammed basic *Test Functions* for all the essential operations: functional test, continuity test, DC or AC parameters measurement, etc. These test functions are very helpful for beginners. For advanced users, custom test functions (also called *Test Methods*) can be programmed directly in C, compiled, and built into the same environment.

The software/hardware interaction is built upon the concept of *live-machine*. When programming through software, data in the tester memory are continuously updated. In others terms, software windows are like views of the tester memory content in real time.

This speeds up the program development and debug as there is no need for compilation or download steps. The counterpart of this interaction scheme is that the software needs the physical tester to operate. For parallel labs, as the hardware is not divisible, it would lead to a dead end without the availability of an *offline* mode. In *offline* mode, the tester hardware is emulated in software so that *SmarTest* operates just the same as in *online* mode (as long as no real test result is expected). Emulated tester can be duplicated so that it is possible to run several *SmarTest* sessions in parallel, which is a Sine qua non condition in a classroom context.

4.3 Network Setup

The network setup has been designed to allow the maximum level of flexibility for distant users. Locally, the *SmarTest* software is hosted by two Linux computers, namely *VERIGY_ON* and *VERIGY_OFF*. The first one is

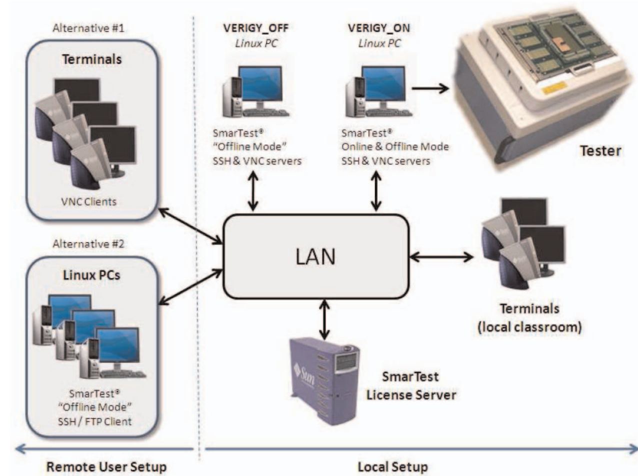

Fig. 5. Network setup for remote access.

physically connected to the tester and is dedicated to *online* sessions. At some point in the lab, each trainee will connect to this computer to run its test program on a real device. The second one runs *SmarTest* in *offline* mode only and is intended to support the multisession development phase. The local classroom is made of simple UNIX terminals running a Virtual Network Computing (VNC) viewer.

Distant users have two options, depending whether they want to install and run *SmarTest* locally or not. The recommended option (Alternative #1 in Fig. 5) is to connect directly to CRTC Linux stations using a VNC client, the same way it is done in the local setup of Montpellier. VNC clients are lightweight software, freely available for all kinds of operating systems, turning any computer into a VNC terminal. There are no other requirements regarding software installation and license checking is totally transparent for the user since *SmarTest* runs on CRTC stations. As VNC technology is a remote desktop approach, it may suffer from Internet latency, although it is not really an issue with today's Internet bandwidth. Anyway, a solution to improve the interactivity with *SmartTest* is to proceed to a local installation, assuming that a Linux station is available. In that case, the network connection is only required for license checking (Alternative #2 in Fig. 5).

VNC technology offers an easy way for the distant access to the tester. Besides, there is another reason to promote this approach in the context of distant learning: the same desktop can be shared between users. This capability brings a lot of interactivity between students and teacher [21]. Indeed, the teacher desktop can be seen from students, allowing live demos to be performed. Also, the teacher can see and take control over any student desktop to contextually bring help where needed (Fig. 6). Coupled with Voice over IP, a virtual classroom has been experienced with trainer and trainees spread anywhere.

5 Labs Content and Organization

The CRTC's primary objective is to support educational programs through practical courses and labs. The usual way to work with distant universities is to organize first training for trainers in Montpellier. The second step is to

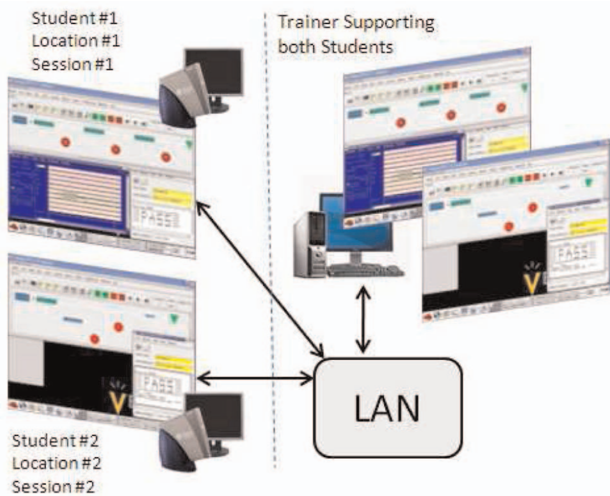

Fig. 6. Illustration of desktop sharing between distant and local users.

help the distant trainer to set up the connection from its place. After that, authorized trainers are free to place a reservation for the tester by checking its availability on CRTC's Website [22]. Temporary user accounts are created upon trainer demand with limited rights so that the local system remains safe. After the completion of training, files are archived, sent to owner, and accounts are destroyed.

The way each training course for student is implemented depends on the local context. The global organization of syllabus, the initial level of the students, and the pedagogical approach of the teaching team make the organization different in terms of number of students, number of groups, and course duration. This demonstrates the good flexibility of the remote system. Once a working time slot is booked through, the tester is fully devoted to the remote center. Then the teacher can use the tester, exactly as if it was located on the local site, and he can implement the training at his own convenience. Offline and Online connections are, therefore, under the trainer responsibility. Note that misuse of the ATE may only damage the device under test, which is a low-cost and disposable part.

Because CRTC remains first user of the tester, we develop and share training material. In the past years, training modules were based on Verigy's educational material, which are mainly developed for test engineers, and so are more focusing on the tester operation than on testing fundamentals. Today, we have identified three educational levels, where industrial testing may be of special interest if addressed relevantly. At undergraduate level (L), only digital circuits are addressed with emphasis on device characterization and *datasheet*-related aspects. At graduate and engineering level (M), modules are sized to provide a real professional experience of the tester usage. Both digital and mixed-signal devices are concerned. Finally, at PhD level (D), advanced techniques such as custom test function coding can be addressed.

5.1 Undergraduate Level

At undergraduate level, students are using electronic components daily, and have become familiar with their *datasheet* without having any idea on how this latter has been constructed. As the only prerequisites for testing a standard IC are the basics of fundamental electronics, we can go through the development of a complete test program. During the training, students often rediscover the role of the circuit *datasheet*. As an example, a majority of students completely ignore the importance of critical parameters such as setup time and hold time for the good design of sequential circuits. The lab part of the training is the occasion for them to visualize and measure these timing parameters. More generally, the proposed training module aims at providing an in-depth exploration of the *datasheet* for a simple digital circuit from the TTL logic family.

TABLE 2
Digital Training Typical Agenda

Day	Program

1	• Tester HW/SW overview
	• Test program development:
	  • Pin configuration, level, timing, Pattern
	  • Continuity and Functional tests implementation
	  • Test flow

2	• Test execution and Result analysis:
	  • Datalogging
	  • Debugging tools

3	• Characterization tests :
	  • AC tests: Vil/Vih, Vol/Voh, leakage
	  • DC tests: set up hold, propagation delay times
	  • Shmoo plots

4	• Advanced test features:
	  • Global variables
	  • Pin Margin, Histogram
	  • Burst mode
	• Preparation to mixed-signal training:
	  • Test methods

5.2 Graduate Level

Digital training courses aim to initiate students and engineers to digital IC test. After completing a digital training, each trainee will be able to 1) make competent use of any digital ATE to test a device for its performance parameters and specifications, 2) build up a testflow to automate the test execution, and 3) create a test program to be executed on the production test floor. The training courses use a standard digital circuit as DUT to simply illustrate all the test functions. Each training course is built up on lessons and related lab exercises. Table 2 shows typical agenda for four days digital training.

Mixed-signal training courses introduce the test of analogue and mixed-signal circuits. After completing the training, students are able to make competent use of the tester to test both ADC and DAC devices for its performance parameters and specifications. They are prepared to plan appropriate tests by utilizing the DSP instruments. Fundamentals of analog testing are addressed, with focus on analog circuit characteristics such as linearity, gain, offset, etc.

5.3 Continuous Education

As the CRTC is a Verigy's backup training center since February 2008, test trainings are also delivered to industrial people. They require Verigy's agreement and are done using Verigy's policy and training materials.

The CRTC trainer is a Verigy-certified trainer who has also 10 years experience in test engineering. The trainer is

TABLE 3
CRTC Tester Usage for Trainings in 2007/2008

Level	Training	#Sessions	#Participant Local	#Participant Distant
Undergraduate	Digital (Datasheet)	2	20	8
Graduate	Digital (Standard)	2	32	18
Ph.D. & Trainers	Digital / MS / Memory	5	26	-
Industrial	Digital / MS	1	4	-
Total			**82**	**26**

skilled in digital, mixed-signal, and memory tests, which allow CRTC to offer a large range of test services. Test trainings are executed based on a predefined planning or on demand according to trainer's availability.

5.4 Tester Usage and Feedback

Trainings organized during the 2007/2008 academic year are listed in Table 3. The global feedback from users about the implementation of the trainings on digital test engineering is very good. The remote access has been proved to be very compliant and adaptable to local context. The opportunity of acceding to a real industrial test tool is fully appreciated. Interestingly, there is no difference between local and distant users' feedback. In both cases, the major limitation of the approach is the physical resource itself (the ATE), which is unique, and therefore, must be shared in time between participants. A way to limit long-time waiting for ATE availability in a classroom is to force most of the setup preparation and debugging in the *offline* mode.

In addition to these trainings, the CRTC platform also supports various projects. First, a teaching project concerns the design and test of a full mixed-signal ASIC with application to magnetic field sensing. Second, CRTC provides support to a research project between LIRMM and Verigy concerning the test of RF circuits using high-speed digital channels. Finally, CRTC drives an internal project that consists in developing new labs allowing the user to customize the DUT using an FPGA. This offers opportunity to have virtually any kind of logic function and to synthesize faulty behavior (static or dynamic faults) in order to introduce diagnosis considerations in the labs.

6 Conclusion

In this paper, the quite unique French experience of sharing heavy test equipment for education and engineering is detailed. Because of the cost of such equipment in terms of both initial investment and required skilled staff for daily operation, the benefit of distant access is obvious. The current testing machine is a V93K platform from Verigy. This up-to-date test equipment is very well represented in the industry in Europe. The machine is hosted by the National Test Resource Center of CNFM (CRTC), which provides large support for access, training, and makes available educational material. Since its creation in 1998, more than a thousand of students and engineers have gained experience on industrial testing by way of CRTC. By now, the use of emerging virtual computing solutions greatly improves the interactivity between distant users and local teacher as virtual desktops can be shared.

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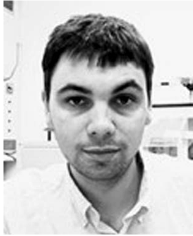

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