Single-Chip FPGA Implementation of a Digital VRM Controller with Interlaced Sampling and Control Technique

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***Abstract*—This paper presents the design and implementation of a singe-chip FPGA based digital VRM controller for multi-phase synchronous buck converters with interlaced current sampling and load current feed-forward compensation techniques. The sampling of the inductor current is synchronized with the middles of leading and trailing edges of the PWM signal of each synchronous buck converter for both turn-on and turn-off. The proposed sampling scheme has a high noise immunity to the common-mode switching noises induced by the switching of the MOSFET and its parasitic junction capacitances resulted by the heat sink. A true average current signal with minimum response time can be measured with accuracy within a switching period. The timing clocks for the digital controller and the digital PWM generator are interlaced with each other to achieve a minimum delay at a same sampling and switching frequency. A digital interface is designed for the connected microprocessor load to adjust the output voltage and provide feed-forward load current compensation according to its clock rate, loading factor, and pipeline scheduling. The realization scheme for the proposed digital VRM controller has been described. Simulation analysis and experimental verifications are given to illustrate the fast dynamic response control of VRM for advanced microprocessors.**

***Index Terms*—digital VRM controller, single-chip FPGA implementation, interlaced sampling and control scheme, synchronous current sampling technique.**

I. Introduction

Advanced power supply technology plays the key role as an enabling technology for development advanced information technology [1]-[2]. The current generation of advanced microprocessors are consuming a rated power of 60-80 watts with a possible peak power of 100-130 watts. If the power requirements roadmap for advanced microprocessors can not be slow down, the increase of power density of the CPU core will hinder the progress of information technology [3]. In order to reduce the power consumption of advanced microprocessors various technologies are being developed to solve this challenging power design issues, these include low power VLSI design technique, asynchronous digital circuit design technique, dynamic power management, adaptive voltage scaling, and parallel processing technique.

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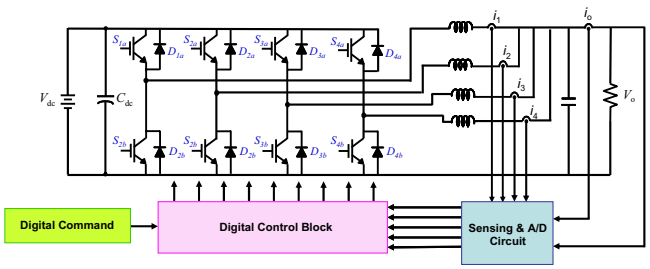


Fig. 1. Block diagram of a digital-controlled multi-phase synchronous buck converter.

The supply voltage needed to power the microprocessors is programmed to decline from the present generation of about 1.2 volts to 0.5 volts near the end of the decade. The supplying current of 100 amperes for an 1.0 volts regulation within 10 millivolts settling time with a load current slew rate of 100 amps per microsecond requires the design of high power density VRM with fast dynamic responses [4].

Multi-phase synchronous buck converter topology has gained its widespread acceptance in VRM applications [5]-[6]. Although increasing the number of phases can lower the per phase current, it also results other problems such as circuit complexity, current sharing during transient response, and enlargement of PCB board area. A proper selection of the number of phases needs an engineering compromise between current per phase, switching frequency, circuitry complexity, size, and efficiency. The integration of the PWM controller with integrated MOSFET gate drivers poses another design issue in the design of high frequency high power density VRM controller. Although this solution benefits with a compact solution with lower component counts, however, because there are four wires needed for each phases, it also presents layout problem due to longer gate traces and limits its maximum switching frequency. Another disadvantage is it also prevents the selection of other MOSFET for gate driver.

A more flexible solution is to provide a programmable and configurable digital VRM controller with design simplicity, application scalability, and optimized control

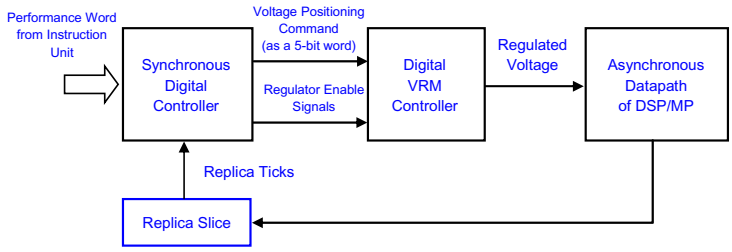


Fig. 2. System level diagram of a power management system for asynchronous datapath of an advanced microprocessor.

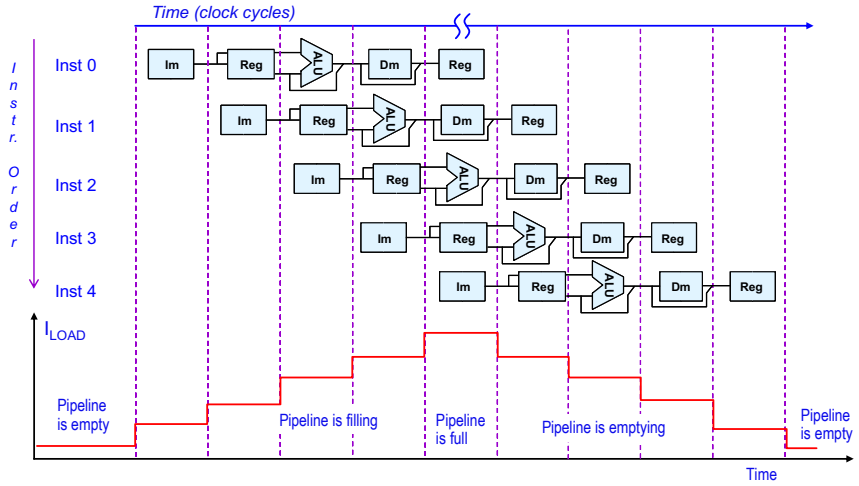


Fig. 3. Current loading profile for the pipeline operation of a microprocessor.

architecture for a target design [7]-[10]. This paper presents the design a digital VRM controller for multi-phase synchronous buck converter by using a novel interlaced sampling and control techniques.

Fig. 1 shows the system architecture of the proposed single-chip FPGA solution for the digital control of a multi-phase synchronous buck converter. The supplying current to the microprocessor is equally shared by the multi-phase synchronous buck converters. Each phase of the DC/DC converter is further phase shifted with an equal electrical degree to reduce the current ripples feeding into the output capacitors bank. The power consumption of a target microprocessor is mainly determined by the activity factor when running a specific program.

The current demanding depends on the execution of pipelined instructions which can be synchronized by a replica tick generated by a replica slice of the target microprocessor. Fig. 2 shows the system level diagram of a power management system for asynchronous data path of an advanced microprocessor. A synchronous digital controller is used to generate the voltage positioning command for a voltage regulation module (VRM) during dynamic power management process to maintain the microprocessor operating in an optimal condition. Fig. 3 shows the current loading profile for the pipeline operation of a microprocessor. It can be observed that the slew rate of the load current depends on the activity factor of each execution phase for a series of pipelined instructions. In order to provide a smooth power flow to the target microprocessor with fast dynamic response, a feed-forward control scheme can be used to improve the dynamic response of a VRM regulator. The proposed digital VRM controller provides a feed-forward controller to speedup its dynamic response under large load current transients.

This paper presents the design a single-chip FPGA implementation of a digital VRM controller for multi-phase synchronous buck converters by using a novel interlaced sampling and control techniques. Section II makes a steady-state analysis of the multi-phase buck converter, section III describes implementation of the digital VRM controller by using FPGA. Simulation and experimental results are given in section IV to validate the proposed digital VRM control scheme and section V is the conclusion.

II. Steady State Analysis

The multi-phase buck converter configuration is show in Fig. 1, this scheme could reduce the total inductor current ripple, and output voltage ripple, and can increase output effective switching frequency. The circuit relative analysis is as follows.

A. Inductor Current Ripple

When the synchronous buck converter is operating in continuous conduction mode, the inductor current ripple of each phase can be expressed as

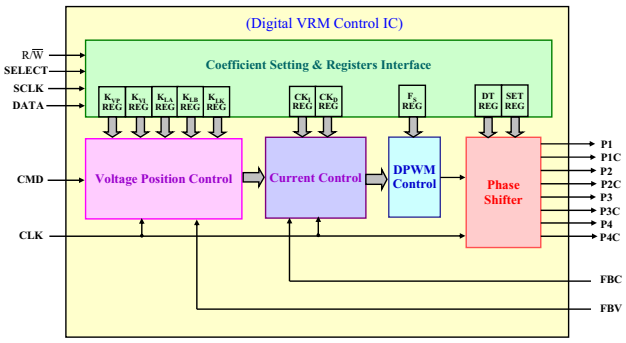


Fig. 4. Functional block diagram of digital VRM controller.

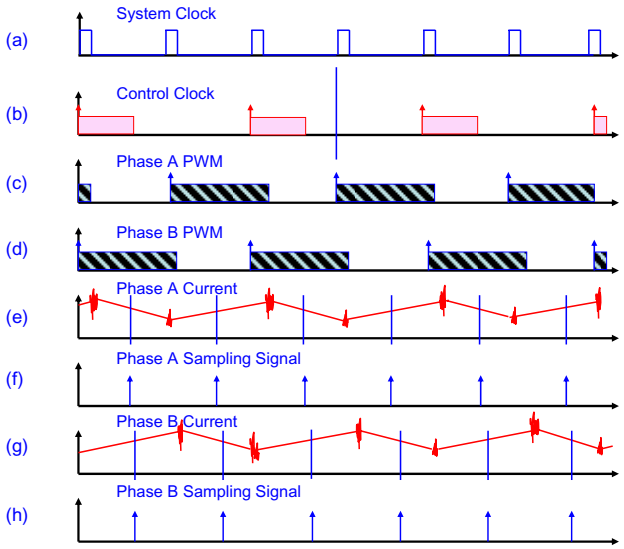


Fig. 5. Multi-phase synchronized sampling scheme.

$$\Delta I_{1p} = \frac{V_o \cdot (V_{in} - V_o)}{2 \cdot V_{in} \cdot L_{1p} \cdot f_{sw}} \tag{1}$$

where V_o is the output DC voltage, V_{in} is the input DC voltage, f_{sw} is the PWM switching frequency, and L_{1p} is the inductor of single-phase synchronous buck converter. The current ripple of the *n*-phase interlaced VRM is as follows

$$\Delta I_{np} = \frac{V_o \cdot (V_{in} - V_o)}{2 \cdot V_{in} \cdot L_{1p} \cdot n \cdot f_{sw}} = \frac{\Delta I_{1p}}{n} \tag{2}.$$

Therefore, the superimposed output inductor current ripple can be reduced to 1/n of the corresponding single-phase inductor current ripple.

B. Output Voltage Ripple

Output voltage ripple in a single-phase synchronous buck converter could be express as

$$\Delta V_{o1p} = \frac{V_o \cdot (V_{in} - V_o)}{16 \cdot V_{in} \cdot L_{1p} \cdot C \cdot f_{sw}} \tag{3}$$

and the output ripple of *n*-phase interleaved VRM is

$$\Delta V_{onp} = \frac{V_o \cdot (V_{in} - V_o)}{16 \cdot V_{in} \cdot L_{1p} \cdot C \cdot (n \cdot f_{sw})^2} = \frac{\Delta V_{o1p}}{n^2}. \tag{4}$$

TABLE I
PIN DEFINITION OF THE INTERLACED SYNCHRONOUS SAMPLING SCHEME

Symbol	Status	Range	Description
CLK	W	1 / 0	Eternal clock, max = 200MHz
RST	W	1 / 0	PWM reset 0：disable 1：enable
ACT	W	1 / 0	selection of "active high / active low" 0：Active low 1：Active high
PHAN[1..0]	W	0~3	number of phase for output 00：1 phase 01：2 phase 10：3 phase 11：4 phase
SAYM	W	1 / 0	selection of symmetry for PWM 0：asymmetric 1：symmetric
FSW[11..0]	W	0~4095	switching frequency
REF1-REF4	W	0~4095	reference for each phase
SAMP[1..0]	W	0~2	sampling method 01：rising sampling 10：down sampling 11：rising & down sampling
ADCI1-ADCI4	R	1 / 0	sampling trigger signal to ADC

This reveals that the output voltage ripple can be reduce by a factor of n^2. The multi-phase interlaced synchronous buck converter for VRMs can share the load current and reduce the current ripple with a lower switching frequency.

III. HARDWARE IMPLEMENTATION

Fig. 4 is the proposed overall function block diagram of digital VRM controller, included voltage loop controller, current loop controller, and digital interlaced PWM generator. The voltage loop controller is mainly formed by incremental form of PI controller and digital first order IIR filter, this filter can be implemented any type compensator, such as phase-lag, phase-lead, lead-lag compensator etc. The output signal of voltage loop control is applied as command for current loop.

Interlaced digital PWM generator (IDPWM) block offers leading-edge modulation, trailing edge modulation, and dual-edge modulation that sampling frequency could be set. Dead-time that prevents the switches conduct in the same time is programmable in the process of modulation. Phase shifter is placed at the end of the digital control block to generate interlaced PWM signal to each phase. The phase shifter also can be applied in interlaced synchronous sampling signal for A/D. Detail description is as follow.

A. Interlaced synchronous sampling mechanism

The synchronous sampling for inductor current of a

TABLE II
PIN DEFINITION OF THE PROGRAMMABLE INTERLACED DIGITAL PWM GENERATOR

Symbol	Status	Range	Description
Clk	W	0 / 1	Eternal clock, max = 200MHz
RST	W	0 / 1	Reset output 0：disable output 1：enable output
SYMS	W	0 / 1	Symmetric selection 0：symmetric wave 1：asymmetric wave
PHSH	W	0 / 1	Phase shift 0：disable 1：enable
PHN[2..0]	W	0~7	out put phase number = PHN+1
FSW[11..0]	W	0~4095	Switch frequency = FSW/CLK
DT[6..0]	W	0~127	Dead-time = DT/CLK
Vcmd[11..0]	W	0~4095	PWM input signal
ph1-ph4	R	0 / 1	PWM output signal

switching converter plays an important role for the robust control of the current dynamics on a scale of its switching period. Peak current mode control scheme has been employed for the current loop regulation, however, it need a negative slope compensation to ensure stability when operating in high duty range and it also suffers from large discontinuity across the DCM boundary.

Fig. 5 shows the proposed interlaced sampling and control scheme. The sampling of the inductor current is synchronized with the leading edge of PWM signals for both turn-on and turn-off. The proposed sampling scheme have a high noise immunity to the common-mode switching noises induced by the switching of the MOSFET and its parasitic junction capacitances resulted by the heat sink. A true average current signal thus can be measured with accuracy within a switching period. The timing clocks for the digital controller and the digital PWM generator are interlaced with each other to achieve a minimum delay for a same sampling and switching frequency. Fig. 6 shows the hardware circuit of the interlaced synchronous sampling scheme. The signal will be compared first, and then the ADC sampling signal will be generated at the middle of the trailing edge PWM. After selecting the sampling type, there are sampling signal for ADC which correspond the phase number. The relation between phase switching frequency and equivalent system switching frequency can be written as

$$f_{swt} = n \cdot f_{swp} \tag{6}$$

where f_{swt} denotes system output effective switching frequency, f_{swp} is phase switching frequency, and n means the number of phase. The equation only stands while the phase interlaced with $2\pi/n$. Table I is the pin assignment description of the interlaced synchronous sampling scheme.

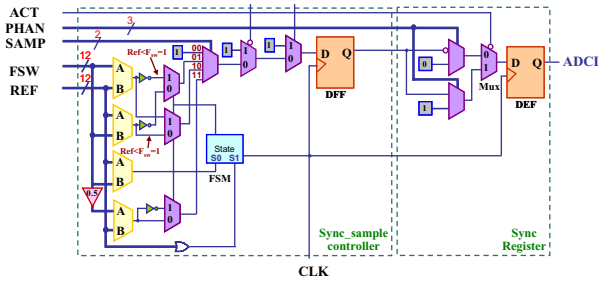


Fig. 6. Hardware circuit of the interlaced synchronize sampling scheme.

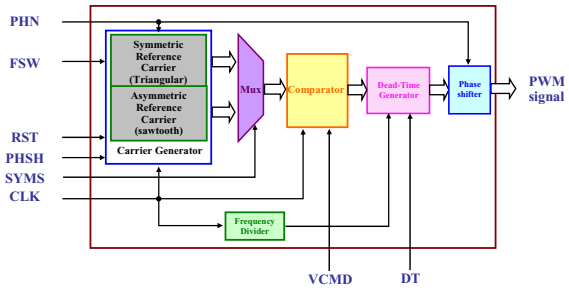


Fig. 7. Programmable interleaved digital PWM generator.

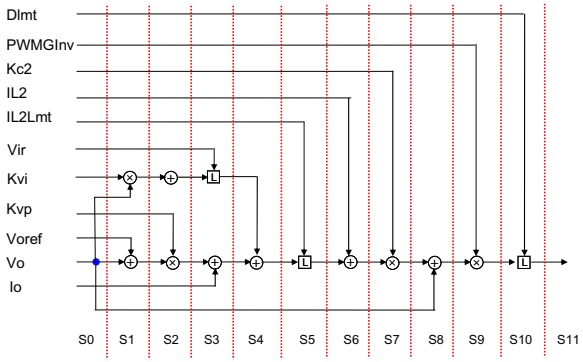


Fig. 8. FSM flow chart of the deadbeat control.

The active mode, phase number, symmetric type, and the sampling method could be chosen.

B. Programmable interlaced digital PWM generator

Fig. 7 shows the functional block diagram of the programmable interleaved digital PWM generator. The PWM generator offer leading-edge modulation, trailing-edge modulation, and dual-edge modulation. Leading-edge modulation and trailing-edge modulation belong to asymmetric reference carrier, while dual-edge modulation belongs to symmetric reference carrier.

From leading-edge modulation scheme, we could get better transient during load-adding event, but not always responsive to load-releasing event. In the other hand, trailing-edge modulation scheme is good for load-releasing transient while it can't guarantee the load-adding transient event.

The switching frequency is programmed by the carrier counter and can be expressed as

$$f_{sw} = \frac{1}{CLK \cdot N_{cnt}} \tag{7}$$

TABLE III
PIN DEFINITION OF THE DEADBEAT CONTROLLER

Symbol	Status	Range	Description
CLK	W	1 / 0	Eternal clock, max = 200MHz
RST	W	1 / 0	controller reset 0：disable 1：enable
D_lmt[11..0]	W	0~4095	Duty limiter
Kc[11..0]	W	0~4095	current loop gain
Kvp[11..0]	W	0~4095	voltage loop proportional gain
Kvi[11..0]	W	0~4095	voltage loop integral gain
IL[11..0]	W	0~4095	inductor loop
IL_lmt[11..0]	W	0~4095	inductor current limiter
Vo[11..0]	W	0~4095	output voltage feedback
Voref[11..0]	W	0~4095	voltage reference
Io[11..0]	W	0~4095	output current feedback
So[11..0]	R	0~4095	controller output

where *CLK* is the system clock and N_{cnt} denotes the bit-length of the carrier counter. Table II shows pin definition of the programmable interlaced digital PWM generator scheme.

C. Digital controller with feed-forward compensation

The control loop may be divided into voltage loop and current loop. In this paper adopted deadbeat control for voltage loop and current loop to achieve good dynamic response. The voltage loop and current loop deadbeat control law can be derived as follow [11]

$$i_{com}(k)=\left(K_{vp}+\frac{K_{vi}}{z-1}\right)\cdot[v_{com}(k)-v_o(k)]+\frac{1}{n}i_o(k) \quad (8)$$

$$v_{ci}(k)=K_{ci}[i_{com}(k)-i_{Li}(k)]+v_o(k), \quad i=a,b,c,d \quad (9)$$

in (8), $i_{com}(k)$ is current loop command per phase, $v_{com}(k)$ is voltage loop command, $v_o(k)$ is output voltage feedback, $i_o(k)$ is output current feedback, n is the number of phase, K_{ci} is deadbeat control law gain of current-loop and $K_{ci} = L_i/T_s$. In (9), $i_{Li}(k)$ is inductor current feedback per phase, $v_{ci}(k)$ is PWM modulated voltage per phase, i denotes the phase sequence, K_{vp} is deadbeat control law gain of voltage-loop and $K_{vp} = C_o/T_s$, K_{vi} is integral gain of voltage-loop. The large load current change with high slew-rate will result significant voltage transients. In order to improve the transient response and reduce the steady-state error, we can include an integrator into voltage control loop to reduce its steady-state error. Table III shows the pin definition of the deadbeat controller. To minimize circuit realization of the adder and multiplier, a scheduling strategy for realizing the compensator by using finite-state-machine (FSM) is presented. Fig. 8 shows the flow chart of FSM of the deadbeat controller. The computing process of both control loops takes one adder, one unit delay register, and one multiplier. Furthermore, the control parameters can be tuned. The first half process take charge in counting the voltage loop control, while the last five states is used to perform the current control loop.

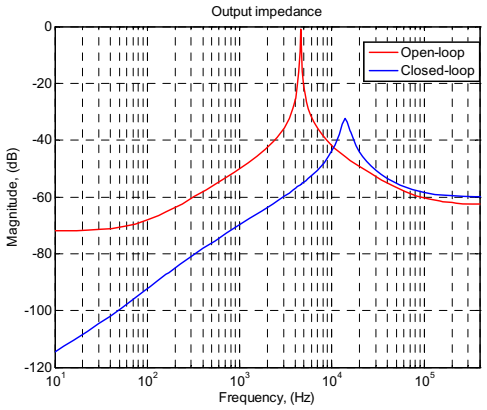


Fig. 9. Frequency response of output impedance of the multi-phase synchronous buck converter.

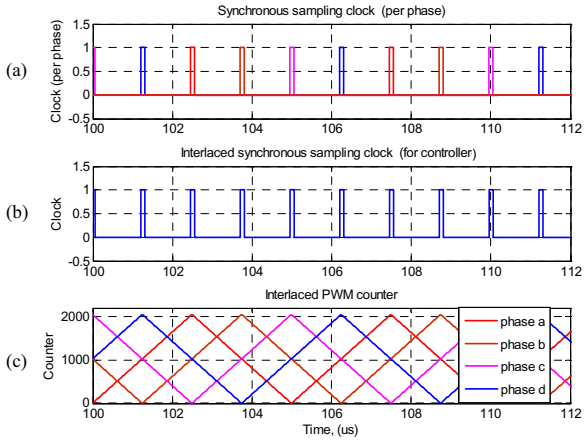


Fig. 10. Experimental results of the interlaced synchronous sampling.

Fig. 9 shows frequency response of output impedance for the multi-phase synchronous buck converter with open-loop and closed-loop control. At low frequency which is less than resonant frequency, it has -60dB gain under open-loop, and the digital controller can attenuate gain of output impedance.

In the voltage loop, proposed novel feed-forward method is presented. A concept as the output current of the VRM demanding depends on the execution of pipelined instructions which can be synchronized by a replica tick generated by a replica slice of the target microprocessor.

In the literatures, sensing output current feedback to control loop can improve output voltage transient. However, it is influence by line parasitic elements, the output current of the VRM slew rate is lower than the equivalent current of the microprocessor (microprocessor slew rate is 1.6A/ns, VRM output current slew rate is 30A/μs [12]). Both microprocessor applied load changing information and control loop architecture are proposed. The feed-forward control signal information is indirectly obtained by the

TABLE IV
CONVERTER DESIGN PARAMETERS

V_o reference voltage	2V
V_i input voltage	5V
P_o full load output power	100W
n number of phase	4
f_{sw} switching frequency	200 KHz
L_i phase inductors (i=1,2,3,4)	50nH
C_o output capacitor	5mF
r_L inductance equivalent series resistance	1mΩ
r_C capacitor equivalent series resistance	1mΩ

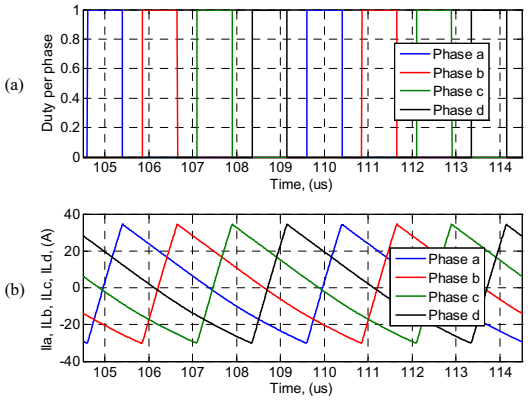
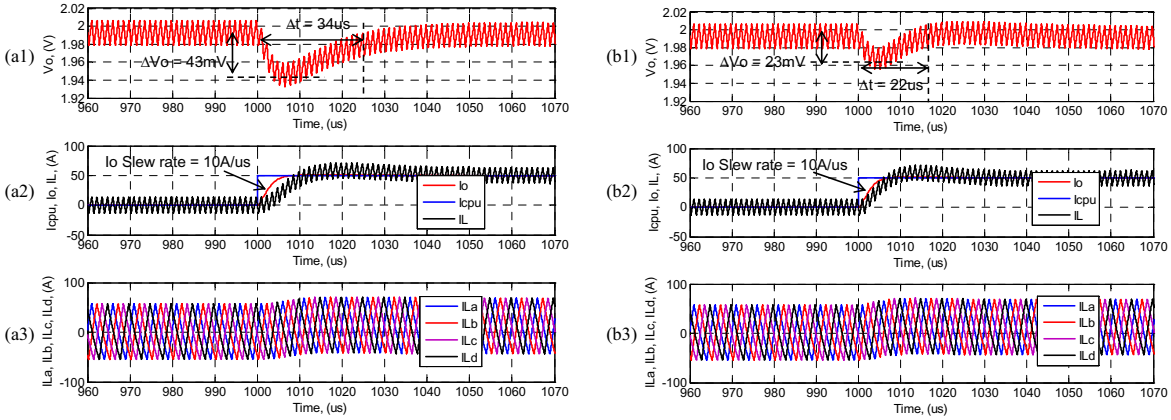


Fig. 11. Experimental results of the 4-phase interlaced PWM generator.



(a) without feed-forward control. (b) with feed-forward control.

Fig. 12. Simulation results for the feed-forward control under deadbeat control.

predictive results of microprocessor. The signal is applied into the control loop to improve the system dynamic response. Therefore the information could speedup the system dynamic under large load current transients.

IV. SIMULATION AND EXPERIMENTAL VERIFICATION

This simulation platform is based on integrated with the Matlab/Simulink and Modelsim simulation software. The Simulink does not only simulate the digital signal processing, but also offer the simulation of the analog environment. Thus, we could quickly revise the errors. We used the power block set toolbox of Simulink and constructed a multi-phase synchronous buck converter, according to the VHDL language design and implement digital controller. Experimental verification of the designed digital VRM controller is realized by using a single-chip FPGA (EP2C35) from Altera. The FPGA has been widely used in digital logic circuit design due to its flexibility and its short time to market. Design parameters of the constructed VRM are listed in Table IV. The experimental result of the interlaced synchronous sampling Over-sampling scheme of the load current is shown in Fig. 10. Fig. 10(a) shows the sampling signal of each phase and the pulse signal is synchronized with peak of the dual-edge PWM reference as shown in Fig. 10(c), and Fig. 10(b) is the clock signal for synchronous sampling signal.

Fig. 11 shows experimental results of the four-phase interlaced PWM generator, switching frequency is 200 KHz per phase, duty of per phase is 16% by considerate deadtime is 0.4μs. From Fig. 11 we may observe that the PWM signal of each other differ 90^0 per phase each other. Fig. 12 shows simulation results of the transient responses for VRM output voltage with and without the proposed feed-forward control. Simulation condition is the output current of VRM from 0.2A changing to 50A and slew-rate of load current 10A/μs. In Fig. 12(a), the output voltage drops to 43mV, and settling time is 34μs. Fig. 12(b) shows that the output voltage drops to 23mV, and settling time is 22μs. Comparing simulation results both Fig. 12(a) and Fig. 12(b), we may find out that the better output voltage transient response could be obtained by using proposed method.

V. CONCLUSION

This paper presents a digital VRM controller for multi-phase synchronous buck converter for advanced microprocessors. The digital VRM controller includes a novel interlaced sampling, a digital compensator, and an interlaced PWM generator. The proposed sampling scheme have a high noise immunity to the common-mode switching noises induced by the switching of the MOSFET, and its parasitic junction capacitances resulted by the heat sink, The timing clocks for the digital controller and the interlaced PWM generator are interlaced with each other to achieve a minimum delay for the same sampling and switching frequency. Event driven is used for the proposed feed-forward controller to result appropriate compensate quantity, like reduce sensor cost. The event driven can predictive load varying range to predictive compensation, and the faster dynamic response will be obtained. Experimental verification of the designed digital VRM controller has been realized by using a single-chip FPGA. Experimental results show the designed digital VRM controller can achieve a fast dynamic response.

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