Abstracts of Current Computer Literature

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1) LOGIC AND SWITCHING THEORY; SEQUENTIAL MACHINES

Use of Predicate Calculus in Proving Correctness and Other Properties of Programs—*see* 8812.

Resolution Theorem-Proving in Predicate Calculus—*see* 8828.

Resolution Graphs for Deductions in First-Order Predicate Calculus—*see* 8833.

8776

A Note on the Solution of Sequential Boolean Equations, J. W. Ulrich (U. New Mexico, Albuquerque, N. Mex.); *IEEE Trans. Comput.* (Short Notes), vol. C-20, Feb. 1971, pp. 231–234.

The problem of solving sequential Boolean equations is examined in terms of nondeterministic finite transducers. An upper bound for the delay is established and a method for obtaining a deterministic equivalent is described.

8777

Three-Level Realizations for Threshold Functions, C. W. Hoffner, II, and J. P. Robinson (U. Iowa, Iowa City); Rep. THEMIS-UI-TR-24, 26 pp., July 1970; CFSTI, AD 714 168, $3.00.

The paper considers three-level AND-OR gate realizations for threshold functions. The three-level realizations presented require substantially fewer gates and gate inputs than the minimum gate two-level realizations for the same functions. For example, the minimum gate two-level realization for the seven-or-more out of 14 function requires 3004 gates and 21 021 gate inputs; the three-level realization presented for this function requires 120 gates and 658 gate inputs.

Accelerated Relaxation Method for Threshold Switching Theory—*see* 8842.

8778

Complexity of Partially Defined Combinational Switching Functions, D. R. Smith (State U. New York at Stony Brook, Long Island); *IEEE Trans. Comput.*, vol. C-20, Feb. 1971, pp. 204–208.

The complexity of the switching networks necessary to realize arbitrary combinational functions is studied. Asymptotic upper and lower bounds for fully defined functions are well known, while lower bounds also exist for partially defined combinational functions. The present paper supplements these results with the upper bounds for the partially defined functions. The results have possible relevance to pattern recognition.

8779

Algebraic Fault Analysis for Constrained Combinational Networks, G. E. Whitney (Western Electric Corp., Princeton); *IEEE Trans. Comput.*, vol. C-20, Feb. 1971, pp. 141–148.

A sequential machine that processes its inputs without changing state can be represented as a constrained combinational network. A system of Boolean equations that represent such a network must include assertions that formalize the required constraints. These constraints can be expressed as assertions about certain gate inputs and certain gate outputs within the network. In such networks, redundant and partially redundant gates are not pathological. The fault analysis method presented provides for the testing of both sides of an irredundant gate and for the detectable side of a partially redundant gate. Given the appropriate system of equations, the solution set for this system defines the test vectors for a particular fault. If the solution set is empty, then no test exists. Obtaining the solution to such a system of equations is equivalent to proving a theorem about the network. A procedure is given for solving the equations using alternating strategies which provides an efficient search through the solution space.

8780

An Investigation into Redundancy and Testability of Combinational Logic Networks, R. Dandapani, S. M. Reddy and J. P. Robinson (U. Iowa, Iowa City); Rep. THEMIS-UI-TR-32, 29 pp., Sept. 1970; CFSTI, AD 714 157, $3.00.

Some results on redundancy and testability of combinational logic networks are given. It is shown that there exist tree networks that are testable relatively easily for redundancy and faults. It is also shown that the multilevel networks proposed not only require less hardware but also fewer tests to detect faults than the equivalent two-level networks.

8781

Topological Solution of Bilateral Switching Networks, L. Mazer (Ames Res. Cen., Moffett Field); *IEEE Trans. Comput.* (Short Notes), vol. C-20, Feb. 1971, pp. 234–238.

A method is described for synthesizing bilateral switching networks using a topological solution that does not employ algebraic or linear graph techniques. Using the eye as a pattern detector, one may trace an optimum path directly on the truth table from the input to the one or more desired outputs. This method overcomes many of the difficulties that have been encountered with relay contact logic, and at the same time helps the logician seek a planar symmetrical solution that is so desirable for monolithic circuits composed of MOS (metal–oxide semiconductor) devices.

8782

Ambiguity in Graphs and Expressions, R. Book (Harvard U., Cambridge), S. Even (Weizmann Inst. of Sci., Rehovot, Israel), S. Greibach (UCLA, Calif.); and G. Ott (Sperry Rand Res. Cen., Sudbury); *IEEE Trans. Comput.*, vol. C-20, Feb. 1971, pp. 149–153.

A regular expression is called unambiguous if every tape in the event can be generated from the expression in one way only. The flow-graph technique for constructing an expression is shown to preserve ambiguities of the graph, and thus, if the graph is that of a deterministic automaton, the expression is unambiguous. A procedure for generating a nondeterministic automaton which preserves the ambiguities of the given regular expression is described. Finally, a procedure for testing whether a given expression is ambiguous is given.

8783

Cellular Multihead Turing Machine, L. Librizzi (Polytechnic Inst. of Brooklyn, Farmingdale); Rep. PIBEP-70-058, RADC-TR-70-181, 45 pp., Sept. 1970; CFSTI, AD 714 557, $3.00.

The Turing machine is a mathematical model for describing procedures. It can do any calculation that can be done by modern day computers. One disadvantage of the Turing machine is its very slow speed. One way to increase the speed is to increase the number of states of the machine or the number of symbols that the machine can read and write. Another way to increase the speed without increasing the complexity to a great extent is to use a cellular approach and not use a fixed number of heads. New heads will be generated whenever needed and these new heads will generate as many more heads as needed to do the job. Whenever a head completes its assigned task it will disappear. A system that does this is investigated and a few examples are worked out, including a universal type of multihead Turing machine. It is shown that the multihead machine is actually doing a parallel type of processing instead of the serial type done by the single-head machine.

8784

A Linked List Structure for the Description of Directed Graphs and its Application to Synthesis and Reduction of Special Finite State Automata, R. Hartenstein (Inst. Nachrichtenverarbeitung und Nachrichtenübertragung der Universität Karlsruhe); *Elektron. Rechenanl.*, vol. 12, Aug. 1970, pp. 208–216.

The principles of programming an algorithm for synthesis and reduction of finite state acceptors and similar structures are described. The algorithm is based on a modified signal flow graph technique, known from the solution of linear algebraic equation systems. For the description of directed graphs for finite state automata and regular expressions a special list structure is used, which allows efficient storage requirements and computing time.

8785

Periodic Representations and *T*-Partitionable Equivalents of Sequential Machines, J. W. Grzymala-Busse (U. Poznan, Poland); *IEEE Trans. Comput.*, vol. C-20, Feb. 1971, pp. 190–198.

This paper deals with the problem of finding nontrivial periodic representations, which not necessarily null transient duration, of deterministic sequential machines. The well-known results in this area, based on means of d-equivalence partitions or regular d-partitions on the set of internal states of a sequential machine A, are generalized. Apart from this, the problem of finding nontrivial periodic representations of A is solved by the well-known methods of input-independent partitions on the set of internal states of A and by the operation of the (τ, T) numeration introduced here. Furthermore, the problem of determining T-partitionable equivalents of a sequential machine is solved. It is shown that, for a strongly connected machine A, a minimal T-partitionable equivalent of A is the fixed analog of the extension of the maximal periodic representation of A. Moreover, for a connected machine the bound for the cardinality of the state set for the minimal T-partitionable equivalent of A is given. The algorithm for determining the minimal T-partitionable equivalents of a connected machine is presented.

8786

A Remark on the Concepts of Input-Memory and Output-Memory of Sequential Machines; *IEEE Trans. Comput.* (Corresp.), vol. C-20, Feb. 1971, p. 239.

The definitions of input memory and output memory of a sequential machine are examined and an attempt is made to clarify some confusion in the literature regarding the concepts of input memory and output memory.

8787

A Realizable Model for Stochastic Sequential Machines, S. E. Gelenbe (U. Michigan, Ann Arbor); *IEEE Trans. Comput.*, vol. C-20, Feb. 1971, pp. 199–204.

A new model for stochastic sequential machines is introduced. This model consists of a deterministic Mealy-type synchronous sequential machine some of whose inputs are random number generators while the outputs of another set of random number generators are used to perturb the output function of the deterministic Mealy machine. Thus this model is physically realizable in terms of random number generators, logic, and memory elements. It is shown that this model and the Shannon model of a stochastic sequential machine are coextensive and a procedure is given, through a proof of this result, for obtaining one from the other.

8788

An Improved Method of Prime *C*-Class Derivation in the State Reduction of Sequential Networks, R. G. Bennetts (U. Southampton, Southampton, England); *IEEE Trans. Comput.* (Short Notes), vol. C-20, Feb. 1971, pp. 229–231.

The state reduction of sequential networks is achieved by selecting a minimal set of prime *C* classes satisfying the cover and closure requirements. The derivation of all the *C* classes and subsequent prime *C* classes has been illustrated by Grasselli and Luccio and relies on maximal *C*-class decomposition. In this note, an alternative method for deriving the prime *C* classes is described. The method does not involve the maximal *C* classes and is algorithmically easier to implement.

8789

The Avoidance and Elimination of Function Hazards in Asynchronous Sequential Circuits, R. R. Hackbart (General Motors Corp., Milwaukee) and D. L. Dietmeyer (U. Wisconsin, Madison); *IEEE Trans. Comput.*, vol. C-20, Feb. 1971, pp. 184–189.

Armstrong *et al.* have shown how critical races and function hazards can be suppressed in asynchronous sequential circuits by using gate delays to advantage rather than introducing explicit delay elements, if certain delay assumptions are satisfied. This paper shows that the same techniques may be used to design circuits which will respond reliably to simultaneous changes of several input variables. Theorems are presented which enable one to identify rows of a flow table that are free of function hazards and others that contain function hazards which can be avoided with the techniques of Armstrong. Those row function hazards which cannot be so avoided are eliminated by introducing a "hazard" variable.

8790

Generation of a Clock Pulse for Asynchronous Sequential Machines to Eliminate Critical Races, J. G. Bredeson and P. T. Hulina (Penn. State U., University Park); *IEEE Trans. Comput.* (Short Notes), vol. C-20, Feb. 1971, pp. 225–226.

A circuit for generating a clock pulse for asynchronous circuits is given, and when used with transition sensitive flip-flops eliminates critical races for an arbitrary state assignment. Thus the minimum number of internal variables may be used. Furthermore, logic and sequential hazards will not affect the circuit performance.

2) DIGITAL COMPUTERS AND SYSTEMS

Modular LSI Control Logic Design with Error Detection—*see* 8792.

3) LOGIC DEVICES AND CIRCUITS (HARDWARE)

8791

An Iterative Array for Multiplication of Signed Binary Numbers, J. C. Majithia and R. Kital (McMaster U., Hamilton, Ont., Canada); *IEEE Trans. Comput.* (Short Notes), vol. C-20, Feb. 1971, pp. 214–216.

An iterative array for multiplication of signed binary numbers is described. It uses controlled adder–subtractor cells. The negative numbers are in two's complement form and the product, if negative, is also available in this form without requiring any additional operations.

8792

Modular LSI Control Logic Design with Error Detection, W. N. Toy (Bell Tel. Labs., Naperville); *IEEE Trans. Comput.*, vol. C-20, Feb. 1971, pp. 161–166.

This paper describes a modular approach of implementing control circuitry. It is achieved by the use of multifunctional binary decoder circuits in conjunction with a transistor array high-speed READ-ONLY memory. In decoding the binary to one-out-of-*N* operation, faults in the circuitry may cause errors in the output. The concept of odd and even parity of the binary data is used in sorting the *N* decoder outputs into two groups; one contains odd parity input combinations, the other even parity input combinations. If an extra output is produced for any single input fault, the error occurs in the output belonging to one group and the correct output belongs to the other group. This scheme provides an effective method of detecting decoder faults. The use of the decoder circuits with built-in error detection together with a transitor emitter array gives a modular integrated design of the control functions.

8793

Enhancing Testability of Large-Scale Integrated Circuits via Test Points and Additional Logic, M. J. Y. Williams (Stanford U., Stanford); Rep. TR-4602-1, SU-SEL-70-065, 71 pp., Sept. 1970; CFSTI, AD 714 511, $3.00.

This report studies methods of using test points in conjunction with additional logic gates to provide an easy means to set or check the state. Among several logic modification schemes, the most useful appears to be one in which a single test point can be used to switch the circuit into a second mode of operation, a "test mode." In the test mode the flip-flops are reconnected to form a shift register, so that the state can be easily set or checked: however it is not possible to guarantee correct operation in this mode in the presence of a fault. After an initial state has been set, the circuit can be switched to normal mode for a test, then returned to the test mode so that the final state can be checked. For a synchronous sequential circuit whose state can be easily set or checked, the problem of generating a test to detect a given logical fault reduces to the problem of generating a test for the fault in a purely combinational network of similar complexity. The cost of such circuit modifications is analyzed.

Use of Error Correcting Codes in Integrated Circuit Memory Arrays—*see* 8836.

Topology of Monolithic MOS Switching Circuits—*see* 8781.

8794

Magnetoelastic Resonance Characterization of Core Plane Assemblies, B. Mills (IBM Corp., Kingston); *IEEE Trans. Magn.*, vol. MAG-6, Sept. 1970, pp. 682–684.

Magnetostrictively induced elastic resonance (MER) of a ferrite core serves as a technique for characterizing the core in the environment of the plane assembly and differentiating core anomalies from wiring induced anomalies not discernable by pulse techniques alone. The shifts of the resonant frequencies as a result of the change in a core from a constrained to an unconstrained mechanical state explains the ability of the MER technique to discriminate unambiguously between damaged and undamaged cores.

History Effect of Ferrite Cores as Analog Storage Elements—*see* 8863.

8795

Coercive Force Measurements in Plated Wire, J. H. Chaffin, III (Honeywell Res. Cen., Hopkins); *IEEE Trans. Magn.*, vol. MAG-6, Sept. 1970, pp. 573–576.

Coercive force values for plated wire as determined on a conventional hysteresis looper are discussed. In particular, the variation of H_c with easy-axis drive amplitude as well as the lack of agreement between the looper H_c and the easy-axis disturb threshold for a discrete bit written into the plated wire is investigated. It has been confirmed that the H_c variation is a rise-time, not a drive amplitude, effect. In addition, the disagreement between the discrete bit digit-disturb threshold and the looper H_c occurs because the looper cannot measure any value below the nucleation threshold of the plated wire.

8796

Effect of On-Line Flash Anneal on Aging Properties of NDRO Multilayer Plated Wire, M. Terajima, Y. Gomi, and H. Ikawa (Nippon Telegraph and Telephone Public Corp., Tokyo, Japan); *IEEE Trans. Magn.*, vol. MAG-6, Sept. 1970, pp. 716–719.

Aging properties of the plated wire stabilized by on-line flash annealing for 6 s were investigated and a sufficient stabilizing effect has been obtained. The wire has a multilayer construction including three Permalloy layers and two Ni-Co hard layers, and has good nondestructive readout (NDRO) properties. Aging was accelerated by dc and pulsed hard-axis fields at temperatures between 50°C and 150°C. The largest change has been found in I_{d2} which is the upper limit of the digit current margin. Provided that life-time is the time required for the 10 percent I_{d2} degradation, a typical wire has a lifetime of 100 years under the dc hard-axis field at 40°C. According to the extrapolation from the lifetime distribution of the wires, the first failure bit in a million bits operating under dc field at 40°C is predicted after 20 years. Since in actual memory devices the wires are driven by a word pulse field instead of a dc field, much longer time will be required before the first failure.

4) DIGITAL STORAGE AND INPUT-OUTPUT EQUIPMENT

8797

FET Memory Systems, L. M. Terman (IBM Corp., Yorktown Heights); *IEEE Trans. Magn.*, vol. MAG-6, Sept. 1970, pp. 584–589.

The metal–oxide–semiconductor field-effect transistor (MOSFET) is finding widespread application as a technology for memory systems, due both to advantageous device and technology characteristics, and to the unique requirements of the memory environment. The technology has proven quite versatile, and among the applications are random access systems, shift registers, and READ-ONLY storage. Both complementary and noncomplementary technologies have been used. The background and philosophy of using MOSFETS as a memory technology are reviewed, and the recent developments, trends, and the current state of the art are summarized.

Transistor Array High-Speed READ-ONLY Memory for Modular Control Circuitry—*see* 8792.

8798

Two New Integrated Ferrite Memories for Non-Desctructive Read-Out, F. Wittgruber (Inst. Nachrichtenverarbeitung der Technischen Hochschule Darmstadt); *Elektron. Rechenanl.*, vol. 12, Aug. 1970, pp. 193–200.

Two new ferrite memories are described. Important advantages of these memories are nondestructive readout and batch fabrication. Binary information is stored by saturating the ferrite material around a hole. For reading information only reversible flux change is used. Physical dimensions, developed by computations and laboratory tests, are given. Finally, the two ferrite memories are compared.

8799

The Stapelblock: A Novel Technique for Manufacturing Highly Reliable Ferrite Core Memory Stacks, W. Maiwald (Siemens Co., Munich, Germany); *IEEE Trans. Magn.*, vol. MAG-6, Sept. 1970, pp. 684–687.

In an effort to arrive at highly reliable ferrite core storages of low weight, small dimensions, and high mechanical strength under dynamic loads, a new technique has been developed for the manufacture of the so-called Stapelblock. In contrast to conventional designs, the matrix planes are glued one on top of the other and the whole stack is attached to a single common base plate. This solidly bonded sandwich is an extremely compact unit of high inherent mechanical stability. Each matrix plane consists of a thin plate to which the cores are bonded elastically. Those drive wires which link all planes are threaded in during the manufacturing process as single lengths of wire. It has, therefore, been possible to eliminate the frames usually required for accommodating the wire terminals as well as all internal matrix connections.

History Effect of Ferrite Cores as Analog Storage Elements—*see* 8863.

8800

Two Approaches for Increasing Storage Density in Modern Digital Computing Systems, N. M. Schmitt (U. Arkansas, Fayetteville) and J. L. Melsa (Southern Methodist U., Dallas); *IEEE Trans. Comput.*, vol. C-20, Feb. 1971, pp. 167–175.

Modern digital computing systems are primarily limited in how densely information may be recorded on the magnetic storage elements by the manner in which the information is retrieved (detected) from these storage facilities. Current systems store information at a density around 1000 bits per inch (bit/in); system elements, other than the detection process, could easily handle densities in excess of 3000 bit/in. This paper describes the signal present at the output of the READ-WRITE head and suggests two systems by which detection at high bit densities may be accomplished. The error rate associated with each system is given and the results are applied to a computer system using a magnetic disk file as the storage element. It is demonstrated that these detection procedures can meet the widely accepted standard of one error in one billion bits at reasonable signal-to-noise ratios.

Minimization of Disc Rotational Delay in Time—*see* 8820.

8801

Stress Insensitive Permalloys for Memory Application, T. C. Tisone and W. B. Grupen (Bell Tel. Labs., Allentown), and G. Y. Chin (Bell Tel. Labs, Murray Hill); *IEEE Trans. Magn.*, vol. MAG-6, Sept. 1970, pp. 712–716.

A description of the development of a family of high-squareness low-stress-sensitivity Permalloys of controlled coercive force for application as the soft magnetic element in the piggyback twister-type memory is given. Since both the hard- and soft-magnetic elements are wrapped simultaneously around the conductor core, the magnetic properties of both elements must be optimized by a single post-wrap annealing treatment. Previous work on a Co-Fe-Au alloy as the hard magnetic element has led to an annealing temperature range of 800–900°C, which must now be adopted for the treatment of the soft magnetic element as well. From published data on the compositional dependence of magnetocrystalline anisotropy and saturation magnetostriction in Ni-Fe-Mo alloys, an optimum composition, 6 percent Mo-80.5 percent Ni-13.5 percent Fe was first devised for which $dB_r/d\sigma \simeq 0$, $B_r/B_s > 0.9$, and $H_c \simeq 0.3$ Oe after post-wrap annealing. By adding small amounts of Be (0.4–0.7 percent) or Zr (0.2–0.4 percent), the coercive force can be controlled to any value up to 3 Oe as a result of precipitation. At the same time, low stress sensitivity was retained and squareness improved.

8802

NDRO Thin-Film Memory Device Exhibiting Triangular Hysteresis Loop, H. S. Belson and F. B. DeSavage (U. S. Naval Ordnance Lab., Silver Spring), R. S. Tebble and M. R. Parker (U. Salford, Salford, England); *IEEE Trans. Magn.*, vol. MAG-6, Sept. 1970, pp. 722–724.

Certain thin Permalloy films which have a basically uniaxial character show square hysteresis loops in both easy and hard direction. The hard-direction coercivity H_{c2} is about half that of the easy direction. If a saturating magnetic field is applied at an angle α, a few degrees from the hard direction, a loop typical of uniaxial films results. Application of a small bias field normal to the drive field results in a triangular loop. This has two stable remanent states, in the first of which the magnetization has been left in a hard-direction low-permeability zero state. The other remanent state has the magnetization in a high permeability, easy direction, the one state. Whether the interrogating pulses of magnitude less than H_{c2} will result in an output pulse or not depends on the state of the device. No destruction of the stored information occurs. It is possible to write into either state by using the coincident current techniques, as long as precautions are taken against creep from the hard direction.

8803

Improving Fine Striped Memory Magnetic Properties, S. Oshima, T. Kobayashi, T. Kamibayashi, A. Okada, Y. Komazawa, and K. Komuro (Kokusai Denshin Denwa Co. Ltd., Tokyo, Japan); *IEEE Trans. Magn.*, vol. MAG-6, Sept. 1970, pp. 725–728.

Evaporation, electroplating, and etching were used to develop high-density, high-speed, and low-cost fine striped memory (FSM) which is a planar film memory with completely closed digit line flux paths. The results of three important experiments on FSM and its development, structure, and production are described. Three conclusions have been obtained from the experiments. First, a 300-Å thick evaporated Permalloy undercoating is needed to improve the magnetic properties of the electroplated Permalloy. Second, a completely closed flux path assures full output and operating stability. Third, a flux keeper, which is applied to memory strips, and for which embedded word lines are apart from the strips, assures high signal-to-noise ratio and low driving current. An effective flux keeper has been used to make a high-density (5000 bit/cm^2) memory.

8804

Prediction of Device Performance of Integrated Flat Film NDRO Devices, C. H. Lin and J. F. Fresia (IBM Corp., Essex Junction); *IEEE Trans. Magn.*, vol. MAG-6, Sept. 1970, pp. 660–662.

A simple graphical method is proposed to predict device performance of an integrated flat-film memory cell. The method uses a set of experimentally determined write and creep curves as fundamental design parameters. The method can provide such important information as signal flux and drive currents once the device geometries and keeper permeability are chosen. Good agreement has been obtained between prediction and experiment.

8805

The Physical Analysis of Laminated Ferrite Wafer Individual Storage Element, V. V. Bardidge, E. M. Larin, and V. I. Perekatov (Academy of Sciences of the U.S.S.R., Moscow); *IEEE Trans. Magn.*, vol. MAG-6, Sept. 1970, pp. 677–681.

Physical processes in a laminated ferrite wafer (LFW) storage element are considered. A mathematical technique for calculating the flux reversal processes of the storage element is proposed. The technique makes it possible to evaluate the effect of the address write current on the output signal quantitatively. The problem of the digit current influence on the storage element performance is considered. The threshold value of this current is shown to be determined by the coercitive force of the ferrite times the cross-section perimeter of the digit line.

8806

Uniaxial Anisotropy in Polycrystalline Material, W. H. Gerling (Inst. Werkstoffe der Elektrotechnik, Rheinisch-Westfalische Technische Hochschule, Aachen, Germany); *IEEE Trans. Magn.*, vol. MAG-6, Sept. 1970, pp. 737–741.

A kind of undirectional anisotropy determining one easy direction of magnetization in a limited field range results from the preferential cone for the position of spontaneous magnetization. In single domain particles, the preferential cone causes a constricted magnetization curve, parts of which are similar to a reversible rectifier characteristic that is not found in constricted Perminvar-type loops. The properties of this anisotropy are discussed by the example of hexagonal crystals; calculated magnetization curves and experimental results are given. The characteristic described may be useful in memory application with nondestructive readout and nonlinear applications.

8807

Reconstruction Effects in Magnetic Holography, R. S. Mezrich (RCA Labs., Princeton); *IEEE Trans. Magn.*, vol. MAG-6, Sept. 1970, pp. 537–541.

Magnetic holography, a storage method based on the combination of techniques of magnetooptics and holography, is shown to have features which are unique to either of these techniques. In contrast to the usual situation in magnetooptics, reconstruction may be obtained with either the Faraday or polar Kerr effect, using polarized or unpolarized light. Furthermore the reconstruction will not be elliptically polarized if linearly polarized light is used for readout. In contrast to the usual case in holography, the first-order diffracted wave is polarized at 90° to both the incident and zeroth-order waves. This feature allows a considerable increase in the attainable signal-to-noise ratio in the reconstruction. These and other features are described analytically and demonstrated experimentally.

8808

Polarization and Efficiency in Magnetic Holography, H. M. Haskal (Honeywell, Inc., Waltham); *IEEE Trans. Magn.*, vol. MAG-6, Sept. 1970, pp. 542–545.

Reconstruction effects in a magnetic hologram can easily be interpreted if one assumes a linearly polarized plane wave readout beam. The field transmitted through or reflected off the hologram is rotated via the Faraday or Kerr effect. By decomposing the merging field into two orthogonal components, one can define separate transmission functions for each polarization. The diffracted field and the efficiency of the magnetic grating are readily computed from these transmission functions. For a binary magnetic grating all diffraction orders, with the exception of zeroth order, are polarized orthogonally to the incoming polarization. For a sinusoidal magnetic grating, the various diffraction orders alternate in polarization with the zeroth order polarized in the same direction as the incoming polarization.

8809

Thermomagnetic Writing in GdIG, W. D. Doyle, G. K. Goldberg, and W. E. Flannery (Sperry Rand Corp., Philadelphia); *IEEE Trans. Magn.*, vol. MAG-6, Sept. 1970, pp. 548–553.

A model for thermomagnetic writing in a GdIG platelet held at its compensation temperature is developed and confirming experimental data are presented. It is postulated that magnetization reversal occurs by domain nucleation and expansion. The relationship between the applied field H, the final bit diameter D, and the absorbed energy $P\tau$ is shown to be

$$H = K^{-1}[(D^2\rho cw)/(\alpha P\tau)][(1/2)E_c + \sigma_w/D]$$

where $K=0.112$ is a normalization constant, ρ the density, c the specific heat, w the sample thickness, α a constant relating the magnetization and the temperature, E_c the domainwall coercive pressure, and σ_w the wall energy per unit area. Domains with $D<D_c=2\sigma_w/E_c$ are unstable and collapse when the sample returns to the compensation temperature. Measurements are reported of the dependence of D on H for several values of $P\tau$ for a 13-μm thick platelet of aluminum doped GdIG. The quantitative agreement between theory and experiment is good. Observations of domain switching during the heat pulse application confirm all the major features of the model. The results show that in thick and low coercive force platelets, an excessive amount of power is required to write at moderate fields and the bit density is limited by the instability for $D<D_c$. Typical values are $P=100$ mW, $\tau=1$ μs, $H=100$ Oe, and $D_c=20$ μm. In thin and high coercive force films it should be possible to write 10-μm size bits with a field of <100 Oe and a power level of 10 mW absorbed in 1 μs.

8810

An Experimental Micropicture Mass Storage System for Retrieval and Transmission of Information, F. Schön (Siemens AG, München); *Elektron. Rechenanl.*, vol. 12, Aug. 1970, pp. 201–207.

This article describes the general principles and functions of an experimental system for the true and faithful storage, retrieval, and transmission of textual and pictorial information. Special attention is given to the micropicture technique, the method of selecting certain picture sections for recognizing details, and narrow-band information transmission with multipicture video recording at the individual terminals. After dealing with the functions and design of the positioning and transmission unit, which is attached to the mass storage, the article goes on to describe the interoperation with an information retrieval system and the practical application of the overall system with the aid of an example taken from the field of engineering design.

8811

Strain-Biased Ferroelectric-Photoconductor Image Storage and Display Devices, J. R. Maldonado and A. H. Meitzler (Bell Tel. Labs., Murray Hill); *Proc. IEEE*, vol. 59, Mar. 1971, pp. 368–382.

A device suitable for image storage and display applications is described in which the image is stored as a spatially varying birefringence and can, by means of suitably polarized light, either be observed directly or projected onto a viewing screen. The basic device consists of a sandwiched structure of uniform thickness layers, comprising transparent electrodes, a photoconductive film, and a plate of fine-grained ferroelectric ceramic. In order to establish a preferred orientation of the polarization in the plane of the plate, a uniform strain is induced in the plate by placing it either in tension or compression ("strain biasing"). The plate then becomes birefringent, with the principal axes of the optical indicatrix along the strain axes. The magnitude of this birefringence can be controlled by an electric field applied in the thickness direction, and this forms the biasis of the device operation. In operation, the image to be stored is projected or scanned onto the photoconductive film. A voltage applied to the transparent electrodes develops, in the ceramic, a transverse field having an intensity modulated by the photoconductive film. When the field is removed, the desired image is stored as a spatial modulation of the birefringence of the ceramic plate. To erase the image the entire structure is flooded with light in the presence of an electric field in the reverse direction, and the plate regains its initial state of uniform birefringence. A large number of experimental devices have been fabricated and tested in the laboratory. In addition to describing the basic device structure, experimental results are presented showing the level of performance obtained from present devices, and a physical interpretation of device operation in terms of domain switching processes is provided.

Light Pen Input of Patterns and Their Recognition—*see* 8827.

5) PROGRAMMING OF DIGITAL MACHINES

8812

The Application of Formal Logic to Programs and Programming, C. D. Allen; *IBM Syst. J.*, vol. 10, no. 1, 1971, pp. 2–38.

The use of first-order predicate calculus in proving correctness and other properties of programs is shown to be possible in practical stiuations. The necessary concepts and theory are explained and some practical examples are worked through.

8813

Conversion of Limited-Entry Decision Tables to Computer Programs—A Proposed Modification to Pollack's Algorithm, K. Shwayder (U. Chicago); *Commun. Ass. Comput. Mach.*, vol. 14, Feb. 1971, pp. 69–73.

Pollack has proposed an algorithm for converting decision tables into flow charts which minimize subsequent execution time when compiled into a computer program. Two modifications to this algorithm are proposed. The first relies on Shannon's noiseless coding theorem and the communications concept of entropy but does not completely test the ELSE rule. The second modification completely tests the ELSE rule but results in more executions than the first modification. Both modifications result in lower execution time than Pollack's algorithm. However, neither modification guarantees a globally optimal solution.

8814

CYLINDERS: A Relational Data Structure, P. E. Weston (U. Illinois, Urbana); Rep. TR-18 AFOSR-70-2584TR, 84 pp., Feb. 1970; CFSTI, AD 714 607, $3.00.

A form of list structure is described which permits an efficient representation of relational data structures. The general notions of the PLEX and of ring structures, because of their proven value, have been used as a basis; but by systematically treating the array structure of the PLEX as an implicit form of linkage which is complementary to the explicit links carried by pointers, a new form of linked data structure emerges, which is called CYLINDER. While CYLINDERs are built up from two or more simple rings of pointers, they characteristically exhibit a multiplicity of closed search paths, which are usable in the construction of data representations. Examples of CYLINDER applications are discussed and a subroutine system used in CYLINDER programming is described.

Linked List Structure for Describing Directed Graphs for Regular Expressions—*see* 8784.

8815

FORTRAN Extended-Precision Library, H. Kuki and J. Ascoly; *IBM Syst. J.*, vol. 10, no. 1, 1971, pp. 39–61.

This paper discusses a Fortran subprogram library developed primarily to support extended-precision floating-point arithmetic. The general strategy, which makes limited use of guard digits, is developed to achieve high accuracy with reasonable execution time and storage space. In addition to describing some previously unpublished algorithms, the authors present subprograms for simulating extended-precision arithmetic and for input and output conversion.

8816

A Guide to CORAL Programming, A. A. Callaway (Royal Aircraft Estbl., Farnborough, England); Rep. RAE-TR-70102 TRC-BR-20193, 56 pp., June 1970; CFSTI, AD 714 658, $3.00.

Coral is a high-level programming language which is to a large extent machine-independent in that programming in Coral does not normally require special knowledge of the computer on which the program is to run, only of the implementation for that computer. Coral is based broadly on Algol 60 but is extended and improved in many areas. In this report no reference is made to similarities between Coral and Algol; Coral is treated as an individual language and, therefore, no knowledge of other language is necessary for complete understanding. It is intended that this report should serve as a guide both for the novice programmer and for the experienced programmer who wishes to make use of CORAL's special facilities.

8817

Variability in Language Processors, G. E. Lindstrom (Carnegie-Mellon U., Pittsburgh); AFOSR-70-2578TR, 145 pp., July 1970; CFSTI, AD 714 695, $3.00.

The thesis proposes some techniques for the introduction of variability in language processors, in order to achieve more economy and convenience, and suitability to new modes of use. Some of the desired new capabilities are midexecution program recomposition, dynamic program organization, multiple program subexecutions, and programmer interaction with the execution. The modification techniques proposed are applicable to any one-pass processor, but are most effective when applied to highly compilation-oriented languages. A system capable of applying these techniques to an appropriate compiler is designed. Given a compiler description and design parameters for each of the modification techniques listed above, the system can produce an experimental interpreter for the modified language. This new processor then possesses features commonly associated with conversational, simulation, and debugging systems. An example of such a design is provided in the form of a conversational Simula system design. The resulting system possesses features present in Simula 67, as well as new features not previously available.

8818

A Technique for Generating Interpretive Translators for Problem-Oriented Languages, E. L. Murphree, Jr., and S. J. Fenves (U. Illinois, Urbana); *BIT*, vol. 10, no. 3, 1970, pp. 310–323.

This paper presents a technique for generating translators for problem-oriented and other command- or data-oriented languages which can be interpretively executed. The system consists of: 1) a stored grammar or table, representing in a modified graph form the syntactically valid statements and the corresponding semantic actions; 2) a set of application procedures, written in a procedural language; 3) a universal translator, which performs reading, input conversion, matching input items against the grammar, and calling the procedures specified by the grammar. The generator consists of the translator and a specific grammar and set of procedures, which together convert the problem-oriented description of the source grammar into the table used by the translator for execution.

8819

Parallel Processing with the Perfect Shuffle, H. S. Stone (Stanford U., Stanford); *IEEE Trans. Comput.*, vol. C-20, Feb. 1971, pp. 153–161.

Given a vector of N elements, the perfect Shuffle of this vector is a permutation of the elements that are identical to a perfect shuffle of a deck of cards. Elements of the first half of the vector are interlaced with elements of the second half in the perfect shuffle of the vector. It is indicated by a series of examples that the perfect shuffle is an important interconnection pattern for a parallel processor. The examples include the fast-Fourier transform (FFT), polynomial evaluation, sorting, and matrix transposition. For the FFT and sorting, the rate of growth of computational steps for algorithms that use the perfect shuffle is the least known today, and is somewhat better than the best rate that is known for versions of these algorithms that use the interconnection scheme used in the Illiac IV.

Cellular Multihead Turing Machine That Does Parallel Processing—*see* 8783.

8820

Analysis of Some Time-Sharing Techniques, N. R. Nielsen (Stanford U., Stanford); *Comm. Ass. Comput. Mach.*, vol. 14, Feb. 1971, pp. 79–90.

The effectiveness of certain time-sharing techniques such as program relocation, disk rotational delay minimization, and swap volume minimization is investigated. Summary data are presented, and the findings are discussed. The vehicle for this investigation was a Simula based simulation model reflecting an early framework for a planned Burroughs B6500 time-sharing system. Inasmuch as the B6500 system is based upon the use of variable sized segments and a dynamic overlay procedure, data is also presented which provides some indication of the effectiveness of this type of organization in a time-sharing environment. The design characteristics and operational capabilities of the simulation model are also described.

8821

A Policy-Driven Scheduler for a Time-Sharing System, A. J. Bernstein and J. C. Sharp (General Electric, Schenectady); *Commun. Ass. Comput. Mach.*, vol. 14, Feb. 1971, pp. 74–78.

The services received by a processor for a time-sharing operating system can be characterized by a resource count w_iR_{ij} where R_{ij} is the number of units of service received by process j from resource i and wi is the cost per unit of the service. Each class of users can be characterized by a policy function which specifies the amount of service a user who belongs to this class should receive as a function of time. Priority changes dynamically as a function of the difference between the service promised to the user by the policy function and the service he actually receives. A scheduling and swapping algorithm which keeps the resource count of each process above its policy function will provide the specified level of service. Overhead can be reduced by avoiding swaps of processes which have received at least this level of service. The algorithm has been implemented in a general purpose operating system, and it has provided significantly better service to interactive and to batch jobs than the previous scheduler.

8822

On the Probability Distribution of the Values of Binary Trees, H. Hurwitz, Jr. (General Electric, Schenectady); *Commun. Ass. Comput. Mach.*, vol. 14, Feb. 1971, pp. 99 102.

An integral equation is derived for the generating function for binary tree values, the values reflecting sorting effort. The analysis does not assume uniformly distributed branching ratios, and therefore is applicable to a family of sorting algorithms discussed by Hoare, Singleton, and van Emden. The solution to the integral equation indicates that using more advanced algorithms in the family makes only minor reductions in the expected sorting effort, but substantially reduces the variance in sorting effort. Statistical tests of the values of several thousand trees containing up to 10 000 points have given first, second, and third moments of the value distribution function in satisfactory agreement with the moments computed from the generating function. The empirical tests, as well as the analytical results, are in agreement with previously published results for the first moment in the cases of uniform and nonuniform distribution of branching ratio, and for the second moment in the case of uniform distribution of branching ratio.

8823

A New List-Tracing Algorithm, R. R. Fenichel (M.I.T., Cambridge); Rep. MAC-TM-19, 28 pp., Oct. 1970; CFSTI, AD 714 522, $3.00.

List-processing systems have each allowed use of only a single size and configuration of list cell. This paper describes a system which allows use of arbitrarily many different sizes and configurations of list cell, possibly not specified until run time.

8824

PADEL—A Pattern Description Language, K. J. Breeding (Ohio State U., Columbus); Rep. ESL-2768 AFOSR-70-2586TR, 44 pp., June 1970; CFSTI, AD 714 594, $3.00.

A large class of optical pattern recognition problems may be described in terms of line drawings. Such line drawings are particularly amenable to the composition of strings of descriptors which may be processed in many ways to produce picture rotations, reflections, and others as well as to extract pattern features. The paper describes line drawings in symbol strings. The language is a transformational grammar in which elements of the line drawings, or picture, correspond to elements in the description. The correspondence is reversible so that given a grammatically correct string in Padel a line drawing may be constructed. Using the language, several topological transformations are described in which the picture is modified by simple manipulation of the strings. First the simple transformations of rotations, reflections, and scale changes are described. Then a nonuniform, one-dimensional scale change is described in which the pictures scale is changed along one axis only. This may be termed "rubber sheet warping." Finally the process of identifying pattern feature is described. It is then shown how PADEL may be applied to the recognition of fixed oriented line drawings. Thus, the language is shown to be very useful in recognizing hand printed alpha numeric characters. Examples of this recognition process are given.

8825

Topological Manipulation of Line Drawings Using a Pattern Description Language, K. J. Breeding and J. O. Amoss (Ohio State U., Columbus); Rept. ESL-2768-3 AFOSR-70-2585TR, 39 pp., Aug. 1970; CFSTI, AD 714 593, $3.00.

A large proportion of the pictures dealt with in computer graphics are line drawings. In the process of displaying these drawings certain topological manipulations such as rotations, reflections, and scaling may be desired. The paper describes how such manipulations may be carried out by transformations on strings describing the picture. The string language used is a pattern description language called Padel. Pictures in two- and three-dimensional space are considered. The transformations described for two-dimensional pictures are rotations, reflections about an arbitrary axis, and uniform scale changes. A nonuniform scale change consisting of scaling along an arbitrary line is also described. Such scaling may be termed "rubber sheet warping." The pattern description language is next extended to three-dimensional objects by representing the branch labels as three tuples the element of which are the branch direction cosines. Rotations of the pictures about the coordinate axis are then described. It is then shown that the angular relationships among the branches of the picture remain invarient under this rotation. An inverse rotation is then introduced. Projections of the picture onto the principle planes is next described followed finally by projections onto arbitrary planes.

Use of the Perfect Shuffle in Sorting—*see* 8819.

6) LINGUISTICS, DOCUMENTATION, AND HUMANITIES

Micropicture Mass Storage System for Information Retrieval and Transmission—*see* 8810.

7) BEHAVIORAL SCIENCE, PATTERN RECOGNITION, AND ARTIFICIAL INTELLIGENCE

8826

Application of Game Tree Searching Techniques to Sequential Pattern Recognition, J. R. Slagle and R. C. T. Lee (Nat. Inst. Health, Bethesda); *Commun. Ass. Comput. Mach.*, vol. 14, Feb. 1971, pp. 103–110.

A sequential pattern recognition (SPR) procedure does not test all the features of a pattern at once. Instead, it selects a feature to be tested. After receiving the result of that test, the procedure either classifies the unknown pattern or selects another feature to be tested, etc. Medical diagnosis is an example of SPR. In this paper the authors suggest that SPR be viewed as a one-person game played against nature (chance). Virtually all the powerful techniques developed for searching two-person, strictly competitive game trees can easily be incorporated either directly or by analogy into SPR procedures. In particular, one can incorporate the "mini-average backing-up procedure" and the "gamma procedure," which are the analogues of the "minimax backing-up procedure" and the "alpha-beta procedure," respectively. Some computer simulated experiments in character recognition are presented. The results indicate that the approach is promising.

8827

Light Pen Input of Patterns and Their Recognition, W. Gohring (AEG-Telefunken, Konstanz); *Elektron. Rechenanl.*, vol. 12, Aug. 1970, pp. 188–193.

Pattern recognition on a PDP-7 with DECTAPEs, precision incremental CRT display type 340, and light pen is described. A pattern is written on the display, using light pen, then it is recognized within 0.1 s. The pattern together with its class, interesting intermediate results of the recognition process, and some commands are displayed. One can now correct, if necessary, the class and store the pattern on DECTAPE for further studies. The program is of high modularity, so that, while loading the program, one can choose the alphabet, the recognition process, an adaptation rule, the starting "norm-patterns," the intermediate results, and the way they are displayed.

Language Useful in Recognizing Handprinted Alphanumeric Characters—*see* 8824, 8825.

Accelerated Relaxation Method for Pattern Recognition—*see* 8842.

Interactive Pattern Recognition—*see* 8856.

8828

Experiments in Automatic Learning for a Multipurpose Heuristic Program, J. R. Slagle and C. D. Farrell (Nat. Inst. Health, Bethesda); *Commun. Ass. Comput. Mach.*, vol. 14, Feb. 1971, pp. 91–99.

An automatic learning capability has been developed and implemented for use with the MULTIPLE (MULTIpurpose Program that LEarns) heuristic tree-searching program, which is presently being applied to resolution theorem-proving in predicate calculus. MULTIPLE's proving program (PP) uses two evaluation functions to guide its search for a proof of whether or not a particular goal is achievable. Thirteen general features of predicate calculus clauses were created for use in the automatic learning of better evaluation functions for PP. A multiple regression program was used to produce optimal coefficients for linear polynomial functions in terms of the features. Also, automatic data-handling routines were written for passing data between the learning program and the proving program, and for analyzing and summarizing results. Data was generally collected for learning (regression analysis) from the experience of PP.

8829

Generalization Learning Techniques for Automating the Learning of Heuristics, D. A. Waterman (Carnegie-Mellon U., Pittsburgh); *Art. Intell.*, vol. 1, nos. 1/2, 1970, pp. 121–170.

This paper investigates the problem of implementing machine learning of heuristics. First, a method of representing heuristics as production rules is developed which facilitates dynamic manipulation of the heuristics by the program embodying them. Second, procedures are developed which permit a problem-solving program employing heuristics in production rule form to learn to improve its performance by evaluating and modifying existing heuristics and hypothesizing new ones, either during an explicit training process or during normal program operation. Third, the feasibility of these ideas in a complex problem-solving situation is demonstrated by using them in a program to make the bet decision in draw poker. Finally, problems which merit further investigation are discussed, including the problem of defining the task environment and the problem of adapting the system to board games.

8830

Heuristic Search Viewed as Path Finding in a Graph, I. Pohl (IBM, Yorktown Heights); *Art. Intell.*, vol. 1, no. 3, 1970, pp. 193–204.

This paper presents a particular model of heuristic search as a path-finding problem in a directed graph. A class of graph-searching procedures is described which uses a heuristic function to guide search. Heuristic functions are estimates of the number of edges that remain to be traversed in reaching a good node. A number of theoretical results for this model, and the intuition for these results, are presented. They relate the efficiency of search to the accuracy of the heuristic function. The results also explore efficiency as a consequence of the reliance or weight placed on the heuristics used.

8831

The Correctness of Nondeterministic Programs, Z. Manna (Stanford U., Stanford); *Art. Intell.*, vol. 1, nos. 1/2, 1970, pp. 1–26.

In this paper properties of nondeterministic programs are formalized by means of the satisfiability and validity of formulas in first-order logic. The main purpose is to emphasize the great variety of possible applications of the results, especially for solving problems of the kind: "Find a sequence of actions that will achieve a given goal."

8832

Renamable Paramodulation for Automatic Theorem Proving with Equality, C. L. Chang (Dep. Health, Education, and Welfare, Bethesda); *Art. Intell.*, vol. 1, no. 4, 1970, pp. 247–256.

Roughly speaking, in automatic theorem proving with equality, paramodulation is a substitution rule for equality. In this paper, renamable resolution is extended to paramodulation. Renamable paramodulation is paramodulation of two clauses which become positive after an R-renaming. The R-refutation completeness of renamable resolution and renamable paramodulation for functionally reflexive systems is proved. That is, if a set S of clauses is R-unsatisfiable and if F is the set of the functionally reflexive axioms for S, then the empty clause can be derived from $S \in \{x=x\} \in F$

by using renamable resolution plus renamable paramodulation.

8833

Resolution Graphs, R. A. Yates and B. Raphael (Stanford Res. Inst., Menlo Park), and T. P. Hart (L. G. Hanscom Field, Bedford); *Art. Intell.*, vol. 1, no. 4, 1970, pp. 257–289.

This paper introduces a new notation, called "resolution graphs," for deductions by resolution in first-order predicate calculus. A resolution graph consists of groups of modes that represent initial clauses of a deduction and links that represent unifying substitutions. Each such graph uniquely represents a resultant clause that can be deduced by certain alternative but equivalent sequences of resolution and factoring operations. Resolution graphs are used to illustrate the significance of merges and tautologies in proofs by resolution. Finally, they provide a basis for proving the completeness of a proof strategy that combines the set of support, resolution with merging, linear format, and Loveland's subsumption conditions.

8834

An Examination of the Geometry Theorem Machine, P. C. Gilmore (IBM, Yorktown Heights); *Art. Intell.*, vol. 1, no. 3, 1970, pp. 171–187.

In five papers, Gelernter, Rochester, Hansen, and Loveland sketched in outline what they call a geometry theorem machine and described results that were obtained when a computer was programmed to simulate the machine. More precisely, they described an algorithm for constructing proofs for theorems of an axiomatic theory which is a portion of plane geometry. The papers are written in such a way that one can only conclude by inference details of the axiomatic theory and the algorithm for finding proofs for theorems in the theory. The purpose of this paper is to supply some of these details.

8835

REF-ARF: A System for Solving Problems Stated as Procedures, R. E. Fikes (Carnegie-Mellon U., Pittsburgh); *Art. Intell.*, vol. 1, nos. 1/2, 1970, pp. 27–120.

This paper describes an effort to design a heuristic problem-solving program which accepts problems stated in a nondeterministic programming language and applies constant satisfaction methods and heuristic search methods to find solutions. The use of nondeterministic programming languages for stating problems is discussed, and REF, the language accepted by the problem solver ARF, is described. Various extensions to REF are considered. The conceptual structure of the program is described in detail and various possibilities for extending it are discussed. The use of the input language and the behavior of the program are described and analyzed in 16 sample problems.

8) MATHEMATICS

8836

Parallel Implementation of Arithmetic Operations in Extension Fields, G. I. Davida (U. Iowa, Iowa City); Rep. THEMIS-UI-TR-26, 19 pp., July 1970; CFSTI, AD 714 170, $3.00.

Parallel implementation of arithmetic operations in finite fields is usually limited to the binary field, i.e., the field of two integers. Serial implementation of arithmetic operations is accomplished through the use of shift registers. It would be highly desirable in many applications to be able to carry out arithmetic operations, in the extension field of a field of elements, in parallel. For instance, if error correcting codes are to be used in integrated circuit memory arrays, parallel decoding would be mandatory. Most of the encoding and decoding algorithms for error correcting codes are implemented in a serial fashion. Methods of implementing arithmetic operations in parallel, particularly multiplication and division, are presented in this paper for any $GF(q_m)$, where q is a prime number and m is a positive integer.

8837

A Statistical Model of Roundoff Error for Varying Length Floating-Point Arithmetic, M. Tienari (U. Helsinki, Finland); *BIT*, vol. 10, no. 3, 1970, pp. 355–365.

A model is presented which explains the behavior of the roundoff error in a result quantity when computing precision is varied. A set of hypotheses concerning this *a posteriori* model is tested in a matrix inversion algorithm. The characteristics of the algorithm where the error model is valid are discussed. As an application of the model, the usual estimation procedure for roundoff error, consisting of comparing the results computed in two different precisions, is analyzed statistically.

FORTRAN Extended-Precision Library for Floating-Point Arithmetic—*see* 8815.

8838

An Interval Arithmetic Package for the UNIVAC 1108, T. D. Ladner and J. M. Yohe (U. Wisconsin, Madison); Rep. MRC-TSR-1055, 98 pp., May 1970; CFSTI, AD 714 151, $3.00.

The report describes a program package which implements interval arithmetic for the Univac 1108 computer. In addition to the basic arithmetic operations, the package provides interval versions of standards library functions, conversions to and from other data types, complete fault trapping capabilities, and other supporting functions. General guidance and references are provided to aid in the implementation of such a package for other computers.

8839

Complex Interval Arithmetic, J. Rokne and P. Lancaster (U. Calgary, Alberta, Canada); *Commun. Ass. Comput. Mach.*, vol. 14, Feb. 1971, pp. 111–112.

Complex interval arithmetic is defined using real interval arithmetic. Complex interval division is defined so as to assure smallest possible resulting intervals.

Iterative Array for Multiplication of Signed Binary Numbers—*see* 8791.

8840

A Simple Postcorrection for Nonrestoring Division, V. T. Rhyne (Texas A and M U., College Station); *IEEE Trans. Comput.* (Short Notes), vol. C-20, Feb. 1971, pp. 213–214.

The nonrestoring division algorithm offers the advantages of speed and logical simplicity when working with signed, two's-complement binary numbers. The algorithm does not assure sign agreement between the calculated quotient and remainder, however, which is a disadvantage in some applications. This paper describes a postcorrection that will force sign agreement between quotient and remainder. The corrective operation is very simple to implement, especially in microprogrammed arithmetic units.

8841

Primes Forming Arithmetic Series and Clusters of Large Primes, H. Riesel (Royal Inst. Tech., Stockholm, Sweden); *BIT*, vol. 10, no. 3, 1970. pp. 333–342.

By a sieve method and the use of a computer, a search for a primes forming arithmetic series is reported. The longest series found contained 13 primes. If the local prime density in an interval is unusually large, there is said to be a cluster of primes in the interval. Clusters of large primes are searched for by looking for repetitions of patterns of primes chosen from the beginning of the prime series. The densest large cluster found is 429 983 158 710+11, 13, 17, 19, 23, 37, 41, 43, 47, 53, and 59, with 11 primes out of 49 numbers. The average prime density this high up in the number series is one number only in about 27.

8842

The Accelerated Relaxation Method for Linear Inequalities, C. L. Chang (Dep. Health, Education, an Welfare, Bethesda); *IEEE Trans. Comput.* (Short Notes), vol. C-20, Feb. 1971, pp. 222–225. Feb. 1971.

An algorithm called the accelerated relaxation method for finding a solution of a set of inequalities is given. Experimental results show that the accelerated relaxation method is far more efficient than the relaxation method, the fixed increment method, and the generalized-inverse Ho–Kashyap algorithm.

8843

Approximation of Convex Data, G. M. Phillips (U. St. Andrews, Scotland), and P. J. Taylor (U. Southampton, England); *BIT*, vol. 10, no. 3, 1970, pp. 324–332.

A method is described of obtaining convex polynomial approximations to discrete sets of convex data. The approximations are best convex combinations of certain component convex functions. A Weierstrass-type theorem is proved to justify the choice of component functions, and numerical illustrations are given.

8844

Approximation by Non-Negative Algebraic Polynomials, M. M. Chawla (U. Illinois, Urbana); *BIT*, vol. 10, no. 3, 1970, pp. 243–248.

A theorem is proved which gives an estimate for the approximation of a continuous function f by polynomials resulting from the convolution of f with nonnegative algebraic polynomials p_n. Jackson's theorem can be deduced from it by choosing a particular p_n whose second Chebyshev–Fourier coefficient is sufficiently close to -1.

8845

Piecewise Approximation of Functions of Two Variables and its Application in Topographical Data Reduction, T. Pavlidis (Princeton U., N. J.); Rep. TR-86 AROD-8244; 4-A, 31 pp., Sept. 1970; CFSTI, AD 714 696, $3.00.

A method to obtain variable-boundary piecewise polynomial approximations of functions of two variables $f(x, y)$ is presented. A two state scan is used. In the first stage one uses the one-dimensional algorithm for a set of parallel directions in the domain of $f(x, y)$. Then a similar algorithm is applied on the coefficients of the polynomials, i.e., it finds segments where groups of certain coefficients do not differ significantly from their average value. Computer tests of the algorithm on map data gave significant data reduction ratios (about 40:1) for mean-square error of approximation around 2 percent of the relative altitudes.

Use of the Perfect Shuffle in Polynomial Evaluation—*see* 8819.

8846

A Simplified Definition of Walsh Functions, R. B. Lackey and D. Meltzer (Ohio State U., Columbus); *IEEE Trans. Comput.* (Short Notes), vol. C-20, Feb. 1971, pp. 211–213.

A simple method is presented which defines Walsh functions in terms of products of Rademacher functions, but which preserves the ordering of the Walsh functions necessary to retain the notion of increasing number of zero crossings, or sequency.

8847

On Machine Precision, Computation Error and Condition Number in Solving Linear Algebraic Systems, N.-K. Tsao and F. F. Kuo (U. Hawaii, Honolulu); Rep. THEMIS-A70-13 AFOSR-70-2576TR, 19 pp., Sept. 1970; CFSTI, AD 714 598, $3.00.

The relationship among the machine precision, computation error, and condition number in solving linear algebraic systems is derived for the floating elimination method by using backward error analysis. It is shown that the negative of the logarithm of the relative error is proportional to the machine precision for fixed system and to the negative of the logarithm of the condition of the system for fixed t. It is also shown that for fixed relative error, the machine precision required to achieve this is proportional to the logarithm of the condition of the system. Numerical experiments have been carried out and the observed data coincide with what was expected.

8848

Perturbation Bounds for Means of Eigenvalues and Invariant Subspaces, A. Ruhe (Ulmek U., Sweden); *BIT*, vol. 10, no. 3, 1970, pp. 343–354.

When a matrix is close to a matrix with a multiple eigenvalue, the arithmetic mean of a group of eigenvalues is a good approximation to this multiple eigenvalue. A theorem of Gershgorin type for means of eigenvalues is proved and applied as a perturbation theorem for a degenerate matrix. For a multiple eigenvalue bounds are derived for computed bases of subspaces of eigenvectors and principal vectors, relating them to the spaces spanned by the last singular vectors of corresponding powers of the matrix. These bounds assure that, provided the dimensionalities are chosen appropriately, the angles of rotation of the subspaces are of the same order of magnitude as the perturbation of the matrix. A numerical example is given.

8849

Degrees of Freedom and Modular Structure in Matrix Multiplication, H. C. Andrews (U. South. Calif., Los Angeles) and K. L. Caspari (ITT-Electrophysics Labs., Hyattsville); *IEEE Trans. Comput.*, vol. C-20, Feb. 1971, pp. 133–141.

An algorithm is presented which enables certain matrix multiplications in a digital computer to be implemented with a considerable savings in storage and computational operations. For $N \times N$ matrix vector multiplication (that is, a multiplication of a matrix by a vector) a maximum of $N \sum_{r=0}^{n-1} p_r$ storage words are necessary compared to normal full matrix storage requirements of N^2 locations. In addition only $N \sum_{r=0}^{n-1} p_r$ computer operations are necessary compared to N^2 operation in a general vector matrix multiplication. N is chosen to be a highly composite number, $N = \prod_{r=0}^{n-1} p_r$, and the p_r are integers. The algorithm takes advantage of the redundancies in the definition of certain matrices and develops a matrix description based on the number of degrees of freedom necessary in defining an $N \times N$ matrix. The algorithm is optimal in the sense that it describes a vector matrix multiplication in exactly as many operations as available degrees of freedom $N \sum_{r=0}^{n-1} p_r$ (no greater number of degrees of freedom could be implemented in fewer operations). The matrix transformation formulation is based largely on noting the use of lexicographic positional digit notation in keeping track of the few parameters describing the final N by N matrix. The algorithm includes the generation of the fast Fourier transform, fast Hadamard transform, fast Walsh transform, fast Kronecker matrix transform, and an infinite class of transformation unnamed but potentially useful in generalized spectral analysis as well as coding, bandwidth reduction, and feature selection. A modular computer development is presented for possible special purpose computer implementation. Experimental results are presented to show application of both the algorithm in general and modular construction in particular.

Use of the Perfect Shuffle in Matrix Transposition—*see* 8819.

8850

Some Algorithms for Numerical Quadrature Using the Derivatives of the Integrand in the Integration Interval, T. Havie (CERN, Switzerland); *BIT*, vol. 10, no. 3, 1970, pp. 277–294.

Some quadrature formulas using the derivatives of the integrand are discussed. Generalizations of both the ordinary and the modified Romberg algorithms are obtained as special cases. In all cases the error terms are expressed in terms of Bernoulli polynomials and functions.

8851

Uniformly Maximumnorm Stable Difference Schemes, B. Hakberg; *BIT*, vol. 10, no. 3, 1970, pp. 266–276.

Sufficient conditions for maximumnorm stability, uniform in the mesh widths, of implicit two-level difference schemes with constant coefficients are given. Uniform stability is a necessary and sufficient condition for consistent difference schemes to be convergent, when the mesh widths are unrelated.

8852

Convergence of Finite-Difference Techniques for a Harmonic Mixed Boundary Value Problem, J. R. Whiteman (Brunel U., England) and J. C. Webb (U. Texas, Austin); *BIT*, vol. 10, no. 3, 1970, pp. 366–374.

The paper deals with the convergence of finite-difference approximations for a harmonic mixed boundary value problem. In particular the case when the boundary contains a slit is considered.

Hybrid Computer Solution of Optimal Control Boundary Value Problems—*see* 8865.

8853

Stable Marriage Assignment for Unequal Sets, D. G. McVitie (I.C.L., England) and L. B. Wilson (U. Newcastle upon Tyne, England); *BIT*, vol. 10, no. 3, 1970, pp. 295–309.

The theory and algorithms developed by the authors in a previous paper for the stable marriage assignment for equal sets are extended to the ease of unequal sets. The main theorem in this paper shows that a person unmarried in one stable marriage solution will be unmarried in any other stable marriage solution.

8854

Research in Near-Ring Theory Using a Digital Computer, J. R. Clay (U. Arizona, Tucson); *BIT*, vol. 10, no. 3, 1970, pp. 249–265.

In this paper it is shown how the computer has played a valuable role in research in the theory of near-rings. Basically, the author has used the computer to generate examples of near-rings to be applied for meaningful conjectures and counter-examples. All the near-rings of order less than 8 have been listed previously. Since there is only one non-Abelian group of order less than 8, it is natural to still be curious as to what happens when one tries to construct a near-ring from a non-Abelian group. The methods used by the author to construct near-rings from groups are illustrated on the two non-Abelian groups of order 8. Specifically, for each non-Abelian group of order 8, it was decided to construct all near-rings enjoying one of the following four properties: 1) near-ring with identity; 2) near-rings without two-sided zero; 3) near-rings with no zero divisors; 4) idempotent near-rings, i.e., near-rings for which $x^2 = x$ for all x.

Ambiguity of Graphs of Automata—*see* 8782.

Linked List Structure for Describing Directed Graphs for Regular Expressions—*see* 8784.

Heuristic Search Viewed as Path Finding in a Graph—*see* 8830.

Resolution Graphs for Deductions in First-Order Predicate Calculus—*see* 8833.

9) PROBABILITY, MATHEMATICAL PROGRAMMING, DIGITAL SIMULATION, INFORMATION THEORY, AND COMMUNICATION SYSTEMS

8855

An Algorithm for Finding Intrinsic Dimensionality of Data, K. Fukunaga and D. R. Olsen (Purdue U., Lafayette); *IEEE Trans. Comput.*, vol. C-20, Feb. 1971, pp. 176–183.

An algorithm for the anslysis of multivariant data is presented along with some experimental results. The basic idea of the method is to examine the data in many small subregions, and from this determine the number of governing parameters, or intrinsic dimensionality. This intrinsic dimensionality is usually much lower than the dimensionality that is given by the standard Karhunen–Loève technique. An analysis that demonstrates the feasability of this approach is presented.

8856

Interactive Use of Problem Knowledge for Clustering and Decision Making, E. A. Patrick and L. Y. L. Shen (Purdue U., Lafayette); *IEEE Trans. Comput.* (Short Notes), vol. C-20, Feb. 1971, pp. 216–222.

An approach to clustering and decision making is presented where a prior problem knowledge is inserted interactively. The problem knowledge inserted is in the form of subcategory mean vectors and covariance matrices and in the expert's confidence that these means and covariances accurately characterize the category. Then observations of patterns from the category are used to update these *a priori* supplied means and covariances. The extent to which new observations update the *a priori* values depends upon the expert's *a priori* confidence. The expert can observe his *a priori* knowledge being modified with training patterns. Through interaction, the expert is in control of the automatic pattern recognition; furthermore, he is likely to learn from the interactive experience. This clustering technique differs from earlier interactive clustering in that this technique allows for insertion of *a priori* knowledge and updating as new training samples become available. The pragmatic reason for designing the procedure arose when considering problems in medical diagnosis and classifying touching biological cells. Extensions of the concept to include the insertion of nonlinear relationships for representing problem knowledge appear very important to the authors.

8857
A Method to Calculate the Distribution Function When the Characteristic Function is Known, H. Bohman (Skandia Insur. Co., Stockholm, Sweden); *BIT*, vol. 10, no. 3, 1970, pp. 237–242.

A formula for numerical inversion of characteristic functions based on the Poisson formula is presented, and a numerical example is also given.

8858
The Fourier Transform and Some of its Applications, L. B. Palmer (Naval Res. Lab., Washington, D. C.); Rep. NRL-7170, 22 pp., Sept. 1970; CFSTI, AD 713 935, $3.00.

The discrete Fourier transform and the inverse transform of a finite set of data points are derived. By relating these transforms to a "fast Fourier transform," it is shown how they may be used efficiently in convolving two sets of data points, digital filtering, computing lagged products, and estimating amplitude spectra. Some of the difficulties encountered in using transforms in these areas are discussed, and computation times for direct evaluation of the results are compared with those using transform methods.

Use of the Perfect Shuffle in the Fast Fourier Transform—*see* 8819.

Generation of Fast Fourier and Other Transforms for Spectral Analysis—*see* 8849.

8859
High Speed Generation of Maximal Length Sequences, A. Lempel and W. L. Eastman (Sperry Rand Res. Cen., Sudbury); *IEEE Trans. Comput.* (Short Notes), vol. C-20, Feb. 1971, pp. 227–229.

The construction described in this note makes possible the generation of any given linear shift register sequence of maximal period $p=2^n-1$, at a rate k times faster than the shift pulse rate. The construction is valid for any positive integer k which is not a multiple of p and it employs at most k linear shift registers to degree n or less.

Random Number Generator Model for Stochastic Sequential Machines—*see* 8787.

Statistical Model of Roundoff Error for Varying Length Floating-Point Arithmetic—*see* 8837.

8860
Hybrid and Digital Simulation of Optimal Stochastic Control Systems, E. C. Tacker and T. D. Linton (Louisiana State U., Baton Rouge); Rep. THEMIS-LSU-T-TR-38 AFOSR-70-2593TR, 39 pp., Aug. 1970; CFSTI, AD 714 614, $3.00.

By means of studying a particular system it is shown that a controller optimized on a deterministic basis can be considerably inferior to one optimized by explicitly including system uncertainties and disturbances. Hybrid and digital computation techniques as they apply to simulating stochastic control systems are discussed. The model equations are formulated in discrete-time and the majority of the simulation tasks are performed by the digital computer. This study together with one reported elsewhere (AD 714 613), serve to illustrate how the high-speed capabilities of hybrid computers can be effectively employed in the design by simulation of stochastic control systems.

Simulation Model of Some Time-Sharing Operating Systems—*see* 8820.

Simulation of Extended-Precision Arithmetic—*see* 8815.

Application of Game Tree Searching Techniques to Sequential Pattern Recognition—*see* 8826.

Use of Dynamic Programming in Optimal Sequential Pattern Recognition—*see* 8826.

Accelerated Relaxation Method for Mathematical Programming—*see* 8842.

8861
Cascaded Tree Codes, J. L. Ramsey (M.I.T., Cambridge); Rep. TR-478, 115 pp., Sept. 1970; CFSTI, AD 714 268, $3.00.

Cascaded codes are long codes that are constructed by successively encoding a series of relatively short constituent codes. The purpose of cascading is to facilitate decoding by dividing the composite decoding process into a sequence of relatively simple steps, each of which corresponds to the decoding of one of the constituent codes. Cascading techniques in which the constituent codes are tree codes are studied, the efficiency attainable with cascading is determined, and the attainable error probability is bounded in terms of the composite decoding complexity.

Use of Error Correcting Codes in Integrated Circuit Memory Arrays—*see* 8836.

10) SCIENCE, ENGINEERING, AND MEDICINE

8862
Interactive Scheduling System, A. C. Brewer; *IBM Syst. J.*, vol. 10, no. 1, 1971, pp. 62–79.

Design principles, file structures, and programming techniques of a scheduling system that approximates the overall magnitude and complexity of an airline scheduling system are discussed. Used worldwide by the National Aeronautics and Space Administration to schedule its manned and unmanned space flight missions up to one year in advance, the system operates in either batch or interactive modes to produce, modify, and observe actual and simulated schedules.

11) ANALOG AND HYBRID COMPUTERS

8863
History Effect of Ferrite Cores as Analog Storage Elements, W. Geisselhardt (Inst. Nachrichtengerate und Datenverarbeitung, Technische Hochschule, Aachen, Germany); *IEEE Trans. Magn.*, vol. MAG-6, Sept. 1970, pp. 687–690.

Studies on 2- and 3-mm ferrite cores for use as storage elements in an analog core memory are presented. The information is stored as the flex level of the magnetic core. The partial flux-switching is performed by voltage pulses with constant amplitude but varying length. Between writing and reading an error appears which is caused by the reversible portion of the flux and whose value depends upon the switched flux level. It is shown that there exists a relation between the magnitude of the error and the characteristic properties of the cores. The measured character of the error depends on how often a particular WRITE-READ cycle is repeated before changing the amplitude of the switched flux. A history effect was found to be the reason for this. A special method has been developed to drive the cores in a matrix array. In this mode the history effect did not occur.

8864
Analog-to-Digital System, R. S. Walker and W. R. Hudson (U. Texas, Austin); RR-73-4, 115 pp., Apr. 1970; CFSTI, PB 195 399, $3.00.

The Hewlett-Packard 2115 analog-to-digital (A-D) facility purchased for data processing in conjunction with the SD Profilometer is described in the report. Included is a general discussion of the A-D problem and the various subsystems in the A-D system. A detailed description is provided for: 1) an interface and patch logic module which was built by project personnel to interface external signs with this facility; 2) the A-D and TAPE WRITE programs necessary for system operations; and 3) the operating and data validation procedures required to use the equipment. All additional interface cabling and hardware diagrams and computer program listings that are necessary for complete documentation of the A-D system are also included.

8865
Hybrid Computer Solution of Optimal Control Problems, G. C. Machaels and V. Gourishankar (U. Alberta, Edmonton, Alberta, Canada); *IEEE Trans. Comput.* (Short Notes), vol. C-20, Feb. 1971, pp. 209–211.

This paper discusses limitations which arise when a method proposed by Miura *et al.* is used for solving certain two-point boundary value problems on the hybrid computer. It is shown that the method proposed will not work in all cases. An example where the method fails is given. However, to emphasize the basic elegance and usefulness of this method, an extension to cover a more general target set is also introduced.

Hybrid and Digital Simulation of Optimal Stochastic Control Systems—*see* 8860.

12) REAL-TIME SYSTEMS AND AUTOMATIC CONTROL; INDUSTRIAL APPLICATIONS

Hybrid and Digital Simulation of Optimal Stochastic Control Systems—*see* 8860.

Hybrid Computer Solution of Optimal Control Boundary Value Problems—*see* 8865.

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