

16.5 A 10b 100MS/s 4.5mW Pipelined ADC with a Time Sharing Technique

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For the applications requiring medium-to-high resolution ADCs, the pipelined architecture is considered to be the most optimal structure in terms of power consumption and area. With range overlap and redundant bit at each pipelined stage, the sub-ADC can tolerate large comparator offsets, thereby, leaving the linearity and accuracy requirements for the DAC and the residue gain stage. Typically, the multiplying DAC (MDAC), which is the combination of a DAC and a gain stage, requires a high-gain wide-bandwidth opamp and is the most critical building block. The opamps draw static currents from their power supplies and consume most of the power in a pipelined ADC. Many techniques have been reported to achieve a low-power design by avoiding the high-gain opamp, such as zero-crossing based circuits [1, 2], dynamic source-follower amplification [3], and capacitive charge-pump [4]. These techniques replace the conventional opamps with other low-power dynamic circuits to minimize the static power consumption, but in these alternative structures the conversion gain is not as well-predicted as the opamp-based design. Therefore, additional calibration circuits are typically required to compensate the conversion gain error. Another low-power pipelined ADC is presented in [5] and uses high-performance analog MOS transistors which are not easily obtained in a standard digital CMOS process.

An opamp sharing technique is commonly used to reduce the power consumption by decreasing the total number of opamps [6]. As shown in Fig. 16.5.1, an opamp can be shared by two adjacent stages due to the two-phase operation nature in a pipelined ADC. Therefore, half of the opamps can be removed, leading to 50% power reduction. Although opamp sharing is an attractive technique because of its simplicity and effectiveness, it is not optimal and can be further improved. Based on the 1st-order settling time approximation, the required transconductance of the opamp in a pipelined stage is derived as,

$$g_m > (C_L/T_S) \times n \times \ln 2, \quad (1)$$

where C_L is the total loading capacitance, n is the required resolution of the back-end ADC, and T_S is the available settling time. In a pipelined ADC, the noise and resolution specifications at the front-end stages are more stringent than those of the back-end stages. Therefore, the minimum power design constraint of the opamp is set by stage j in Fig. 16.5.1 and therefore, the power dissipation of stage $(j+1)$ is more than necessary if it shares the same opamp with stage j .

To reduce the equivalent power consumption in Fig. 16.5.1, the evaluation time for stage j and for stage $(j+1)$ can be different, and the opamp can be powered off at stage $(j+1)$ as soon as the MDAC settles. Shown in Fig. 16.5.2, the opamp is turned off for half of the original evaluation time by properly choosing the stage resolution and the loading capacitance C_L . Therefore, the equivalent power consumption at stage $(j+1)$ is halved compared to the conventional opamp sharing technique. However, turning off the opamp leads to the penalty of long settling time because the opamp needs a power-on time to reach its normal bias condition. To avoid this design dilemma, the time-sharing technique is used in the presented ADC.

Figure 16.5.3 shows the presented 10b pipelined ADC architecture with 2.5b conversion in each stage. Instead of turning off the opamp, it can be reused by the next stage. Therefore, the ADC not only shares the opamp but also shares the evaluation time of the MDAC2 and MDAC3 stages. To reduce the power consumption, the front-end sample-and-hold (S/H) circuit is removed because the S/H dissipates significant power and contributes additional noise that degrades SNR. To maintain the characteristics of Nyquist sampling in this work, the input signal paths are carefully designed and simulated on the circuit and layout-level to minimize the input delay mismatch seen between the MDAC1 and sub-ADC. Each MDAC stage resolves three bits with one redundant bit for the digital correction. Therefore, with the opamp and evaluation time sharing, the pipelined

ADC in Fig. 16.5.3 uses only one opamp to complete the 10b conversion. Theoretically, the evaluation time of the MDAC3 stage can be shortened to further reduce the power consumption since the resolution requirement is lower than that of the MDAC2 stage. However, in this work, MDAC2 and MDAC3 stages have identical evaluation time in order to keep the same level of complexity and power consumption of the clock generation circuit. One issue behind the opamp sharing is that no reset phase is reserved for the opamps, and therefore, memory effects will occur and degrade the conversion accuracy. Shown in Fig. 16.5.3, a dual input pair opamp is used in this work. By switching the bias current between the input differential pairs, the parasitic charge stored on the non-active input nodes is removed to avoid the sample-to-sample memory effects.

The presented 10b pipelined ADC is fabricated in a 90nm digital CMOS technology and uses standard threshold voltage devices only. Figure 16.5.4 shows the measured output spectrum for a 1 and 50MHz input signal when the ADC operates at 100 MS/s. The SNDRs are 55.0 and 53.9dB for the 1MHz and 50MHz inputs, respectively. Figure 16.5.5 shows the measured DNL/INL and its dynamic performance with different sampling rates and input frequencies. The maximum DNL is 0.81/−0.62 LSB and the maximum INL is 1.00/−0.89 LSB. The SNDR decreases 1.1dB with the input frequency increasing to 50MHz. Therefore, the effective resolution bandwidth (ERBW) is larger than the Nyquist band even though no S/H circuit is used. Figure 16.5.6 shows a comparison table with other pipelined ADCs fabricated in 90nm CMOS. Because the architecture contains only one opamp and requires no calibration circuits, the presented ADC occupies 0.058mm². The power consumption of the core analog circuits, including the opamp, biasing circuits and the comparators, is 3.7mW. The digital part consumes 0.8mW while operating at 100MS/s from a 1.0V supply. The figure-of-merit (FOM) used for comparison is

$$\text{FOM} = \text{Power}/(f_s \times 2^{\text{ENOB}}). \quad (2)$$

The FOM of the presented ADC is 98fJ/conversion-step. Thus, the ADC is more power efficient than some of the dynamic amplification designs. Figure 16.5.7 is the chip micrograph. The total area including pads is about 860×860μm², and the active area occupies only 220×260μm².

Acknowledgement:

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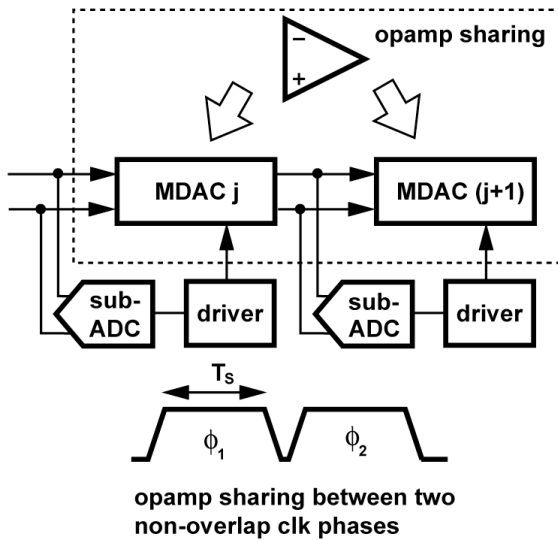


Figure 16.5.1: Opamp sharing between two pipelined stages.

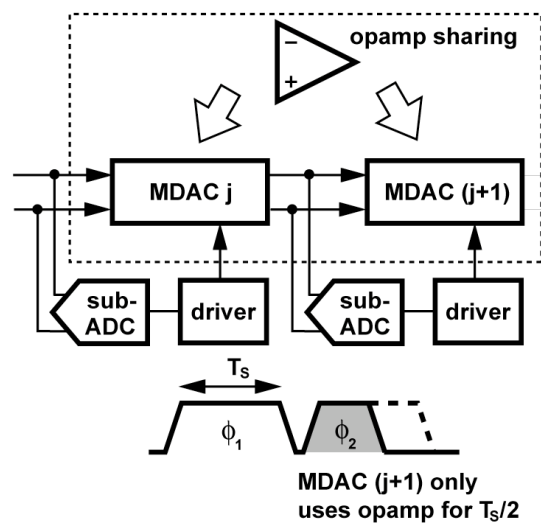


Figure 16.5.2: Different evaluation time of phases to reduce the power consumption at stage (j+1).

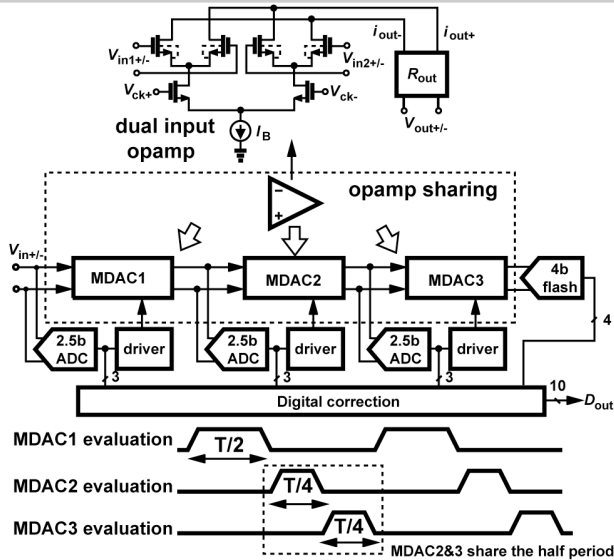


Figure 16.5.3: ADC architecture.

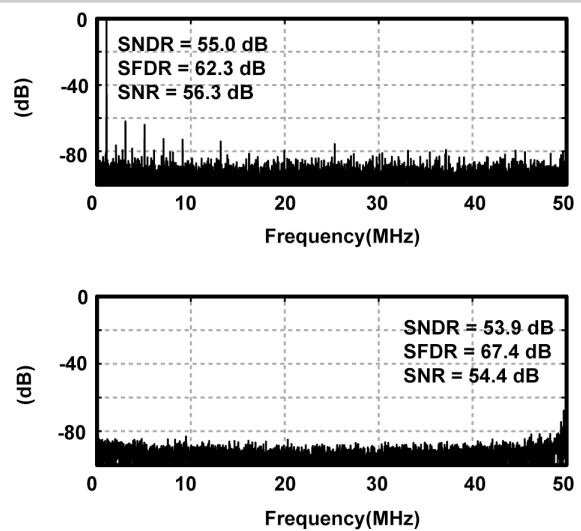


Figure 16.5.4: Measured spectrum with sampling rate of 100MHz and input frequencies of 1 and 50MHz.

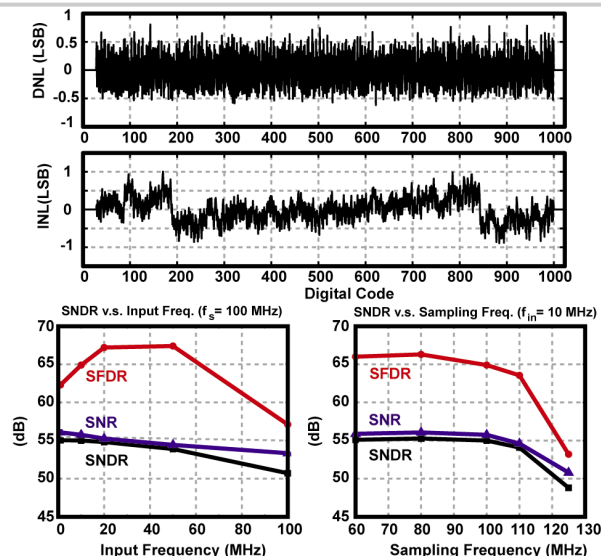


Figure 16.5.5: Measured DNL/INL and dynamic performance summary.

	[7] JSSC07'	[8] ISSCC07'	[6] ISSCC07'	[3] JSSC09'	This Work
Resolution	10b	10b	10b	9.4b	10b
Technology	90-nm CMOS	90-nm CMOS	90-nm CMOS	90-nm CMOS	90-nm CMOS
Conversion Rate	100 MHz	80 MHz	30 MHz	50 MHz	100 MHz
SNDR	55.3 dB	55.0 dB	58.4 dB	49.4 dB	55.0 dB
DNL	0.70 LSB	0.80 LSB	0.47 LSB	0.38 LSB	0.81 LSB
INL	0.70 LSB	1.00 LSB	0.80 LSB	1.29 LSB	1.00 LSB
Supply	1 V	0.8 V	1 V	1.2 V	1 V
Power Dissipation	33 mW	6.5 mW	4.7 mW	1.44 mW	4.5 mW
Input Freq. Range	50 MHz (-2.2dB)	40 MHz (-3.6dB)	15 MHz (-3dB)	25 MHz (-1.7dB)	50 MHz (-1.1dB)
Active Area	4.03 mm ²	0.637 mm ²	0.32 mm ²	0.123 mm ²	0.058 mm ²
FOM	694 fJ/Conv.	177 fJ/Conv.	232 fJ/Conv.	119 fJ/Conv.	98 fJ/Conv.

Figure 16.5.6: Comparison table.

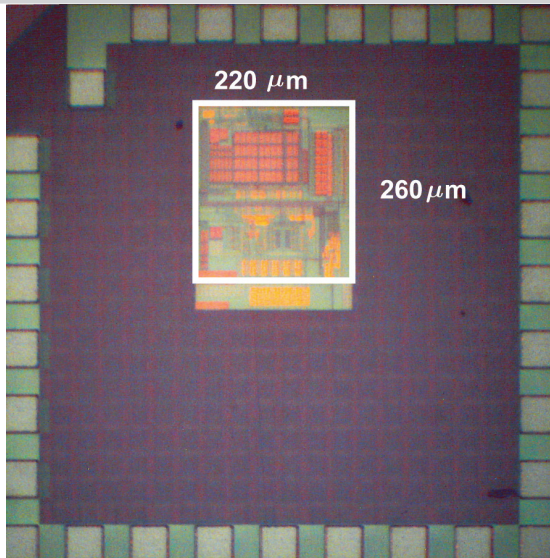


Figure 16.5.7: Chip micrograph.