A $\Delta-\Sigma$ PLL-Based Spread-Spectrum Clock Generator With a Ditherless Fractional Topology

Ching-Yuan Yang, *Member, IEEE*, Chih-Hsiang Chang, *Student Member, IEEE*, and Wen-Ger Wong

***Abstract*—A triangular-modulated spread-spectrum clock generator using a $\Delta-\Sigma$-modulated fractional-N phase-locked loop (PLL) is presented. The PLL employs a multiphase divider to implement the modulated fractional counter with increased $\Delta-\Sigma$ operation speed. In addition, the phase mismatching error in the phase-interpolated PLL with multiphase clocks can be randomized, and finer frequency resolution is achievable. With a frequency modulation of 33 kHz, the measured peak power reduction is more than 11.4 dB under a deviation of $\pm 0.37\%$. Without spread-spectrum clocking, the PLL generates 2.4-GHz output with 18.82-ps peak-to-peak jitter. After spread-spectrum operation, the measured up-spread and down-spread jitter can achieve 52.59 and 56.79 ps, respectively. The chip occupies $950 \times 850\ \mu\mathrm{m}^2$ in 0.18-μm CMOS process and consumes 36 mW.**

***Index Terms*—Fractional divider, fractional-N phase-locked loop (PLL), multiphase signals, phase interpolation, spread-spectrum clock generation (SSCG), $\Delta-\Sigma$ modulator.**

I. Introduction

ELECTROMAGNETIC interference (EMI) is a real issue that must be dealt with to meet the maximum allowed regulated level in consumer electronic products. Many ways have been used to diminish EMI, such as shielding, pulse shaping, low-voltage differential clocking, and spread-spectrum clocking. Among these, spread-spectrum clock generation (SSCG) is an effective and popular method for high-speed systems since the system clock is one of the major contributors in EMI and the cost to the system is minimal. This technique is to slightly modulate the system clock of the computing devices such that the radiated power level in a given bandwidth is lowered [1], [2].

Clock generation is usually done with a phase-locked loop (PLL), and the common technique to produce SSCG is to apply and insert modulation into the PLL. The clock frequency can be modulated by imposing a signal on the control node of a voltage-controlled oscillator (VCO) [3] or using a fractional-N technique to change the divider ratio to produce the modulation[4]–[6].

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In many fractional-N PLLs, an oversampling $\Delta-\Sigma$ modulator can be used to interpolate the control signal of the programmable divider [7], [8]. Although this is a commonly used method for integrated applications, the design complexity is considerably increased because the SSCG needs a very small range of the fractional divide ratios. In addition, the clock speed of the modulator is limited by the reference in the PLL.

In this paper, a ditherless fractional-N PLL combining an oversampling $\Delta-\Sigma$ modulator is adopted in a PLL for SSCG applications. In the PLL, the VCO with multiphase outputs is divided by a fractionally programmable divider, which introduces a multiphase-switching approach in the digiphase synthesizer to reduce the periodic tones by the phase error cancellation before the phase-frequency detector (PFD) [9]. The complete fractional part is established by the $\Delta-\Sigma$ modulator, which provides a selected number of fractional control signals to cause the overall fractional division. Combining both concepts of $\Delta-\Sigma$ modulation and multiphase-switching fractionality, the reference frequency and $\Delta-\Sigma$-modulated speed can be increased for a given frequency resolution, and the phase errors resulting from mismatch in the multiphase switching can be randomized and shaped by the $\Delta-\Sigma$ modulator.

This paper is organized as follows. A basic concept of fractional synthesis is reviewed in Section II. Section III describes the implementation of the SSCG building blocks. Section IV gives a linear model for noise analysis. Simulated and experimental results are presented in Section V, followed by a conclusion.

II. Basic Concepts Of System Architecture for Fractional Synthesis

A. System Architecture

In conventional integer-N PLL-based synthesizers, the resolution is the same as the reference frequency. Since the required frequency deviation of the SSCG is small, such as less than 0.5% for serial ATA applications [10], it results in the narrow channel spacing in the PLL and is thereby accompanied by a small loop bandwidth which leads to slow dynamics [8]. In the case of a fractional-N PLL, the output frequency is a fractional multiple of the reference frequency, resulting in a narrow channel spacing along with a higher frequency for the phase detector. Consequently, the loop bandwidth can be widened, and faster settling time and lower close-in phase noise of the PLL are achieved.

Fig. 1 shows the building blocks of the SSCG architecture, which consists of a PLL, a $\Delta-\Sigma$ modulator, and a triangular-modulated profile. The PLL is a digiphase-based fractional-N synthesizer with a multimodulus fractional divider (MMFD).

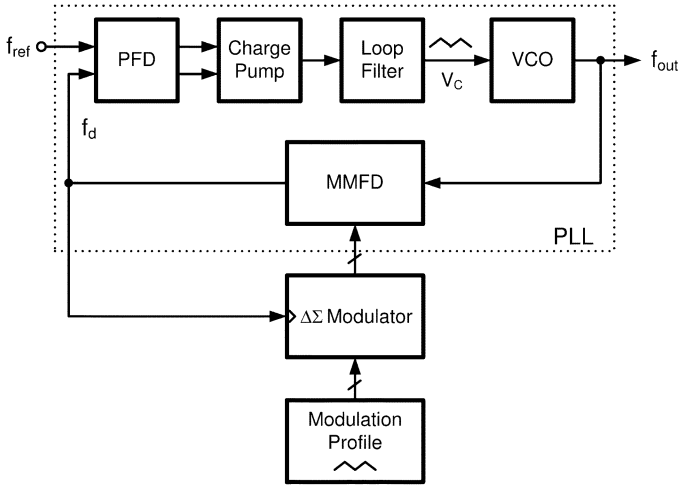

Fig. 1. System architecture.

The instantaneous phase error can be canceled by a phase-compensated technique before the PFD [9]. When the PLL is locked, neglecting the modulated operation of the $\Delta-\Sigma$ modulator to the MMFD, the output frequency of the PLL is $(M \pm k/16) f_{\rm ref}$, and the synthesizer operates as a modulo-31 fractional-N frequency synthesizer for $k = 0, \ldots, 15$.

As shown in Fig. 1, the complete fractional-N division uses a$\Delta-\Sigma$ modulator to achieve fine frequency resolution with a randomly modulated MMFD. The $\Delta-\Sigma$ modulation technique is similar to the random jitter method with noise-shaping property [8]. The PLL can act as a low-pass filter to the modulator quantization noise to suppress the noise at high frequencies. Shown in Fig. 2(a) is the conceptual plot of the proposed fractional PLL for SSCG. The output spread frequency changing over the time is represented on the left side. In this case, the output frequency can increase by fractions using a$\Delta-\Sigma$ modulator, as shown on the right side of Fig. 2(a). The $\Delta-\Sigma$ modulator is based on a third-order multistage noise-shaping (MASH) cascade modulator [11]. By having a multilevel quantizer, the eight-level quantizer expands the active division range from $\{M, M + 1/16\}$ to $\{M - 3/16, M - 2/16, \ldots, M + 3/16, M + 4/16\}$.

By clocking the $\Delta-\Sigma$ modulator, the overall fine-fractional division has been created which has more resolution than the basic division by MMFD in the PLL. An expression that is applicable to the fractional synthesis in SSCG is the following:

$$N_F = M + \frac{F}{16 \times 2^P} \tag{1}$$

where N_F is the resulting divisor and F is related to the input of the P-bit $\Delta-\Sigma$ modulator. A triangular frequency modulation profile introducing to F for an up-spreading clock generation is shown in Fig. 2(a), where f_m is the modulation frequency. The frequency deviation can be represented by

$$\delta = \frac{F_{\max}}{16 \times M \times 2^P} \tag{2}$$

where $F_{\max}$ denotes the maximum value of F. Similarly, Fig. 2(b) shows a down-spread frequency function which can be done by negative F during $\{M, M - 1/16\}$.

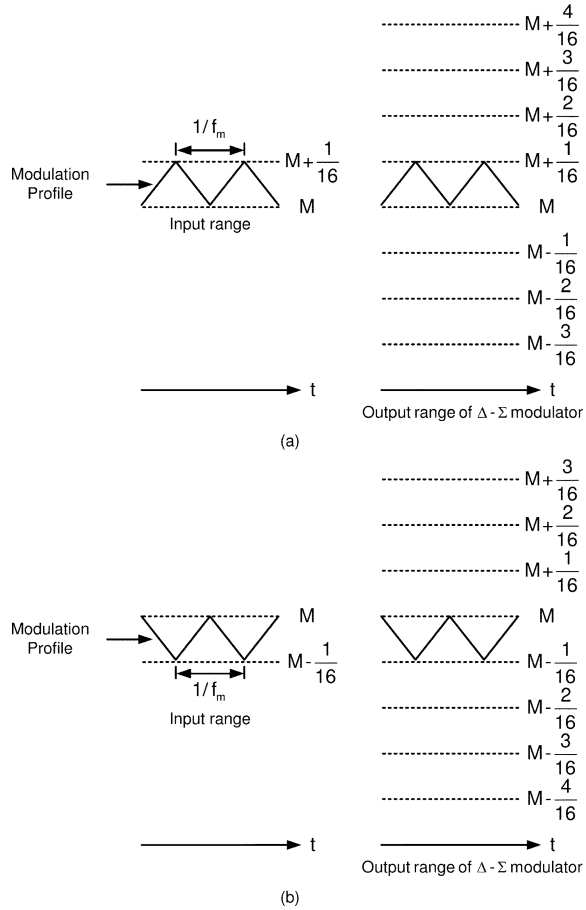

Fig. 2. Basic concept of $\Delta-\Sigma$ fractional division. (a) Up-spread frequency case. (b) Down-spread frequency case.

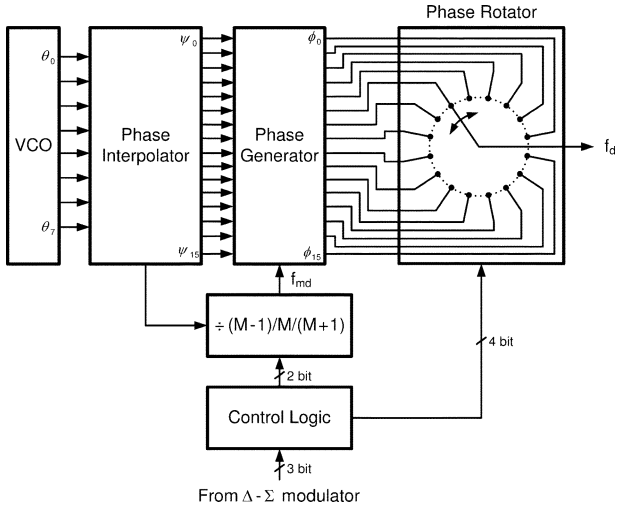

Fig. 3. Block diagram of the MMFD.

As can be seen, this case combines the digiphase-based fractional-N PLL with the $\Delta-\Sigma$ modulator, thereby achieving a high-resolution fractional division and mitigating the design complexity of the $\Delta-\Sigma$ modulator.

B. Edge-Combining Fractional Divider

The noninteger dividing values in a fractional PLL can be achieved by the periodic dithering of the dividing ratio between integer values. However, the dithering leads to a periodic phase

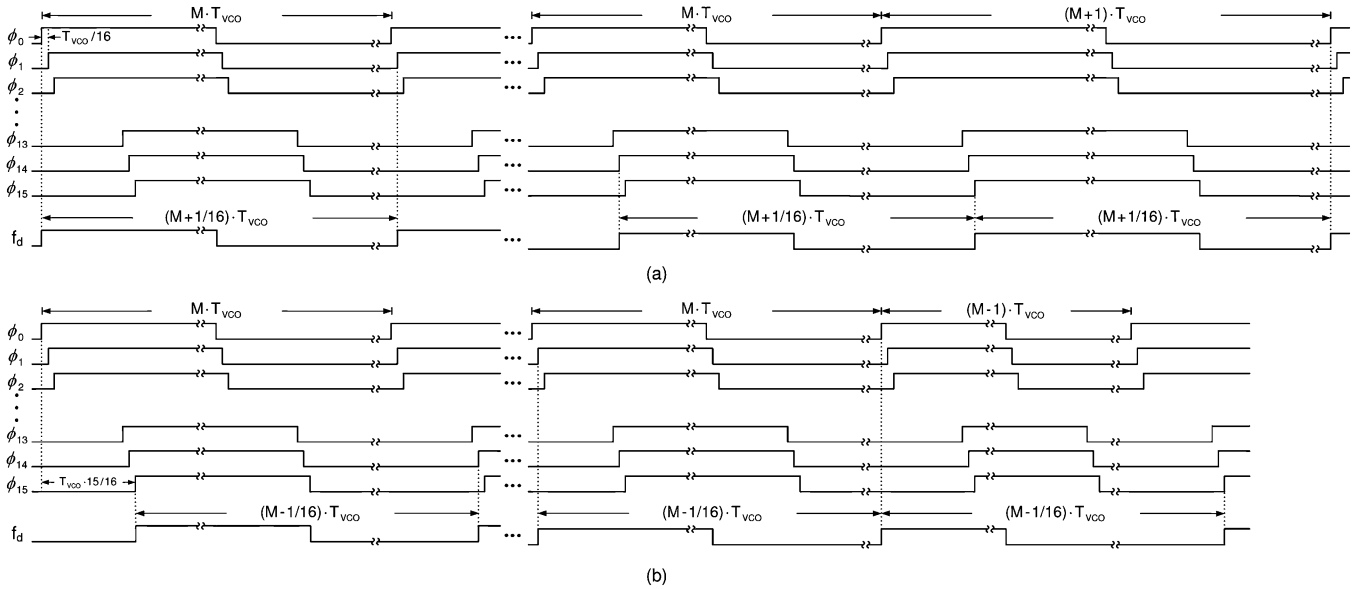

Fig. 4. Operation of the MMFD when (a) $F = 1$ and (b) $F = -1$.

error and introduces spurious tones in the output spectrum. If multiphase clock signals are available, the noninteger divider is directly implemented without dithering [12].

The multimodulus divider with noninteger dividing values is based on the circuit in Fig. 3. It consists of a phase interpolator, a 16-phase phase generator, a phase rotator, a logic controller, and an integral divider which has a triple-mode division ratio of $(M-1)/M/(M+1)$, depending on the selected up and down spread-spectrum modes. A ring VCO is a convenient way to generate multiple phases. Eight clock phases are generated using four-stage ring oscillator built with differential delay elements. Following the VCO, more finely spaced clocks are generated by a phase interpolator, which has 16-phase outputs. The triple-modulus divider is used to divide the VCO frequency by $(M-1)$, M, or $(M+1)$ with phase compensation from the phase generator and rotator to perform fractionality. The fractional division ratio can be represented by $(M + k/16)$. A set of phase-shift waveforms, $\phi_0, \ldots, \phi_{15}$, is obtained by the phase generator, and the amount of the phase shift is 1/16 of the VCO period. By manipulating the waveform set, an output waveform whose period is a fractional multiple of the VCO period is generated. For example, when the desired fractional value is 1/16, the phase rotator multiplexes the phase-shift waveforms with the following cyclic sequence: $\phi_0 \rightarrow \phi_1 \rightarrow \cdots \rightarrow \phi_{15} \rightarrow \phi_0 \cdots$, and the output period of the fractional divider becomes $(M+1/16)T_{\rm vco}$, as shown in Fig. 4(a). The division ratio should periodically switch from M to $(M+1)$ when the output waveform is multiplexed fromϕ_{15} to ϕ_0. For arbitrary k, in general, the output period T_d can be calculated as

$$T_d = \left(M + \frac{k}{16}\right) T_{\rm vco} = MT_{\rm vco} + \frac{k}{16} T_{\rm vco}. \tag{3}$$

The instantaneous timing error due to the divide-by-M is determined by

$$\Delta T_M = T_d - MT_{\rm vco} = \frac{k}{16} T_{\rm vco}. \tag{4}$$

Similarly, the instantaneous timing error due to the divide-by-$(M+1)$ is determined by

$$\Delta T_{M+1} = T_d - (M+1)T_{\rm vco} = -\left(1 - \frac{k}{16}\right) T_{\rm vco} \tag{5}$$

Since the timing error sequence can be predicted from the logic controller, the timing correction is possible if the right phase is added with opposite direction of timing sequence. Similarly, the operation for negative values of k can also be verified, and the fractional division ratio of $(M - 1/16)$ is an example also shown in Fig. 4(b), while the phase-shift sequence is changed to $\phi_{15} \rightarrow \phi_{14} \rightarrow \cdots \rightarrow \phi_0 \rightarrow \phi_{15} \cdots$. Note that the division ratio should switch from M to $(M-1)$ if the output is multiplexed from ϕ_0 to ϕ_{15}.

C. Summarized Features of the Proposed SSCG Architecture

Since the required frequency deviation of the SSCG is quite small, it requires a narrow channel spacing by using $\Delta{-}\Sigma$ modulation. A conventional $\Delta{-}\Sigma$ modulated technique is usually employed to modulate the integer-N divider in PLLs and produce a triangular waveform with a small deviation as control signal on a VCO. Unlike the integer-N divider, in this work, a multimodulus divider can provide noninteger dividing values. Compared with the integer-N PLL with a $\Delta{-}\Sigma$ modulator for SSCG applications, the proposed structure desires fewer bits for $\Delta{-}\Sigma$ modulation to satisfy the requirement in (1). It also results in a higher oversampling frequency of the reference clock for the $\Delta{-}\Sigma$ modulator and the PLL. In this way, enlarging the reference frequency of the PLL can get a wider loop bandwidth and a faster switching speed. In addition, since the quantization noise is sharped by the oversampling clock with higher frequencies, the quantization noise can be more attenuated by the filtering characteristic in the PLL, as discussed in Section IV.

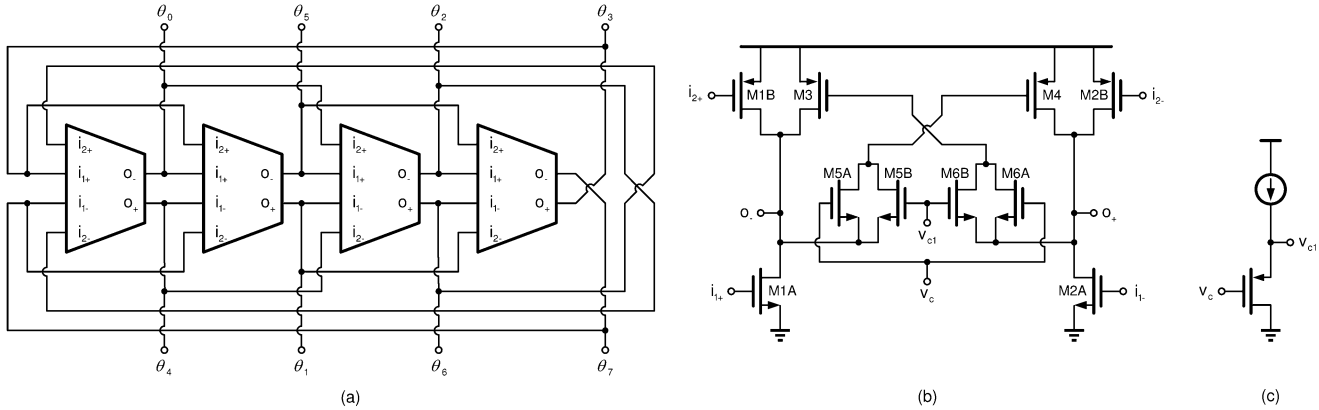

Fig. 5. (a) Ring VCO with dual-delay paths. (b) Delay cell of the VCO. (c) Control circuit.

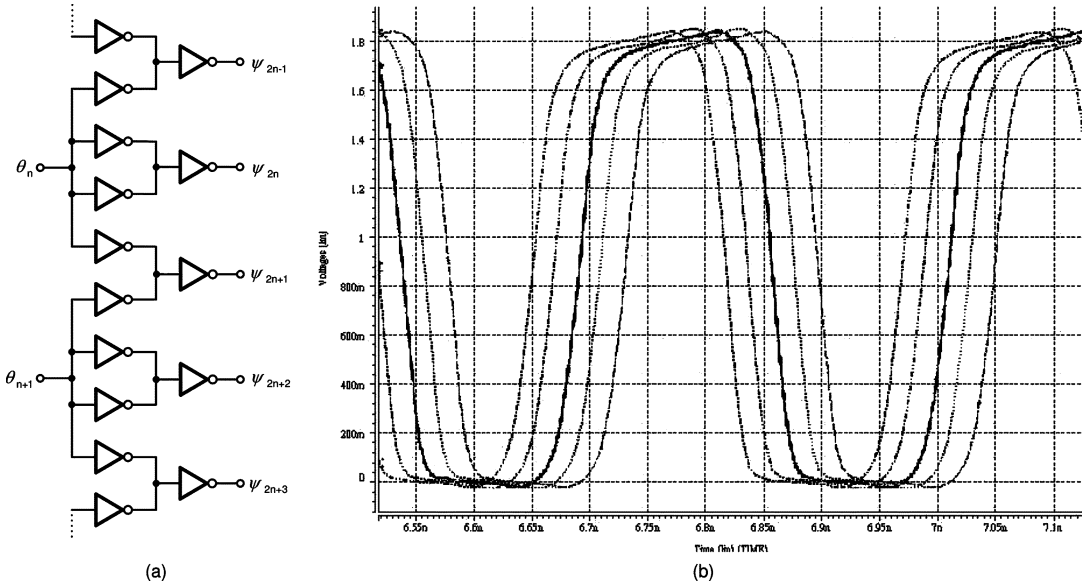

Fig. 6. Clock phases tapped from the VCO by an interpolator for finer phase spacing.(a) Interpolation cell. (b) Simulated output waveforms.

III. Circuit Implementation

A. VCO

By using a dual-delay ring structure to implement the VCO, as shown in Fig. 5(a), higher operation frequency and wide tuning range are achieved simultaneously [13]. In this circuit, a differential structure is selected for duty balanced clock pair generation, and device size and silicon layout are carefully done for the circuit matching. The ring oscillator is a fully integrated VCO that depends on a series of delay stages and an inversion in the signal path to produce the desired periodic output signals. In order for the ring to oscillate with an even number of stages, the differential outputs of one of the stages are twisted to introduce an additional inversion. As shown in Fig. 5(a), eight clock phases are generated.

As shown in Fig. 5(b), a full-switching delay cell is designed in the VCO [13]. The cell has a differential structure to immune to the power-supply- and substrate-injected noise sources. A pair of pMOS load transistors, i.e., M3 and M4, is added to constitute a CMOS latch. Two cross-coupled pairs of nMOS transistors, i.e., M5A and M5B and M6A and M6B, control the maximum gate voltage of the pMOS load transistors and limit the strength of the added latch. An nMOS pair of M1A and M2A operates as a dominant input path, while a pMOS pair of M1B and M2B acts as a nondominant path available to the delay cell.

Fig. 5(c) shows the voltage shifter by using a source follower for control voltages. The overall control configuration can provide a wide dynamic range, which is generated by summing the tuning characteristics from v_c and v_{c1}. When v_c is below the threshold voltage, M5A and M6A are turned off while the delay cell still normally operates due to v_{c1} driving to M5B and M6B. As v_c increases, the latch of M3 and M4 becomes strong, and it resists the voltage switching in the differential delay cell. As a result, the delay time increases. With the help of the positive feedback of the latch, the transition edge of the output waveforms remains sharp in spite of slow delay time. Note that the output signals eventually exhibit rail-to-rail swings.

B. Phase Interpolator

Fig. 6(a) shows the phase interpolation for finer phase spacing. To generate phase spacing of less than a delay of a unit delay cell in the VCO, clock phases separated by one buffer

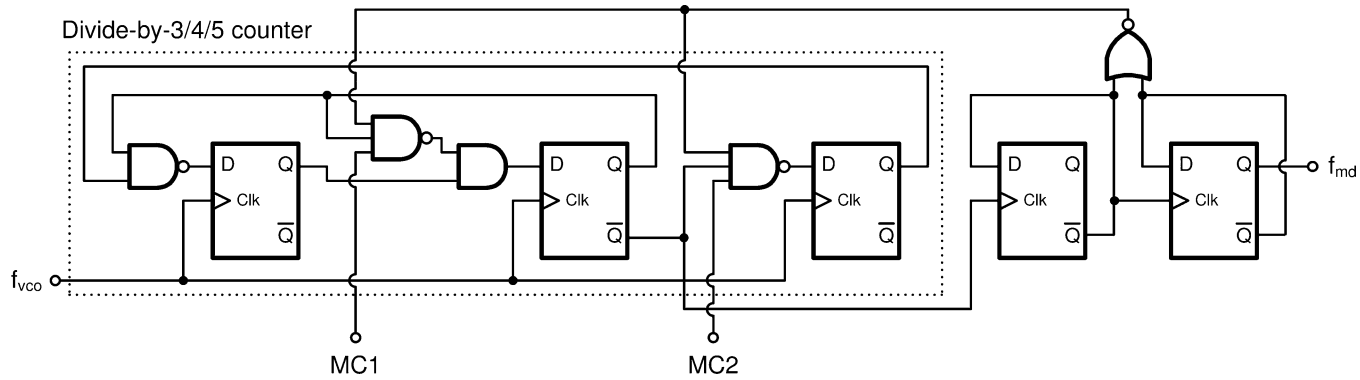

Fig. 7. Triple-modulus integer divider in the MMFD.

delay are interpolated by an interpolator. Since the interpolator has an intrinsic delay, the clock phases are also delayed by a noninterpolating buffer so that the interpolator output is a clock phase between the clock phases from the buffers [14]. The simulated output waveforms are shown in Fig. 6(b).

C. Triple-Modulus Integer Divider

The triple-modulus divider is the high-frequency building block in the PLL. This circuit shown in Fig. 7 divides the frequency of the VCO output signal by a factor of 15/16/17, depending on the logic values of the control modes (MC1 and MC2). It consists of a synchronous divide-by-3/4/5 counter as the first stage and an asynchronous divide-by-4 counter as the second stage. The circuits in the first stage are fully differential, while the single-ended logic circuits are used in the second stage. To reduce the supply noise, an emitter-coupled-logic-like differential logic is used in the high-speed stage [15]. The toggle flip-flops are made by true-single-phase-clock D-type flip-flops of [16].

D. Phase Generator

Although Fig. 6 provides 16-phase VCO signals, it is difficult to implement such a high-speed frond-end circuit with low power consumption for the fractional divider. One way to overcome the speed and power consumption limits is to use the multiphase waveforms of the divider (in Fig. 7), which can maintain the resolution to a fraction of the intrinsic phase spacing but can lower the speed as well as power consumption. In Fig. 8(a), the multiphase generator is used to precisely generate the output 16-phase waveforms shown in Fig. 4. Note that dummy elements are added for matching each output with the same capacitive load. The operation of the phase generator can be explained by the timing diagrams of Fig. 8(b). The sampling signals are generated by the phase interpolator [in Fig. 6(a)], which have a sampling time interval of $T_{\rm vco}/16$. Since the sampled signal is from the divider, the multiphase outputs of the phase generator have a period of $15T_{\rm vco}$, $16T_{\rm vco}$, or $17T_{\rm vco}$ with a very small time difference of $T_{\rm vco}/16$.

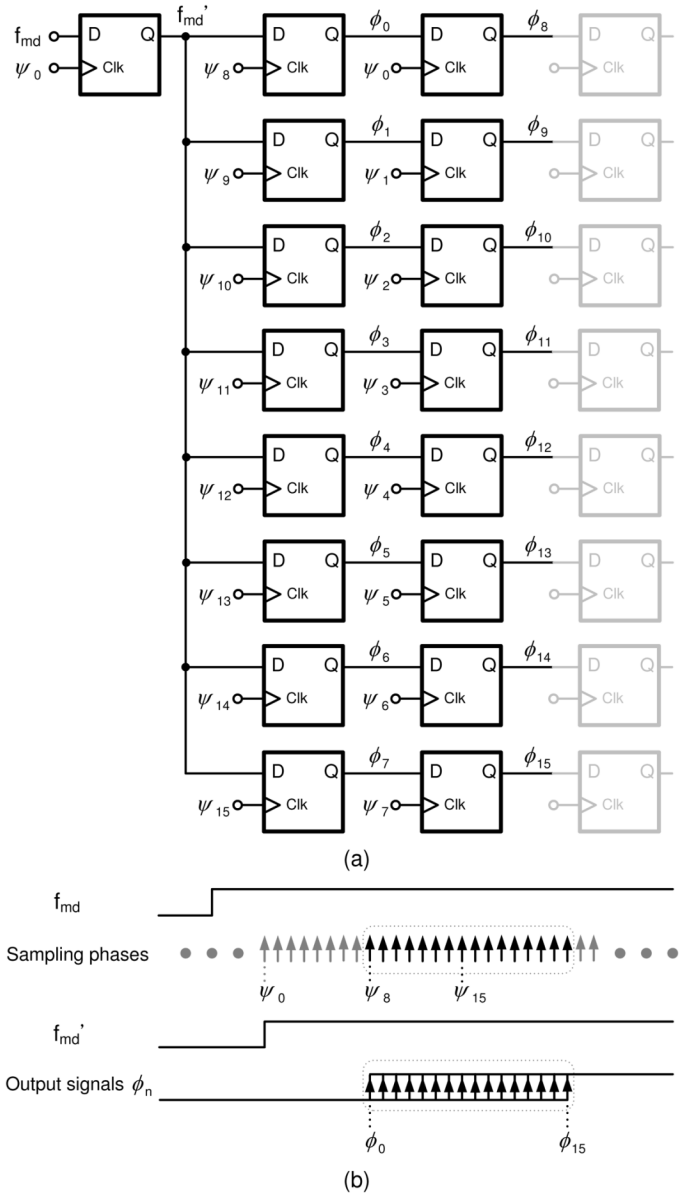

Fig. 8. Multiphase outputs following the divider in Fig. 7. (a) Scheme. (b) Timing diagram.

E. Phase Rotator

The phase rotator, shown in Fig. 9, employs a pseudo-NMOS logic design and provides the function of phase selection and the phase-combined generation to produce the output signal. Compared to the conventional static CMOS logic circuit, the transistor number, the capacitive load, and the layout area of the

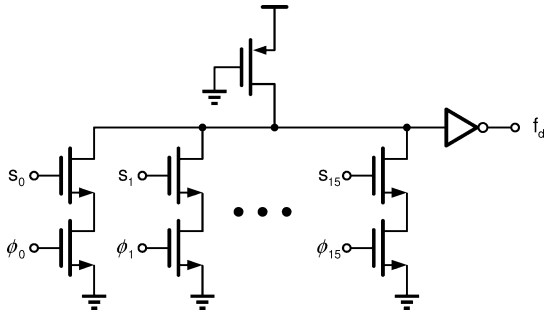

Fig. 9. Phase rotator.

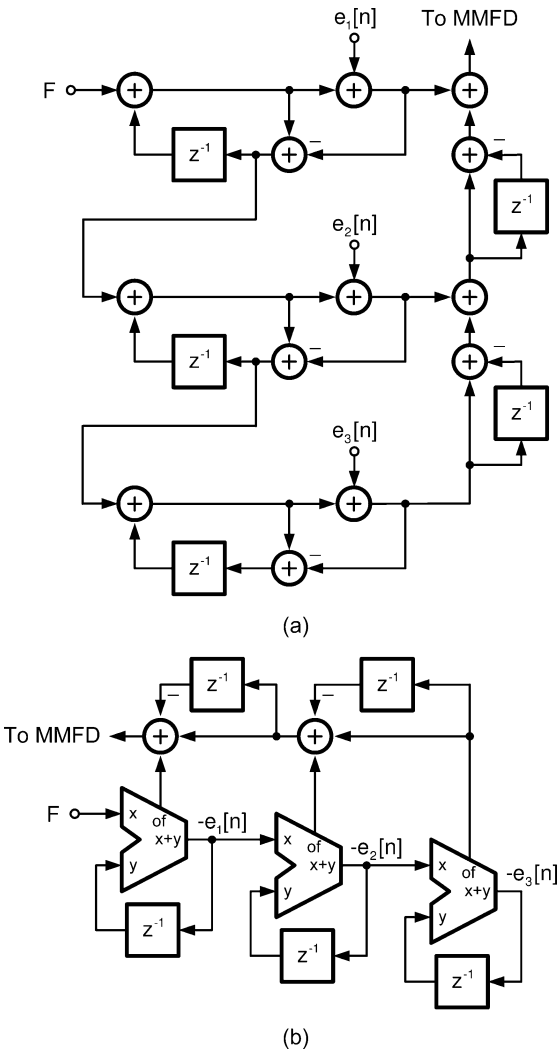

Fig. 10. $\Delta-\Sigma$ MASH modulator. (a) Signal-flow graph. (b) Equivalent digital implementation.

pseudo-NMOS logic are reduced. The single pMOS pull-up has much lower resistance and capacitance than a series of stacked pMOS devices.

F. $\Delta-\Sigma$ Modulator

Fig. 10 shows the 8-bit third-order $\Delta-\Sigma$ modulator, implemented by the third-order MASH technique [11]. The MASH technique is based on cascading stable first-order modulators and using the quantization error of the previous stage as the input

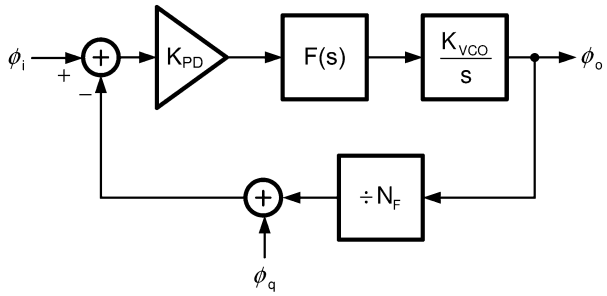

Fig. 11. Linear phase-domain model with quantization noise source.

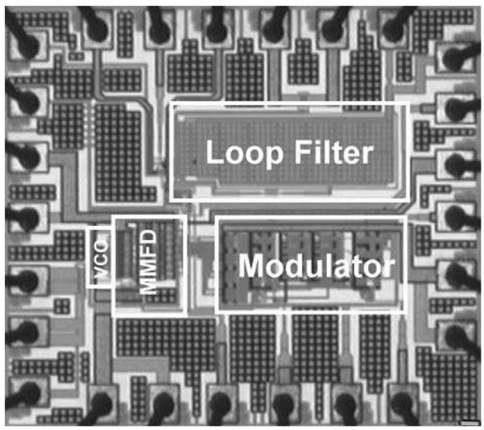

Fig. 12. Microphotograph of the SSCG circuit.

signal of the succeeding one to obtain an inherent stable modulator of higher order. The outputs of the different stages are merged in a manner that the quantization error of the first stage is canceled out, and only the quantization error of the last stage remains, filtered with a high-pass function of the order number of stages cascaded. With the $\Delta-\Sigma$ modulator, the output frequency of the proposed fractional-N PLL can thus be calculated by

$$f_{\rm vco}(z) = f_{\rm ref} \cdot \left(M + \frac{F}{16 \times 2^P}\right) + f_{\rm ref} \cdot E_3(z) \cdot (1 - z^{-1})^3. \tag{6}$$

The equation shows that the output of the PLL is composed of the reference signal multiplied by the wanted fractional number plus the quantization noise shaped by a third-order high-pass. The noise can be filtered by the low-pass transfer function of the PLL.

The $\Delta-\Sigma$ modulator offers finer frequency resolution with a digital word without reducing phase detector frequency. On the other hand, the $\Delta-\Sigma$ modulator can be used to randomize the multiphase outputs of the divider in the PLL, thereby reducing the interpolated phase mismatch [17].

G. Others

Charge-pump PLLs incorporating a sequential-logic PFD have been widely used [18]. Reasons for its popularity include tracking, frequency-aided acquisition, and low cost. The purpose of the charge pump is to convert the logic states of the PFD into analog signals suitable for controlling the VCO.

TABLE I
COMPARISONS WITH OTHER WORKS AND PERFORMANCE SUMMARY

Refs.	[4]	[5]	[6]	This work
Technology (μm)	0.18 CMOS	0.15 CMOS	0.18 CMOS	0.18 CMOS
Supply voltage	1.8 V	1.5 V	1.8 V	1.8 V
Operating frequency	1.5 GHz	1.5 GHz	1.5 GHz	2.4 GHz
Modulation method	Δ-Σ modulated divider			
Modulation profile	Triangular			
Modulation type	Down spread	Down spread	Down spread	Up/down spread
Modulation frequency	30.1 KHz	31.1 KHz	31 KHz	33 KHz
Spread ratio	0.5%	0.5%	0.5%	0.37%
Peak power reduction	9.8 dB	10.0 dB	14.77 dB	$>$ 11.4 dB
Jitter performance	With spread: ΔT_{rms}: 3.24 ps ΔT_{pk-pk}: 58.3 ps	With spread: ΔT_{rms}: 8.1 ps	With spread: ΔT_{rms}: 5.55 ps ΔT_{pk-pk}: 34.2 ps	W/o spread: ΔT_{rms}: 2.81 ps ΔT_{pk-pk}: 18.82 ps Up spread: ΔT_{rms}: 9.96 ps ΔT_{pk-pk}: 52.59 ps Down spread: ΔT_{rms}: 9.74 ps ΔT_{pk-pk}: 56.79 ps
Power dissipation	77 mW	54 mW	34.2 mW	36 mW
Chip area	1750×9400 μm^2	880×480 μm^2 (w/o IO)	560×310 μm^2 (w/o IO)	950×850 μm^2

The loop filter introducing extra poles and zeros is made by passive components and is used to set the noise and transient performance of the PLL.

IV. SIMPLIFIED LINEAR ANALYSIS

Since each edge of the fractional-N divider output is periodically synchronized with one of the multiphase signals from the VCO and interpolator, the timing information on the delay mismatches is contained in the divider output. In addition, the $\Delta-\Sigma$ modulator introduced to the fractional-N divider can randomize and shape the effects in these mismatches. Therefore, the equivalent divider with fractionality can be modeled as an ideal fractional divider plus a quantization noise source, as shown in Fig. 11. The transfer function from this phase error source to the VCO output is given as

$$H_q(s) = \frac{\phi_o(s)}{\phi_q(s)} = -\frac{N_F K_{\rm PD} K_{\rm VCO} F(s)}{N_F s + K_{\rm PD} K_{\rm VCO} F(s)} \qquad (7)$$

where ϕ_q and ϕ_o denote the input quantization noise and the output, respectively, $F(s)$ is the impedance of the loop filter, $K_{\rm PD}$ is the gain of the phase detector and charge pump, and $K_{\rm VCO}$ is the VCO sensitivity. Note that other noise sources are not shown in Fig. 11. The transfer function for quantization exhibits a low-pass characteristic. Therefore, quantization noise outside the loop bandwidth can be attenuated by the low-pass filtering function of the loop.

V. SIMULATED AND EXPERIMENTAL RESULTS

The proposed SSCG circuit was fabricated in a 0.18-μm N-well CMOS technology. Fig. 12 shows the microphotograph with a chip area of 950×850 μm^2. This circuit is fully integrated with an on-chip filter and operates under a 1.8-V supply voltage. The measured VCO transfer function by varying the controlled voltage is shown in Fig. 13, which has a monotonic frequency range of 2.30–2.47 GHz. The overall specifications of the SSCG circuit with several prior works are given in Table I.

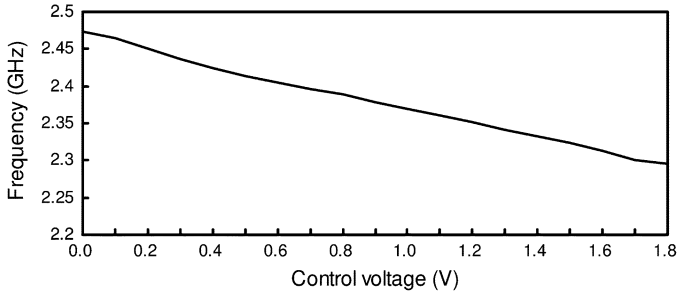

Fig. 13. Measured tuning characteristic of the VCO.

The modulation frequency is approximately 33 kHz. The modulation profile is provided by a 4-bit triangular waveform generator and is used to to control the four most significant bits (MSBs) of the $\Delta-\Sigma$ modulator. With a reference frequency of 150 MHz, the PLL provides a 2.4-GHz output frequency. The simulated transient characteristic of the modulated output frequency for SSCG in down-spread operation is shown in Fig. 14. Fig. 15 shows the measured spectra of the 2.4-GHz output signals without and with up-spread [Fig. 15(a)] and down-spread [Fig. 15(b)] spectrum clocking, and the ratios of frequency deviation are 0.37% and -0.37%, respectively. The peak amplitude reduction can achieve more than 11.4 dBm. In addition, the measured waveforms are shown in Fig. 16. As can be seen, the measured jitter performance of the output clock without spreading is shown in Fig. 16(a), which has rms jitter of 2.81 ps and peak-to-peak jitter of 18.82 ps. After spread-spectrum operation, the up-spread clock has rms jitter of 9.96 ps and peak-to-peak jitter of 52.59 ps shown in Fig. 16(b),

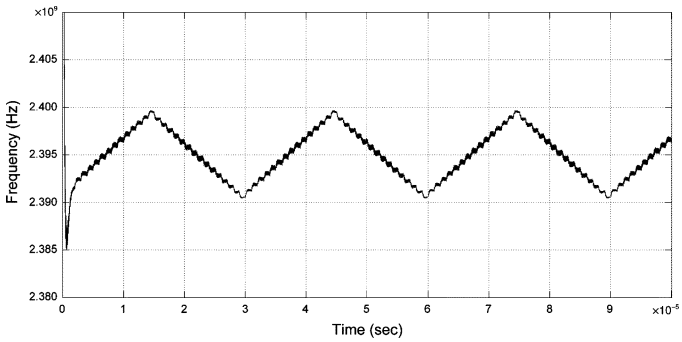

Fig. 14. Simulated down-spread plot of the proposed fractional PLL for SSCG with a triangular profile.

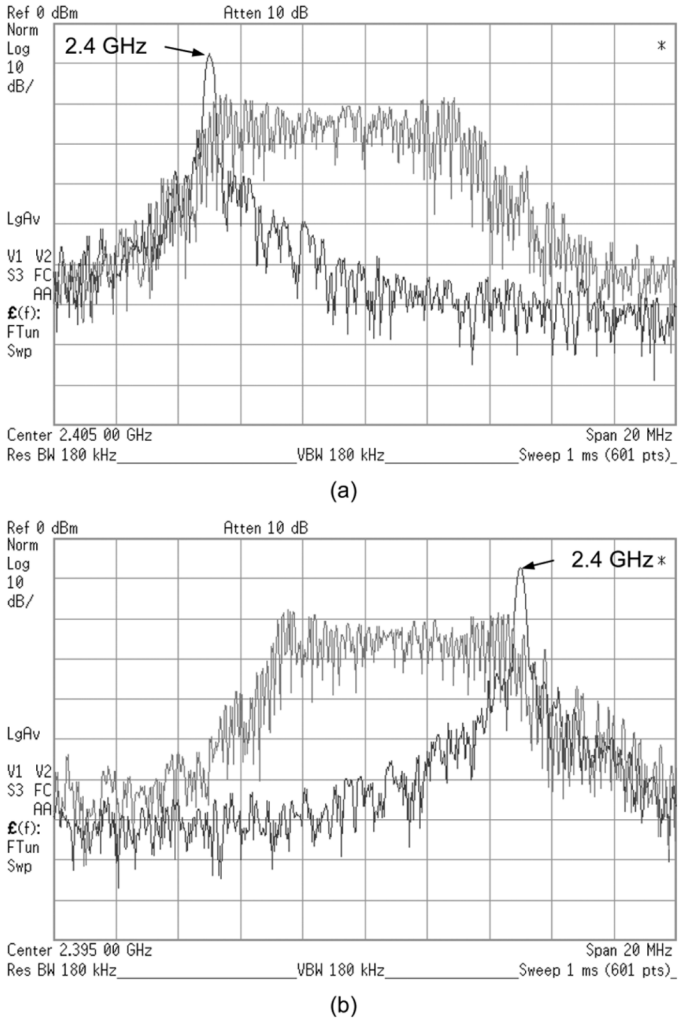

Fig. 15. Measured spectra of the output signals. (a) Without and with up spread. (b) Without and with down spread.

while the down-spread clock has rms jitter of 9.74 ps and peak-to-peak jitter of 56.79 ps shown in Fig. 16(c).

VI. Conclusion

A 2.4-GHz $\Delta-\Sigma$-modulated fractional-PLL-based SSCG circuit with triangular modulation on the multiphase VCO fabricated in a 0.18-μm CMOS process is presented. The $\Delta-\Sigma$ modulator and the PLL employ a phase-interpolated technique with multiphase outputs that can be randomized and provided

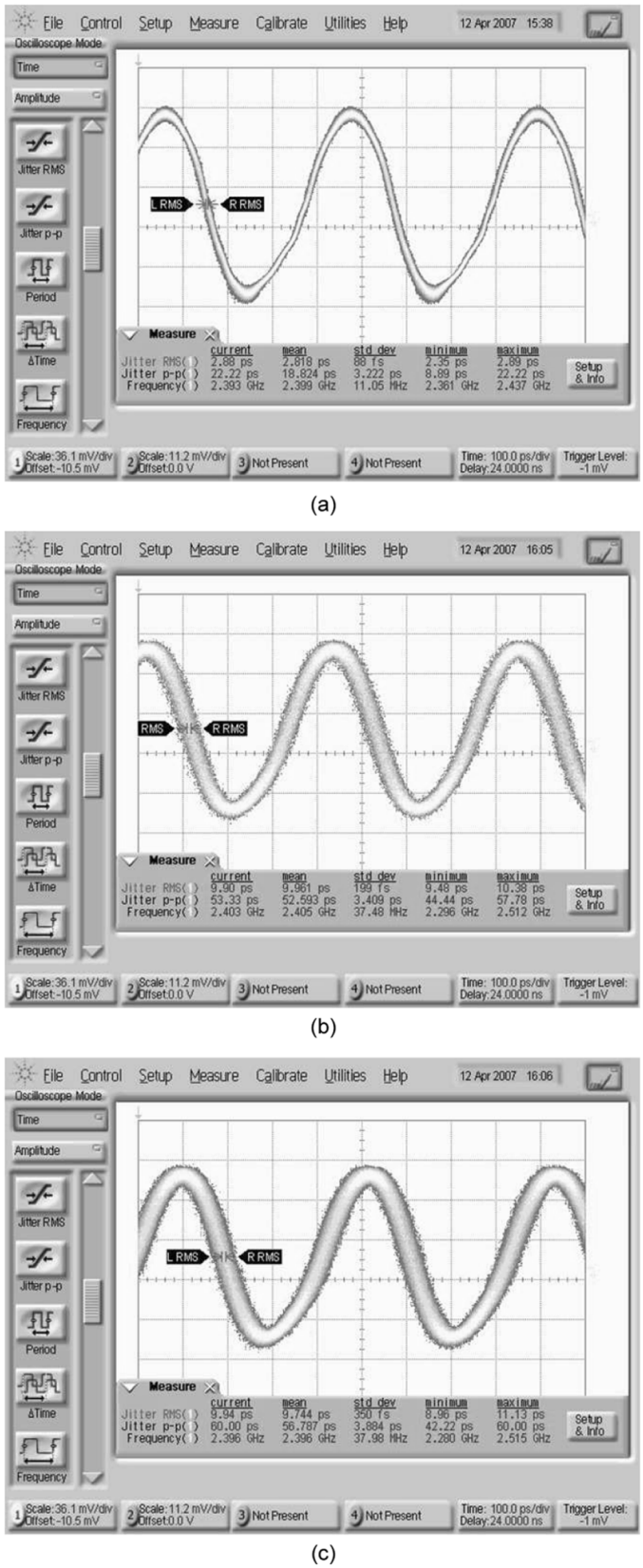

Fig. 16. Measured output jitter when the PLL generates 2.4-GHz output. (a) Without spread-spectrum clocking. (b) With up-spread-spectrum clocking. (c) With down-spread-spectrum clocking.

finer frequency resolution for SSCG applications. The measured spectra show that clocking peak amplitude is attenuated, and the proposed architecture does achieve the spread-spectrum function, as expected.

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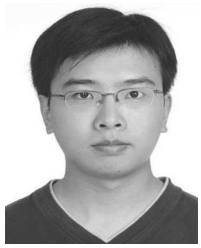

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