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On-Chip Sinusoidal Signal Generation with Harmonic Cancelation for Analog and Mixed-Signal BIST Applications

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Abstract This work presents a technique for the on-chip generation of analog sinusoidal signals with high spectral quality and reduced circuitry resources. The proposed generation technique consists of a modified low-order analog filter, that provides a sinusoidal output as response to a DC input, combined with a harmonic cancellation strategy to improve the linearity of the generated signal. The proposed generator has the attributes of digital programming and control, low area overhead, and low design effort, which make this approach very suitable as test stimulus generator for built-in test applications. An integrated prototype designed in a 180nm CMOS technology is presented in order to show the feasibility of the technique. Results obtained from the prototype show a THD around −80dB.

Keywords On-chip signal generators · On-chip sine-wave generators · Harmonic cancellation · Analog BIST · Mixed-signal BIST

1 Introduction

Nowadays, commercial trends in the IC industry, including telecommunications, multimedia, instrumentation, automotive, etc. are driving the integration of complex mixed-signal electronics systems consisting of tightly integrated analog, mixed-signal, RF, and digital circuitry onto a single IC substrate. Despite this increase in complexity, design and manufacturing costs have remained reasonably contained due to steady developments in design tools and technological advances. However, in this evolution there is a simultaneous increase in the cost of testing and diagnosing these devices in such a way that test is becoming a dominant factor in overall production cost [13].

Usually, the main test difficulties in a complex mixed-signal IC are due to the test of non-digital parts. Traditional specification-based tests of analog, mixed-signal and RF embedded blocks are costly and time-consuming procedures, that require dedicated test access to internal nodes of the system, and expensive Automated Test Equipment. Moreover, they demand high quality input stimuli, high data volume acquisition, high processing capability, etc.

A promising solution to these pressing issues is the development of analog and mixed-signal BIST. BIST techniques are aimed at moving some of the ATE functionality into the DUT, reducing this way the complexity –and hence the cost– of the external tester. In this framework, the generation of spectrally pure sinusoidal signals has a wide variety of potential applications in the field of analog and mixed-signal testing. In fact, most of the analog and mixed-signal subsystems in a SoC, such as analog filters, A/D converters, signal conditioners, etc, can be characterized by applying a sinusoidal test stimulus and analyzing the response. For that purpose, the applied stimulus must exhibit higher linearity than the DUT and be able to sweep its entire input range. Providing an efficient method for the on-chip generation of such a stimulus can be identified as a

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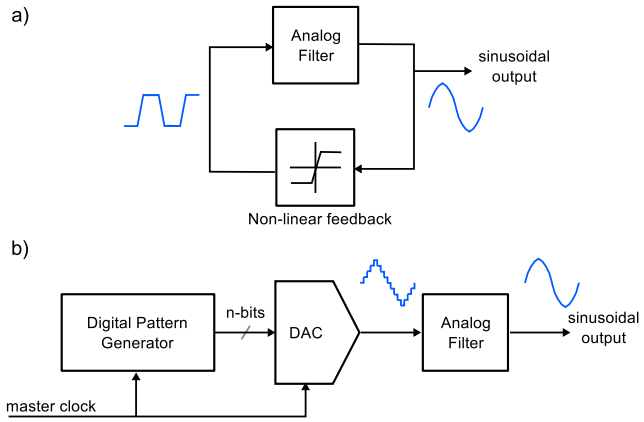

Fig. 1 a) Typical closed-loop sinusoidal signal generator; b) Typical open-loop sinusoidal signal generator

key point to extend many test programs to a full-BIST scheme.

This work addresses this objective and presents an efficient on-chip sinewave generation technique. It consists of a modified analog filter that outputs a sinusoidal signal as response to a DC excitation, combined with a very simple harmonic cancellation technique.

This paper is organized as follows. Section 2 reviews briefly some previous strategies for sine-wave generation. Section 3 presents the theoretical basis of the proposed generation technique, and then Section 4 discusses its practical implementation. Section 5 details the design of a demonstrator prototype in a 180nm CMOS technology, while Section 6 provides some relevant results to assess the performance of the prototype and compares it to current state-of-the-art. Finally, Section 7 summarizes the main contributions of this work.

2 Previous works

Analog test stimulus generation for BIST applications is still an open research topic in the test community. Indeed, a number of different strategies for analog signal generation have been published for the last years [1–7, 9, 10, 12, 14, 15, 18].

Classical approaches for the on-chip generation of sinusoidal test stimuli can be roughly classified into the two categories depicted in Fig. 1: closed-loop generators, which consists of a filtering section with a non-linear feedback mechanism [1, 4, 12], and open-loop generators, which are based on a digital pattern generator followed by a D/A conversion and a filtering stage [2, 5, 14].

Concerning closed-loop oscillators, the quality of the generated signal depends strongly on the linearity and selectivity of the filter and the shape of the non-linear feedback function. Highly selective filters and smooth non-linear feedback functions are needed for the generation of low-distorted sinusoids. These two requirements usually make the design of this family of generators a challenging task.

On the other hand, typical open-loop generators, based on the D/A conversion and filtering of a stored digital pattern, bring the advantage of a digital interface for control and programmability tasks. In this case the linearity of the generator is affected by two main sources: the D/A converter and the output analog filter. Digital techniques have been proposed for canceling harmonic components at the output of the DAC by measuring these unwanted components and pre-distorting the input codes of the DAC accordingly [9, 10, 15]. These techniques require a precise measurement of the distortion components, and a DAC with a high enough resolution to handle the pre-distorted codes. With regard to the output filter, its order has to be high enough to cancel the out-of-band quantization noise (which may be cumbersome for techniques based on $\Sigma\Delta$ modulation such as the works in [5, 14]), and in any case the linearity of the filter will limit the linearity of the generated output signal.

Some recent proposals for sinusoidal signal generation combine a closed-loop oscillator and a harmonic cancellation technique to provide highly linear sinusoidal signals [6, 7, 18]. These techniques are based on the fact that adding time-shifted versions of a periodic waveform it is possible to cancel some of the harmonic components in the original waveform. The generation strategy proposed in [6] combines time-delayed versions of a square-wave signal provided by a digital ring oscillator. As a result of this combination low-frequency harmonics are canceled, while high frequency harmonics are later attenuated by a passive RC filter. The linearity of the generated signal is limited in this case by the accuracy of the timing and the mismatch in the components that perform the combination of the time-delayed signals.

On the other hand, the approach in [7, 18] is based on combining the outputs of a phase-shift oscillator. The work demonstrates that by properly weighting and summing the output signals of a phase-shift oscillator, it is possible to obtain sinusoids with a very low harmonic distortion. Good linearity figures are demonstrated using discrete on-board prototypes. However, moving the technique to an on-chip implementation may be problematic due to the extensive use of analog processing, which would demand large on-chip resources and power consumption.

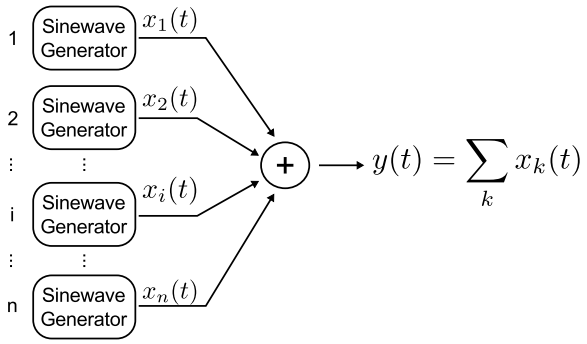

Fig. 2 Conceptual block diagram of a sine-wave generator with harmonic cancellation. Each $x_i(t)$ is a time-delayed version of the same sine-wave

As an alternative, the technique presented by the authors in [3] makes use of a similar harmonic cancellation strategy, but instead of employing an oscillator, we propose to use the efficient methodology for sine-wave generation presented in [2]. This generation technique is based on a low-order modified analog filter with a DC input and programmable input elements, in such a way that the filter performs signal generation and filtering of the unwanted spectral components at the same time. Harmonic cancellation is achieved by digitally programming the input elements at no extra cost. The present work is an extended and improved version of the previous one in [3].

3 Theoretical basis

Figure 2 shows a conceptual block diagram of a signal generator with harmonic cancellation. It is composed of a set of n matched sinusoidal signal generators that provide time-delayed versions of the same sinusoidal signal. The set of time delayed signals $x_i(t)$ are added to provide harmonic cancellation on the output sine-wave signal $y(t)$. Let us discuss each stage in this conceptual diagram separately.

3.1 Harmonic cancellation

Harmonic cancellation is a classical linearization method based on combining time-delayed versions of a periodic signal. This technique has been successfully employed in different applications, such as polyphase networks [11] and push-push and triple-push oscillators [16, 17]. Our proposed sine-wave generator takes advantage of this strategy for improving the spectral purity of the generated sinusoidal signal above the performance of the individual matched generators in Fig. 2.

Let us consider signal $x_1(t)$ generated by the first of the matched basic generators in Fig. 2. Signal $x_1(t)$ is a periodic signal that can be expressed as a Fourier series expansion,

$$x_1(t) = \sum_{k=1}^{\infty} A_k \cos(k\omega_0 t + \varphi_k) \tag{1}$$

where A_k and φ_k are the amplitude and phase of harmonic component k in signal $x_1(t)$, respectively, and ω_0 is the fundamental frequency of $x_1(t)$.

Let us consider a time-shifted version of signal (1),

$$x_1(t+\Delta t) = \sum_{k=1}^{\infty} A_k \cos(k\phi)\cos(k\omega_0 t + \varphi_k) - \sum_{k=1}^{\infty} A_k \sin(k\phi)\sin(k\omega_0 t + \varphi_k) \tag{2}$$

where $\phi = \omega_0 \Delta t$ is the applied phase shift. Let us accept for the sake of the argument that each matched generator in Fig. 2 can be clocked to generate time-shifted versions of the same sinusoidal signal with different delays Δt_i, and let us now define signal $y(t)$ as the sum,

$$y(t) = x_1(t) + \sum_{i=1}^{p} [x_1(t+\Delta t_i) + x_1(t-\Delta t_i)] \tag{3}$$

where the $n-1$ additional generators in Fig. 2 are used to provide $p = (n-1)/2$ pairs of signals of opposite delays, Δt_i and $-\Delta t_i$, respect to signal $x_1(t)$. From equations (1), (2), and (3) it can be derived,

$$y(t) = \sum_{k=1}^{\infty} A_k \left[1 + 2\sum_{i=1}^{p} \cos(k\phi_i)\right] \cos(k\omega_0 t + \varphi_k) \tag{4}$$

where $\phi_i = \omega_0 \Delta t_i$. That is, as a result of combining time-shifted versions of the original signal $x_1(t)$ with opposite time-shifts, we can build a signal $y(t)$ whose spectral content is that of signal $x_1(t)$ scaled by coefficients $1 + 2\sum_{i=1}^{p} \cos(k\phi_i)$. If phase-shifts ϕ_i are properly selected such that these coefficients are small for a given k, unwanted harmonic components in $y(t)$ can be attenuated or completely cancelled. Equation (4) holds whenever there is a perfect matching between the individual generators. In other words, the linearity of signal $y(t)$ will not depend on the non-linearity of each individual generator, but on their matching.

3.2 Basic sine-wave generation technique

Let us consider now each individual sinusoidal generator in the diagram in Fig. 2. Our proposed signal generator is a modified linear system, as the one conceptually depicted in Fig. 3, whose input stage has been adapted to provide a programmable gain. Let us consider a generic n-th order linear system with one input

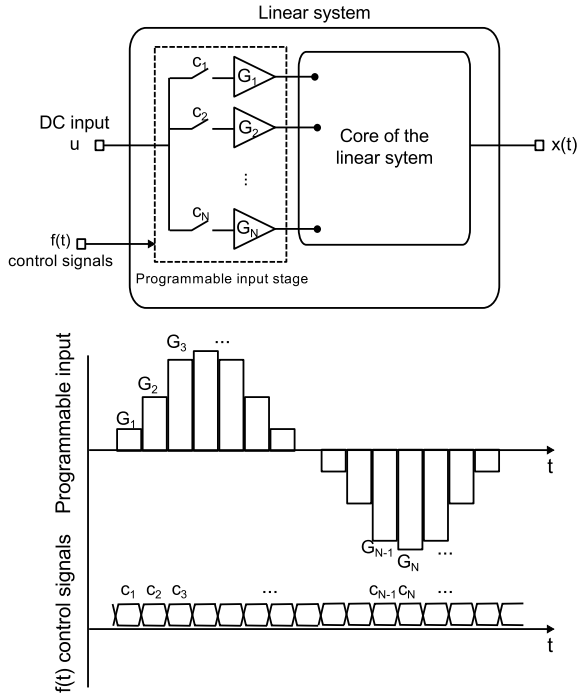

Fig. 3 Conceptual block diagram of our basic sinusoidal signal generation

$u(t)$ and one output $x(t)$. The functionality of this system can be described in terms of its state variables, $[z(t)]$, as

$$\begin{aligned} [\dot{z}(t)] &= [a]\,[z(t)] + [b(t)]\,u(t) \\ x(t) &= [c]\,[z(t)] + d(t)u(t) \end{aligned} \tag{5}$$

where $[z(t)]$ is a $n \times 1$ column vector, coefficient $[a]$ is an $n \times n$ matrix, coefficient $[b(t)]$ is an $n \times 1$ column vector, coefficient $[c]$ is a $1 \times n$ row vector, and coefficient $d(t)$ is a scalar. Due to the programmable nature of the input elements of the system, coefficients $[b(t)]$ and $d(t)$, which link the input to the core of the system, are time dependent.

Let us consider the particular case,

$$\begin{aligned} [b(t)] &= [b]\,f(t) \\ d(t) &= d \times f(t) \\ u(t) &= u \end{aligned} \tag{6}$$

where $[b]$, d, and u are constants and $f(t)$ is a time-dependent, externally controlled function. This particular case represents a system, excited by a DC level, whose input elements vary in time according to a given function $f(t)$, as it is depicted in Fig. 3. Using the Laplace transform, it can be derived from (5) that,

$$\begin{aligned} X(s) &= H(s)\,\{F(s) \otimes u\} = uH(s)F(s) \\ x(t) &= h(t) \otimes \{f(t)u\} = u\,\{h(t) \otimes f(t)\} \end{aligned} \tag{7}$$

where capital letters denote the Laplace transform, operator $\otimes$ stands for convolution product, $H(s)$ is a transfer function of value,

$$H(s) = [c]\,\{s\,[I] - \{a\}\}^{-1}\,[b] + d, \tag{8}$$

function $h(t)$ is the inverse Laplace transform of $H(s)$, and I is the $n \times n$ identity matrix.

From (7) it is clear that the system, as response to a constant input u, delivers an output signal $x(t)$ which is the function $f(t)$ processed accordingly to the impulse response $h(t)$ and scaled by a factor u. Let us remember at this point that function $f(t)$ represents the externally controlled variation of the input elements of the system. Then, if we build an array of programmable input elements weighted as the values of a sampled sinusoid and we connect these input elements sequentially to the signal path as depicted in Fig. 3, equation (7) means that the output of the system will then be a filtered and scaled version of the sampled sinusoid defined by the sequentially-connected input elements.

Selecting properly the impulse response $h(t)$ and the number of programmable levels in $f(t)$, it has been proved that this strategy can be used to implement efficient and precise sinusoidal generators [2]. In particular, in [2] we shown that low-pass filter stages are very convenient for this application, given that the main harmonic component in $f(t)$ is placed in the passband, and the rest of undesired components in the rejection band of the filter. However, the linearity of the generated signal depends on the accuracy of the programmable sine-weighted input levels: in general, these weights are non-integer real numbers, but their implementation is naturally limited by the fabrication process resolution. As it will be shown in this paper, the application of harmonic cancellation techniques greatly relaxes the input step precision requirements, enabling practical feasibility of highly linear generators.

4 Practical implementation

The proposed generator with harmonic cancellation takes advantage of the previous analytical results. Thus, according to (4) a practical design should combine $2p+1$ sinusoidal signals with precise delays tuned for canceling unwanted harmonic components. This section explores a methodology for performing this combination efficiently using the proposed basic sine-wave generator.

4.1 Merging signal generation and harmonic cancellation

A direct implementation of the generator based on the conceptual block diagram in Fig. 2 is clearly not practical. The use of $2p+1$ matched generators is costly in terms of power and silicon area. Additionally, any mismatch between the generated signals would have a negative impact in the harmonic cancellation. Instead of that, we propose to perform the harmonic cancellation (3) at the input of a single basic generator by taking advantage of its programmable input levels. This way, harmonic cancellation and analog filtering of the generated signal are combined on a single block. Our design objective is then to use harmonic cancellation for attenuating low-order harmonic components, while higher order ones are attenuated by the filter itself. Let us consider harmonic cancellation and filtering separately.

Harmonic cancellation : Let us consider the sequence of discrete-time samples f_q defined by the programable input elements of the basic generator in Fig. 3,

$$f_q = \sin\left(q\frac{2\pi}{N}\right) \quad q = 0, 1, 2, ... \tag{9}$$

where N is the number of steps in one period of the step-wise sinusoid, and amplitude values have been normalized for simplicity.

Let us define f_{q+m} and f_{q-m} as shifted versions of f_q,

$$f_{q\pm m} = \sin\left((q \pm m)\frac{2\pi}{N}\right) \quad q = 0, 1, 2, ... \tag{10}$$

where m is an integer number, $1 \leq m \leq N/2$.

To enable harmonic cancellation, we propose to modify the programmable input elements in the basic generator to perform, at the generator input, the sum,

$$f_y = f_q + \sum_m [f_{q-m} + f_{q+m}] \tag{11}$$

which is analogous to (3). The set of samples f_y describes also a periodic function with N samples per period. If we assume p different m values, then each sample in f_y is the sum of $2p+1$ terms.

An interesting property is that if the ratio m/N is chosen to assure that $f_q \neq f_{q+m} \neq f_{q-m}$ for each q, then each element in sequence f_y can be generated by summing $2p+1$ different elements of the original sequence f_q. This property can be exploited for an efficient implementation of the generator: samples in f_y can then be generated using the original array of input elements by connecting $2p+1$ different input elements to the signal path simultaneously. In addition, as we are effectively reusing the same elements for defining f_q and $f_{q\pm m}$, their matching is ensured by construction.

The previous analysis shows that it is possible to include harmonic cancellation at the input array of programmable elements in our basic generator. However, in a practical implementation, the choice of parameters p, m, and N should be carefully considered.

Let us consider firstly the choice of parameter p, that is, how many signals are going to be combined in order to implement the harmonic cancellation scheme. Combining a high number of signals would allow the cancellation of different harmonic components at the same time, as it is demonstrated in [7], but this would also increase the complexity of the input stage of the generator. Given that our generator is intended for on-chip test applications, increasing the complexity –which in turn may increase the overhead– is to be avoided. Our choice in this work is the simplest structure, $p = 1$, that requires the addition of a single pair of delayed signals.

Secondly, the shift, m, has to be determined. Two main constraints have to be taken into account to comply with our design objectives: the delay should be chosen in order to cancel the most significant low-order harmonic component in f_q, and the ratio m/N should be chosen to assure that $f_q \neq f_{q+m} \neq f_{q-m}$ for each q in order to simplify the design of the array of input elements. Concerning the choice of the delay, it can be easily proved that the lowest-order, most significant harmonic component in f_q, assuming a fully-differential implementation and uniform random errors in the samples, is the third-order harmonic distortion component [2] . From (4), it is straightforward to deduce that a phase-shift of $\pm 2\pi/9$ will cancel the third harmonic distortion. Taking into account the requirement $f_q \neq f_{q+m} \neq f_{q-m}$ for each q, we can build these phase-shifts with a shift $m = \pm 2$ using step-wise sine-waves with $N = 18$ steps per period. The choice of an 18-step sine-wave is also in agreement with the design guidelines given in [2] for the basic generator: a 18-step sine-wave can be build with an array of only 4 different input elements, which leads to efficient implementations.

Filtering : After harmonic cancellation, higher order harmonic components will be attenuated by the generator itself according to equation (7). Then, regarding the system transfer function $H(s)$, we need to match its shape to the frequency of interest in the application. In this sense, a low-pass shape is clearly the most convenient whenever the main harmonic of f_y is in the passband and any unwanted spectral components are in the rejection band.

A benefit of the harmonic cancellation technique is that the lowest-order significant harmonic can be cancelled, so the requirements on the transfer function in terms of attenuation can be relaxed, and hence low-order filters can be used without penalizing the linearity of the output.

4.2 Estimation of performance limits

This section explores, by means of numerical simulations, the performance figures that can be obtained by the proposed sinusoidal signal generator, and the design trade-offs affecting these figures. Thus, from our previous analysis it should be clear that the main performance limitations of the proposed approach are given by the realization of precise step levels for f_q, the selected linear system $H(s)$, and the effectiveness of the proposed harmonic cancellation strategy.

Other limiting factors, such as the non-linearity or the noise characteristics of the selected linear system are related to each particular implementation, and not to the proposed generation strategy itself. These contributions can be added *a posteriori* over our behavioral simulation results, once that a specific implementation for the linear system has been set. For this reason, these contributions related to a particular implementation will not be considered in this section.

The performance of the proposed generation strategy has been analyzed in terms of THD. Our analysis considers an 18-step sine-wave for sequence f_q with random errors in the values of its steps. In a particular implementation, these errors will emerge from mismatches between devices, process variations, etc. Concerning the system transfer function, $H(s)$, our analysis considers a fully-differential low-pass second-order filtering section with a relatively low value of the quality factor, $Q = 5$. The main tone in f_q has been made coincident to the corner frequency of the filter, so higher order harmonics will lay in the rejection band.

Regarding the harmonic cancellation scheme, we are going to explore all possible pairs of integer delays, $\pm m$, for our 18-step sine-wave f_q, i. e. from $m = 0$, which means no harmonic cancellation applied, to $m = \pm 9$. According to equation (4), this means that after combining $f_q + f_{q-m} + f_{q+m}$, the magnitude of each harmonic component A_k in the original 18-step sine-wave f_q is going to be scaled by a factor $\|1 + 2\cos(k\frac{2\pi m}{18})\|$, where k is the index of each harmonic component and m is the integer shift applied to the delayed sequences $f_{q\pm m}$. Table 1 lists the values of these scale factors for each value of k and m.

Taking into account that the generated signal will be filtered by a second-order low-pass filter, it is advantageous to concentrate the effects of the harmonic cancellation in the lowest order harmonic components. Thus, from Table 1 the case $m = \pm 2$ seems to be the most appropriate since the third harmonic is canceled, the fifth is attenuated, and although the seventh and ninth components are amplified, they will be attenuated by the low-pass filtering. For $m = \pm 4$ or $m = \pm 8$, the third harmonic is also canceled but the fifth is amplified. In addition, the power of the fundamental tone is also reduced with respect to the $m = \pm 2$ case.

Table 1 Scaling factors for each harmonic component A_k as a function of the integer delay m

delay m	A_1	A_3	A_5	A_7	A_9
1	2.9	2	0.6	0.5	1
2	2.5	0	0.8	1.3	3
3	2	1	2	2	1
4	1.3	0	2.5	0.8	3
5	0.6	2	0.5	2.9	1
6	0	3	0	0	3
7	0.5	2	2.9	0.6	1
8	0.9	0	1.3	2.5	3
9/0	1	1	1	1	1

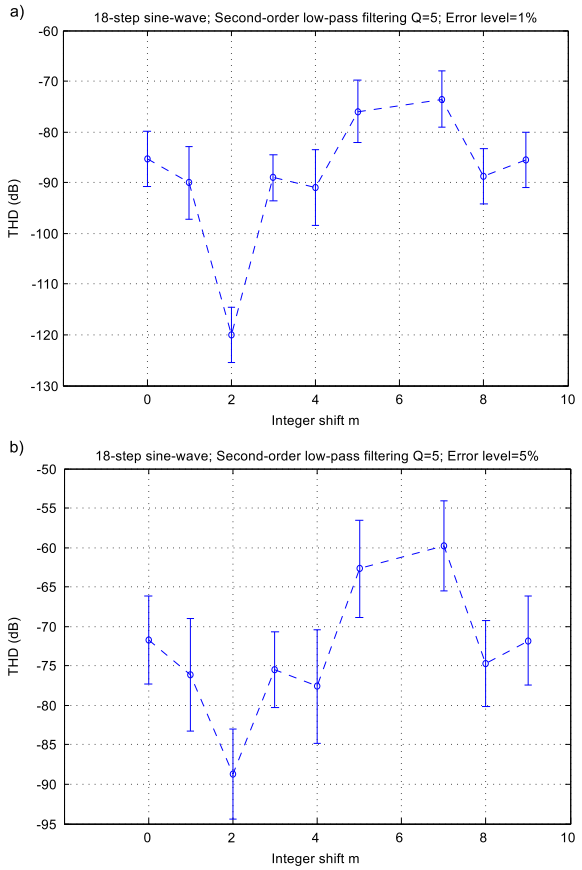

Fig. 4 THD of the generated sinusoid as a function of the integer shift m for a) 1% maximum error level, and b) 5% maximum error level

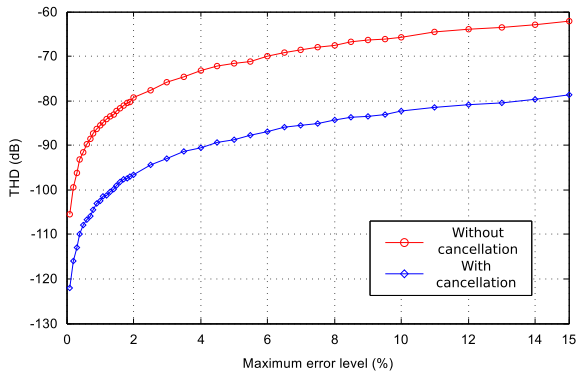

Fig. 5 THD of the generated sinusoid vs. error level in the input elements, with and without harmonic cancellation

In order to verify our assumptions we performed a set of statistical numerical simulations using maximum errors of 1% and 5% in the levels of the step-wise sine-wave f_q. Figure 4 shows the obtained average performance in terms of THD, after 1000 runs of the experiment, as a function of the integer delay, m, employed for the harmonic cancellation. Error bars show the obtained $\pm 1\sigma$ variation interval for each point.

As it was expected, best performance is obtained for integer shift $m = \pm 2$, which corresponds to a delay of $\pm 2\pi/9$ and the cancellation of the third harmonic component. Very low THD figures can be obtained even with a 5% error level.

In order to make a comparison to the performance of the basic generator without harmonic cancellation, Fig. 5 shows the obtained average performance in terms of THD as a function of the error in the step levels for both the basic generator and the generator with harmonic cancellation. Results were obtained again by numerical statistical simulation. A total of 1000 instances of the generator were created to compute each data point. In both cases, the base sequence f_q was set to a 18-step sine-wave, and a second-order low-pass filter with $Q = 5$ was employed. A delay of $m = \pm 2$ was used in the harmonic cancellation case. THD figures are greatly improved due to the application of the harmonic cancellation technique. As it can be seen in Fig. 5, THD is boosted around 16dB.

From a designer point of view, Fig. 5 shows how the accuracy requirements of the step levels can be greatly relaxed due to the application of harmonic cancellation. Thus, for example, a target THD of -90dB would require an accuracy of 0.5% for the generator without cancellation, while with the addition of harmonic cancellation, an accuracy of 4.5% is enough to get the same performance.

The dispersion on the THD value is relatively high, with a standard deviation in the order of 5dB. However

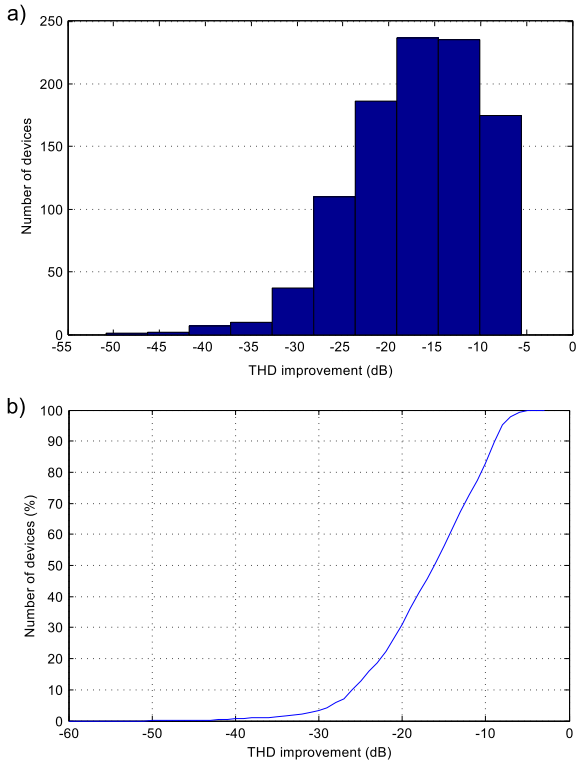

Fig. 6 Statistics of THD improvement: a) Histogram of the THD improvement; b) corresponding Cumulative Density Function

some care must be taken to properly interpret this datum. Indeed, it is logical to suppose that the THD of the generators with and without cancellation are highly correlated. To get more insight into this issue, Fig. 6 shows the histogram and the associated Cumulative Density Function (CDF) of the THD improvement obtained by harmonic cancellation for the 1000 generators simulated at the 1% error level. We first observe the distribution is not Gaussian. This could be expected since the THD is expressed in decibels. In a worst case scenario, the minimum improvement observed for these 1000 trials is 6dB, while the CDF plot shows that the median value is around 16dB. The best observed improvement can be as high as 50dB at the tail of the CDF. Similar simulations have been carried out for different error levels with no significant differences.

Obtained results suggest that the application of the harmonic cancelation technique not only improves the linearity of the original generator, but it also reduces the impact of random errors in the input elements. This is an advantage compared to previously presented generators using harmonic cancelation such as [6, 7, 18]. These previous works are based on matching different stages for the generation of time-delayed signals, so any mismatch between the stages has a negative impact on the harmonic cancellation. In our proposed generator

Table 2 Normalized capacitor values

C_A	C_B	C_C	C_D	C_F	C_I
5.15	14.26	1	2.89	1.02	1

the three time-delayed signals used for harmonic cancellation are built simultaneously from the same elements, reducing this way the influence of mismatch.

5 Design

In order to show the feasibility of the proposed generation technique, we have designed a demonstrator in a standard 180nm CMOS technology. Figure 7 shows the system level block diagram of the generator. The design has been derived from a Fleischer-Laker biquad [8] in a fully-differential low-pass configuration. This discrete-time system operates with two non-overlapping clock phases ϕ_1 and ϕ_2. Table 2 lists the normalized capacitor values of the filter core, which correspond to a peak gain of 0 dB, a pole quality factor $Q = 5$, and a corner frequency placed at one-eighteenth of the clock frequency. The proposed design has been optimized for minimizing capacitance spread and the unit capacitor value is 103fF.

The only modification with respect to the original filter is that the input capacitor has been replaced by a switching scheme controlled by signal ϕ_{in} and a programmable capacitor that is composed by an array of four capacitors C_{Ii} weighted as,

$$C_{Ii} = C_I \sin\left(i\frac{2\pi}{18}\right) \quad i = 1, 2, 3, 4. \tag{12}$$

The realization of irrational sinusoidal weights in (12) was a cumbersome point in the design of the basic generator [2] (without harmonic cancellation) because a high accuracy was required in the definition of these sinusoidal steps. One of the advantages of the introduction of the harmonic cancellation technique is that the new generator has a high tolerance to errors in the step levels, as it can be deduced from Figures 4 and 5. Hence, for the design of this prototype each of the sinusoidal weights has been approximated to a close –and easier to integrate– rational value.

The input programmable array is controlled by signals c_i, $i = 1, ..., 4$ and ϕ_{in} as depicted in Fig. 7 and excited by a DC signal u. Under these operating conditions, the input array feeds to the core of the filter the sum of three 18-step sinusoids, with phases 0, $+2\pi/9$, and $-2\pi/9$, enabling signal generation and harmonic cancellation in a single block.

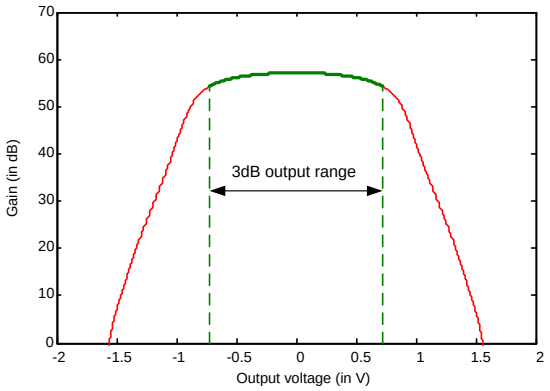

Fig. 8 Amplifier gain versus output voltage

Table 3 Amplifier characteristics

Parameter	Value
Gain	57 dB
Gain Bandwidth product	192 MHz
Phase margin	82^o
Slew-rate	132 V/μs
Output range (-3 dB)	1.4 V_{pp}

Given that, by construction, the peak frequency of the filter core is one-eighteenth of the clock frequency, the output signal frequency and the peak frequency are coincident by design. In this way, non-desired high-order harmonics are pushed to the rejection band of the filter. Also, in this arrangement, the frequency of the generated signal can be easily programmed to accommodate the output stimulus to a particular application by scaling the clock frequency. The amplitude of the generated stimulus, on the other hand, can be also programmed by scaling the reference input voltage u.

The amplifiers have been designed using a one-stage folded-cascode fully-differential architecture. This kind of structure offers a good trade-off between gain, bandwidth, and design complexity, while its main drawback is a limited output swing due to the cascode elements. The main characteristics of the designed amplifier can be found in Table 3. The output range is computed for a 3dB loss with respect to the maximum gain as depicted in Fig. 8.

The phase generator is based on a classical NAND feedback loop with a chain of inverters. This circuit has been designed to guarantee non-overlapped clock phases ϕ_1 and ϕ_2 under worst-case process variations. Other effects, such as alterations in the duty cycle or jitter noise, play a less important role in the performance of the proposed switched-capacitor implementation, provided always that signals are correctly settled.

Concerning the switches, typical CMOS switches have been adopted and they have been sized for mini-

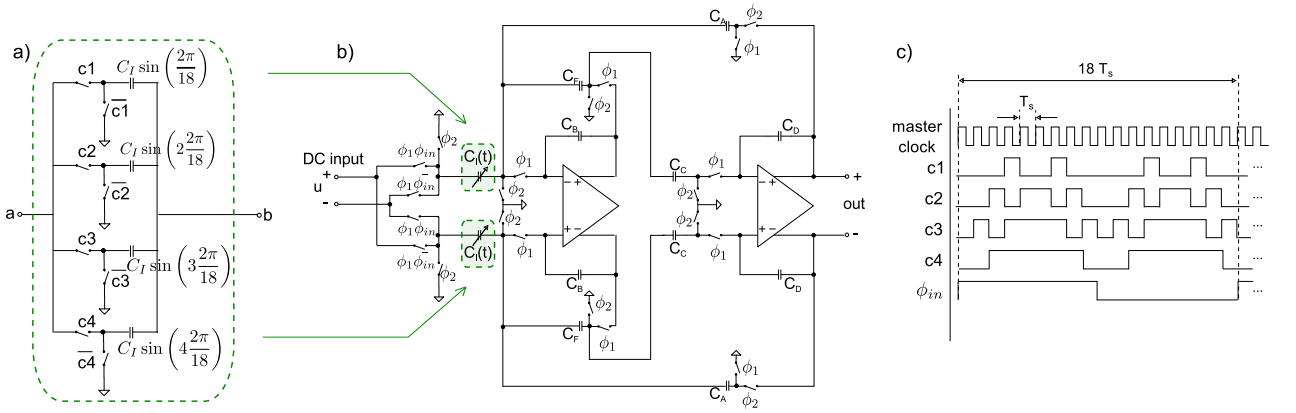

Fig. 7 a) Programmable input capacitor; b) SC implementation of the proposed generator technique; c) Master clock and control signals for three phase-shifted sinusoids of phases 0, $+2\pi/9$, and $-2\pi/9$

Fig. 9 Layout view of the sinusoidal generator with harmonic cancellation

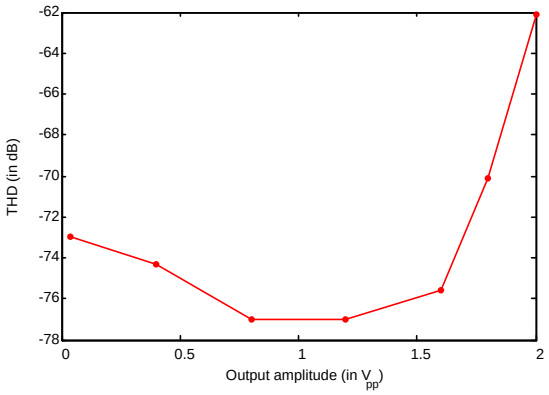

Fig. 10 Total Harmonic Distortion versus sine amplitude

mizing clock feedthrough. Fig. 9 shows the layout view of the complete generator in the selected 180nm CMOS technology. It occupies an area of $160\mu m \times 260\mu m$, and it drains a power of 3.24mW operating at 20MHz clock frequency. These figures include also an integrated phase generator, that occupies $50\mu m \times 20\mu m$ and drains $48\mu W$

6 Simulation results

In this section we present simulation results obtained including all the parasitics extracted from the layout.

Let us first check the performance limits of the prototype. In order to check the maximum amplitude of the generator, we set the clock frequency at 20MHz, which leads to a sine wave at approximately 1.11MHz, an varied the reference voltage (quoted u in Fig. 7) sampled by the input capacitor array in order to change the amplitude of the generated sine-wave. The Total Harmonic Distortion (THD) was computed from the Fourier Transform of the output signal. Figure 10 displays the obtained results. A degradation is observed beyond $1.2V_{pp}$, which is obviously due to the limited output range of the amplifiers. This result is coherent with the 3dB output range of the amplifier in Table 3.

For the dynamic behavior of the circuit, we fixed the output amplitude to approximately $800mV_{pp}$, which is close to the THD minimum value obtained in Fig. 10, and varied the master clock frequency. This automatically varies the fundamental frequency since the frequency ratio is fixed to 1/18 by design.

Figure 11 shows the obtained THD versus frequency. We observe a degradation beyond 10MHz and a peak THD value slightly below -80dB. This confirms that our amplitude simulation at 20MHz was only marginally affected by dynamic errors. Once again, this result is coherent with the gain-bandwidth product of the amplifier in Table 3. The amplifier settling time constant is 9.6 times smaller than half a clock period at 10MHz but only 4.8 times at 20MHz.

The performance in the process corner is summarized in Table 4. It can be seen that the performance for a clock frequency at 20MHz and an amplitude of $800mV_{pp}$ is limited in the slow NMOS slow PMOS cor-

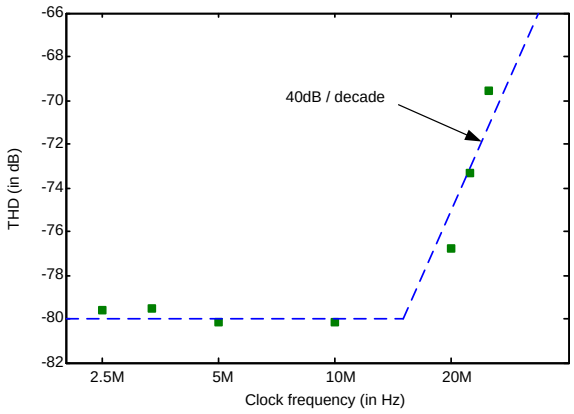

Fig. 11 Total Harmonic Distortion versus clock frequency

Table 4 Process corner

Corner type	Typ	$f_N f_P$	$f_N s_P$	$s_N f_P$	$s_N s_P$
THD @20MHz	76dB	76dB	74dB	77dB	65dB
THD @10MHz	80dB	77dB	79dB	80dB	77dB

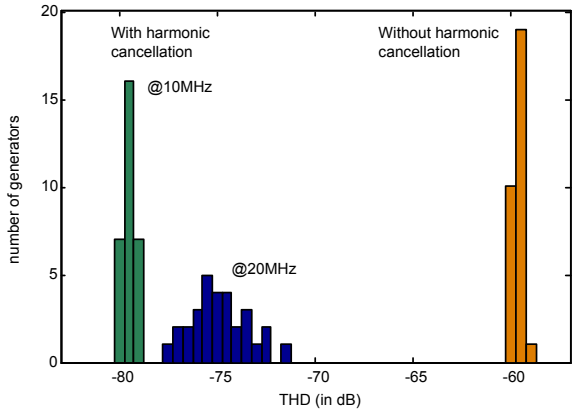

Fig. 12 THD histograms of MonteCarlo process simulation with and without harmonic cancellation

ner. The results seen in Figure 11 suggest that this is a dynamic limitation. This is confirmed by a second corner simulation run at 10MHz.

To further quantify these trends, we performed a 30 MonteCarlo process simulations, both at 10MHhz and 20MHz. The results are almost identical for the generator without cancellation because the performance-limiting factor is not the filter distortion but the capacitor inaccuracies, so we only represent one of the two histograms. On the other hand, the generator with cancellation exhibits a mean THD of -79.5dB, with a standard deviation of 0.33 dB at 10MHz and 75 dB with a standard deviation of 1.4dB at 20MHz.

Figure 13 shows the evolution of THD with temperature for an amplitude of $800mV_{pp}$ and for clock frequencies of 10MHz and 20MHz. A performance degradation is observed at high temperatures for the clock

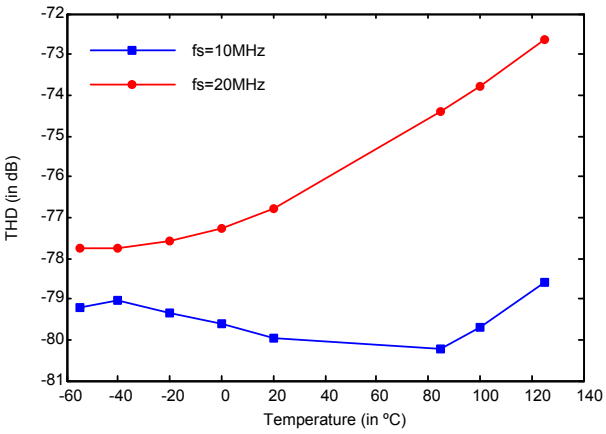

Fig. 13 Total Harmonic Distortion versus Temperature

set at 20MHz which is coherent with the slow corner degradation.

In order to validate the benefits of the harmonic cancellation scheme, we performed several Monte Carlo mismatch simulations using the mismatch models provided in the Process Design Kit. The amplitude is set to $400mV_{pp}$ and the clock frequency to 10MHz. This design point is deliberately more conservative than the maximum performance point because we want to concentrate on effects of capacitor inaccuracy.

The first simulation was performed with the harmonic cancellation enabled and the second one with the harmonic cancellation disabled. The prototype has been designed with roughly approximated capacitor ratios. Actually, the standard deviation of the errors in the capacitors of the input bank is equivalent to a maximum error level of approximately 14% in Fig. 5. This equivalence is only an approximation, since the capacitors values in the experiment of Fig. 5 were drawn from a uniform random distribution while here we have a single particular case. To complete the validation and be as fair as possible, that is to say to compare the prototype to the best possible matched design, we adjusted the input capacitor values to the limit of the layout grid and performed a third Monte Carlo run. Take into account that this simulation of the schematic does not include any possible edge effects that would appear in a real fabrication process.

Figure 14 shows the results of three Monte Carlo mismatch simulations. It can be seen that the circuit with the proposed harmonic cancellation consistently achieves a THD that is 16dB lower than without the proposed scheme, in perfect agreement with the theoretical results of Fig. 5. Compared to the generator with the capacitors somewhat ideally matched to the limit of the grid accuracy, the proposed technique still achieves a significant 10dB improvement. The dispersion of the

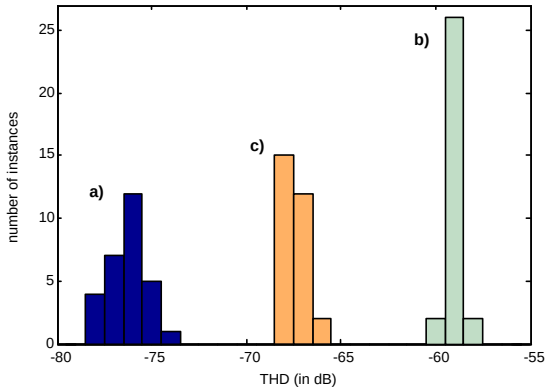

Fig. 14 Monte Carlo simulation of mismatch effects on THD, a) with harmonic cancellation and 14% capacitor errors, b) without harmonic cancellation and 14% capacitor errors, c) without harmonic cancellation and residual layout grid errors.

THD can be explained in part by the mismatch variations of the capacitors but also by second order effects that gain relevance at lower THD levels. Anyhow, it appears that systematic inaccuracies clearly dominate the degradation here, even for the best-matched case.

We can thus affirm that proposed harmonic cancellation scheme is much less sensitive to the mismatch of the input capacitors and allows to push the linearity beyond the technological limits of generators without harmonic cancellation.

Finally, Table 5 shows a comparison to some recently proposed solutions for analog sinusoidal signal generation. The selected signal generators are compared in terms of area, linearity, power consumption, and output swing. Rather than a direct comparison, Table 5 is aimed to put the obtained results into perspective. Indeed, it is not possible to establish which approach is the best without taking into account at the same time a particular application scenario. Keeping that in mind, the best performance in terms of linearity is achieved by the phase-shift oscillator with harmonic cancellation in [7]. However, this generator employs extensive analog hardware resources, so its application is intended for an on-board implementation rather than for integration into a BIST strategy. Also, the operation of the presented prototype is limited to low-frequency and high supply voltage operation. The time-mode oscillator with harmonic cancellation in [6] has the highest operation frequency among the considered solutions, but its output swing is limited, and the required area of the proposed implementation, that includes a multiple-input passive network for harmonic cancellation and filtering, is comparatively high. The work presented in this paper is a clear improvement with respect to our previous one in [2] in all aspects, and compared to the works in [6, 7] it offers the widest output swing and smallest area, while linearity figures are comparable.

In terms of hardware resources, our proposed implementation is also comparatively advantageous. It only requires a second-order linear stage that can be efficiently implemented with two integrators. The approach in [7] employes a chain of integrators (three or five, depending on the implementation) followed by an active analog adder and a complete output filter. The proposal in [6], on the other hand, proposes an efficient all-digital implementation of the individual signal phases, but the passive network used for adding and filtering these signal phases for harmonic cancellation penalizes the overall area.

7 Conclusions

This work presented a novel technique for the generation of highly linear analog sinusoidal signals using a harmonic cancellation technique. The proposed generator is based on a modified low-order analog filter with a DC input and programmable input elements, in such a way that the filter performs signal generation, harmonic cancellation and filtering of the unwanted components. The harmonic cancellation technique not only improves the linearity of the output signal, but it relaxes the design of the filter and the required accuracy of the programmable input elements.

An integrated prototype has been developed in a 180nm CMOS technology to show the feasibility of the technique. Post-layout electrical simulation results show a significant improvement in the linearity of the generated signal with respect to the generator without harmonic cancellation. Compared to other reported generators based on the harmonic cancellation principle, our approach is, by construction, less sensitive to mismatch and requires less hardware resources, while it achieves comparable linearity figures, making the presented generator very suitable for built-in test applications.

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Table 5 Comparison to state-of-the-art

	Time-mode oscillator [6]	Phase-shift oscillator [7]	Discrete-level generator [2]	This work
Technology	130nm	Discrete components	0.35μm	180nm
Area	$0.186mm^2$	–	$0.15mm^2$	$0.04mm^2$
THD	-72dB	-82dB	-67dB	-77dB
Frequency	10MHz	29kHz	62.5kHz	1.11MHz
Output swing	228mVpp (19% of V_{DD})	7Vpp (23% of V_{DD})	1Vpp (30% of V_{DD})	1Vpp (56% of V_{DD})
Supply voltage	1.2V	30V	3.3V	1.8V
Power	4.04mW	–	5.8mW	3.24mW

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