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Design of Low Power 2-D Dct Architecture Using Reconfigurable Architecture

[1]Venkata pavan kumar .B, [2]Ch.Venkateswarlu
[1] M.Tech student, [2]Assistant professor, Pragati Engineering College,Surampalem.

***Abstract**: This Research paper includes designing a area efficient and low error Discrete Cosine Transform. This area efficient and low error DCT is obtained by using shifters and adders in place of multipliers. The main technique used here is CSD(Canonical Sign Digit) technique.CSD technique efficiently reduces redundant bits. Pipelining technique is also introduced here which reduces the processing time.*

I. Introduction

Multimedia data processing, which encompasses almost every aspects of our daily life such as communication broad casting, data search, advertisement, video games, etc has become an integral part of our life style. The most significant part of multimedia systems is application involving image or video, which require computationally intensive data processing. Moreover, as the use of mobile device increases exponentially, there is a growing demand for multimedia application to run on these portable devices. A typical image/video transmission system is shown in the Figure 1.

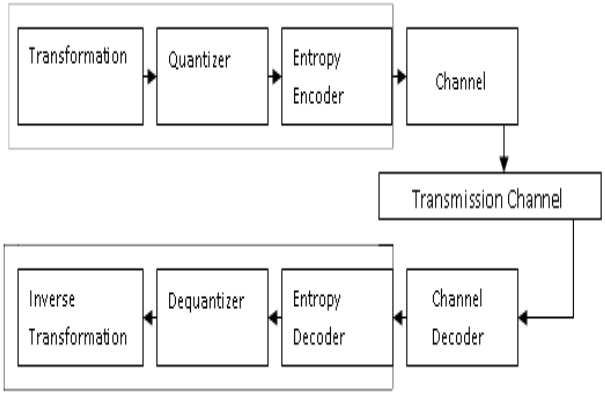


Figure1. Image/Video Transmission System

In order to reduce the volume of multimedia data over wireless channel compression techniques are widely used. Efficiency of a transformation scheme can be directly gauged by its ability to pack input data into as few coefficients as possible. This allows the quantizer to discard coefficients with relatively small amplitudes without introducing visual distortion in the reconstructed image.

In image compression, the image data is divided up into 8x8 blocks of pixels. (From this point on, each color component is processed independently, so a "pixel" means a single value, even in a color image.) A DCT is applied to each 8x8 block. DCT converts the spatial image representation into a frequency map: the low-order or "DC" term represents the average value in the block, while successive higher-order ("AC") terms represent the strength of more and more rapid changes across the width or height of the block. The highest AC term represents the strength of a cosine wave alternating from maximum to minimum at adjacent pixels.

II. JPEG Encoder

The JPEG encoder is a major component in JPEG standard which is used in image compression. It involves a complex sub-block Discrete Cosine Transform (DCT), along with other quantization, zigzag and Entropy coding blocks. In this architecture, 2-D DCT is computed by combining two 1-D DCT that connected by a transpose buffer. The architecture uses 4059 slices, 6885 LUT, 58 I/Os of Xilinx Spartan-3 XC3S1500 FPGA and works at an operating frequency of 65.55 MHz.

Vector processing using parallel multipliers is a method used for implementation of DCT. The advantages in the vector processing method are regular structure, simple control and interconnect, and good balance between performance and complexity of implementation. For the case of 8 x 8 block region, a one-

dimensional 8- point DCT followed by an internal transpose memory, followed by another one dimensional 8-point DCT provides the 2D DCT architecture. Here the real time DCT coefficients are used for matrix multiplication. Using vector processing, the output Y of an 8 x 8 DCT for input X is given by $Y = C*X* C^T$, where C is the cosine coefficients and C^T are the transpose coefficients. This equation can also be written as $Y=C * Z$, where $Z = X*C^T$.

The calculation is implemented by using eight multipliers and storing the co-efficients in ROMs. At the first clock, the eight inputs xOO to x07 are multiplied by the eight values in column one, resulting in eight products (POO _0 to POO 7). At the eighth clock, the eight inputs are multiplied by the eight values in column eight resulting in eight 586 products (P07 0 to P07 7). From the equations for Z, the intermediate values for the first row of Z are computed. The values for ZO (0 -7) can be calculated in eight clock cycles. All 64 values of Z are calculated in 64 clock cycles and then the process is repeated. The values of Z correspond to the 1-DDCT of the input X. Once the Z values are calculated, the 2D-DCT function Y can be calculated from Y = C*Z.

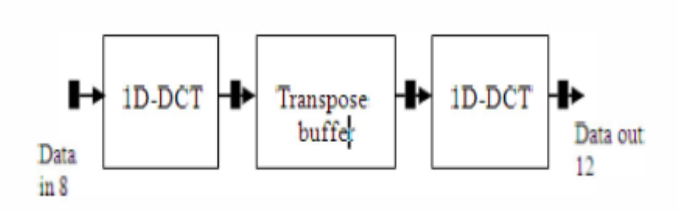


Figure 2. 2-D DCT Architecture

The maximum clock frequency is 65. 55 MHz when implemented with a Spartan FPGA XCS1500 device.

III. Multiplier-less 2-D DCT/IDCT Architecture For JPEG

The Discrete Cosine transform is widely used as the core of digital image compression. Discrete Cosine Transform attempts to de-correlate the image data. After de-correlation, each transform co-efficient can be encoded independently without losing compression efficiency. In this paper we present VLSI Implementation of fully pipelined multiplier less architecture of 8x8 2D DCT/IDCT. This architecture is used as the core of JPEG compression hardware. The 2-D DCT calculation is made using the 2-D DCT separability property, such that the whole architecture is divided into two 1-D DCT calculations by using a transpose buffer. The architecture described to implement 1-D DCT is based on Binary-Lifted DCT. The 2-D DCT architecture achieves an operating frequency of 166 MHz. One input block of 8x8 samples each of 8 bits each is processed in 0.198µs. The pipeline latency of proposed architecture is 45 Clock cycles

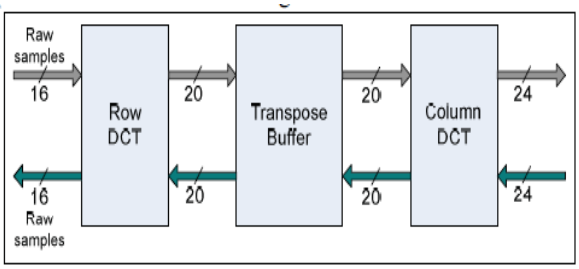


Figure 3 Architecture of 2-D DCT

Figure 2. shows the architecture of 2-D DCT. 2D-DCT/IDCT design is divided into three major blocks namely Row-DCT, Transpose Buffer, and Column-DCT. Row-DCT and Column-DCT contains both 1DDCT (Figure 4) by Row . Access of Transpose buffer DCT and Column DCT is efficiently managed to achieve the performance and minimal usage of resources in terms of area.

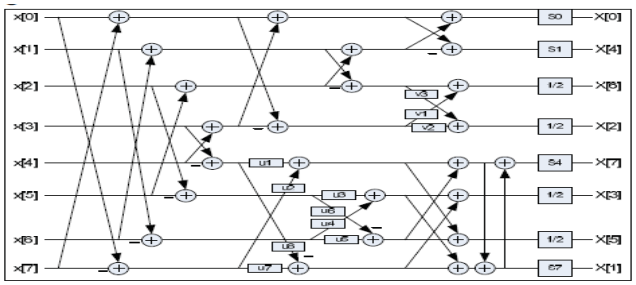


Figure 4. Architecture of 1-D DCT

During Forward transform, 1D-DCT structure (Figure 4) is functionally active. Row-DCT block receives two 8-bit samples as an input in every cycle. Each sample is a signed 8- bit value and hence its value ranges from -128 to 127. The bit width of the transformed sample is maintained as 10-bit to accommodate 2-bit increment.

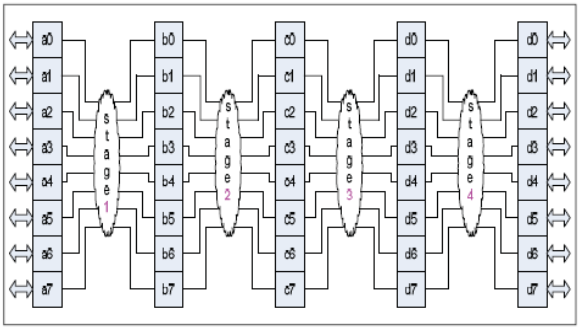


Figure 5. Four stage pipeline 1D-DCT.

1D-DCT computation architecture (Figure 4) has a four stage internal pipeline shown in Figure 5.Transpose Buffer receives two 10-bit samples as an input every cycle. Each sample is a signed 10-bit value and hence its value ranges from -512 to 511. Since there is no data Manipulation in the module the output sample width remains as input sample width i.e. 10-bit. Transpose buffer has sixty-four 10-bit registers to store one 8X8 block 1D-DCT samples. Transpose operation on 8X8 block data is performed by writing the transformed samples in row-wise and reading them in column-wise and vice versa. Transpose Buffer block guarantees that the nth 8X8 block data will be written into the registers after (n-1) th 8X8 block data has been completely read out for further processing. The latency of the block is 31 cycles since the data can be read only after full 8X8 block is written in the registers. Column DCT block receives two 10-bit samples as an input in every cycle. Input samples are internally buffered.

The 2D-DCT/IDCT architecture efficiently operates up to 166MHz. Pipeline latency for the initial 8x8 block with each element of 8 bits is 45 clock cycles which is due to 7 cycles at Row-DCT, 31 cycles for Row-DCT operation to complete, 7 cycles at Column-DCT. Effectively to perform complete 2D DCT on one 8x8 will take 33 Clock cycles on availability of continuous input data to process. For operating frequency of 166 MHz, the processing time of 8x8 blocks is 0.198µs.

IV. Quantization Architecture

Two dimensional DCT takes important role in JPEG image compression. Architecture and VHDL design of 2-D DCT, combined with quantization and zig-zag arrangement, is described. The architecture is used in JPEG image compression. The output of DCT module needs to be multiplied with post-scaler value to get the real DCT coefficients. Post-scaling process is done together with quantization process. 2-D DCT is computed by combining two 1-D DCT that connected by a transpose buffer. This design aimed to be implemented in cheap Spartan 3E XC3S500 FPGA. The 2-D DCT architecture uses 3174 gates, 1145 Slices and 11 multipliers of one Xilinx Spartan-3E XC3S500E FPGA and reaches an operating frequency of 84.81 MHz. One input block with 8 x 8 elements of 8 bits each is processed in 2470 ns and pipeline latency is 123 clock cycles.

This architecture adopts the scaled 1-D DCT algorithm. It means the DCT coefficients produced by the algorithm are not the real coefficients. To get the real coefficients, the scaled ones must be multiplied with post-scaler value. Equation (1) is showing scaled 1-D DCT process.

$$\mathbf{y' = C\,x} \qquad (1)$$

Variable **x** is 8 point vector. **C** is Arai's DCT matrix and **y'** is vector of scaled DCT coefficients. To get the real DCT coefficients, y' must be element by element multiplicated with post-scaling factor. It is shown in (2).

$$\mathbf{y = s\,.*\,y'} \qquad (2)$$

Constant **s** is vector of post-scaling factor. Figure 6 shows the block diagram representation of the entire system.

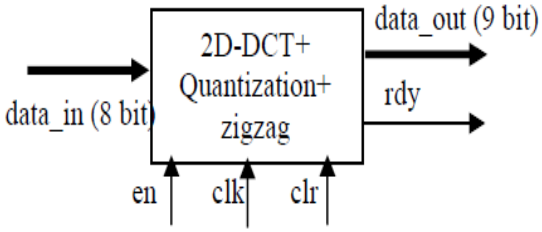


Figure 6. Block Diagram of entire system

The DCT input/output has 8 points and data has to be entered and released in sequential manner, it takes 8 clock cycles for each input and output process. Totally, 8 points 1D-DCT computation needs 22 clock cycles. 1D-DCT computation is done in pipeline process. Figure 7 shows 1-D DCT architecture with pipelining.

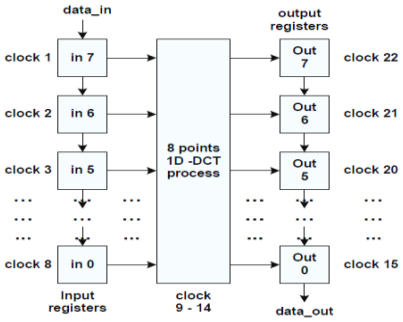


Figure 7. 1-D DCT with pipelining

The 2-D DCT architecture was described in VHDL. This VHDL was synthesized into an Xilinx Spartan 3E family FPGA. According to synthesis result, maximum time delay produced is 5.895 ns. That constraint yields minimum clock period 11.790 ns. Maximum clock frequency can be used is 84.818 MHz. The 2-D DCT architecture uses 3174 gates, 1145 Slices and 11 multipliers.

The stronger operator, multiplication is transformed to simple shift and adds operations by applying Horner's rule. This reduces the power consumption. For example, consider the cosine coefficients c and g, **c *X** = $2^5 + 2^4 + 2^2 + 1$ (X) = $(2^4$ (**3**) + **5**) (X) and **g*X** = $2^3 + 2^2$ (X)= 2^2(**3**) (X) and the common terms they share is 3X. The common terms among the cosine basis are the partial outputs. These blocks are termed as *precomputing* units and an unit is shown in the Figure 3. The intermediate results from the precomputing blocks are added in the final stage yielding the DCT coefficients. The 3A is constructed by expressing it as 3A = 1A+2A = {1A + (1A<<1)}. Similarly the 5A can be expressed as {1A + (1A<<2)}.

A. Low Power Odd And Even Architecture

The stages involved in the determination of 1-D DCT coefficients are precomputing, odd DCT and even DCT. The proposed architecture is a multiplier less architecture. The representation of cosine basis in CSD format reduces power consumption as it has less number of ones. Each multiplication of the cosine coefficients with the sequence are expressed using Horner's rule [6].

The sub structure sharing is carefully done so that it contains the actual sequence i.e. 1A prevalently. This keeps the result of the shift and adds nearly matching the direct multiplication of the cosine basis with the sequence. The Odd DCT precomputing units have 1A, -1A, 3A, and 5A structures to be shared. 3A can be expressed as $(1A+2^1A)$ and 2^1A is obtained by left shifting A by 1 place to the left. Similarly 5A=1A+(A<<2).
The even DCT contains the DC part of the transformed image i.e. in frequency domain. Hence care should be taken in calculating the Z0 value. The corresponding cosine basis is d and is represented as $d = 2^5 + 2^3 + 2^2 + 1$. The precomputing unit of the even DCT consists of 1A, -1A and 3A only.
The odd and even modules use four precomputing instances each. The outputs from the precomputing units are fed to the final adder stage. The final adder outputs are the desired DCT coefficients. The image pixel value is represented in 8-bits and hence the output of the adder and subtractor has 9-bits.The input to the row DCT has 9-bits and its output is chosen to have 12 bits. Thus the column DCT is fed by 12-bit inputs. The DCT coefficients are quantized to have 12-bits.

B. Synthesis Results

The 2-D DCT architecture is implemented with Verilog HDL and simulated using MODELSIM for functional verification. Finally it is synthesized using QUARTUS II tool and mapped on to a Cyclone III device (65 nm). The simulated results are shown below. The DCT coefficients obtained through this architecture is verified against MATLAB results.

Device Utilization Summary

Flow Status	Successful - Tue Jun 19 12:56:31 2012
Quartus II Version	9.0 Build 132 02/25/2009 SJ Web Edition
Revision Name	twodf
Top-level Entity Name	dct2d
Family	Cyclone III
Device	EP3C5F256C7
Timing Models	Final
Met timing requirements	N/A
Total logic elements	4,758 / 5,136 (93 %)
Total combinational functions	4,605 / 5,136 (90 %)
Dedicated logic registers	2,106 / 5,136 (41 %)
Total registers	2106
Total pins	172 / 183 (94 %)
Total virtual pins	0
Total memory bits	0 / 423,936 (0 %)
Embedded Multiplier 9-bit elements	0 / 46 (0 %)
Total PLLs	0 / 2 (0 %)

Power Analysis Report

PowerPlay Power Analyzer Summary	
PowerPlay Power Analyzer Status	Successful - Thu Aug 23 11:48:37 2012
Quartus II Version	11.0 Build 208 07/03/2011 SP 1 SJ Web Edition
Revision Name	qa
Top-level Entity Name	dct_algorithm
Family	Cyclone III
Device	EP3C16F484C6
Power Models	Final
Total Thermal Power Dissipation	80.09 mW
Core Dynamic Thermal Power Dissipation	0.00 mW
Core Static Thermal Power Dissipation	51.82 mW
I/O Thermal Power Dissipation	28.26 mW
Power Estimation Confidence	Low: user provided insufficient toggle rate data

A low complexity 2-D DCT architecture has been designed. The sub structure sharing removes the redundancy in the DCT calculation. The architecture can be pipelined to meet high performance needs such as applications in HD televisions, satellite imaging systems.

VI. Implementation of the proposed approach

Raw image data used in applications such as high definition television, video conferencing, computer communication, etc. require large storage and high speed channels for handling huge volumes of image data. In order to reduce the storage and communication channel bandwidth requirements to manageable levels, data compression techniques are inevitable. To meet the timing requirements for high speed applications the compression has to be achieved at high speeds.

A. Pipelining

The speed of the system depends on the time taken by the longest data path which is known as the critical path. To increase the speed of the architecture, pipelining technique can be used. Pipelining is the technique of introducing latches along the data path so as to reduce the critical path. Reduction in the critical path increases the speed of operation. Pipelining latches can only be placed across any feed-forward cutest of the architecture graph. The clock period is then limited and the critical path may be between i.An input and a latch, ii.A latch and an output, iii. Two Latches an input and an output.

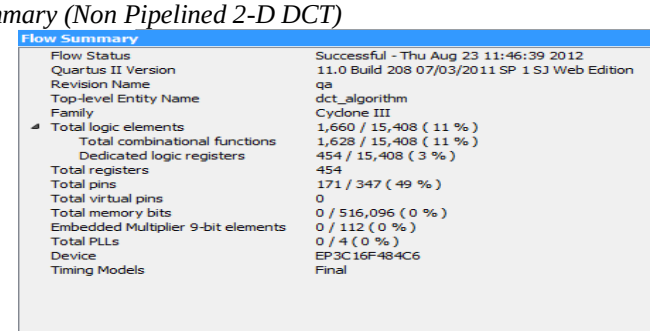
In this architecture, the pipelining is of fine grain type as the pipeline latches are introduced inside the 1-D module. The critical path of the 1-D module is from the input to the output. This includes the computational time of precomputing modules and the final adders as well. The critical path time is from the onset of the input xi$\pm$xj and the arrival of zk (i=0,1,,2,3;j=4,5,,6,7 and k=0 to 7). The speed can be improved if latches are introduced between the shifter and adder module of precomputing modules. After pipelining the critical path is from the input(X) to 3X generator.

The architecture is synthesized into Stratix family EP1S10 device (for high performance needs). The results are shown in the Table1

Design Unit	FMAX Summary
2-D DCT Without Pipelining	126.25MHz
2-D DCT With Pipelining	295.95MHz

Table 1. Frequency summary

B.Device Utilization Summary (Non Pipelined 2-D DCT)



Flow Summary	
Flow Status	Successful - Thu Aug 23 11:46:39 2012
Quartus II Version	11.0 Build 208 07/03/2011 SP 1 SJ Web Edition
Revision Name	qa
Top-level Entity Name	dct_algorithm
Family	Cyclone III
Total logic elements	1,660 / 15,408 (11 %)
Total combinational functions	1,628 / 15,408 (11 %)
Dedicated logic registers	454 / 15,408 (3 %)
Total registers	454
Total pins	171 / 347 (49 %)
Total virtual pins	0
Total memory bits	0 / 516,096 (0 %)
Embedded Multiplier 9-bit elements	0 / 112 (0 %)
Total PLLs	0 / 4 (0 %)
Device	EP3C16F484C6
Timing Models	Final

Design Unit	**Frequency Report**
2-D IDCT	115.85MHz

C. Image Analysis Results

Figure 8. Original Image

Figure 9. Reconstructed From DCT Coefficients

VII. Conclusion

The 2-D DCT and 1D-DCT architectures which adopts algorithmic strength reduction technique to reduce the device utilization pulling the power consumption low have thus been designed. The DCT computation is performed with sufficiently high precision yielding an acceptable quality. The pipelined 2-D DCT architecture achieves a maximum operating frequency of 185.95 MHz. The first eight 2-D coefficients arrived at the nineteenth clock cycle and for the full 64 coefficients, it took about 26 clock cycles to compute. The future work can be oriented towards developing an encoder by architecting a quantizer, based on the strength reduction technique and an entropy encoder.

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