Design and Development of Nanoelectronic Binary Decision Tree Device based on CMOS and QCA (Quantum-Dot Cellular Automata) Nanotechnology

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ABSTRACT
Evolution of microelectronics towards miniaturization is one of the main motivations for Nanotechnology. CMOS Technology has been targeted to integrate more and more Devices per unit area of Silicon-substrate, but there is limitation in scaling-down CMOS Circuits/Devices. Like Nanotechnology, QCA (Quantum-Dot Cellular Automata) is another alternate Technology having ability to reduce the Device-sizes beyond the CMOS Devices. The QCA enables the Moore's law to double the Devices every 18 months.

The continued improvements in miniaturization, speed and power reduction in information processing devices, sensors, displays, logic devices, storage devices, transmission devices, communication devices, etc. will bring another Technical Revolution, which will change our life.

The Design Strategies focus on CMOS Technology (<50 nanometer) and QCA Technology to achieve low power consumption, low voltage operation, high operating frequency, minimized number of transistors/gates/devices, reduced fabrication cost, high speed communication, flexibility, programmability, and service efficiency.

In our Research Work, we would like to focus on Design & Development of Nanoelectronic Binary Decision Tree Device based on CMOS and QCA (Quantum-Dot Cellular Automata) Nanotechnology as Building Blocks, for constructing more complex Circuits/Devices, defining Features/Functionalities and monitoring Status of WiMAX/WiFi/Satellite and other Wireless Communication Systems.

Index Terms- NANOTECHNOLOGY; NANOELRCTRONIC; NANOELECTROMECHANICAL SYSTEMS (NEMS); VLSI; MOSFET; NMOS; PMOS; CMOS; Bicmos; QCA; BINARY DECISION TREE; Wimax; Wifi**;**

1. INTRODUCTION
NANOTECHNOLOGY is derived from the evolution of microelectronics towards miniaturization. The famous empirical Moore's Law states that number of Transistors per chip doubles every 18 months. The Semiconductor Industry Association (SIA) has developed a Roadmap for continued improvements in miniaturization, speed and power reduction, to overcome CMOS Technology's scaling limitations. Specifying Nanostructures (Transistors) within the size of 1-50 nanometers for simulation of Nanotechnology Devices, based on CMOS Technology & QCA Technology will be the initial approach, followed by enhancements/refinements.

Rapid advancements in Nanotechnology, such as Nanomaterials, Nanometer CMOS Devices, Nanoelectronic, Nanoelectromechanical Systems (NEMS), Nanophotonic Devices, etc. are going to bring radical changes in the society and particularly in Wireless Communication, where small, smart and speedy systems are everyone's first choice. This is possible as application of Nanotechnology is taking place in WiMAX/WiFi/Satellite and other Wireless Communication systems, which is 'State-of-the-Art' Technology at the moment. [3], [4], [6].

The MOS Process is categorized as NMOS, PMOS, and CMOS. The basic Devices in MOS Processes are the p-channel and n-channel MOSFETs. The p-channel MOSFETs are not as attractive as those of n-channel MOSFETs because the mobility of p-type material is poorer than of the n-type material. In CMOS (Complementary Metal-oxide Semiconductor) Technology, both N-Type and P-Type Transistors are used to realize Logic Functions. It is the dominant Semiconductor Technology for Microprocessors, Memories and Application Specific Integrated Circuits (ASICs). CMOS has advantages over NMOS and Bipolar Technology, as it has smaller power dissipation only when Circuit switches. It consumes very little power, particularly for Mobile Communication. This allows integration of many more CMOS Gates on an IC than NMOS or Bipolar Technology and fabricating VLSI Circuits with much better performance. [8], [10], [12].

WiMAX (World-wide Interoperability for Microwave access) will offer Broadband Wireless Access at Data Rate of Multiple Mega Bits per Second to the End-user within a range of Several Kilometers. WiMAX supports a variety of Wireless Broadband Connections: High-bandwidth MANS (Metropolitan-Area Networks), Cellular Base Stations and Internet for WiFi. WIMAX is a complement to Fixed, Portable and Mobile Access. The Multimode SMART WiMAX will allow End User Devices to support New High-speed Services in many Different Network Environments. This can be achieved with Nanotechnology based WiMAX/WiFi Devices/Components. A Wireless Communication System can be upgraded and deployed as 'Mobile Ad Hoc Access Wireless System' and 'Portable Internet' with Nanotechnology based WiMAX/WiFi Communication System. [9], [13], [14], [15].

WiMAX opens the Door to thousands of Applications to connect People together. With the high Data Rate, Applications will include Video Transfer, Voice Calls, and many other Services. Development of Communication Devices based on NANOTECHNOLOGY and its Applications is one of the Grand Challenges for this Century.

Devices developed for IT, Data Storage and Wireless Communications will have Potential Applications in Defence, Aerospace, Automotive, Consumer Technologies, Business, Education, Research and many more areas.

2. QCA TECHNOLOGY

QCA was first introduced in 1993 by Lent et al. It represents an emerging Technology at the Nanotechnology level. QCA uses Quantum Wells with 4 Quantum-Dots having 2 mobile Electrons to represent Logic States. The Electrons can move to different Quantum-Dots in the QCA Cell by means of Electron Tunnelling and its position is determined based on the Columbic Force, positioning one electron from the other one in diagonally located Quantum-Dots. The Electrons are able to tunnel between the Dots. Based on the Electrons' positions, there are two possible Polarizations (-1 or +1), indicating Binary 0 and Binary 1. The Polarization of each Cell depends upon the Polarization of its previous neighboring Cell. The QCA Cell Architecture is shown in Fig. 1.

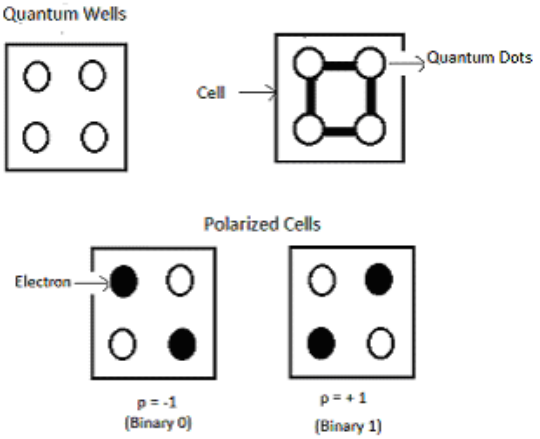
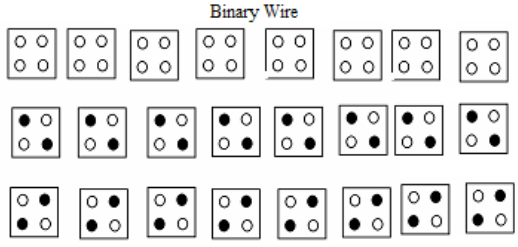


Fig. 1: QCA Cell Architecture

A Binary Wire and Inverter Chain are shown in Fig. 2. The Binary Wire is known as Logic Signal Transmission Channel, where the Cells transmit information in Coded form (0 or 1) from one Cell to another without any current flow. Polarization of each Cell depends upon the polarization of its previous neighboring Cell only. In the Inverter Chain, the Code of the previous neighboring Cell is inverted (0 to 1 or 1 to 0) and thus the transmission of Code takes place. In QCA, the Information propagates along a line of Cells due to Columbic Charge interaction, compared to conventional Electronic Current in CMOS Devices. The Columbic Force is responsible for all the Logic Operations and transfer of the States from one location to another.



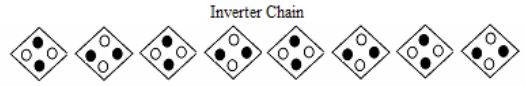
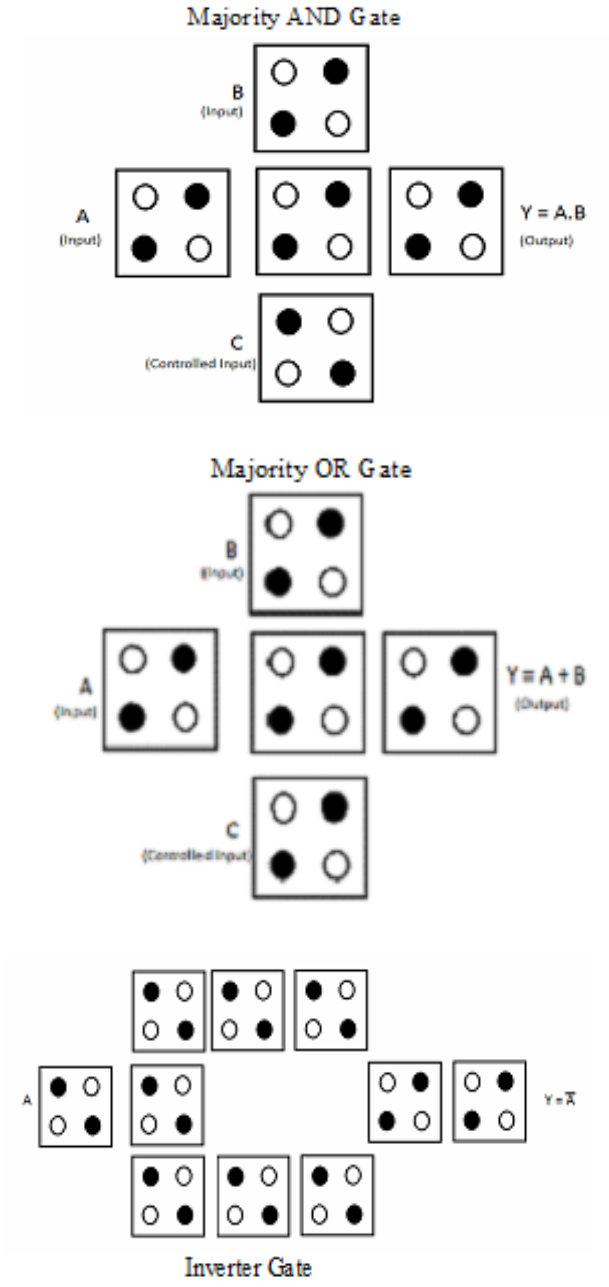


Fig. 2: Binary Wire & Inverter Chain

QCA is based on the encoding of Binary Information in the Charge configuration within Quantum-Dot Cells. QCA is implemented based on Majority Gate having three Input, one Output and one Center (Device) Cells. If A, B, C are Inputs then Output = M(A,B,C) = AB+BC+CA. If the input polarization of Control Input is fixed to +1 (logic 1), the OR logical operation is performed and in the case of -1 (logic 0) the AND logical operation is performed. The NOT logical operation is performed when the Cells are placed diagonally. The Majority OR, AND, and NOT Gates are shown in the Fig.3.



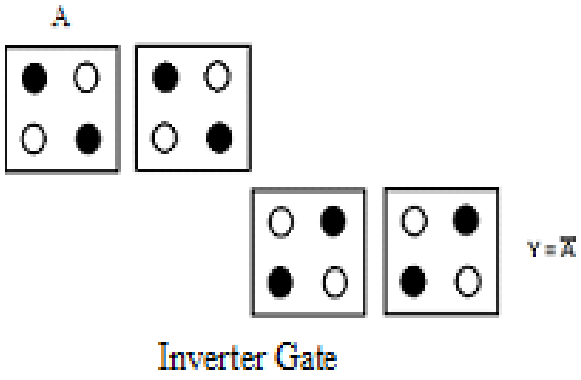


Fig. 3: QCA Cell Logic Gate

A multizone Clock mechanism is required for proper Data Propagation in the QCA Circuit. Four Clock Signals having 90 degree relative phase difference with each other are used for the operation of the QCA Circuits. The four Clock Phases/States are identified as Switch, Hold, Release and Relax States and the four Clocking Zones are identifies as Zone 0, Zone 1, Zone 2 and Zone 3. Each Cell in a Clocking Zone is connected to one of four Phases of the QCA Clock. The polarization of the QCA Cell is determined in the Switch and Hold States depending on the polarization of the neighboring Cell. The Release and Relax States are unpolarized. Each Cell is latched and unlatched with the changing of the Clock Signal. The Clock synchronizes and controls the flow of information as well as supplies the necessary power to the Cells. The QCA Clock and QCA Clock Zones are shown in Fig. 4. [1], [2], [5], [7], [11].

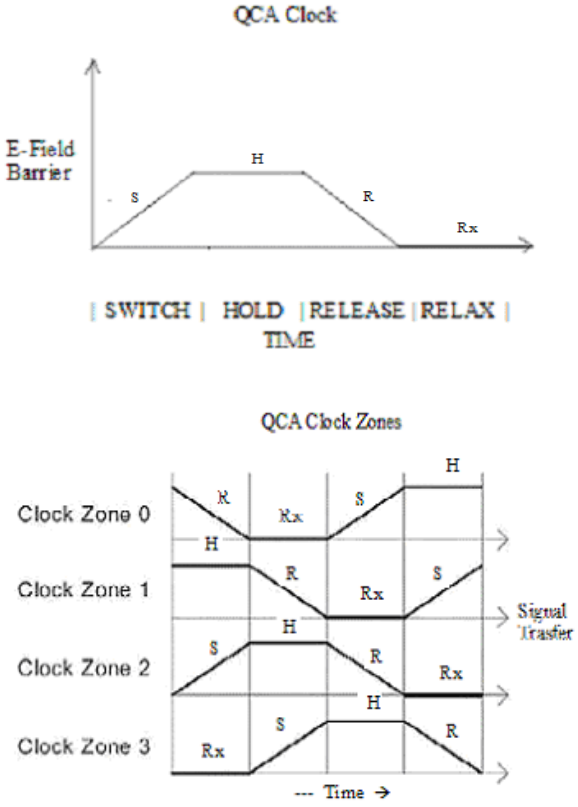


Fig. 4: QCA Clock Signal

3. METHODOLOGY

Our approach will be to design, develop and qualify a 'Nanoelectronic Binary Decision Tree Device to the scale of < 50 nanometer, based on CMOS Technology, using CADENCE Software Tool. Reduction in the number of Components through Integration and Optimization of Performance is also exercised in this Design Simulation. Depending on the facility available, it seems that the 'Molecular Nanoelectronics' Technology and the 'Top-down' approach is more suitable for obtaining Nanostructure within the size of 1-50 nanometers scale. A QCADesigner Simulator is used to layout and verify QCA Logic Design for the Binary Decision Tree Device (to the scale of <20 nanometer)..

4. BINARY DECISION TREE (BDT):

The proposed Binary Decision Tree (BDT) is shown in Fig. 5. It determines that any combination of three conditions/tests/inputs out of four being (+) ve affirms success. A BDT Gate is suitable for SOP (Sum-of-Products) Function expressed as a Summation (OR) of Products (AND) terms. A BDT Logic Function is one that implements the operations in the order AND then OR. As for example; X = (X1 + X2 + X3 + X4) = ((a.b.c) + (a.b.d) + (a.c.d.) + (b.c.d)).

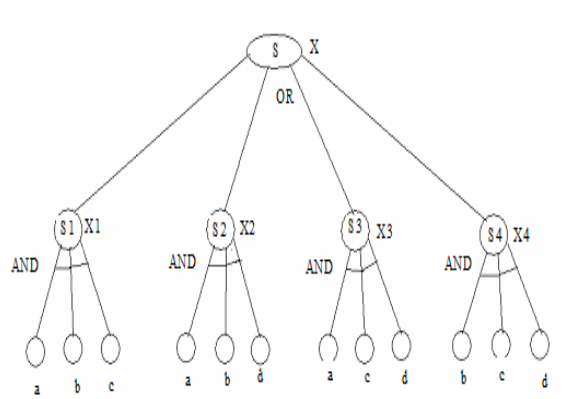


Fig. 5: Binary Decision Tree

5. SIMULATION MODELS & RESULTS ANALYSIS

We have developed two Simulation Models: a) CMOS Model and b) QCA Model for the Binary Decision Tree and the Simulation Results are analysed accordingly.

5.1 CMOS MODEL

Using CADENCE Software Tool, a Model of the Binary Decision Tree is simulated and its performance is analysed. A Model of Binary Decision Tree – Logic Circuit is shown in Fig. 6. The Model has four AND Gates, each having three inputs, and the outputs of the AND Gates are inputs of the OR Gate. These Gates are detailed with CMOS Circuits.

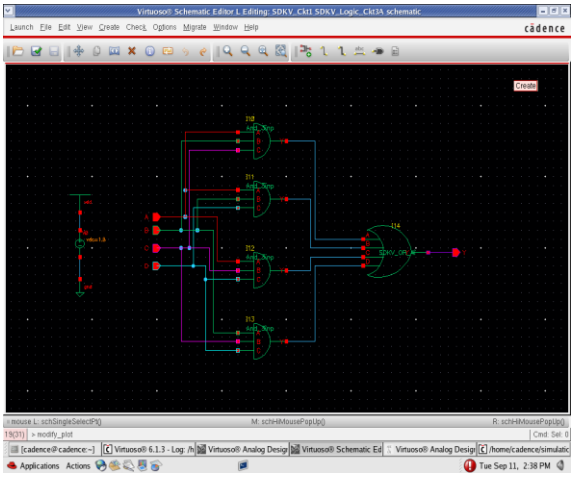


Fig. 6: Binary Decision Tree – Logic Circuit

A Model of Binary Decision Tree – CMOS Circuit is shown in Fig. 7. The Model is simulated using CADENCE Software Tool (for 1.8V and 45 nanometer scale). The Model is analysed with two sets of Inputs and the Transient Responses are recorded in Fig. 8 and Fig. 9.

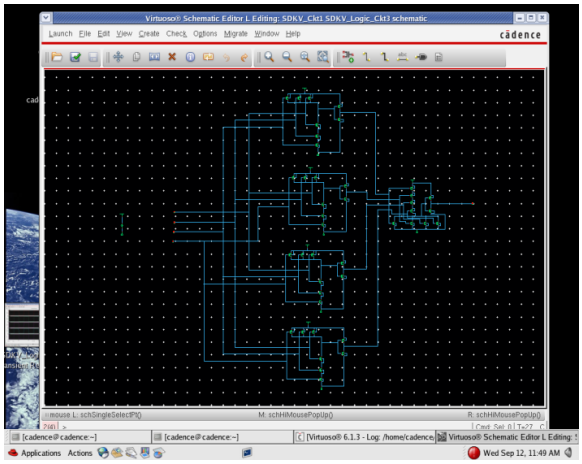


Fig. 7: Binary Decision Tree – CMOS Circuit

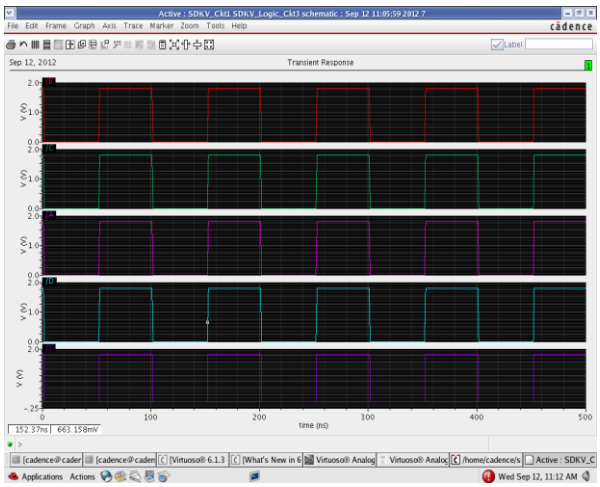


Fig. 8: Binary Decision Tree – Transient Response-A

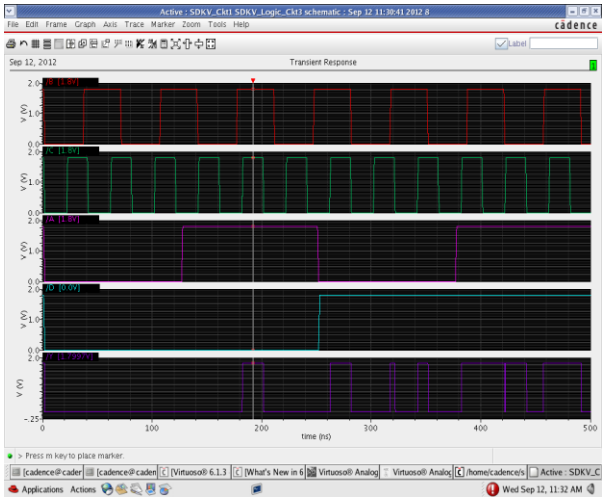


Fig. 9: Binary Decision Tree – Transient Response–B

5.2 QCA MODEL

Using QCADesigner Simulator, a Model of the Binary Decision Tree is simulated and its performance is analysed. The Model has four AND Gates, each having three inputs, and the outputs of the AND Gates are inputs of the OR Gate. These Gates are detailed with QCA Logic Circuits. A QCA AND Logic with three inputs and a QCA OR Logic with four inputs are shown in Fig. 10.

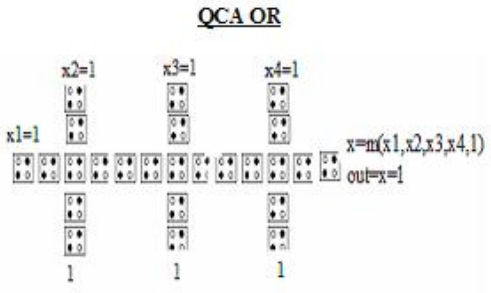
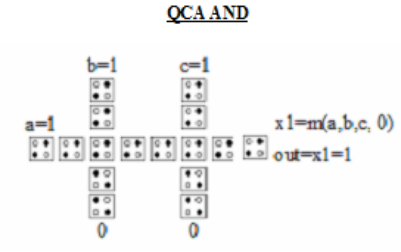


Fig. 10: QCA Logic Circuit

A QCA Binary Decision Tree as shown in Fig. 11 is designed with four QCA AND Logic, each having three inputs (all 1), and one QCA OR Logic with the outputs of the four QCA AND Logic as inputs. The QCA Logic is defined as follows:

QCA AND Logic 1: x1 = m(a,b,c,0) = m(1,1,1,0) = 1
QCA AND Logic 2: x2 = m(a,b,d,0) = m(1,1,1,0) = 1
QCA AND Logic 3: x3 = m(a,c,d,0) = m(1,1,1,0) = 1
QCA AND Logic 4: x4 = m(b,c,d,0) = m(1,1,1,0) = 1
QCA OR Logic 1: x = m(x1,x2,x3,x4,1) = m(1,1,1,1,1) = 1.



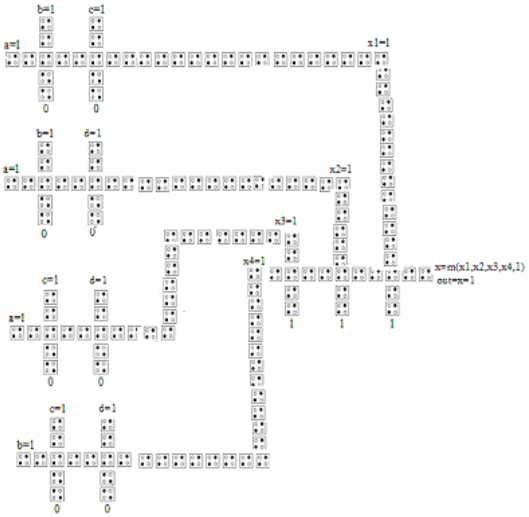


Fig. 11: QCA Binary Decision Tree

Using QCA Simulator, a Simulated Model of the QCA Binary Decision Tree is developed (<20 nanometer) as shown in Fig. 12. The Model consists of four QCA AND Logic and one QCA OR Logic. The Simulation Results are shown in Fig. 13 & Fig. 14.

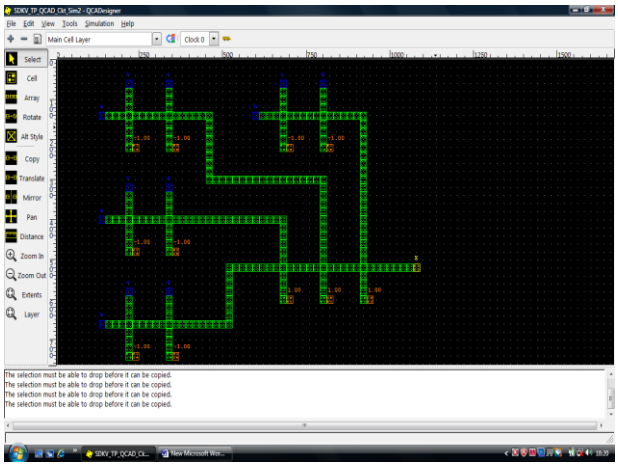


Fig. 12: QCA Binary Decision Tree - Simulated Model

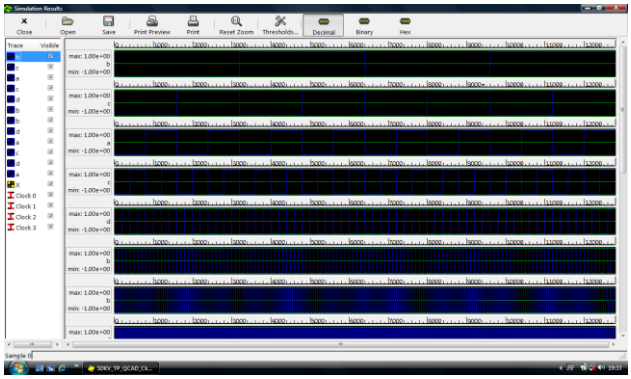


Fig. 13: QCA Binary Decision Tree Simulation Result Part-A

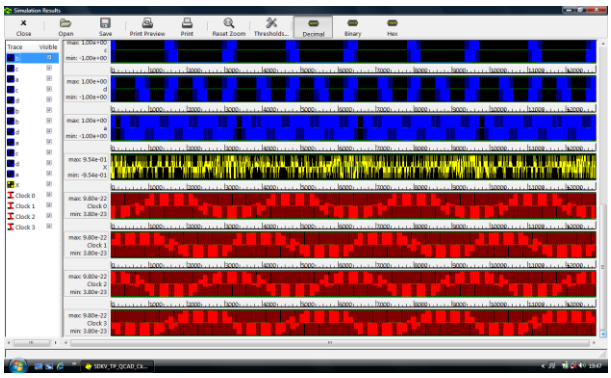


Fig. 14: QCA Binary Decision Tree Simulation Result Part-B

6. CONCLUSION

In our Research Work, we have focused on Design & Development of Nanoelectronic Binary Decision Tree Device, based on CMOS & QCA Nanotechnology as Building Blocks for Communication Devices, and a comparative evaluation is performed. In CMOS Technology Transistors are used to construct Gates/Devices while in QCA Technology Cells are used to construct Gates/Devices. The CMOS Model is simulated and qualified for 1.8V and 45 nanometer scale. The QCA Model is simulated and qualified for Cell size <20 nanometer. It is verified that the QCA Circuits are similar to the CMOS Circuits and it minimizes the complexity, delay and size. Our objective is to design and develop CMOS and QCA based Circuits/Devices as Building Blocks which can be used for constructing more complex Circuits/Devices, defining Features/Functionalities and monitoring Status of WiMAX/WiFi/Satellite and other Wireless Communication Systems.

Applications of CMOS & QCA Nanotechnology in WiMAX/WiFi Wireless Communication will lead towards Architectural Innovation & Smart Devices, Value Added Services, Full Scale QoS (Quality of Service) and Higher Reliability and Security. Our Research Work will help in addressing Long term Technical Challenges pertaining to "*Design, Development and Application of CMOS & QCA Nanotechnology in WiMAX/WiFi/Satellite and other Wireless Communication Systems,"* and provide feedback to ICs Designers/Managers, Wireless Standards Managers, Wireless and Internet Service Providers and other Interest Groups.

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