

Mixed Signal Design Paradigms for Analog Circuit Design in Deep Submicron CMOS

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Introduction

This analog circuit's research addresses the development of creative new paradigms that underlie the design, and layout of reliable, reproducible, high yield, high performance, analog integrated circuits fabricated in deep submicron CMOS technology. The Research and Development (R&D) effort is partitioned into two technologically related, but otherwise independent projects. The first of these projects produces new mixed signal design paradigms that exploit a microcontroller embedded on chip. Upon circuit boot up, the microcontroller assesses circuit performance, compares assessed performance with design targets, and automatically makes circuit adjustments to optimize Input/Output (I/O) performance. The second project is focused on an alternative analog design paradigm that supplants the realization of a high performance analog IC with a Digital Signal Processor (DSP). This sufficiently high speed DSP emulates the desired analog Signal Input/Signal Output (I/O) performance. Among the advantages associated with DSP emulation of analog networks is considerable flexibility in controlling, adjusting, and optimizing analog performance. It even enables reconfiguration of analog cells.

The first (microcontroller) project can be executed and completed without initializing the second (DSP) project. But the second project arguably profits from the experience gained on the first. Each of the two R&D projects can be executed in nominally thirty months.

Vision One: Micro-Controlled Analog ICs

The vision of R&D Project One is to develop new mixed signal Integrated Circuit (IC) design paradigms that exploit an embedded microcontroller to monitor circuit performance, compare monitored performance with programmed design targets, and automatically adjust appropriate circuit voltages and currents to minimize disparities between monitored and expected analog IC performance. The project focuses on the development and design of high performance analog ICs fabricated in deep submicron CMOS technologies. Much of the initial work addresses the identification and nature of requisite adjustments in static, or quiescent, voltage and current levels. But to the extent that these static corrections influence large signal transient and small signal network behavior, the control of signal dynamics at potentially high frequencies also receives attention. In view of the availability of the Advanced RISC Machine (ARM) architecture, an actual design of a suitable microcontroller is unnecessary. Nevertheless, some time is spent to review the salient aspects of ARM architectural utilization and its associated reduced instruction set computing (RISC) schema to ensure maximal effectiveness of the microcontroller deployed to optimize the performance of sophisticated analog circuits.

Why are microcontrollers essential in deep submicron MOS?

For conventional biasing, deep submicron MOSFETs featuring reasonable gate aspect geometries are plagued with anemic forward transconductances, significant channel length modulation (CLM), potentially non-negligible bulk-induced threshold modulation (BITM), appreciable drain-induced barrier lowering (DIBL), and imperfect gate self-alignment. They also endure strong lateral channel electric fields

that achieve critical strengths commensurate with carrier velocity saturation for even relatively small drain-source voltages. Additionally, deep submicron transistors typically boast exceptionally thin gate oxides. These thin oxide layers give rise to strong vertical fields that beget hot electrons. The foregoing and related other shortfalls limit achievable gain and output resistance in common source transconductors, they inhibit small output impedances in source followers, and they degrade the quality of traditional current sinks and sources. Second order device phenomena also impair the attainable matching in current mirrors and other subcircuit types, and they deleteriously affect large signal transient and steady state responses, bandwidth, signal to noise ratio, and steady state I/O linearity.

The problem is that the accurate and repeatable quantification of the majority of the aforementioned and related other shortfalls, which is an absolute prerequisite to a reliable mitigation of their impact, is a daunting challenge. In particular, deep submicron channel lengths and the circuit level modifications required to compensate for small channel lengths exacerbate the engineering significance of a myriad of ill-defined and/or poorly controlled physical device parameters. For example, the I/O current ratio of a simple current mirror becomes progressively more sensitive to carrier mobilities, electron Debye lengths, substrate impurity concentrations, oxide contaminants, and intrinsic carrier concentrations. These and other physical issues and properties are generally accommodated in circuit simulators by curve fit lookup parameters that defy physical interpretation and resist accurate geometrical scaling.

R&D approach

To compensate reliably for a plethora of high performance analog design issues, a design paradigm entailing an embedded microcontroller is proposed to monitor and optimize I/O performance. This tack does not mean that the uncontrolled design can be sloppy or marginal. Indeed, it must still be capable of achieving targeted performance, despite the presence of numerous vagarious device and circuit physical parameters. In effect, the embedded microcontroller expunges "vagarious" from this condition by suitably compensating for them at the circuit level. This compensation requires the identification of suitable control ports, such that when energized by corrective voltages and currents, the controlled ports facilitate optimal operating corrections. Obviously, it

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is necessary to identify a cadre of pragmatic canonic analog cells and other analog networks. Definitive manual and computer-aided analyses must then be executed on these networks, as well as on the canonic cells of analog MOSFET technology, to identify the critical parameters in need of voltage-controlled or current-controlled adjustment. Implicit to this task is the formulation of a definitive library for analog circuit design. But the most important fruit of this vision is consistently reproducible and accurate designs of sophisticated analog circuit cells in deep submicron CMOS technologies.

Vision Two: DSP Emulation of Analog ICs

The vision of R&D Project Two is to develop a new mixed signal design paradigm that exploits digital signal processing to emulate the I/O performance of desired analog systems. Although the idealized square law characteristic curves of individual MOSFETs can be emulated, preliminary thinking suggests the efficacy of directly emulating the performance of an entire analog network or system. Such performance need not be restricted to linear networks; for example, it may be of interest to emulate the idealized operation of a Gilbert, four-quadrant multiplier, a phase-locked loop, or a voltage-controlled oscillator. Moreover, the performance to be emulated can include static, large and small signal transient, and small signal, behavior. Included among the performance metrics that can be embraced by DSP emulation are gain, impedance levels, bandwidth, distortion, noise, settling time, group delays, quality factors, self-resonant frequencies, and so forth.

Why might DSP emulation prove profitable in high performance analog systems?

Two advantages of the proposed DSP approach to analog system emulation surface immediately. First, the desired or targeted I/O performance can be ideally emulated. This to say, for example, that perfect linearity, infinitely large signal to noise ratio, zero or infinitely large port impedances, precise 20 dB/decade frequency response

rolloff, perfectly flat group delays in the frequency domain, and other idealized performance can be ostensibly emulated. A second advantage is the convenient programmability of desired responses, as well as considerable flexibility in adjusting the parameters that control the nature of these observed responses.

R&D approach

Aside from defining the specific types of analog systems in which vested interests can be argued, there is considerable work that must be done at the software and hardware levels to develop the DSPs that are deemed suitable for a broad range of analog networks and systems. At a minimum, this work must respond proactively to the following issues:

- The frequency response and the response speeds, in general, of the emulated system will be determined by the speed of the utilized DSP. It follows that design measures that assure suitably high speeds in DSPs must be fully developed, explored, and tested.
- How does noise in the DSP affect emulated performance, and how can these noise effects be mitigated?
- What bit accuracies are required of the DSP?
- How transient responses in the DSP reflect to emulated analog performance, and how can undesirable transient phenomena be mitigated?
- Is there a power dissipation penalty associated with the deployment of a DSP with acceptable bit accuracy? Can a low power, very high speed DSP be designed reproducibly and with high yield in deep submicron CMOS technology?
- What is the complexity and footprint of the requisite DSP hardware?
- Other questions and issues are surely expected to surface.