Compact Frontend–Electronics and Bidirectional 3.3 Gbps Optical Datalink for Fast Proportional Chamber Readout

S. Lüders[a]IPP]Institute for Particle Physics, ETH Zurich, 5232 Villigen PSI, Switzerland, R. Baldinger[b][IPP], D. Baumeister[c]ASIC]ASIC–Laboratory, Kirchhoff–Institute for Physics, 69120 Heidelberg, Germany, K. Bösiger[d]UNIZH]Physics Institute, University of Zurich, 8057 Zurich, Switzerland, R. Eichler[e][IPP]*, M. Feuerstack–Raible[f][ASIC], C. Grab[g][IPP], S. Löchner[h][ASIC], B. Meier[i][IPP], P. Robmann[j][UNIZH], B.A. Schmid[k][UNIZH], U. Stange[l][ASIC], S. Steiner[m][UNIZH], U. Straumann[n][UNIZH], S. Streuli[o][IPP], K. Szeker[p][IPP]† P. Truöl[q][UNIZH]

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The 9600 channels of the multi–wire proportional chamber of the H1 experiment at HERA have to be read out within 96 ns and made available to the trigger system. The tight spatial conditions at the rear end flange require a compact bidirectional readout electronics with minimal power consumption and dead material.
A solution using 40 identical optical link modules, each transferring the trigger information with a physical rate of 4×832 Mbps via optical fibers, has been developed and commisioned. The analog pulses from the chamber can be monitored and the synchronization to the global HERA clock signal is ensured.

1. Introduction

An optical link and frontend electronics has been developed to read out all 9600 channels of the H1 experiment's central inner multi–wire proportional chamber (*CIP*) within the time between two bunch crossings, i.e. 96 ns. The application requires a bidirectional multi–purpose link: the digitized chamber information has to be provided to the trigger system 40 m away, selected analog pulses should be accessible for monitoring purposes and the whole frontend electronics must be synchronized to the global HERA clock signal. Furthermore, the optical link and readout electronics must fit in the available space of a 130 mm long open cylinder with inner and outer radii of 152 mm and 198 mm. No commercial solution for optical links fulfill these requirements in one compact unit.

*Corresponding author. Phone: +41 1 633 2018, Fax: +41 1 633 1233, e–mail: eichler@particle.phys.ethz.ch
†Present address: Physics Institute, University of Zurich, 8057 Zurich, Switzerland

The custom–made solution is composed of forty identical *optical link modules*, where a 64–fold multiplexing reduces the number of data lines. Each module performs an optical transmission with a physical rate of 3.3 Gbps. Precisely aligned VCSEL and PIN diode arrays allow for bidirectionality. The bending of optical fibers by 90° within 2 mm minimizes the overall height of the design.

A short overview of the CIP upgrade is given in Section 2 and the general layout is discussed: Each of the optical link modules consists of an on–detector unit, two optical hybrids with optical cables and a receiver unit. Their functional designs are presented in Sections 3, 4 and 5, respectively. The performance of the optical link and frontend electronics is presented in Section 6.

2. CIP Upgrade and General Layout

With the year 2000 upgrade of the HERA electron–proton collider at DESY, an increase in luminosity by a factor of five is anticipated. The expected higher background rate, predominantly beam–wall and beam–gas reactions, necessitates an improvement of the CIP to provide high background rejection efficiency of the z–vertex trigger [1,2].

The redesigned CIP [3] is built of five concentrical cylinders (*layers*) with radii from 152 mm to 198 mm. In the azimuthal angle, each layer is equally subdivided into 16 *segments*, each consisting of 120 *pads*[1] along the symmetry axis (z–*axis*). Charged particles traversing the chamber are detected by the 9600 pads, which provide space points and timing information. The direction of tracks can be inferred from the pattern of hit pads. For electron–proton collisions intersections of tracks with the z–axis come mostly from the interaction region, while the dominating background originates from proton beam losses upstream of the experiment. Experience has shown, that such background tracks seen by the H1 experiment are typically intersecting the z–axis at 0.5 to 1.5 m upstream of the mean *ep* interaction position. A new trigger system based on the latest FPGA family will identify these upstream events and is presently being commissioned. According to simulations this new trigger will improve the background rejection capability of the first level trigger by an order of magnitude compare to the previous z–*vertex trigger* [4].

The decision has to be made for *every* bunch crossing. Thus all 9600 pads have to be read out within the time between two bunch crossings, i.e. within 96 ns, corresponding to the bunch crossing frequency of 10.4 MHz (*HERA clock*). From the timing information, the bunch crossing number can be deduced.

Each of the forty identical optical link modules is used to read out all 2×120 pads of two adjacent segments (a *double–segment*) of a layer with a rate of 10.4 MHz. The *on–detector electronics unit* amplifies and shapes the signals from the pads, discriminates and serializes them to 4×15 bit words. After a second level 16–fold multiplexing, this *trigger information* is transferred to the *receiver electronics unit* 40 m away, located outside the main detector. Thus the total digitized information per module sums up to a data rate[2] of 4×624 Mbps. The on–detector electronics component must be synchronized to the global HERA clock signal therefore the system requires bidirectionality. The receiver electronics provides the global HERA clock and retrieves the multiplexed trigger information, which is de–serialized and distributed to the *trigger system*. Additionally, analog signals from each pad are transmitted and accessible for monitoring purposes.

To retain high geometrical acceptances for the new CIP and neighbouring detectors in the H1 experiment, the available space for mechanical support structures and electronics is limited to a 130 mm long open cylinder with inner and outer radii of 152 mm and 198 mm, respectively, located at the backward end flange[3] of the CIP. This tight space has to be shared between on–detector electronics, their suspension and cooling, low and high voltage power cables and gas supply lines (Figure 1). The power consumption has to be minimized to avoid an excessive heat dissipation inside the H1 experiment due to limited cooling possibilities.

Only an optical transmission allows high serial data rates, suppresses crosstalk and decouples detector and trigger system, while reducing the number of cables and the power consumption to a minimum. A readout with copper cables as formerly done would increase that volume by a factor of ten, would require even more driving power and would produce an unwanted high contribution to the dead material. In addition, an electrical transmission at the required high rates will likely induce noise into the very sensitive liquid argon calorimeter of the H1 experiment.

The optical link between on–detector electronics and the receiver electronics is established by two *optical hybrids* which perform opto–electrical (re)conversion of all data lines, i.e. four digital

[1] In fact, the CIP uses a projective geometry requiring 119 pads on the innermost layer, and 112, 106, 99 and 93 pads on the following layers, respectively. But for symmetry reasons, each optical link module will be capable of handling 120 pads.

[2] In principle, each optical link module is capable to transmit at a data rate of 4×1000 Mbps at maximum.

[3] The term "backward" labels the $-z$ end of the H1 experiment pointing in the direction of the electron beam.

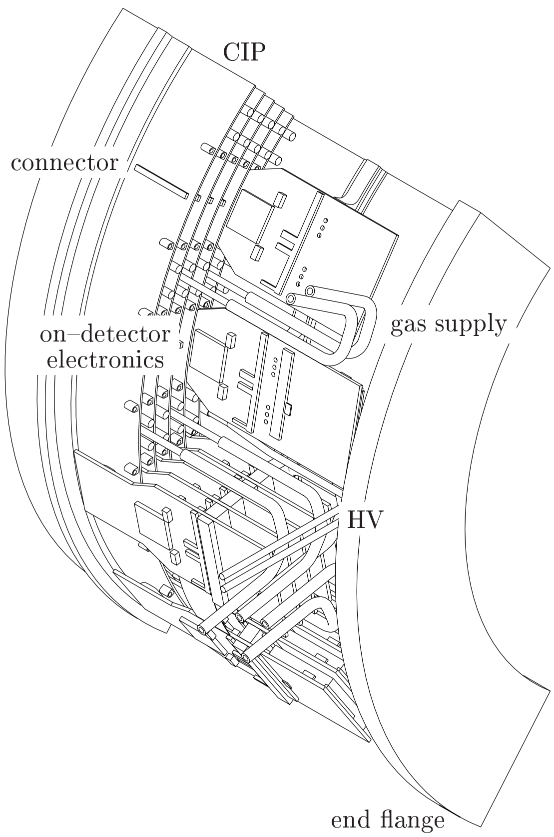

Figure 1. Illustration of the on–detector units mounted on the CIP. Four segments of the five layer CIP with gas tubes and HV cables are shown on the left. Five on–detector units stacked on top of each other and supported by cooling blocks are plugged on the lower segments; one unit is mounted on each of the upper segments. Their top sides face to the symmetry axis.

channels for the trigger information, two analog channels and two channels for the HERA clock signal. Experience with opto–mechanics has already been collected in the ETH Zurich group. An analog optical readout for the H1 experiment has been successfully operated since 1995 [5,6].

3. On–Detector Electronics Unit

Each on–detector unit collects the charge from 2 × 120 pads. Their charge is conducted via micro coax cables [7] to the rear end flange of the CIP. For each segment, a connector (Fujitsu FCN 298 [8], 120 contacts, 500 μm pitch, 2.5 mm height) passes the 120 channel pad information to a pair of analog readout (*CIPix*) chips. The CIPix chip amplifies, shapes, discriminates and four–fold multiplexes the signals. Further compression is done by two 16–fold multiplexers, each driving a differential high–speed data channel at 832 Mbps. After electro–optical conversion by the optical hybrid, the light pulses are transmitted to the receiver electronics unit. The overall synchronization is done with the global HERA clock signal received by the optical hybrid. A low jitter phase–locked–loop (*PLL*) unit [9] generates a 41.6 MHz clock signal, which is distributed to the multiplexer and — in addition to the HERA clock signal — to the CIPix chip. Furthermore, selected analog signals can be branched off before entering the CIPix discriminator to monitor the CIP. These *analog test signals* are also transmitted (Figure 2).

For compactness, one optical hybrid serves a double–segment and is mounted on one of the two separate halves of the on–detector unit. The other half holds the PLL unit and houses the voltage regulators. Due to the curvature of the CIP, a thin four layer flex–capton print bridges all signals via striplines to their destinations: The high–speed data channels and analog test signals are transferred from the other segment to the optical hybrid and, in return, the HERA clock signal is provided to the PLL unit. The flex–capton print is sandwiched between each of the halves. This *rigid–flex* print is produced by Dunkel & Schürholz [10]. It is implemented as an extremely high dense board with microstrip transmission lines and eight layers in total (Figure 3). Its outer dimensions are 130 mm in length, 2 × 49 mm in width and 9 mm in height. The open length of the capton print, i.e. the distance between both halves, increases proportional to the layer radii.

All on–detector units of one layer are connected via an I^2C bus daisy–chain [11]. This allows for a steering of every CIPix chip from a terminal, e.g. all CIPix chips can be initialized layer–wise. In addition, it performs a one–wire serialized temperature measurement [12].

3.1. CIPix IC

The CIPix analog readout chip is custom–made [13]. It amplifies, shapes, discriminates and multiplexes the incoming signals [14].

For each of the 64 analog input channels, it consists of a charge sensitive preamplifier with a gain of 20 mV per 10^5 electrons, a CR–RC semi Gaussian shaper with a peak time of 50 to 70 ns and a comparator. The discriminated signals are synchronized to the HERA clock signal and four adjacent pads are multiplexed (Figure 4). For monitoring and testing purposes, one of the analog signals can be selected and branched off to an analog output. Test pulses of user–defined pattern and frequency can be internally generated. Comparator thresholds, the selection of channels for analog output and test pulses are programmable via the I^2C bus. To protect the bond–wires and the surface, each CIPix chip is sealed ("glob–topped") with protective glue (Epoxy Technology H70S [15]).

The analog signals from 60 pads are processed by a single CIPix chip. Synchronously to the 41.6 MHz clock signal, the CIPix's 15 digital output channels give four successive words with 15 bits each. A *FirstWord bit* tags the first of these words and will make it possible to maintain the synchronization to the HERA clock signal in the trigger system. Together they form the 16 bit *data word*. An EmptyDataSet signal, generated in the case of missing inputs on all 60 input pads of the CIPix chip, serves as the *EmptyDataSet bit*. All 160 EmptyDataSet bits provide a coarse

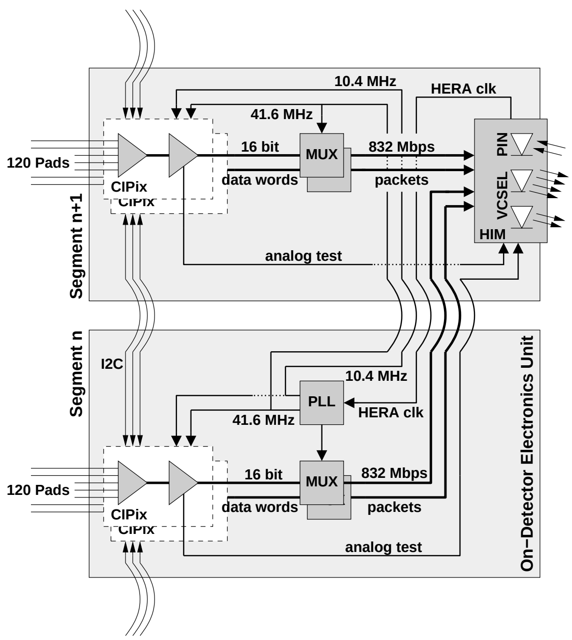

Figure 2. Signal flow of the on–detector electronics unit. A data word consists of the 15 bit trigger information plus the FirstWord bit. For details see text.

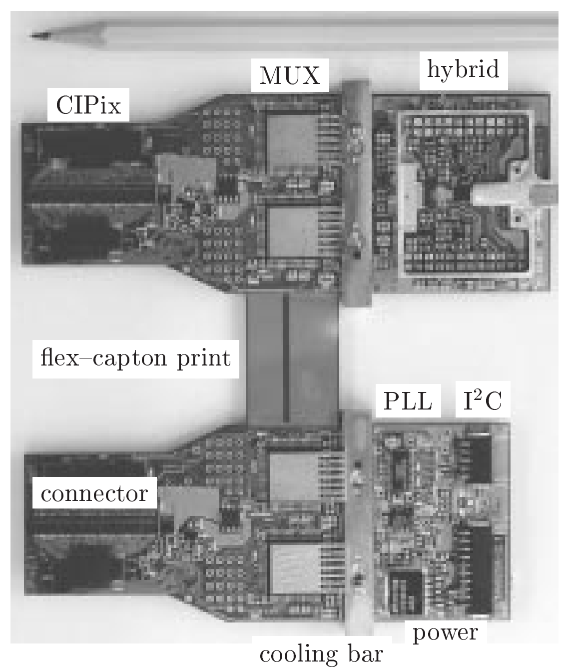

Figure 3. On–detector electronics rigid–flex print serving one double–segment.

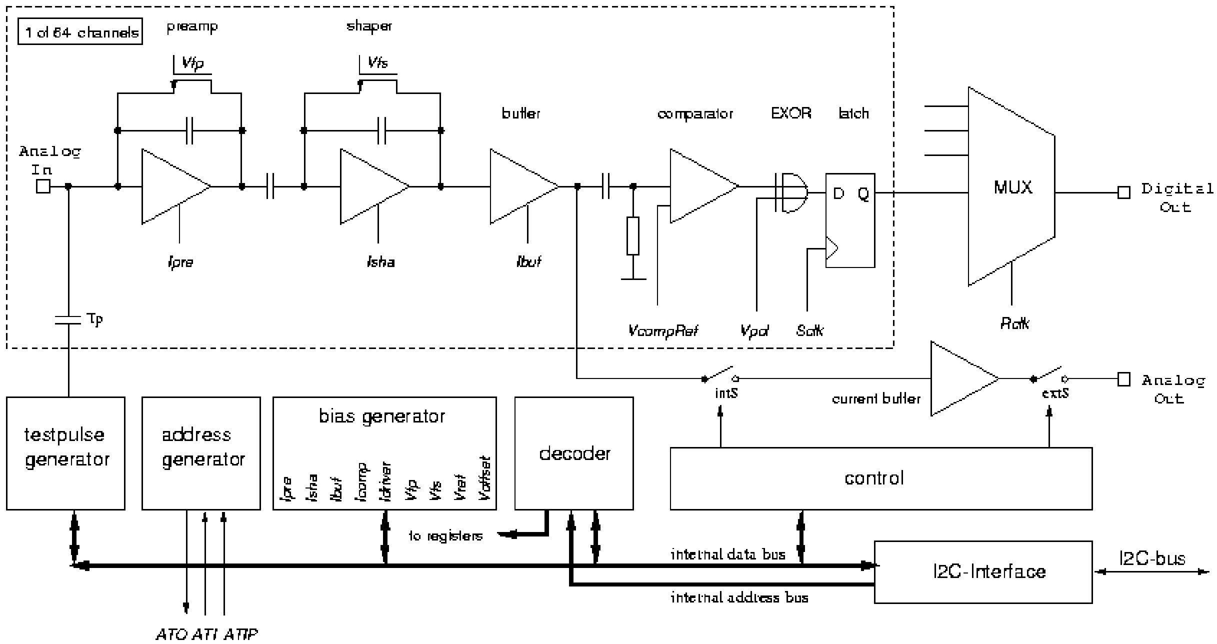

Figure 4. Block diagram of the CIPix chip.

readout and will be used for a trigger decision whether an event is compatible with cosmic ray background or not.

3.2. Multiplexing / Demultiplexing

A further reduction of channels is achieved by building a differential high–speed data link for point–to–point communication between the Hewlett–Packard HDMP 1032 transmitter and the HDMP 1034 receiver [16].

Both bipolar chips provide the transmission of a 16 bit TTL data word plus one flag bit with a serial data rate of 221 to 1190 Mbps. The rate is chosen by an external reference clock signal synchronous with the incoming word. The HDMP 1032 PLL / clock generator locks onto the reference clock signal and multiplies it up to the high–speed serial clock signal. From the data word a special four bit encoding information is generated on the fly, proceeding the data word. Together they give a 20 bit *packet*. On the one hand, the encoding ensures the DC balance of the serial line. The disparity[4] of each data word is determined. Depending on the disparity of the previous data word, an inversion of the actual word is done to keep a 50 % duty cycle. Additionally, the encoding bits provide an error detection, tagging wrongly transmitted words, and include an user–controlled *flag bit*. On the other hand, the unique bit pattern of the encoding scheme incorporates the high–speed clock signal and thus saves an additional clock signal line between transmitter and receiver. The packet is serialized and leaves the HDMP 1032 as a differential 100 Ω terminated ECL compatible high–speed signal.

The HDMP 1034 receiver's Clock Data Recovery unit separates encoding bits and data word from the 20 bit packet, extracts the high–speed serial clock signal and locks to its phase. The data words are (eventually) inverted and then demultiplexed. The Parallel Automatic Synchronization System synchronizes these words to an external

[4]The disparity is defined as the total number of "high" bits minus the total number of "low" bits.

reference clock signal. A master–slave mode allows for a synchronization of several HDMP 1034 chips: A deviation of the relative phase of the data word and the reference clock signal generates a shift request, passed to the master. The master controls the delay of all outputs of all slaves.

Each 16 bit data word is serialized by a HDMP 1032 chip. The EmptyDataSet bit is used as input for the flag bit; the 41.6 MHz clock signal provides the reference clock signal for both HDMP chips. Therefore the digitized trigger information from 60 pads is transmitted every 96 ns with a data rate of 624 Mbps. The overall physical rate includes in addition per 96 ns the four FirstWord bits and 4×4 bits of the encoding scheme (with the EmptyDataSet bit) and amounts to 832 Mbps. The receiver chip re–parallelizes the trigger information and extracts the FirstWord bit and EmptyDataSet bit. Four transmitter / receiver chip pairs — one for each CIPix chip — are used per module.

Bits of one high–speed digital channel have been superimposed for the eye–diagram (Figure 5). The rising and falling edges are well separated. The measurement of the zero–crossing of the rising edge results in a jitter of the data words of 23 ps before entering the optical hybrid.

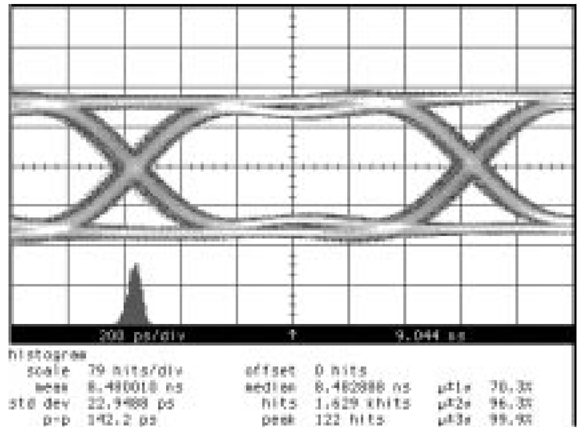

Figure 5. Eye–diagram accumulated from one digital channel and measured directly at the differential output of the 16–fold multiplexer. Shown is the digital level (“high” / ”low”) superimposed for all bits as a function of time. The small histogram gives the jitter. The signal density is given by the greyscale: the lighter the denser.

4. Optical Hybrid

The optical hybrids constitute the interface between the electrical and the optical régime.

Following the signal flow from the CIP to the trigger system, the optical hybrid on the on–detector unit (*HIM*, High–Speed Interconnection Module) acts as a driver for the outgoing 20 bit packets and analog test signals and as a receiver for the incoming HERA clock signal. The optical hybrid on the receiver unit side (*DeHIM*) acts vice versa. The interfacing pins require or deliver differential CMOS logic signals for each data channel, respectively.

Each HIM / DeHIM pair serves one double–segment, i.e. transmits four multiplexed data channels with a physical rate of 4×832 Mbps, two analog test signal channels and two HERA clock signal channels via an optical fiber array with eight fibers.

The four data channels are driven by the Helix HXT 2000 [17] chip optimized for vertical cavity surface emitting laser (*VCSEL*) diodes. The VCSEL diodes convert the electrical signal to light pulses. After 40 m of optical fibers, conventional PIN diodes reconvert the optical to electrical signals. These are amplified by the Helix HXR 2004 receiver chip and produce four differential data signals. Because of the high data rates, the hybrid boards are impedance controlled and realized in four–layers with layer–to–layer blind–via connections [10].

For redundancy two HERA clock signals are transmitted in parallel. Standard SZ 125 drivers match their signal levels with respect to the VCSEL diode specifications. Conexant (formerly Microcosm) MC 2007 receivers [18] convert the PIN diode responses back to voltage–modulated signals. Its active gain control (*AGC*) ensures a stable output signal above the sensitivity limit at about -20 dBm. The two analog test signals are driven by Maxim MAX 4212 operation amplifiers

[19] and received by Conexant MC 2011 (without AGC) chips. These differential analog signals and the HERA clock signal are finally amplified by Maxim MAX 4212 chips.

4.1. Driver and Receiver Circuits

The Helix HXT 2000 driver and the HXR 2004 receiver chips are designed for high–speed optical transmission up to 1.25 Gbps per channel; the HXT 2000 is optimized for VCSEL diodes at 800 to 1500 nm wavelength. The differential inputs to the HXT 2000 — four of them enabled — are amplified and current–modulated. External resistors allow to control the average and modulation current collectively for a VCSEL diode array. Thus the working range, i.e. the laser current, of an array of four VCSEL diodes can be optimized for maximum optical output.

The four channel HXR 2004, compatible to 0.6 pF photodiode arrays, converts the photocurrent from the PIN diodes to differential output voltages. In addition, the average photocurrents can be monitored.

4.2. Vertical Cavity Surface Emitting Laser Diodes

Laser diodes convert current–modulated signals into power–modulated light signals.

In a VCSEL diode the light propagates vertically through the structure (Figure 6). With this orientation the laser cavity can be grown to match the wavelength of the laser light, i.e. 850 nm. The total spectral width of the emission is generally less than 0.5 nm, which ensures a low coherence source. The beam divergence is typically below 12° FWHM. Alternating layers of AlAs and $Al_{0.15}Ga_{0.85}As$ provide the p– and. n–mirror stack surrounding the active region, respectively. With contact to the p–mirror, the VCSEL anode is bonded to the modulating current line, while the GaAs substrate holds the cathode i.e. ground potential [20]. Both, VCSEL and PIN diodes, are grouped in six– and two–diodes dies, respectively, from Truelight Corporation [21]. The specifications for the VCSEL and PIN diode arrays used are given in Table 1. The VCSEL diodes are specified as "class IIIb laser" in the safety standard ANSI Z136.1 [22] and have to be treated as a potential eye hazard.

Because of a delicate passivation, the softer ball–bond process using golden bond wires has been preferred to the wedge–wedge bonding and to the use of aluminum bond wires. Thus ultrasonic vibrations acting on the VCSEL diodes could be minimized and harm to the passivation could be prevented. Together with the required specifications of at least 1.5 mW at 12 mA laser current (i.e. to a slope efficiency of 0.125 W/A) and an uniform power gain over the VCSEL array, the yield has been tested to be about 31 %.

The lasering of the used VCSEL diodes typically starts at a current of 4.5 mA (Figure 7). With appropriate settings for the average and modulation current of the HXT 2000 ($V_{avg} = 1.74 \pm 0.13$ V and $V_{mod} = 1.38 \pm 0.08$ V, respectively) the working range has been optimized. The digital signal levels vary beween -49.1 ± 4.5 dBm for logical "low" and -3.7 ± 0.8 dBm for logical "high", leading to a dynamic range in optical output of approximately 45 dB. The uniformity over a VCSEL diode array is about 1.3 ± 0.7 dB.

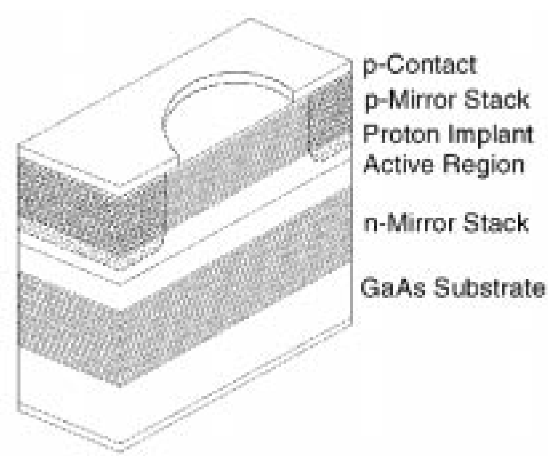

Figure 6. Sketch of a VCSEL diode.

Table 1
Specifications of the VCSEL and PIN diode arrays.

Optical specifications:	VCSEL	PIN
Wavelength	850 nm, multimode	850 nm
Beam profile and divergence	round, $< 12°$	
Active / Sense area diameter	18 μm	120 μm
Slope efficiency / Response at 850 nm	> 0.125 W/A	> 0.6 A/W $\pm$ 3 %
Electrical specifications:	**VCSEL**	**PIN**
$U_{\text{operating}}$	1.7..2.3 V	
U_{reverse}	> 10 V	> 10 V
Serial impedance	typ. 30 Ω	
I_{laser} / I_{dark}	4.5 mA	< 40 nA
C_{total}		< 0.9 pF @ 5 V
$\tau_{\text{rise / fall}}$	< 250 ps	100 ps
Crosstalk		> 30 dB
Mechanical specifications:	**VCSEL / PIN**	
Operating temperature	$< 85°$ C	
Chip thickness	150 μm	
Pitch diode / diode	250 μm	

4.3. Alignment and 90° Bending

In case of the HIM, the sixfold VCSEL and twofold PIN diode arrays are aligned with a precision of 5 μm with respect to each other and with respect to two guiding pins [23]. This provides a pitch of 250 μm in order to match the pitch of conventional fiber ribbon connectors (*MTP connectors* [24]). The guiding pins adjust the connector to the diode arrays (Figure 8).

To obtain the desired precision, each diode array is positioned by a custom–made micro manipulator. The manipulator is mounted on an *xy* table, which makes it possible to perform an accurate position measurement and an optical survey. At its final position, the diode array is lowered and glued onto the hybrid. An optimal mechanical and optical performance has been achieved using a two component conductive glue (Epoxy Technology H21D [15]) with a resistivity of $3 \cdot 10^{-4}\,\Omega/\square$ and a bakeout time of 2 h. On the DeHIM side, sixfold PIN and twofold VCSEL diode dies are aligned with the same accuracy.

Since the distance between two CIP layers is less than 9 mm, it is not feasible to mount the MTP connector above the VCSEL / PIN array. Even if the connector is reduced to its inner core, namely the *ferrule*, adjusting the ferrule perpendicular to the hybrid leaves no space to properly fix the connector to the optical hybrid. In addition, it complicates the installation of the fibers at the end flange. Consequently the ferrule had to be mounted parallel to the optical hybrid, i.e. parallel to the z–axis. Since the diodes send the light perpendicular to the die, the light needs to be redirected. Therefore the 62.5 / 125 μm fibers are bent within 2 mm of height by modifying the ferrule and by using special fibers (GGP fibers from [25]). The performance of the transmission line has been measured to remain stable while the attenuation at each deflection lies below

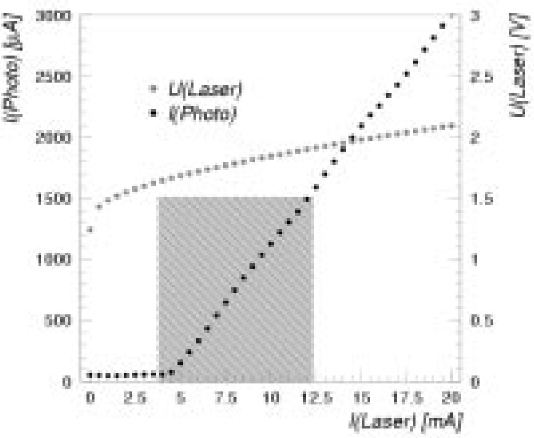

Figure 7. Output power ($\sim I_{\mathrm{Photo}}$) and characteristic curve (U_{Laser}) of a VCSEL diode. The shaded area marks the working range.

2.1 ± 0.9 dB. On the DeHIM side, the fibers are conventionally bent within 10 mm.

Each optical hybrid is embedded in an aluminum casing to provide robustness and handiness, to avoid electrical induction from outside and to shield the VCSEL and PIN diodes from dust. Its outer dimensions are $41 \times 33 \times 6\,\mathrm{mm}^3$. Clamps at the aluminum casing give a proper mechanical connection of the hybrid with the fiber tails of 600 mm length (300 mm at the DeHIM) and prevents outside stress to affect the precise mechanical adjustment of the ferrules to the diodes.

4.4. Optical Cables

In guiding the optical fibers out of the main detector, several aspects have to be taken into account. Safety rules demand that all fibers and the sheathings be halogen–free and inflammable, space constraints require low bending radii of the cables, the CIP and parts of the on–detector electronics should be as easy to maintain as possible and all cables need to have a connection at the *cable distribution area* (CDA) at the backward end of the CIP. For these reasons, the optical transmission line is divided into four parts. Starting at the HIM, its fiber tail is plugged to a 3 m long fiber ribbon cable ending at the CDA. From there, a 36 m cable feeds the signals to the electronics cabin outside the main detector and is connected to the tail firmly attached to the DeHIM casing.

The 600 mm tails, including the 90° bending part, are produced by Schütten Optocommunication [26]. The long distance cables and 300 mm tails are made by Infineon [27]; the short distance cables are from Siecor [28]. The specifications of the cables are listed in Table 2. All cables are assembled with standard MTP connectors (except the ferrule end of the tails) with a typical attenuation of 0.3 to 0.5 dB at each MTP–MTP connection and three connectors per link. Adapters from AMP [29] attach two MTP connectors to another. To obtain a predictable timing between different modules, all cables of each type are chosen to have equal length. Measurements give an average length of 3.12 ± 0.05 m and 36.03 ± 0.15 m,

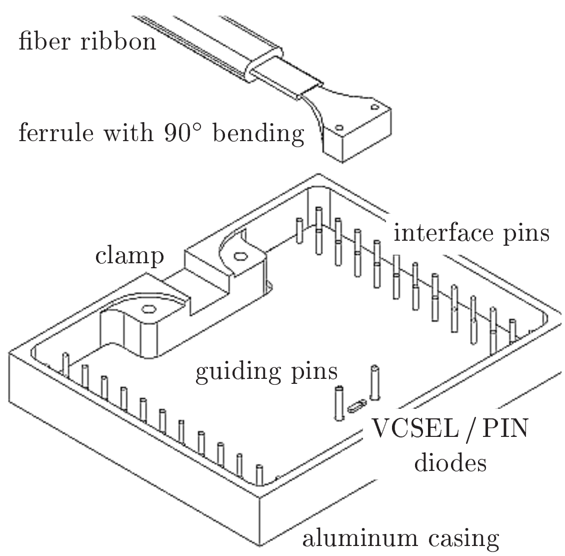

Figure 8. Exploded view of the aluminum casing. Between two guiding pins for the ferrule (enclosing the 90° fiber deflection) are the aligned sixfold VCSEL and twofold PIN diode arrays.

Table 2
Specifications of the fiber ribbons.

Mechanical specifications:	
Fiber count / type	$12 \times 62.5\,/\,125\,\mu$m
Flame resistance	UL-910 (Siecor) LSZH (Infineon)
Dimensions	$< 4.6 \times 2.1\,\mathrm{mm}^2$
Minimum bending radius (long term)	30 mm
Optical specifications:	
Maximum attenuation	4.0 dB/km
Minimum bandwidth	160 MHz × km
Numerical aperture	0.275 ± 0.020

respectively.

5. Receiver Electronics Unit

The receiver unit provides the signals of four adjacent pads, i.e. four successive data words and the EmptyDataSet bits, to the trigger system (Figure 9).

The DeHIM receives the high speed data signals and passes them to the four HDMP 1034 demultiplexers regaining the data words. The demultiplexers are used in the master–slave daisy–chain mode to maintain synchronization of all words, at which anyone of the HDMP 1034 can serve as master. Latches feed the four–fold multiplexed data words and the EmptyDataSet bit with a rate of 41.6 MHz to the backplane that connects the trigger system and the receiver electronics. The incoming global HERA clock signal is received from the backplane and directed via the DeHIM to the on–detector PLL unit. It is also passed to the receiver board's low jitter PLL unit [9] producing the HDMP 1034 reference clock signal. This 41.6 MHz clock signal and the First-Word bit are used in the trigger system for the synchronization of different receiver units.

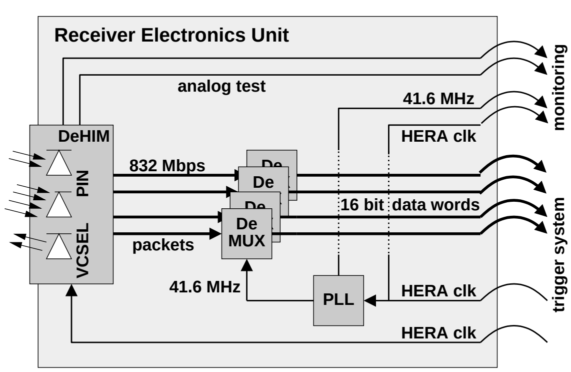

Figure 9. Signal flow of the receiver electronics unit.

The receiver unit board is implemented as a six layer, high density and high speed board with microstrip transmission lines produced by Alwaprint [30]. At the receiver unit's frontplate, the following signals are available for monitoring purposes: the 16 bit data word, the EmptyDataSet bit, the differential analog test signals, the HERA– and the 41.6 MHz clock signal.

6. Performance

The optical link modules will be operated inside the H1 experiment in a 1.16 T magnetic field and only 15 to 20 cm away from the electron beam. Thus they will be exposed to synchrotron radiation and not be accessible from outside without major effort.

Therefore, the modules needed to be tested beforehand for long–term stability, reliability and robustness. Special attention has been paid to the bit–error rate, the transmission of the analog signals and the power dissipation.

Prototypes of the modules have been successfully operated since November 1999. Neither a break–down of any of the used components nor a decrease in the power output of the VCSEL diodes have been observed.

6.1. Link Performance

As soon as the global HERA clock signal is applied, each link module runs autonomously. The PLL unit of the on–detector electronics locks

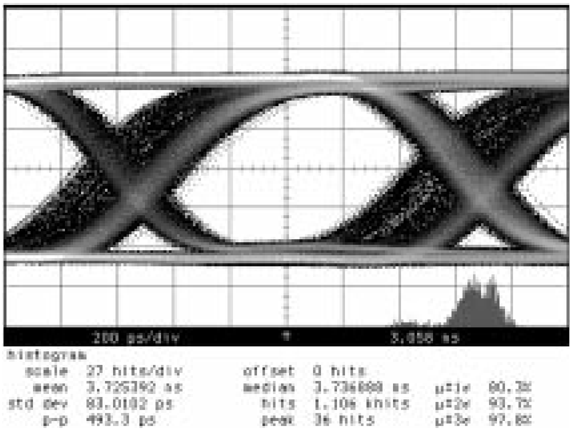

Figure 10. Eye–diagram accumulated from one digital channel and measured directly at the demultiplexer's input. Shown is the digital level ("high" / "low") superimposed for all bits as a function of time. The small histogram gives the jitter. The signal density is given by the greyscale: the lighter the denser.

on the HERA clock signal and distributes the HERA– and 41.6 MHz clock signals to the CIPix chip and multiplexer. After 650 μs the multiplexer has been able to lock on the 41.6 MHz clock signal and the optical link is established. Frequency changes of the HERA clock signal within a window of 8.6 to 11.4 MHz have been proven to be tolerable.

For random data words, i.e. words with 50 % duty cycle, the average light yield has been measured to be -8.7 ± 1.8 dBm at the DeHIM's end of the link after 40 m and three connector pairs. The PIN diodes' high response of typically 63 μA drives the HXR 2004 receiver into saturation, thus noise is suppressed. From the measurement of the bit–error–rate (see below), the lower limit has been estimated to be approximately 15 μA. An eye–diagram of the digital information directly at the demultiplexer's input is shown in Figure 10. The rising and falling edges are well separated. The jitter of the 20 bit packets is about 83 ps. A few percent of the entries shift to earlier crossings, as can be seen in the early sideband of the jitter histogram. The crosstalk between two digital channels and the crosstalk of digital to analog channels lies below -20 dB.

For quantitative tests 16 bit pseudo–random bit patterns were used to simulate the data words at the multiplexer's input. After transmission via the full 40 m link and after demultiplexing, these patterns have been compared with the original input to determine the bit–error–rate. Over a period of ten days, three errors occurred, corresponding to a bit–error–rate below 10^{-14}. This lies far below the tolerated rate of 10^{-9}, i.e. one error per second. All errors could be related to instabilities in the external power supply.

Problems with the synchronization between HDMP 1032 and HDMP 1034 have been seen if the data words imitate the bit pattern of the 16–fold multiplexer's encoding scheme for some hundred periods or if a bit next to an encoding bit is periodical in such a manner that a bit–shift results in another valid encoding bit pattern. In both cases the Clock Data Recovery unit locks on the fake bit pattern instead of the genuine encoding bits. In the operational mode of concern for the H1 experiment, this would require the same pattern of 60 pads of one segment (in a very special arrangement) repeated over many bunch–crossings. This is highly improbable and no reason for concern.

The transmission of the analog signals has been optimized to realize a one–to–one image of the chamber signals. Therefore the amplification of the CIPix chip and of the Maxim drivers in the optical hybrids have been fine–tuned. The peak–time of the analog signal is in the order of 50 ns. From the analog signals, a delay time between CIPix chip input pads and receiver electronics unit frontend of 230 ns has been measured. This is dominated by the delay in the optical fibers of 200 ns. A summary of the specifications of the optical link module is given in Table 3.

6.2. Mechanical Tests

The heat dissipation has been calculated from the measurement of the power consumption of one on–detector unit and gives 6.2 W per module. The total dissipation at the CIP end flange,

Table 3
Specifications of one optical link module.

Optical specifications:	
P_{out} (digital "high")	-3.7 ± 0.8 dBm
P_{out} (digital "low")	-49.1 ± 4.5 dBm
Dynamic range	45 dB
Att. at 90° bending	2.1 ± 0.9 dB
Att. per connector	0.3 . . . 0.5 dB
Crosstalk	< -20 dB
$\langle P \rangle$ after 40 m	-8.7 ± 1.8 dBm
Electrical specifications:	
Jitter HERA clock	43 ps
Jitter 41.6 MHz clk	49 ps
Jitter 20 bit packet	83 ps
	(before HIM: 23 ps)
Delay time	230 ns
	(fibers: 200 ns)
Bit–error–rate	$< 10^{-14}$
Power Dissipation per digital channel	(total 240 channels)
On–detector unit	20 mW @ +3.95 V
	4 mW @ −3.95 V
Receiver unit	13 mW @ +3.3 V
Power Dissipation per analog channel	(total 2 channels)
On–detector unit	110 mW @ +4.4 V
	110 mW @ −4.4 V
Receiver unit	135 mW @ +5 V
	384 mW @ −12 V

i.e. the sum of all 40 modules, is about 250 W, sufficiently low for a water based cooling.

The on–detector electronics has been operated in a magnetic field from 0 to 2 T to simulate the impact of the H1 experiment's magnetic field. The optical output of the VCSEL diodes, the threshold of the CIPix chip, the analog pulse heights, the noise level and the total power consumption of the on–detector electronics have shown no variations within the measurable precision. The jitter of the HERA clock signal remains stable, while jitter of the 41.6 MHz clock signal increases from 49 to 53 ps with a phase shift of 18 ps. Thus no losses in the performance of the optical link due to the magnetic field are expected.

The irradiation at the CIP end flange and thus at the on–detector electronics is estimated to be less than 50 Gy per year [6]. The VCSEL diodes have been irradiated to a flux of about 2×10^{14} neutrons/cm^2, with no measurable change in either threshold or efficiency [31]. After exposure to 200 Gy ± 4 % from a ^{60}Co source, the optical fiber tails and the short distance cables have shown no change in the optical behavior. The same is expected for the 36 m long cables.

6.3. Installation

Forty optical link modules have been successfully installed at the CIP rear end flange in April 2001. All spatial requirements are met. No additional noise has been induced into the liquid argon calorimeter. All modules run autonomously with bit–error–rates well below 10^{-9}. Due to contact problems of the chamber connectors and due to broken bonds at the CIPix chip inputs 0.8 % of all channels are lost. Another 0.9 % inefficiency results from the failure of two VCSEL diodes providing digital signals. For the same reason, one analog channel cannot be monitored.

7. Summary

A fast and compact frontend electronics has been developed to transfer $40 \times 4 \times 832$ Gbps trigger information from the H1 experiment's central inner multiwire proportional chamber to the corresponding trigger system. Forty identical modules have been successfully installed at the chambers end flange and fulfill the tight spatial constraints, while the power dissipation is only about 250 W. The optical transmission has been optimized and is functioning reliably. The bit–error–rate for each module is around 10^{-14}.

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