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Modeling and Performance Evaluation of a Top Gated Graphene MOSFET

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A B S T R A C T

In the modernistics years, Graphene has become a promising resplendence in the horizon of fabrication technology, due to some of its unique electronic properties like zero band gap, high saturation velocity, higher electrical conductivity and so on followed by extraordinary thermal, optical and mechanical properties such as- high thermal conductivity, optical transparency, flexibility and thinness. Graphene based devices demand to be deliberated as a possible option for post Si based fabrication technology. In this paper, we have modelled a top gated graphene metal oxide semiconductor field effect transistor (MOSFET). Surface potential dependent Quantum capacitance is obtained self-consistently along with linear and square root approximation model. Gate voltage dependence of surface potential has been analyzed with graphical illustrations and required mathematics as well. Output characteristics, transfer characteristics, transconductance (as a function of gate voltage) behavior have been investigated. In the end, effect of channel length on device performance has been justified. Variation of effective mobility and minimum carrier density with respect to channel length has also been observed. Considering all of the graphical illustrations, we do like to conclude that, graphene will be a successor in post silicon era and bring revolutionary changes in the field of fabrication technology.

1. Introduction

Scientists have theorized about graphene for years. It has been produced in small quantities for centuries through the use of pencils and other similar graphite applications. With the proliferation of users of modern electronic devices, the condensation of dimensions in Silicon based transistors have countenanced great contraventions as dimension accession atomic sizes and physical limits will be apprehend eventually. Numerous research works has been going on during the lattermost years in search of new materials which can assuage this abridgement. One of the most prominent materials is Graphene which has enticed eminent interest for electronic devices since the demonstration of field-effect carrier modulation [1]-[2]. Graphene, an allotrope of carbon, is a two-dimensional (2D) atomic-scale, hexagonal lattice in which one of the atoms form each vertex. Graphene is a mellifluous monolayer of sp^2 carbon atoms hermetically packed into a two-dimensional (2D) lattice owing to a linear energy dispersion relation [3]. A three-dimensional (3D) layout of honeycomb lattice together with graphene based device is illustrated in Figure 1. Graphene has wrought itself up as a promising material for the next generation high-frequency devices with a view to possessing some of the noteworthy idiosyncratic such as high mobility up to 20,000 $cm^2 V^{-1} s^{-1}$, high saturation velocity, bandgap tunability, and high thermal conductivity etc. [4]-[6]. The operation of transistors fabricated on epitaxial

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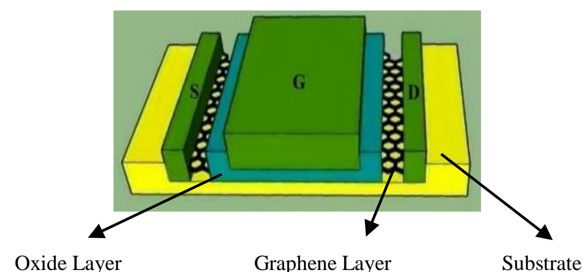

Figure 1. Layout of a Graphene MOSFET

graphene with the current-gain cutoff frequency of 100 GHz has already been executed by the researchers [7]. However, channel length scaling down to only 240 nm could be obtained in these works. Furthermore, newish conveniences for neoteric device applications were generated by ambipolar transport in graphene [8]-[9]. The 2-D geometrical features of graphene equipped it as highly competent with subsisting fabrication technology. In addition to this, the likelihood of a large-scale synthesis of graphene will establish the graphene emerged circuits more feasible historicity in the near future. Thereafter, it is desirable to amplify impenetrable physical model with a view to ameliorating the use of computer-aided design software in order to simulate the complex circuits of upcoming generation [10]-[11]. Hence, it is expected to provide sagacity into the carrier transport in graphene devices. The switching capability between *n* and *p* channel of graphene field effect transistor (GFET) distinguishes itself from other FET technologies [12], where contact resistance comparable to state-of-the-art (SOA) high-speed III–V high electron mobility transistors (HEMT) are demonstrated. The upliftment of GFET devices has been associated by the countenance of electrical models that can be utilized to recount the electrical characteristics of the device, as well as, simulate circuits [13]-[14]. It is seen in [13] that, little unintentional doping of the graphene sample after the top-gate stack deposition which hinders the device of being flawless. In the works of [14], it is observed that, the rise of f_T abruptly diminishes for drain voltages beyond the inflection point of the output characteristics due to the decreasing transconductance and increasing drain conductance. This effect seriously limits the speed performance of GFETs.

In most of the existing physical models of graphene for electrical charge and conduction, the first-principle calculation of tunneling effects, band structures, and carrier transport, however, get the superlative ponderosity [15]-[16]. But, complex numerical calculations are required to find out tunneling current distribution. Furthermore, degeneracy factor needs to be considered in these models. These models are generally superfluous or too perplexed and resource exquisite for modelling of circuits and devices. Graphene MOSFET (G-MOSFET) is one of the greatest aspects regarding the possible solution which can outplay these aforementioned scenarios. Outstanding electronic properties of graphene are leading numerous research works into possible applications of this material in modern nanotechnology devices such as top gated G-MOSFET [17].

An egregious ambridgement remains to be the shortcomings for hermetically packed arrays of nanotubes to attain device performance analogous to silicon FETs, despite field-effect transistors (FET) based on carbon nanotubes being the subject of exquisite research for the last decade [17]- [18]. Some researchers consider Landauer Buttiker's formalism to characterize charge distribution in graphene nanoscroll field effect transistor (GNSFET) and suggest it as a possible replacement of silicon as the next scaled transistor as output current shows good agreement with the experimental results at constant conductance and graphene nanoscale structural parameter [19]. Graphene is not

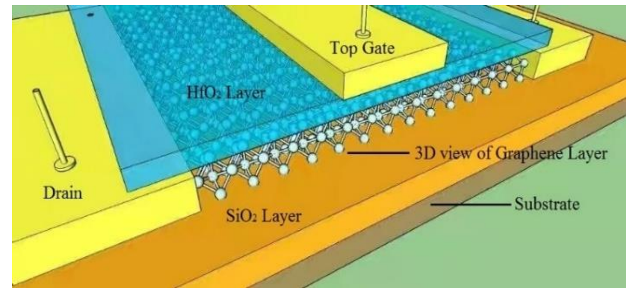

Figure 2. 3D Layout of a Graphene MOSFET

keen on such an assemblage of large parallel arrays and it is capable of designedly being materialized on a full wafer scale. In this paper, a top gated G-MOSFET has been modeled. We have worked on the empirical transistor model with a view to describing transistor operation, as well as, ensuring acceptable accuracy. The variation of quantum capacitance as a function of surface potential has been observed by self-consistent, linear approximation and square root approximation model. Furthermore, the deviation of quantum capacitance in linear approximation and square root approximation is observed. Gate voltage dependence of surface potential, as well as, transconductance have been illustrated in details in the performance evaluation section. Output characteristics and transfer characteristics of the proposed modelling have also been investigated. Later, device output has been investigated with various channel lengths. We also investigated the variation of effective carrier mobility and minimum carrier concentration with respect to the channel length.

The rest of this paper is organized as follows. Proposed model along the mathematical analysis are discussed in Section 2. Section 3 illustrates performance evaluation along with discussions. Finally, conclusions are drawn in section 4.

2. System Modelling

2.1. Device Modelling

Figure 2, shows the 3D layout of a G-MOSFET where the single layer of carbon atoms' arrangement in a honeycomb lattice is illustrated. It is seen that, a 2D single layer of graphene has been disposed onto a Si substrate. This graphene layer works as the channel material which is associated with source and drain. The gate terminal is insulated by an insulating layer of HfO_2. Consequently, an oxide capacitance is evolved there and the charge in the channel can be governed by controlling the gate bias. On the basis of two dimensional electron gas (2DEG) model the quantum capacitance can be represented as [20],

$$C_q = \frac{2q^2 k_B T}{\pi \hbar^2 \upsilon_F^2} \ln 2\left(1 + \cosh\frac{q\varphi_s}{k_B T}\right) \quad (1)$$

where, k_B is the Boltzmann constant, $\hbar$ is the reduced Plank's constant, $\upsilon_F \cong c/300 = 1\times10^8$ cms^{-1} is the Fermi velocity of the Dirac electron and T is the Kelvin temperature. The surface

potential must be set as a function of the gate-source voltage to establish a concise expression for drain current model. The quantum capacitance invades the low surface potential operation. Surface potential can be expressed as [20],

$$\varphi_s = \frac{C_{ox}}{C_{ox} + C_q(\varphi_s)}\left(V_{GS} - V_{CH}\right) \tag{2}$$

The aforementioned expression is transcendental owing to the dependability of φ_s on C_q and vice versa.

2.2. Analytical Approximation of Quantum Capacitance

The quantum capacitance for effectively high surface potentials can be approximated as [21]:

$$C_{q,lin} = 2\xi(Q(\varphi_s)) \tag{3}$$

$$\text{where, } \xi = \frac{q^2}{\pi\hbar^2\upsilon_F^2}$$

Nevertheless, this method disregards the non-zero value of *quantum capacitance* at zero surface potential (Dirac) point.

$$\text{At } \varphi_s = 0;\ C_q = \frac{2q^2K_BT}{\pi\hbar^2\upsilon_F^2}\ln 4 \approx \frac{8.426fF}{\mu m^2} \tag{4}$$

We can take the non-zero charge into account and comprehend the low potential capacitance in a quasi-quadratic mean expression:

$$C_q = C_{qi}\sqrt{1+\left(\frac{q\varphi_s}{k_BT\ln 4}\right)^2} \tag{5}$$

The accuracy of this enhanced model is illustrated in Figure 4. We can now derive the expression of surface potential as a function of the gate voltage with this expedited expression of *quantum capacitance* from equation (5). Let us define $\beta = \frac{C_{ox}}{C_{qi}}, \alpha = \frac{q}{k_BT}\ln 4$. Hence, equation (5) can be rewritten as follows,

$$\varphi_{s,lin} = \frac{\beta}{\beta + \sqrt{1+(\alpha\varphi_s)^2}}\left(V_{GS} - V_{CH}\right) \tag{6}$$

Using Equation (3) the above expression can be linearly approximated to solve for the surface potential as follows:

$$\varphi_{s,lin} = sign(V_{GS})\frac{-\beta \pm \sqrt{\beta^2 + 4\beta\alpha|V_{GS}|}}{2\alpha} \tag{7}$$

However, the solution for our proposed square-root approximation requires a Taylor series expansion as follows:

$$\varphi_s^2\left(\beta^2 + 2\beta\sqrt{1+(\alpha\varphi_s)^2} + 1 + (\alpha\varphi_s)\right) - \beta^2V_{GS} = 0 \tag{8}$$

The solution of Taylor series expansion of equation (8) is:

$$\varphi_s^2 = \frac{-(\beta+1)^2 + \sqrt{(\beta+1)^4 + 4(\beta\ln 2+1)\alpha^2\beta^2V_{GS}}}{2(\beta\ln 2+1)\alpha^2} \tag{9}$$

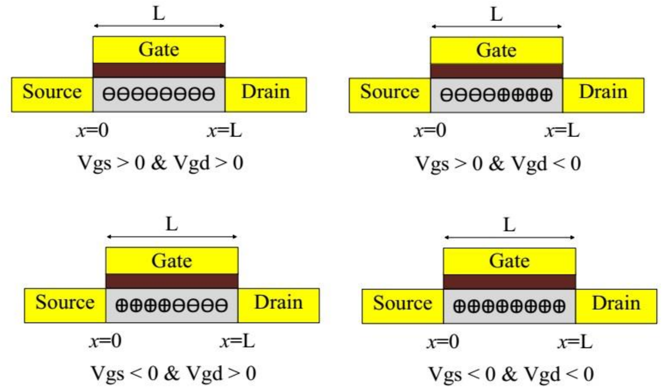

Figure 3: Carrier type in a G-MOSFET channel at 4 different quadrants of the $V_{GS} - V_{GD}$ plane.

2.3. Output and Transfer Characteristics

As the minority carrier deviates from the Dirac point, they can be ignored and majority carriers become dominant. The majority carrier type can be determined depending on the quadrant of the $V_{GS} - V_{GD}$ plane. The type of majority carriers in the G-FET channel can be determined depending on which quadrant of the $V_{GS} - V_{GD}$ plane the device bias is active. The carriers are electrons for $(V_{GS} > 0, V_{GD} > 0)$ both electrons (near the source) and holes (near the drain) for $(V_{GS} > 0, V_{GD} < 0)$ both electrons (near the drain) and holes for (near the source) $(V_{GS} < 0, V_{GD} > 0)$, and holes for $(V_{GS} < 0, V_{GD} < 0)$. The total scenario is illustrated here as follows in Figure 3. The current in the channel can be expressed as follows [23]:

$$I_{DS} = q\frac{W_g}{L_g}\int_0^{Lg} n(x)\,\upsilon_{drift}(x)dx \tag{10}$$

$$\text{where, } n(x) = \sqrt{n_0^2 + \left(\frac{CV(x)}{q}\right)^2} \tag{11}$$

$$\text{and } v_{drift}(x) = \frac{\mu E(x)}{\sqrt[m]{1+\left(\frac{|\mu E(x)|}{\upsilon_{sat}}\right)^m}} \tag{12}$$

where, $n(x), \upsilon_{drift}(x), L_g$ and W_g are the carrier density, drift velocity, channel length, and channel width, respectively. As $dV = E(x)dx$ and $V_{GS} > 0$, $V_{GD} > 0$ in the first quadrant, equation (12) can be rewritten as:

$$I_{DS} = q\frac{W}{L}\int_0^{Lg} n(x)\frac{\mu n(V)}{\sqrt[m]{1+\left(\frac{|\mu n(V)|}{\upsilon_{sat}}\right)^m}}dx \tag{13}$$

The velocity saturation value at average gate voltage is used in the above expression for simplicity. υ'_{sat} can be approximated as follows [23]:

$$\upsilon'_{sat} = \frac{\upsilon_F \zeta}{\sqrt[4]{n_0^2 + \left(C\frac{(V_{GS}+V_{GD})}{2q}\right)^2}} \tag{14}$$

In order to facilitate the equation, the following function is defined as follows:

$$f(a,b) = a\sqrt{1+a^2} - b\sqrt{1+b^2} + \ln\frac{a\sqrt{1+b^2}+b}{b\sqrt{1+b^2}+b} \tag{15}$$

Let us approximate |E(V)| by $V_{GS}-V_{GD}/L$ and define $V'_{GS} = V_{GS}/V_0$; $V'_{GD} = V_{GD}/V_0$ where, $V_0 = Q_0/C$ .Therefore, equation (13) can be written as:

$$I_{DS1} = \frac{\mu_e V_0 Q_0}{\sqrt[m]{1+\left(\frac{\mu_e|V_{GS}-V_{GD}|}{L\upsilon'_{sat}}\right)^m}}\frac{W}{L} f(V'_{GS}, V'_{GD}) \tag{16}$$

In the second quadrant the type of majority carriers change from electrons to holes and $V_{GS} > 0,\ \mathrm{V_{GD}} < 0$

$$I_{DS2} = \frac{\mu_e V_0 Q_0 W}{\sqrt[m]{1+\left(\frac{\mu_e|V_{GS}-V_{GD}|}{L\upsilon'_{sat}}\right)^m} L} f(V'_{GS},0) \quad \frac{\mu_h V_0 Q_0 W}{\sqrt[m]{1+\left(\frac{\mu_h|V_{GS}-V_{GD}|}{L\upsilon'_{sat}}\right)^m} L} f(0,V'_{GD}) \tag{17}$$

In the third quadrant, $V_{GS} < 0,\ \mathrm{V_{GD}} > 0$. Using the same procedure as before

$$I_{DS3} = \frac{\mu_h V_0 Q_0 W}{\sqrt[m]{1+\left(\frac{\mu_e|V_{GS}-V_{GD}|}{L\upsilon'_{sat}}\right)^m} L} f(V'_{GS},0) \quad \frac{\mu_e V_0 Q_0 W}{\sqrt[m]{1+\left(\frac{\mu_e|V_{GS}-V_{GD}|}{L\upsilon'_{sat}}\right)^m} L} f(0,V'_{GD}) \tag{18}$$

and finally, for the forth quadrant, $(V_{GS} < 0,\ \mathrm{V_{GD}} < 0)$ we have

$$I_{DS4} = \frac{\mu_h V_0 Q_0}{\sqrt[m]{1+\left(\frac{\mu_h|V_{GS}-V_{GD}|}{L\upsilon'_{sat}}\right)^m}}\frac{W}{L} f(V'_{GS}, V'_{GD}) \tag{19}$$

The aforementioned equations describe drain current in different quadrants. For all bias conditions, the expression of drain current can be approximated as follows [20]:

$$\begin{aligned} I_{DS} &= I_{DS1}\Theta V_{GS}\Theta V_{GD} + I_{DS2}\Theta V_{GS}\Theta V_{GD} \\ &+ I_{DS3}\Theta V_{GS}\Theta V_{GD} + I_{DS4}\Theta V_{GS}\Theta V_{GD} \end{aligned} \tag{20}$$

Where, $\Theta(x)$ is the step function. In these above expressions, we assume that there is no unintentional charging (doping) in the channel, i.e. $V_{Dirac} = 0$ at low drain voltages $V_{DS} < 1$. Hence, in order to include this effect above equation should be modified by putting $V_{GS} - V_{Dirac}$ and $V_{GD} - V_{Dirac}$ instead of V_{GS} and V_{GD} respectively.

2.4. Transconductance

The convergence of some simulation techniques such as harmonic-balance and transient analysis, requires continuous first and second-order derivatives [23]. Consequently, the model should have continuous high-order derivatives. From the above equations the transconductance can be defined as:

$$g_m = dI_D/dV_{GS}; \quad \mathrm{V_{DS}\ cosntant} \tag{21}$$

Transconductance of the intrinsic device can be approximated in the different quadrants as follows:

$$g_{m_{1,4}} = \frac{2\mu_{e,h}WC}{L\sqrt[m]{1+\left(\frac{\mu_{e,h}|V_{DS}|}{L\upsilon_{sat}}\right)^m}}\left(\sqrt{V_0^2+V_{GS}^2} - \sqrt{V_0^2+(V_{GS}^2-V_{DS}^2)}\right) \tag{22}$$

$$g_{m_{2,3}} = \frac{2\mu_{e,h}WC}{L\sqrt[m]{1+\left(\frac{\mu_{e,h}|V_{DS}|}{L\upsilon_{sat}}\right)^m}}\left(\sqrt{V_0^2+V_{GS}^2} - \sqrt{V_0^2+(V_{GS}^2-V_{DS}^2)}\right) \tag{23}$$

The simplied form maximum transconductance is:

$$g_{m,MAX} = \frac{2\mu_{h,e}}{\sqrt[m]{1+\left(\frac{\mu_{h,e}|V_{DS}|}{\upsilon_{sat}L}\right)^m}}\frac{W}{L}C|V_{DS}| \tag{24}$$

and for high carrier mobility,

$$g_{m,MAX} = 2\upsilon'_{sat}WC \tag{25}$$

This value is acquired from the intrinsic part (without including parasitic drain and source resistances) and therefore it can be considered as an upper limit of the G-MOSFET transconductance.

3. Performance Evaluation

In this subsection, performance evaluation is conducted for our proposed model. We have expressed the surface potential as

a function of the gate-source voltage and quantum capacitance as a function of surface potential. Here a 3 nm HfO_2 top-gate dielectric and zero applied bias i,e, without feeding current into the model has been considered. We have made several approximations for simulating this model such as mobility of electrons & holes are considered equals, absolute room temperature is used, sheet charge density is taken as uniformly distributed. We have neglected the effect of contact resistances, as well as, other parasitic effects (parasitic resistance, parasitic capacitance etc.) However, the parameters used in simulations are summarized in Table 1.

Table 1. System Parameters

Parameters	Value
L (μm)	1
W (μm)	0.5
t_{ox-top} (nm)	3
d_{ox} (nm)	10
n_0 (cm^{-2})	2×10^{11}
$\mu_p = \mu_n$ ($cm^2 V^{-1} s^{-1}$)	7500
C_{ox} (μFcm^{-2})	1.15
υ_F (cm/s)	10^8
T (K)	300

3.1. Surface potential dependence of quantum capacitance

Figure 4 illustrates quantum capacitance as a function of surface potential which is solved self consistently and by both linear and square-root approximation models. Quantum capacitance attains a maximum value of 23.6780 fF/μm^2 in self consistent model for both surface potentials of -0.1 and 0.1 V. At zero potential, it achieves a minimum value of 8.223 fF/μm^2. Maximum quantum capacitances in square root approximation are 25.005 fF/μm^2 at both -1 V and 1 V. Minimum value almost converges to that of actual model. In linear approximation model, maximum value of quantum capacitance is found to be 23.115 fF/μm^2 at both -1V and 1 V. Minimum Quantum capacitance is zero at zero surface potential. For square root model, the model has <10% error for all voltage sweeps, though the minimum error for high voltages is not negligible. As the surface potential increases from Φ_S=0, linear relation resulted from linear density of states (DOS) is clearly observed, which may not be proved by the transport measurement. The deviation from the actual curve near the dirac point is attributed to the charged impurities in the channel. However, this behavior should be studied further. The deviation of quantum capacitance for both linear and square root approximation models from that of actual value are illustrated in Figure 5.

3.2. Effect of gate voltage on surface potential

It is illustrated mathematically in section 2 that surface potential is dependent on gate voltage. For each value of gate voltage, surface potential is obtained self consistently, by linear approximation model and by square root approximation model. From figure. 6 it can be seen that, for each of the cases, at V_{GS}=0, surface potential is also zero. Figure 7 indicates that, at minimum gate voltage (-0.5 V), V_s = -0.12 V, -0.12 V & -0.11 V in self-consistent, linear & square root model respectively. At maximum gate voltage, V_{GS}= +0.5V, the values of surface potential V_s= 0.12 V, 0.11 V & 0.10 V, respectively, in linear, square root and actual model. Figure. 7 shows the deviation of surface potential in linear approximation model and square root approximation model from actual model, which depicts that the later portion is more convergence to the original characteristics.

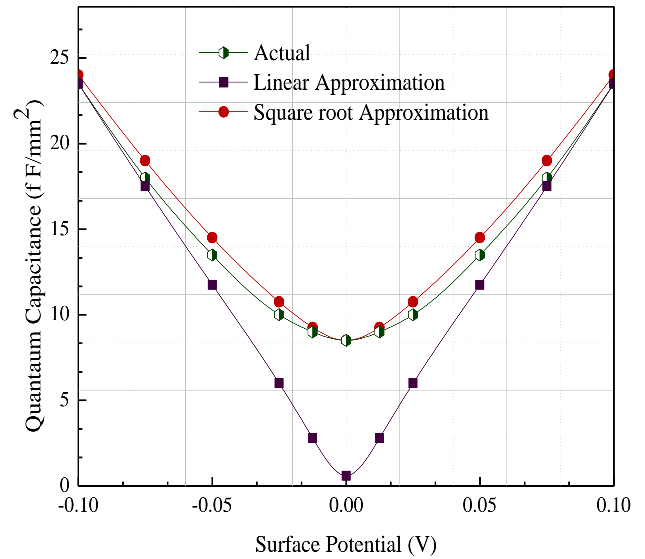

Figure 4. Quantum capacitance as a function of surface potential

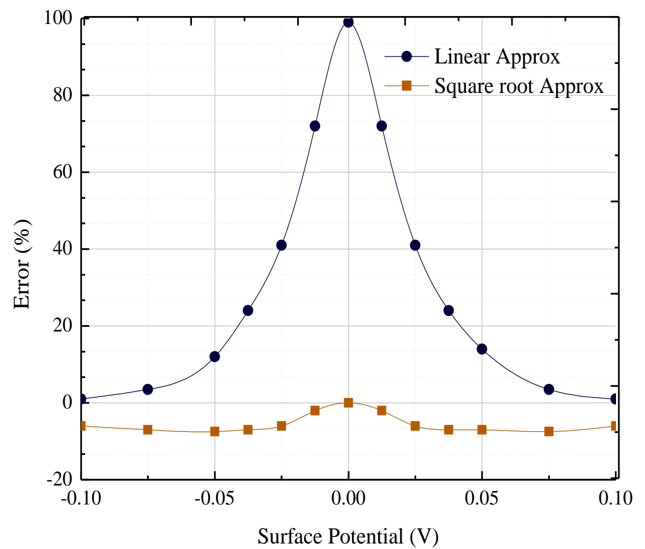

Figure 5. Deviation of quantum capacitance from actual value for both linear approximation model & square root approximation model.

3.3. Output Characteristics

To understand these curves, we focus first on the I_d curve from Fig. 8. for V_{gs-top} = 0.25 V, which shows a pronounced 'kink' in the characteristic similar to the features observed in ambipolar semiconducting nanotubes FET [24], these 'kink's in the I_d characteristics signify the presence of an ambipolar channel. Similar but comparatively smaller 'kink' is also resent

for $V_{gs\text{-}top}$ = -0.25 V. For V_{sd} = $V_{sd\text{-}kink}$, the vanishing carrier density produces a 'pinch-off ' region (Fig. 3) at the drain that renders the current in the channel relatively insensitive to V_{sd} and results in the pronounced kink seen in the I–V characteristic. For V_{sd} > $V_{sd\text{-}kink}$, the minimal density point resides in the channel, producing a pinch-off region that moves from source to drain with increasing drain bias magnitude (Fig. 3.b and 3.c). In this bias range the carriers in the channel on the source side of the minimal density point are holes, and those on the drain side are electrons. The voltage drop across the 'hole' portion of the channel remains fixed at $V_{sd\text{-}kink}$, while the voltage drop across the 'electron' portion increases as V_{sd}–$V_{sd\text{-}kink}$. In this ambipolar regime, the pinch-off

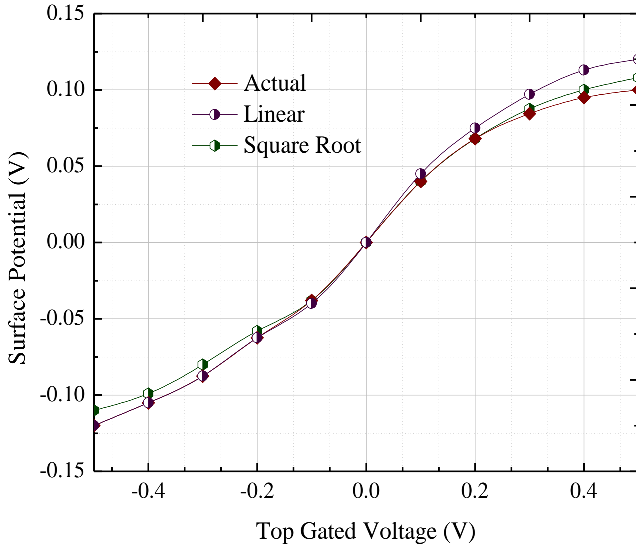

Figure 6. Surface potential vs gate voltage of a graphene MOSFET

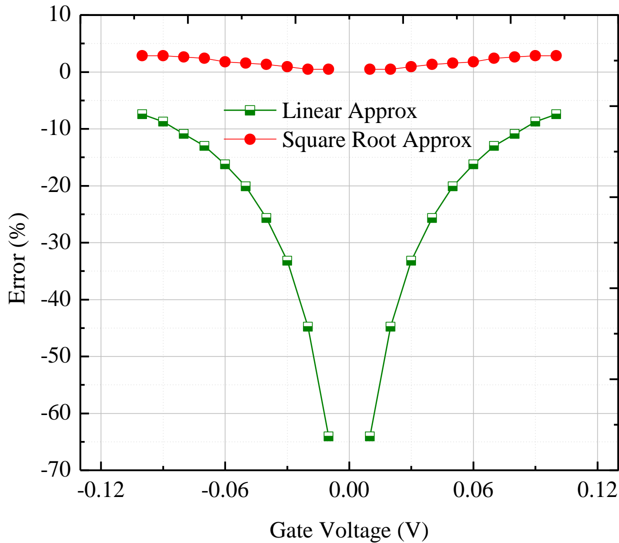

Figure 7. Deviation of surface potential in linear approximation model and square root approximation model from that of actual model.

point becomes a place of recombination for holes flowing from the source and electrons flowing from the drain. As there is no band gap, no energy is released in this recombination. The resulting I-V characteristics are shown in Figure 8. We have extended the analyzed drain to source voltage range beyond the experiment to show the prognostic behavior of the model. The output characteristics set forth a saturation like dispositions. Figure 8 illustrates the change in drain current with the change of drain to source voltage with fixed top gated voltage.

3.4. Transfer Characteristics

A simulated transfer characteristic of I_{DS}-V_{GS} of a top gated G-MOSFET is illustrated in Figure 9. In transfer characteristics curve, G-MOSFET behavior for different values of V_{GS} is investigated keeping V_{DS} fixed. The partial current saturation happens at the gate voltage where the carrier type in the channel starts changing. If V_{GS} increases from its negative value, the

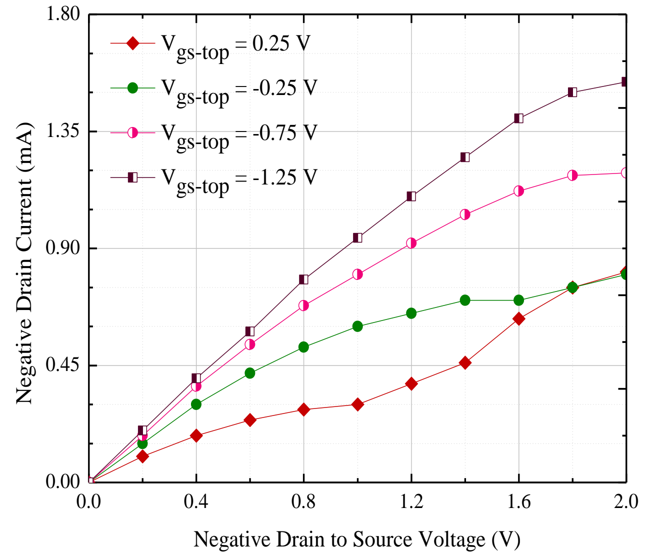

Figure 8. Output Characteristics of G-MOSFET

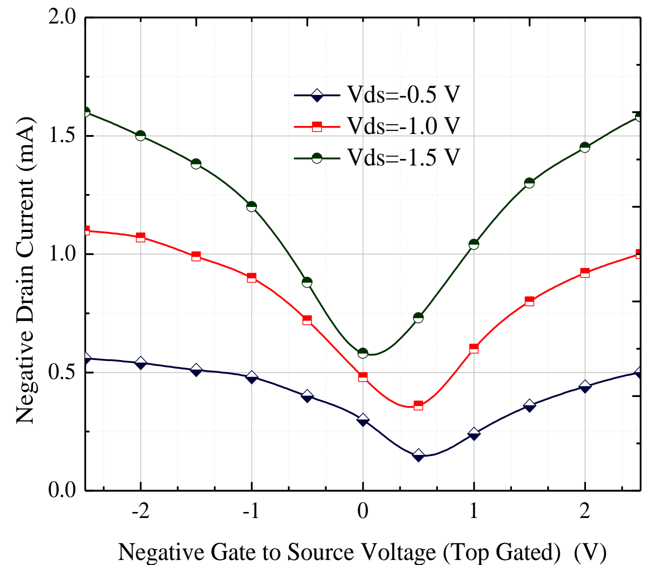

Figure 9. Transfer Characteristics of G-MOSFET

channel potential will be reduced resulting in a smaller hole concentration. The minimum carrier concentration is reached at that point, where V_{CH} is zero. Further increase of V_{GS} would outcome in a negative V_{CH} and therefore electrons would

accumulate and over compensate the diminution of holes. Thus, drain current is found increasing again. Such a characteristic involving both electrons & holes is known as 'ambipolar'. With the increment of negative drain to source voltage the ambipolar characteristics is observed more clearly.

3.5. Transconductance Characteristics

The variation of transconductance with the change of gate voltage is shown in Figure 10. As the gate voltage rises, the transconductance (g_m) changes sign from negative (hole channel conductivity) to positive (electron channel conductivity). The charge neutrality point voltage (V_{CNP}) continues to shift to the

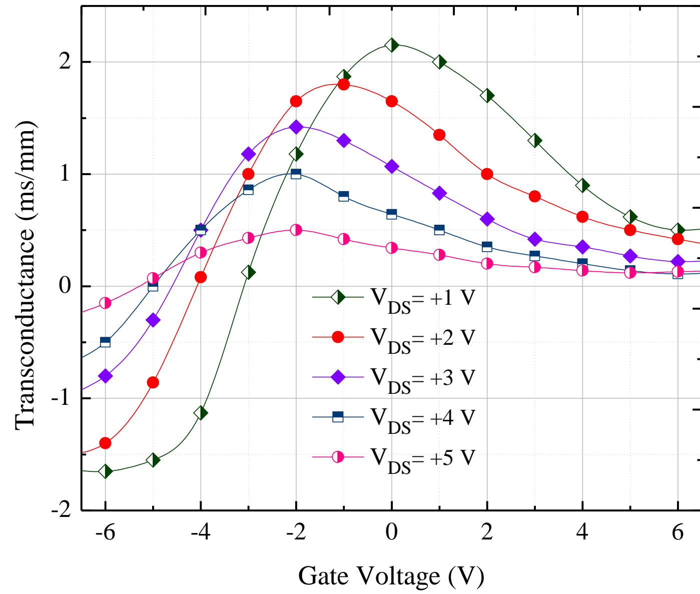

Figure 10. Tranconductance vs Gate voltage of G-MOSFET

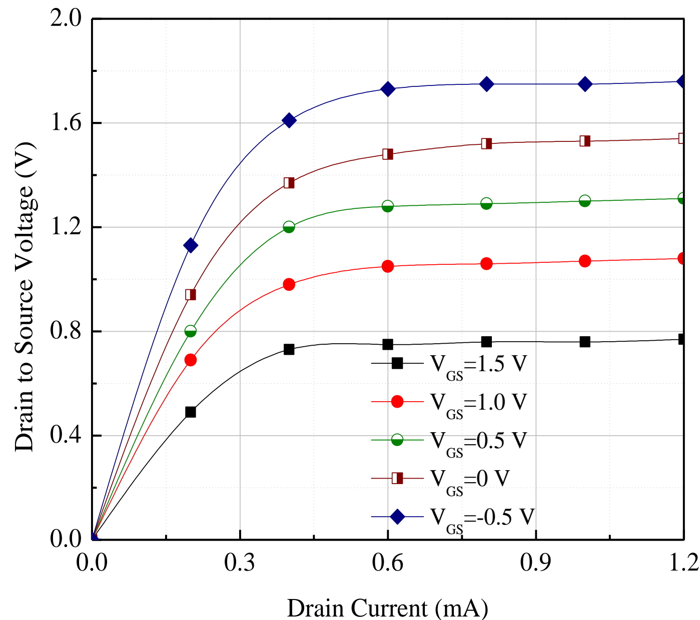

Figure 11. I-V Characteristics with variation of channel length (L=500 nm)

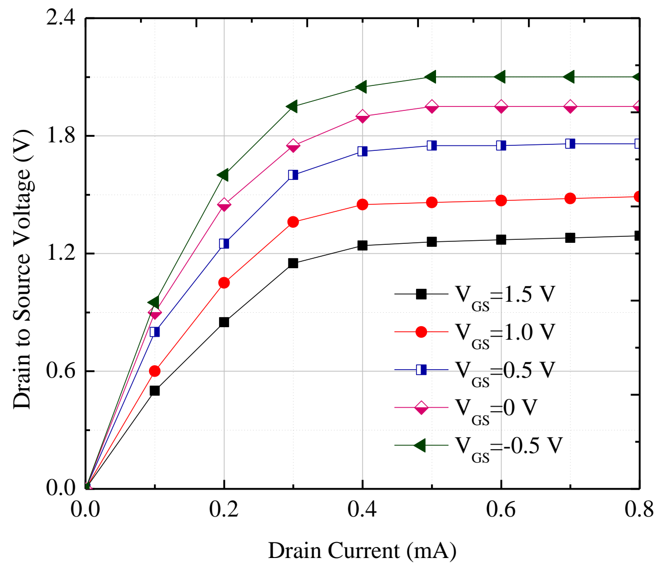

Figure 12. I-V Characteristics with variation of channel length (L=130 nm)

right as the applied drain voltage with $\Delta V_{CNP} \approx 0.5\Delta V_D$. The peak measured transconductance also increased with applied V_D indicating grater carrier concentration in the channel.

3.6. I-V Characteristics with variation of channel length

It is well-known that transport in graphene devices is heavily degraded by charge trapping in the oxide or graphene-oxide interface. This charge trapping is made worse by high drain-source biasing which strongly affects device performance. Figure (fig. 11 & 12) shows I-V measurements at a device size of 500 nm and 130 nm. Strong saturating characteristics are consistently observed in the I-V characteristics. Here the channel length is reduced from 500 nm to 130 nm. The effect of shortening the channel length results a high drain current. It is obvious that, the current is greater for a smaller device. When channel length of 500 nm is considered, a maximum value of drain current of 1.76 mA is obtained. While maximum drain current of 2.1 mA can be achieved by scaling channel length down to 130 nm under the same biasing condition.

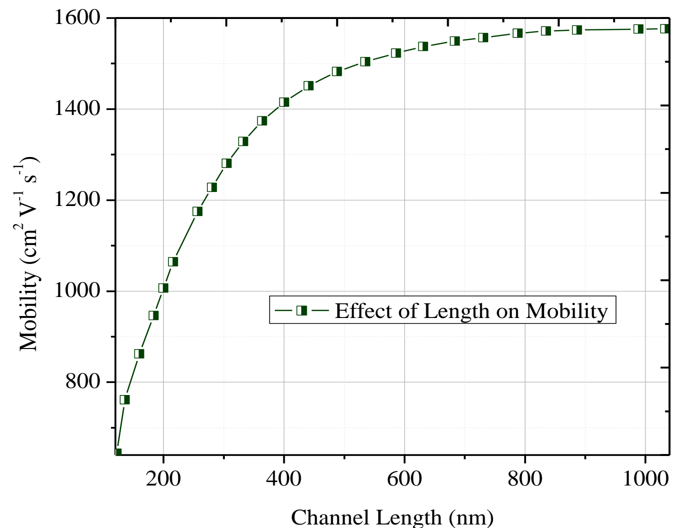

Figure 13. Effect of channel length on mobility

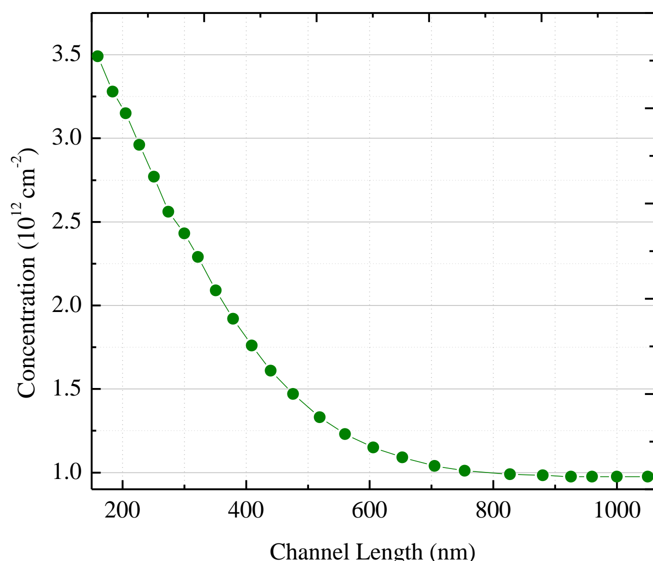

Figure 14. Effect of channel length on Carrier concentration

It is also observed that, the device with shorter channel length goes into saturation more rapidly, thereby, reducing the transit time for the charge carriers, which allows the application of the device in high speed electronics.

3.7. Effect of channel length on mobility and carrier concentration

Figure. 13 & 14 shows the field-effect mobility (μ) and minimum charge-density (n_0) as a function of L, respectively. The effective mobility increases from ~475 cm^2/V sec at 130 nm channel length to ~1615 cm^2/V sec once a channel length of 500 nm is reached. n_0 follows a similar trend, decreasing from ~3.45× 10^{12} cm^{-2} at L = 130 nm to ~0.95×10^{12} cm^{-2} when L = 500 nm is reached. This mobility and impurity concentration variation at short channel lengths may be attributed to a crossover from diffusive to quasi-ballistic transport [25]. However, there is always some scopes of further research for better understandings of the device physics.

4. Conclusion

In this paper, we have modeled and evaluated the theoretical performance of a top gated Graphene MOSFET. We have observed the surface potential dependence of quantum capacitance where surface potential is obtained self-consistently as a function of top gate voltage. The variation of quantum capacitance with respect to surface potential has been obtained using both linear approximation model and square-root approximation model. We also determined the deviation of quantum capacitance in linear approximation model and square root approximation model from that of actual model.

Variation of surface potential behavior with the variation of gate bias is shown in section 3. It is seen that, when gate bias was negative surface potential acquired a negative value with a zero at zero gate bias. When gate voltage was positive, it increases from zero value to some positive value. The output characteristics at a constant gate voltage, as well as, transfer characteristics for a constant drain to source voltage have also been observed. In case of output characteristics, a 'kink' is observed due to transition of charge carriers. Drain current increases linearly then it becomes saturated. In transfer characteristics, when gate voltage increases from a negative value, drain current reduces. At zero gate bias, it becomes partially saturated because a minimum carrier concentration. When gate voltage increases towards positive values, output current tends to rise again revealing the 'ambipolar' behavior of Graphene channel. From the family of curves of transconductance vs gate voltage we observe that after achieving the maximum value, transconductance again tends to fall and goes into partial saturation as the gate bias becomes larger and the channel reaches its saturation. We also evaluated the device performance with channel length scaling. It is found that, with reducing channel length better output could be achieved, but, up to a certain limit. Beyond that short channel effects occurs.

We also determined the effective mobility of charge carriers and minimum carrier concentration in the channel according to channel length. Both illustration yields satisfactory outcomes. Although our works is in embryonic stage, in comparison to others, we can strongly recommend G-MOSFET as a promising candidate for post Si era. As GFETs experiences low I_{on}/I_{off} ratio, opening of band gap in bilayer graphene has made graphene an enduring replacement for semiconductors, specially, in high speed electronics.

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