An Ultra-High Speed Emulator Dedicated to Power System Dynamics Computation Based on a Mixed-Signal Hardware Platform

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***Abstract*—This paper presents an ultra-high speed hardware platform dedicated to power system dynamic (small signal) and transient (large signal) stability. It is based on an intrinsic parallel architecture which contains hybrid mixed-signal (analog and digital) circuits. For a given model, this architecture overcomes the speed of the numerical simulators by means of the so-called emulation approach. Indeed, the emulation speed does not depend on the power system size. This approach is nevertheless not competing against high-performance numerical simulators in term of accuracy and model complexity. It targets to complement the numerical simulators with the advantage of speed, portability, low cost and autonomous functioning. The proof of concept is a flexible and modular 96-node hardware platform. It is based on a reconfigurable array of power system buses called Field Programmable Power Network System (FPPNS). Details on this hardware are given. Two benchmark topologies with, respectively, 17 nodes and 57 nodes are provided. Comparisons with a digital simulator are done in terms of speed and accuracy. The calibration of the system is explained and different applications are proposed and discussed. The promising results of this hardware platform show that the design of a fully integrated solution containing hundreds of power system buses can be achieved in order to provide a low cost solution.**

***Index Terms*—Application specific integrated circuit (ASIC), emulation, mixed analog digital integrated circuits, power system dynamics, power system simulation, power system stability.**

I. Introduction

THE power grid faces many new challenges that it was not designed for and the introduction of renewable energy generation will considerably change its management. First of all, it will provide a bidirectional power flow at the multiple voltage levels of the power grid. Then, the renewable electricity generation is less predictable than that of the conventional method; it leads therefore to a more complex system which must be managed by the power system operators. Finally, the substitution of the major generation center by multiple and distributed production centers will decrease the dynamic stability of the power grid and thus reduce its ability to absorb the kinetic energy after a perturbation.

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A very high-speed system that provides extremely quick decision making from the real-time power system state is therefore needed. It is requested especially for the assessment of the dynamic and transient stability of a given power system. Indeed, the simulation of dynamic/transient phenomenon is computationally much more demanding that steady-state calculations.

Therefore, a system that mixes extremely fast dynamic power system computation and power system optimization will be extremely useful for the dispatching center.

There exist many approaches in order to optimize the economic and ecologic aspects of power systems. Nevertheless, the existing simulators needed to optimize and used by power system operators are currently too slow to be used in a much faster-than-real-time phenomenon for dynamic power system security assessment (PSSA). Indeed, conventional computer architectures (multicore CPU and GPU) suffer mainly from memory access speed limitation [10]. Computation speed of such simulators can be enhanced by means of dedicated hardware architectures. A promising approach based on mixed-signal computation has been developed for addressing this issue [1], [4], [5]. It is based on the so-called phasor emulation (PE) approach [2], [3], [6]. It permits the speed limitation of the digital computation to be overcome by replacing the heavy digital matrix computation necessary to compute the Kirchhoff equation by a reconfigurable array of analog computing. It is then linked to multiple digital processors which solve the generator and load dynamic equations of the system.

This paper is organized as follows. It starts by describing the system architecture developed to provide flexibility and modularity of the analog power system emulator. Then, it presents the architecture of the PE approach and go into the theoretical principles. A set of generators and loads models that can be implemented on the hardware platform are introduced. The mixed-signal hardware platform is presented in detail. The software able to manage the platform is briefly introduced and emulation results of this hardware are provided and validated by comparing with digital reference simulations. Finally, a fully integrated circuit solution that aims to reduce the size of the system and its associated costs is presented.

II. Power System Mapped on a Reconfigurable Array of Nodes

The used concept is based on a modular array of power system nodes. It can be programmed to any power system topology. It is called Field Programmable Power Network System (FPPNS) [1], [8]. Each node can be configured either

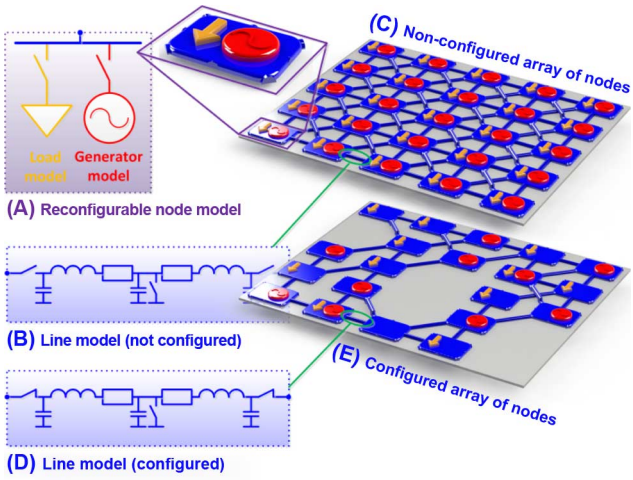

Fig. 1. FPPNS emulation principle.

as a generator, as a load or both. Moreover, such an atom also contains analog reprogrammable components emulating the transmission lines of the power grid. Two stages of computation can be identified: the grid computation and the load, generator models computation. The grid topology is configured through analog switches integrated in the lines model. The switches aim to link nodes together through a line, disconnect lines or creates short-circuit on lines. Fig. 1 shows a single node (A), a reconfigurable line model (B) (D), and the array of nodes (C) (E) to illustrate the FPPNS principle.

In the next section, the advantage of the analog and mixed-signal emulation by means of intrinsic parallelism is explained and compared with the digital computation.

III. Digital Simulation versus Analog Emulation Principles

A. Digital Simulation

The digital simulation of the dynamic and transient stability uses the inverse admittance matrix of the grid in order to link node voltages to injected bus currents that flow in the grid. This matrix equation linking the branch currents and node voltages needs to be computed at each time step when solving a dynamics problem. Therefore, computation time is a square function of the simulated matrix size. Multiple differential algebraic equations (DAE) are also computed at the same time and for each node, in order to simulate the dynamic behavior of the generators and the loads, thus decreasing at the same time the computation speed.

B. Analog Emulation

The analog computation approach of the grid is a mapping between the real grid and the analog emulated grid. Hence the heavy matrix calculation is replaced by an instantaneous analog computation of the grid. Grid emulation can therefore be described as an intrinsic and massive parallel method to compute the grid equations. The PE emulation approach [1] allows the analog computation of both complex currents and complex voltages in the grid by means of analog computation. The complex nature of the grid components is mathematically replaced by separated equivalent resistive networks.

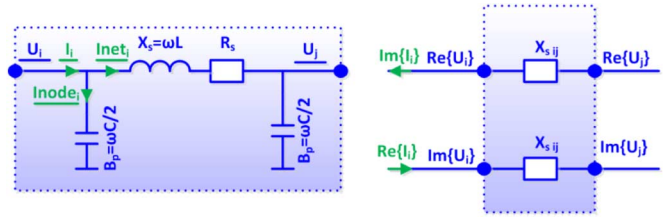

Fig. 2. RLC π-line as modeled in power system transmission line and its corresponding with the PE approach.

C. System Architecture

The architecture of analog emulators can be realized in two ways: using mixed-signal architecture or full analog architecture. In mixed-signal architectures (analog and digital computation) the grid equations are physically computed by means of high bandwidth programmable analog components. Then, the generator and load equations are computed using digital processors. High-speed digital-to-analog converters (DAC) as well as analog-to-digital converters (ADC) allow the linking of analog and digital domains. Such an architecture keeps the same advantage of pure analog computation (computation time is not dependent on the number of nodes). In addition, the complexity and flexibility of the models can be greatly increased with the use of digital processors. Each node contains the necessary interface in order to connect the digital processors. It also contains the programmable blocks which connect each atom together for computing the grid equations analogically. The speed of mixed-signal architecture mainly depends on the DAC and ADC conversion speed [2].

A fully analog architecture means that the overall computation blocks are realized with analog electronic blocks [7]. In a purely analog emulator the computation speed depends on the bandwidth of the analog components that emulate the grid, the generator and the load models [3]. This speed and accuracy limitation is mainly due to the capacitive parasitic effects of the technology used. Therefore, an FPPNS realized with a full analog architecture can be faster than mixed-signal architecture but is much more limited in terms of model flexibility and accuracy. Indeed, a much more intensive calibration process is required before starting a set of emulations. Finally, the design process of a fully integrated and reconfigurable analog emulator is much longer for the same process than for mixed-signal architecture.

In this paper the FPPNS principle has been validated using a mixed-signal architecture and the PE model approach. The next section is dedicated to this model approach.

IV. Phasor Emulation (PE) Approach

A. Grid Model

The PE approach uses a complex representation of voltage and current magnitudes. Fig. 2 illustrates the RLCπ-line equivalent used for transmission branches and its representation with the PE approach.

The relationship that links voltages to currents is given by the admittance of the grid (1). The real and imaginary parts of the currents are divided into two parts (the serial inductive part and parallel capacitive part):

$$\begin{aligned}\underline{I_i} &= \Re e\{\underline{I_i}\} + j\cdot\Im m\{\underline{I_i}\} \\ &= \underbrace{\sum_{j=1}^{n}\left(\frac{1}{R_{S_{ij}} + j\cdot X_{S_{ij}}}\cdot(\underline{U_i}-\underline{U_j})\right)}_{Inet_i} + \underbrace{(\underline{U_i}\cdot(j\cdot B_{P_{ij}}))}_{Inode_i}. \end{aligned} \quad (1)$$

Multiple and isolated analog networks are realized in order to emulate the complex representation of the π-line model. This mathematical modeling is described in (2) and (3):

$$\begin{aligned}\underline{Inet_i} = &\underbrace{\sum_{j=1}^{n}\left(\frac{R_{S_{ij}}}{R_{S_{ij}}^2+X_{S_{ij}}^2}\cdot\left(\Re e\{\underline{U_i}\}-\Re e\{\underline{U_j}\}\right)\right)}_{Network\ A} \\ &+\underbrace{\sum_{j=1}^{n}\left(\frac{X_{S_{ij}}}{R_{S_{ij}}^2+X_{S_{ij}}^2}\cdot\left(\Im m\{\underline{U_i}\}-\Im m\{\underline{U_j}\}\right)\right)}_{Network\ B}-\cdots \\ &\cdots-\underbrace{j\cdot\sum_{j=1}^{n}\left(\frac{X_{S_{ij}}}{R_{S_{ij}}^2+X_{S_{ij}}^2}\cdot\left(\Re e\{\underline{U_i}\}-\Re e\{\underline{U_j}\}\right)\right)}_{Network\ C} \\ &+\underbrace{j\cdot\sum_{j=1}^{n}\left(\frac{R_{S_{ij}}}{R_{S_{ij}}^2+X_{S_{ij}}^2}\cdot\left(\Im m\{\underline{U_i}\}-\Im m\{\underline{U_j}\}\right)\right)}_{Network\ D} \end{aligned} \quad (2)$$

$$\begin{aligned}\underline{Inode_i} = &\underbrace{\left(\frac{1}{R_{P_i}}\cdot\Re e\{\underline{U_i}\}\right)}_{Network\ A}-\underbrace{\left(B_{P_{ij}}\cdot\Im m\{\underline{U_i}\}\right)}_{Network\ B} \\ &+\underbrace{j\cdot\left(B_{P_{ij}}\cdot\Re e\{\underline{U_i}\}\right)}_{Network\ C}+\underbrace{j\cdot\left(\frac{1}{R_{P_i}}\cdot\Im m\{\underline{U_i}\}\right)}_{Network\ D}. \end{aligned} \quad (3)$$

These networks allow separating the real and imaginary part of the current flowing in the grid. Consequently, the use of purely resistive components becomes possible for emulating the RLC Π-lines building the grid. Hence, this mathematical model is easily implemented using a high resistivity layer of most CMOS submicron processes. When modeling high-voltage transmission lines, the serial resistive part R_S of the Π-line can be neglected with respect to the inductive part X_S. The parallel capacitive shunt X_p of the line is considered as a load and is included in the node model. Therefore, the complex current that flows through transmission lines is directly linked to the complex voltage magnitude the inductive and capacitive part of the line (4), (5):

$$\begin{aligned}\Re e\{\underline{I_i}\} = &\underbrace{\sum_{j=1}^{n}\left(\frac{X_{S_{ij}}}{R_{S_{ij}}^2+X_{S_{ij}}^2}\cdot\left(\Im m\{\underline{U_i}\}-\Im m\{\underline{U_j}\}\right)\right)}_{I_{net}\ A} \\ &-\underbrace{\left(B_{P_{ij}}\cdot\Im m\{\underline{U_i}\}\right)}_{I_{node}\ B} \end{aligned} \quad (4)$$

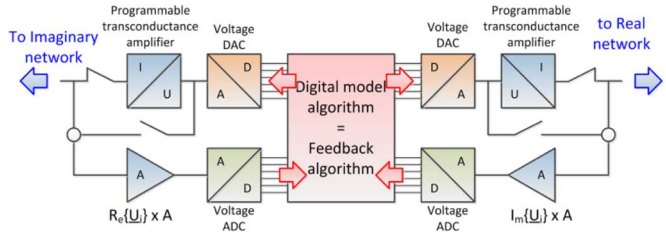

Fig. 3. Interface implementation of the PE mixed-signal approach.

$$\begin{aligned} j\cdot\Im m\{\underline{I_i}\} = &\underbrace{-j\cdot\sum_{j=1}^{n}\left(\frac{X_{S_{ij}}}{R_{S_{ij}}^2+X_{S_{ij}}^2}\cdot\left(\Re e\{\underline{U_i}\}-\Re e\{\underline{U_j}\}\right)\right)}_{I_{net}\ C} \\ &+\underbrace{j\cdot\left(B_{P_{ij}}\cdot\Re e\{\underline{U_i}\}\right)}_{I_{node}\ D}. \end{aligned} \quad (5)$$

Therefore, one ends up with two entirely separated but topologically equivalent networks that are linked together only through the loads and generator nodes.

V. Node Interface Implementation of the Mixed-Signal Phasor Emulation (PE) Approach

Each node is implemented in the same manner and contains the interface that links the digital to the analog computation part (Fig. 3). It can be configured either as a load or a generator model. The interface contains a feedback algorithm able to compute the complex currents or voltages from the complex magnitudes sensed on the node. The implemented algorithm models the electromechanical equations of the generator and the load equations as DAEs. It can also model the shunt susceptance of each node that links the capacitive current to the node voltage.

Now that the theoretical points related to the PE approach and the implementation has been presented, the next section is devoted to describing the power system components modeled in the digital computation part.

VI. PE Approach Generator and Load Models

A. Load Models

The constant impedance load is modeled by injecting complex currents into the node. The currents are related to the admittance and the measured complex voltage of the node. The feedback algorithm is presented in (6):

$$\begin{aligned}\Re e\{\underline{I_{li}}\}_{k+1} &= \Re e\{\underline{Y_{li}}\}\cdot\Re e\{\underline{U_{li}}\}_k - \Im m\{\underline{Y_{li}}\}\cdot\Im m\{\underline{U_{li}}\}_k \\ \Im m\{\underline{I_{li}}\}_{k+1} &= \Re e\{\underline{Y_{li}}\}\cdot\Im m\{\underline{U_{li}}\}_k - \Im m\{\underline{Y_{li}}\}\cdot\Re e\{\underline{U_{li}}\}_k. \end{aligned} \quad (6)$$

The modeling of the *constant power load* also uses complex currents injected into the nodes. The real and imaginary current is related to the constant active and reactive power and the measured complex voltage of the node. The feedback algorithm (3) is as follows:

$$\Re e\{\underline{I_{li}}\}_{k+1} = \frac{P_{li}\cdot\Re e\{\underline{U_{li}}\}_k + Q_{li}\cdot\Im m\{\underline{U_{li}}\}_k}{\Re e\{\underline{U_{li}}\}_k^2 + \Im m\{\underline{U_{li}}\}_k^2}$$

$$\Im m\{\underline{I}_{li}\}_{k+1} = \frac{P_{li}\cdot \Im m\{\underline{U}_{li}\}_k + Q_{li}\cdot \Re e\{\underline{U}_{li}\}_k}{\Re e\{\underline{U}_{li}\}_k^2 + \Im m\{\underline{U}_{li}\}_k^2}. \quad (7)$$

The modeling of the *constant current load* is straightforward and defined by a constant complex current injected into the node. Therefore, this model does not need any feedback.

B. Generator Models

Generator models include the computation of the swing (9). The *classical model* (model 1.0) of the generator can be implemented using the presented interface (Fig. 3). The classical model of the generator needs to compute the active power injected into the grid (8). The power stems from the magnitude of the complex current injected into the node and also from the magnitude of the complex voltage of the node. The validity of the classical generator results is limited to a short time (∼5 s) after a sudden topology change because the internal voltage of the generator is maintained constant. This drawback strictly limits the category of phenomena that can be emulated. The feedback algorithm of the classical model of the generator is as follows:

$$P_e = \Re e\{\underline{U}\cdot\underline{I}^*\} = \Re e\{\underline{U}\}\cdot\Re e\{\underline{I}\} + \Im m\{\underline{U}\}\cdot\Im m\{\underline{I}\} \quad (8)$$

$$\frac{2\cdot H_i}{\omega_0}\cdot\frac{d^2\delta_i}{dt^2} = P_m - P_e \quad (9)$$

$$\Re e\{\underline{I}_{gi}\} = \cos(\delta_i)\cdot\frac{E'}{x'_d} \quad (10)$$

$$\Im m\{\underline{I}_{gi}\} = \sin(\delta_i)\cdot\frac{E'}{x'_d} \quad (11)$$

$\delta = electrical\ generator\ angle\ [rad]$
$H_i = inertia\ of\ the\ generator\ [s]$
$\omega_0 = angular\ frequency\ of\ the\ power\ system\ \left[\frac{rad}{s}\right]$
$P_e = active\ power\ of\ the\ generator\ provides\ to\ the\ network\ [pu]$
$P_m = mechanical\ power\ provides\ to\ the\ generator\ [pu].$

To emulate long-term scenarios, such as stability analysis of voltage and frequency, more advanced generator models are required. This limitation can be removed by using Park's generator model equations. In this more complete generator model, additional phenomena are modeled. More precisely, the classical swing equation (14) is completed by several additional equations: the excitation winding in the direct axis (15), the damper winding in the quadrate axis (16) and the algebraic stator (17) and (18). Note that a further enhancement of the generator model can be achieved by adding controllers such as automatic voltage regulators (AVR) and governors (GOV) [9]:

$$\begin{bmatrix} U_q \\ U_d \end{bmatrix} = \begin{bmatrix} \cos\delta & \sin\delta \\ -\sin\delta & \cos\delta \end{bmatrix}\cdot\begin{bmatrix} \Re e\{\underline{U}\} \\ \Im m\{\underline{U}\} \end{bmatrix} \quad (12)$$

$$P_e = U_q\cdot I_q + U_d\cdot I_d \quad (13)$$

$$\frac{2\cdot H_i}{\omega_0}\cdot\frac{d^2\delta}{dt^2} = P_m - P_e \quad (14)$$

$$\frac{dE'_d}{dt} = \frac{1}{T'_{q0}}\left[-E'_d - \left(x_q - x'_q\right)\cdot I_q\right] \quad (15)$$

$$\frac{dE'_q}{dt} = \frac{1}{T'_{d0}}\left[-E_{fd} - E'_q + (x_d - x'_d)\cdot I_d\right] \quad (16)$$

$$I_d = -\frac{E'_q - U_q}{x'_d} \quad (17)$$

$$I_q = -\frac{E'_d - U_d}{x'_q} \quad (18)$$

$$\begin{bmatrix} \Re e\{\underline{I}_{li}\} \\ \Im m\{\underline{I}_{li}\} \end{bmatrix} = \begin{bmatrix} \cos\delta & -\sin\delta \\ \sin\delta & \cos\delta \end{bmatrix}\cdot\begin{bmatrix} I_q \\ I_d \end{bmatrix} \quad (19)$$

$\mathrm{Re}\{\underline{\mathrm{U}}\}, \mathrm{Im}\{\underline{\mathrm{U}}\} =$ generator or output voltage in grid reference [pu]
$\mathrm{Re}\{\underline{\mathrm{I}}_{\mathrm{li}}\}, \mathrm{Im}\{\underline{\mathrm{I}}_{\mathrm{li}}\} =$ generator or output current in grid reference [pu]
$\mathrm{U_d}, \mathrm{U_q} =$ generator voltage output components in the direct/quadrature axis [pu]
$\mathrm{I_d}, \mathrm{I_q} =$ generator current output components in the direct/quadrature − axis [pu]
$\mathrm{x_d}, \mathrm{x_q} =$ direct/quadrature − axis synchronous reactances [pu]
$\mathrm{x'_d}, \mathrm{x'_q} =$ direct/quadrature − axis synchronous transient reactances [pu]
$\mathrm{E_{fd}} =$ Exciter voltage referred to stator [pu]
$\mathrm{T'_{d0}}, \mathrm{T'_{q0}} =$ direct/quadrature − axis transient open circuit time constant [s].

After having described the implemented models, the next section presents the hardware details of the system.

VII. System Architecture

The hardware architecture is based on two dedicated printed circuit boards (PCBs) shown in Fig. 4 The first board is the mixed-signal board. It contains all the configurable analog components as well as the DAC and ADC converters. The second board is the FPGA board. It contains the digital computation modeling of each node and a high-speed USB communication processor that can communicate directly to any computer. A set of an FPGA and mixed-signal boards can emulate up to 24 nodes and up to 84 branches (Fig. 4). The mixed-signal board is vertically connectable with other mixed-signal boards, enabling an increase of power system topology size. This paper presents the results obtained from a stack of four boards. The system can therefore emulate up to 96 nodes and 336 branches with a 3-D connection possibility. Fig. 5 shows the full hardware platform containing the 3-D connection aspect.

VIII. Mixed-Signal Board Implementation

A. Overview

The mixed-signal board is an array of reconfigurable analog circuits connected to the ADCs and DACs. The converters are connected to the FPGA board through high-speed connectors. Each node holds a DAC interface that provides a configurable

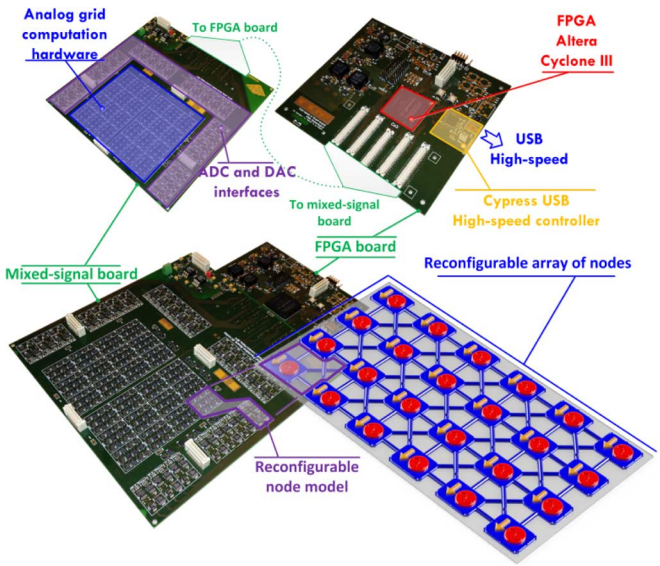

Fig. 4. Hardware platform containing the array of nodes. It contains a mixed-signal board and an FPGA board.

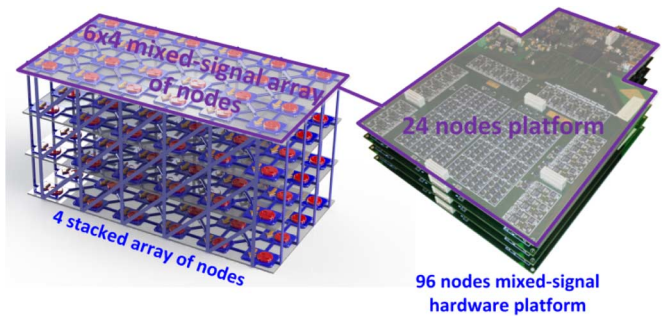

Fig. 5. Stacking of a set of 4 boards for a 96-node power system emulation.

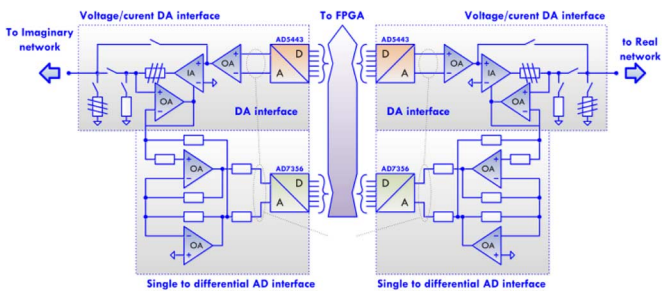

Fig. 6. Implementation of the node interface.

current or a voltage output. The ADC interface contains a single-to-differential voltage interface in order to enhance the signal-on-noise ratio of the system. Indeed, cohabitation between analog signals and high-frequency digital signals needs separation. Therefore, the differential analog pair provides a shielding able to protect the analog signal against digital noise. The 12-bit resolution DAC contains a 50-MHz SPI interface and provides a 2.5-MS/s speed. The dual ADC provides a 12-bit resolution for each node using successive approximation register (SAR) architecture. It operates at 5MS/s using an SPI interface of 110 MHz. Fig. 6 shows the ADC and DAC interface that connects to the node.

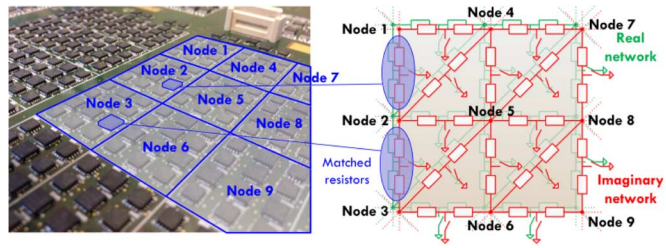

Fig. 7. Resistances matching based on the layout.

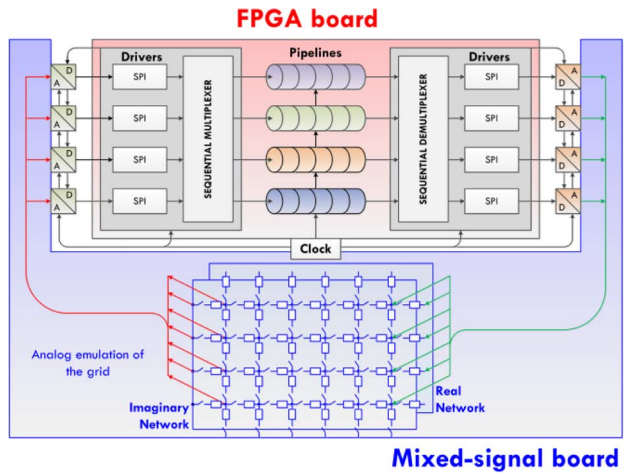

Fig. 8. Architecture of the mixed-signal pipelined computation scheme.

The analog network branch is implemented using multiple 8 bit programmable resistors. A considerable benefit of such components is the large range of linearity when comparing with other techniques like gm-C topologies. As the PE approach is based on two equivalent resistive networks, great attention has been taken in the layout. It aims to ensure that the two resistive networks are equivalent. Therefore the equivalent resistances of both networks are contained in the same package for minimizing the physical variance. This is depicted in Fig. 7.

IX. Load and Generator Digital Computation Scheme

A. Generalities

The digital computation scheme dedicated to the model of the generators and loads is implemented on an Altera Cyclone III EP3C120 FPGA. It solves the DAEs describing the behavior of the generators and the loads at each step (Fig. 8). Computation method is a partitioned scheme for solving the DAE with an explicit method of integration [4].

The need for a high-speed equation solver imposes a particular treatment of data received from the emulated grid. The choice of a pipelined computation [4] is a trade-off between pure sequential computation (time consuming) and pure parallel computation (silicon area consuming). This implementation permits the computation of digital models of up to 24 nodes. The interconnection of multiple sets of boards allows therefore the enhancement of the size of the topology. The developed scheme is highly flexible and easy to debug.

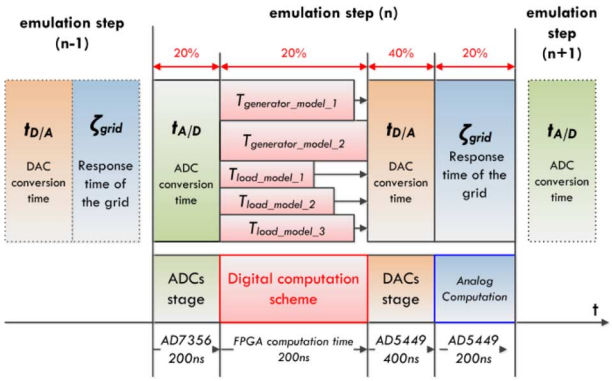

Fig. 9. Timing scheme of one mixed-signal computation step. It contains the ADC conversion stage, the digital computation stage, the DAC conversion stage and the analog emulation response.

B. Computation Speed

The overall system speed is related to multiple computation stages. Indeed, a full mixed-signal emulated step contains the ADC conversion time, the digital computation scheme time, the DAC conversion time and finally the analog emulation time response as depicted in Fig. 9.

The speed of the digital computation stage depends on the implemented topology. Indeed, it is related to the number of generator models implemented as it contains the biggest number of pipeline steps (200 ns for 5 generators per board and 263 ns for 10 generators per board). Nevertheless, this computation time is in the same order of magnitude as the three other stages (DAC, ADC, and analog grid computation). The operating frequencies of physical amplitudes are limited to 1Hz in electromechanical behavior. This corresponds therefore to 1 kHz when emulating 1000 times faster than the time taken by the real phenomena with a time step of 1 ms. A time step of 1 ms is enough for the analyzed phenomena. The bandwidth of the used resistors is 2 MHz and is therefore largely sufficient to operate with this scheme.

C. Pre-Computed Data Operation

Pre-computed data stored in memories (look up tables) is used in order to increase the speed of time-consuming operations related to non-linear expressions. Generator equations contain sine and cosine expressions obtained through this method (10), (11), (12), and (19). The memory depth has been selected to obtain a resolution corresponding to the ADCs and DACs which are the main limitations of the system in terms of resolution. The division operation required by the constant power load equation is obtained using the same concept.

D. Multiple Clock Domains

Multiple clock domains are used in the FPGA architecture. The "fast" clock domain (135 MHz) is used for the pipelined processing unit architecture and parameter saving system. Conversely, the "slow" clock domain (80 MHz) aims to manage the system configuration and the data observation features. The interface between the two domains is provided by the use of a shared dual ports RAM memory.

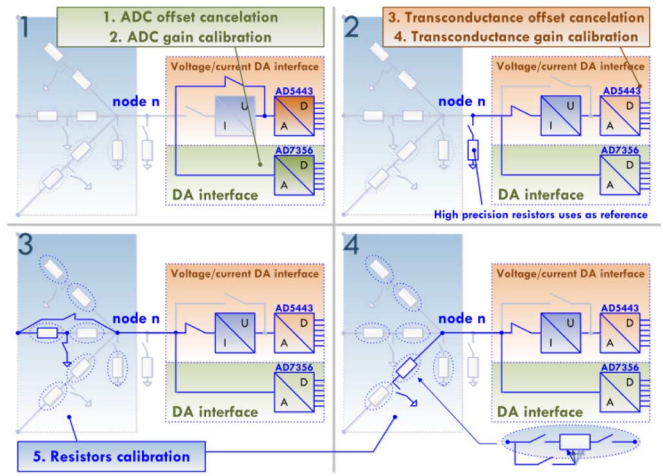

Fig. 10. Calibration process overview. (1) ADC offset and gain. (2) DAC and transconductance offset and gain. (3) Programmable resistors.

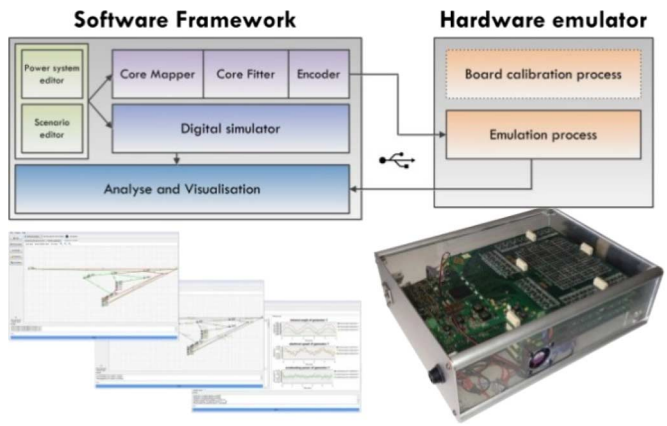

Fig. 11. Software architecture overview.

X. Calibration Process

Mixed-signal computation requires calibration of the analog components before beginning any power system emulation. The calibration methodology is based on the comparison of high-precision components connected to each node used as references. The calibration process (Fig. 10) begins with the ADC offset and gain calibration to establish an accurate reference measure. The offset and gain of the current source is then calibrated. Finally, a binary search algorithm is used for the calibration of every programmable resistor using 0.1% precision resistors as reference.

The full automatic calibration process takes less than 1500 ms per board and only one calibration is necessary before a set of multiple emulations. Calibration is uniquely necessary when hardware temperature as changed.

XI. Configuration and Analysis Software

Dedicated software has been realized for the management, the calibration and the results analysis of the hardware platform (Fig. 11). It contains an easy to use GUI for the power system configuration. The software core contains automatic mappers and a fitter which considerably simplify the emulation configuration process. The mapper core aims to map the power system topology on the 3-D emulator architecture as the fitter

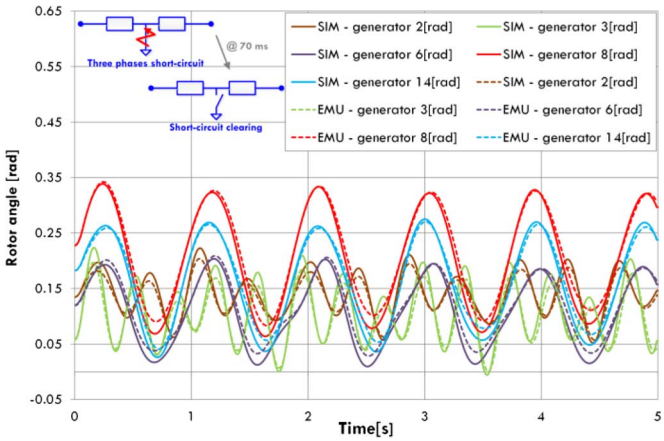

Fig. 12. Comparison between emulated and simulated rotor angles for a three-phase short-circuit (clearing after 70 ms).

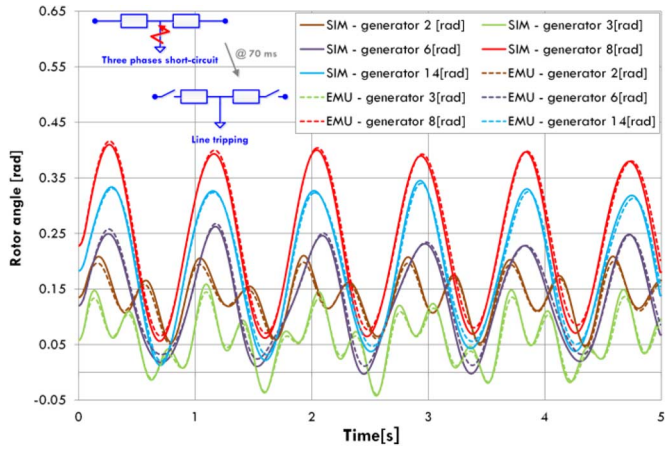

Fig. 13. Comparison between emulated and simulated rotor angles for a three-phase short-circuit (tripping after 70 ms).

core translates the power system parameters into electronic values (resistances, currents, voltages, and gains). The user can choose between digital software simulation and the hardware emulation platform. Finally, visualization and analysis coming from both platforms can be performed.

XII. Comparison of Simulation and Emulation Results for a 17-Node Topology

The proposed mixed-signal architecture is now compared in terms of speed and accuracy with other digital simulators. This simulator has already been validated through EUROSTAG [2]. Different scenarios of comparison based on different topologies are now proposed.

A. Transient Stability Emulation versus Simulation

The first test comparison is based on a 17-bus topology mapped on only one mixed-signal board. This topology contains 6 generators, 8 loads, and 24 branches. The first scenario of comparison is a three-phase short-circuit with a line clearing 70 [ms] after the fault. Fig. 12 illustrates the rotor angles of the generators during the 5 s following the fault.

The second scenario of comparison is applied on the same topology. It also contains a three-phase short-circuit with a tripping of the line after 70 [ms].

As shown in Fig. 12 and Fig. 13, the system provides rotor angle accuracy of less than 0.01 [rad] (0.57 [deg]) during the five seconds after the fault. The speed of the system is 1000 times faster than time taken by the real phenomena with a computation step of 1 [ms]. It takes 5 [ms] for a full emulation of a 5 [s] power system scenario. These results allow the system to be considered for the very interesting applications presented below.

B. Power System Stability Test

The platform allows the user to test the influence of a short-circuit on each branch, one after the other, for a given fault duration. It shows which generator is affected by any instability (loss of synchronism). Based on the same topology as before, stability tests have therefore been realized for short-circuit duration between 100 [ms] and 1000 [ms]. Fig. 14 presents a comparison of the number of unstable cases (at least one generator losing synchronism) for each short-circuit time. Comparisons are done between emulation results and simulation results.

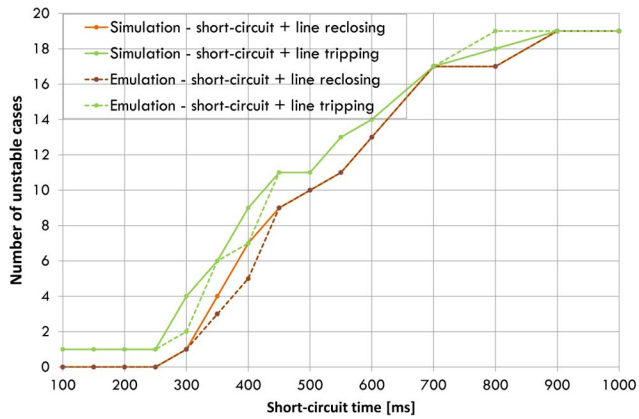

Fig. 14. Comparison between the number of unstable cases for different simulated and emulated short-circuit times. A short-circuit is followed by a reconnection of the line (dark) and subsequent tripping of the line (light).

As shown on Fig. 15, there are some slight differences between emulation and simulation results. This is due to differences between the floating point values of admittance and the corresponding analog components even with calibration. A complete critical clearing time (CCT) analysis shows more precisely these differences.

C. Critical Clearing Time (CCT) Analysis

The platform is also able to perform a binary search algorithm that analyses the CCT of each branch in the topology. A comparison between simulated CCT, emulated CCT and non-calibrated CCT results is shown in Fig. 15. It shows that multiple CCT analysis can be done using mixed-signal emulation. Moreover, calibration enhances the accuracy of the results by reducing the error to within a range of 5% (10% without calibration). Emulation of a 57-node topology is therefore detailed in the next section in order to provide results and trends for a larger network.

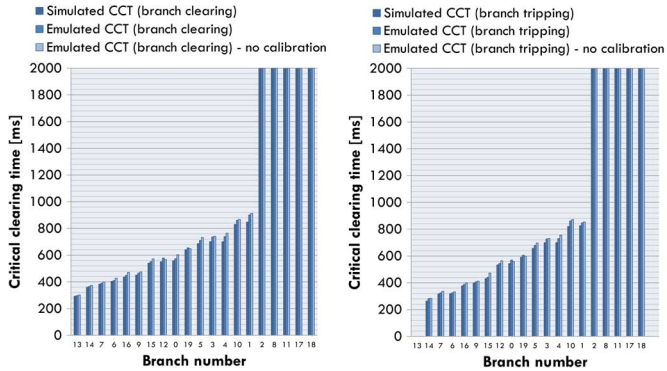

Fig. 15. Comparison between simulated CCT, emulated CCT and emulated CCT without calibration. On the left, the scenario contains the line clearing after the fault. On the right, the scenario contains the line tripping after the fault.

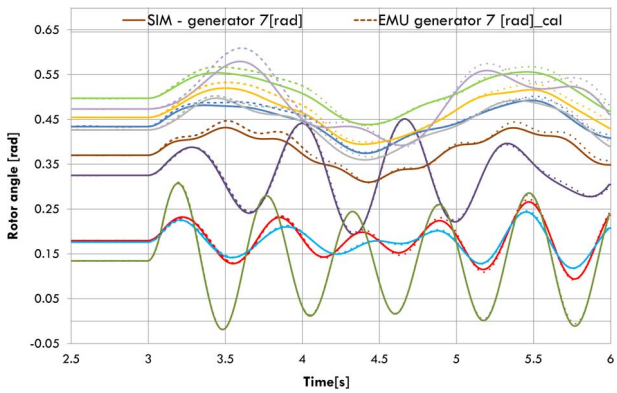

Fig. 16. Comparison between emulated rotor angles and simulated rotor angles for a three-phase short-circuit (clearing after 70 ms).

XIII. Comparison of Simulation and Emulation Results for a 57-Node Topology

As validation, the IEEE 57-node topology [11] has been mapped onto hardware. Fig. 16 shows the comparison between the simulated rotor angle results and the emulated rotor angle results.

Speed of the system is maintained 1000 times faster than the time taken by the real phenomena. Nevertheless, enlarging the size of the power system shows that the accuracy is slightly reduced. Fig. 17 shows the CCT analysis results. It shows that calibration is mandatory before any accurate emulation. Indeed, CCT relative error between simulation and emulation is less than 25% after calibration as it can reach up to 60% before the calibration of the system.

XIV. Further Work

A new integrated circuit has been designed and realized in parallel with this work. It aims to enhance the density, the size of the emulated power system and reduces the cost of the platform. It contains up to 6 nodes on a 16[mm^2] chip area. Speed enhancement targets 2000 times faster than the time taken by the real phenomena. Those chips can be analogically interconnected in order to further increase the number of nodes. The authors intend to follow-up the presented work with the describing and testing of the new integrated circuit (Fig. 18).

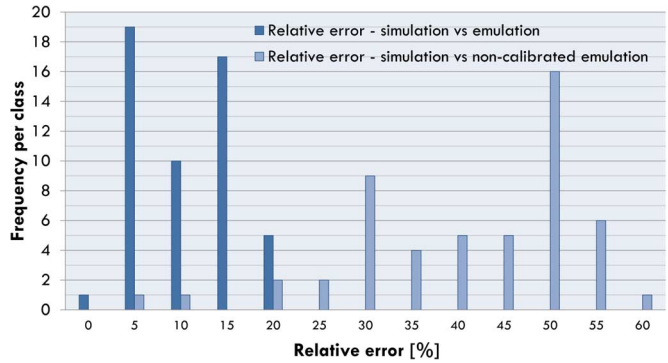

Fig. 17. Results of the relative error between simulated CCT and emulated CCT for the 57-node IEEE power system.

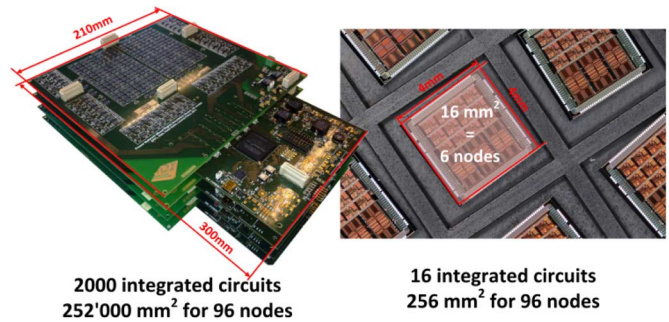

Fig. 18. New ASICs reducing the cost and enhancing the density of the system.

XV. Conclusion

This paper presents an ultra-high speed hardware platform dedicated to compute dynamic and transient power system phenomena. It validates the feasibility of such an emulator for a power system of hundred nodes with a speed enhancement of 1000 times faster than the time taken by the real phenomena. Moreover, it shows that system calibration is essential when increasing the size of the emulated network. A new ASIC that aims to increase the number of nodes has been realised in parallel. Considering the comparison results between standard electronics and integrated circuit electronics [2], the authors predict that a new hardware platform containing up to 600 nodes is possible with an accuracy equivalent to the presented platform.

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