# Survey of FPGA applications in the period 2000 – 2015

**Technical Report** · March 2017

DOI: 10.13140/RG.2.2.16364.56960



**3 authors**, including:

Johannes Romoth
Bielefeld University
**6** PUBLICATIONS **40** CITATIONS

SEE PROFILE

Mario Porrmann
Bielefeld University
**188** PUBLICATIONS **1,718** CITATIONS

SEE PROFILE

# Survey of FPGA applications in the period 2000 – 2015

Johannes Romoth, Mario Porrmann, and Ulrich Rückert
Center of Excellence Cognitive Interaction Technology, Bielefeld University, Germany

***Abstract*—Since their introduction, FPGAs can be seen in more and more different fields of applications. The key advantage is the combination of software-like flexibility with the performance otherwise common to hardware. Nevertheless, every application field introduces special requirements to the used computational architecture. This paper provides an overview of the different topics FPGAs have been used for in the last 15 years of research and why they have been chosen over other processing units like e.g. CPUs.**

## I. Introduction

While FPGAs as a high performance computing platform are still overshadowed by CPUs and in recent years by GPGPUs, they do have an impact in several fields of scientific computing. The three main contributions FPGAs offer are hard real-time computations, parallelism, and a high user I/O pin count, including protocol independent high-speed serial links, which allow the FPGA to be connected to almost every application specific circuit. Over the last 15 years numerous publications have named FPGAs as the main component for their implementation. It is therefore safe to say that FPGAs have evolved from a mainly "glue logic" component, which could also implement some basic Boolean functions [1], to a versatile high performance computing platform.

In this paper IEEE listed scientific publications in the period between 2000 and 2015 were evaluated in order to get an overview of the typical application fields FPGAs are used in. Figure 1 depicts the quantity of all IEEE listed publications up until the year 2015 which are tagged with the keyword "FPGA". Starting in 1989 with just 2 publications, the number slowly increased to 391 in the year 2000. For the next 10 years FPGAs were gaining more and more attention from various research groups. In 2010 a peek in terms of publication quantity was reached with 2906 papers, journal entries and book chapters. Up until today FPGAs have not lost the researchers' interest, although the number of publications has settled down a little compared to 2010. Publications tagged with the keyword "FPGA" all have a different focus on the topic. While most papers show the implementation of various applications on available FPGAs, other publications propose new FPGA architectures or reconfiguration methodologies. This survey takes a closer look on the different applications using FPGAs. To understand why FPGAs were chosen over CPUs, DSPs, or GPGPUs for the specific implementation it is necessary to identify the applications that benefit the most from their usage. Future design decisions can be based on this compiled information when it comes to evaluating if FPGAs are a promising target platform. This counts besides the fact that an ASIC realization is not feasible due to economic reasons.

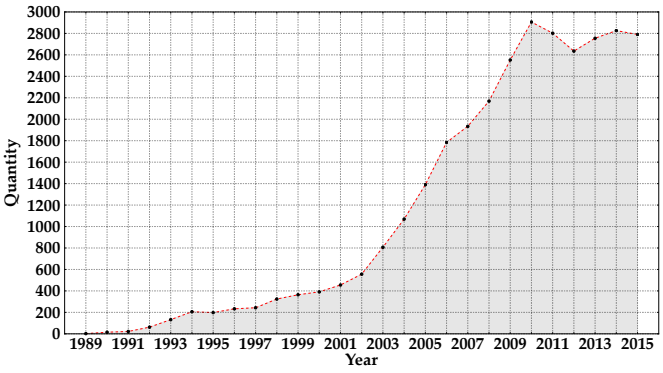


Fig. 1. IEEE listed FPGA related publications per year

The paper is structured as follows. Starting with an explanation and a graphical overview of the distribution of FPGA applications in the reviewed publications, the significant identified fields are introduced. The conclusion sums up the results. All reviewed literature is listed with categorization and keywords in the final section.

### A. Related Work

While [2] includes an overview of application fields for FPGAs and FPGA-cluster, it focuses on giving a general overview of working with this kind of technology and therefore lacks the detail given in this paper.

A more detailed view on the topic is given in [3]. Nevertheless, the main focus of the publication lies in highlighting the differences in the design process, especially comparing the design process of software based systems with the respective FPGA based approach.

Highlighting the use of reconfigurable hardware as a platform for digital controller, the only implementations shown in [4] are from the field of control engineering. Still, the author identifies three main reasons for a technology migration onto FPGAs or similar reconfigurable hardware, namely algorithm acceleration, flexibility, and implementation cost.

The evaluation [5] concentrates on the architectural development and challenges of modern FPGAs. Nevertheless, it confirms the reasons for using FPGAs as a hardware platform given in this survey.

Emphasizing the capabilities of high-level synthesis tools in order to implement new designs or migrate software tasks onto FPGAs, the survey of [6] gives an in-depth overview of the different tools currently available. Although the benefits of using the specific tools to transfer algorithms from different application fields are shown, an evaluation which applications would benefit the most and why is not given.

## II. Application fields of FPGAs

The following 22 application fields were identified during the review. To qualify as a distinctive category there have to be at least two independent publications of two or more different contributing authors. This work does not separate applications targeting single FPGAs from those running on a set of FPGAs or an FPGA-cluster. All application fields identified in the publications listed in the section of *Related Work*, could be verified and are discussed in the following paragraphs. Although some application fields listed could be categorized as subcategories of others, e.g. fuzzy logic as part of control engineering, the authors chose to highlight them separately, since the mechanisms of the implementation or the requirements leading to an FPGA realization differ.

Since the publication count listed in the IEEE Xplore digital library exceeds more than 2000 papers, book articles, journal entries, etc. per year in the recent years, it is impossible to manually analyze all of them. As shown in figure 1 there are some years with higher publication counts than others. Therefore, a random sample of 50 publications for each year has been analyzed, which might result in an over representation of specific topics for the given year, especially when the overall quantity of publications is rather small, like for example in the early 2000s.

The complete list of all categorized papers is given in table I. The distribution presented in figure 2 shows that some scientific areas seem to benefit specifically from the computational functions FPGAs offer. Several implementations can be categorized to more than one application and are therefore visible in all the corresponding vertical bars. Figure 3 gives an overview of the percentage of the application fields in regard to all analyzed publications. For the sake of readability, both figures use the same color encoding.

The three areas communication, image processing, and control engineering benefit in particular from implementing their specific algorithms in FPGAs, with 17%, 15%, and 14% of the total publications respectively. This can also be derived from figure 2 since these three topics show the largest publication count, with only some minor exceptions, in all given years.

### A. Application fields

The following sections will shortly introduce the different application categories and show why the authors have chosen to use FPGAs for their implementation rather than other computing architectures.

*1) Communication:* In order to be used in the hard real-time environment of e.g. software defined radio, complex algorithms like FFT and FIR have to be implemented in the FPGA. Since the continuity of the data stream may not be interrupted, parallel computations of the information allows a much lower clock rate than the actual incoming data rate. Again, like in the relative field of mathematics, DSP hard-macros in modern FPGA technology allow the integration of otherwise distributed computations in a single circuit. This leads to an overall power saving and more adaptable system design.

*2) Image processing:* Typical tasks in image processing are to evaluate single images or multiple frames of a video signal for dedicated criteria like object tracking or depth and movement information extraction. The field of robotics also benefits from the results gained by image processing on FPGAs. The main reason for implementing algorithms in FPGAs is the parallelism which allows e.g. real-time image filtering for pre-processing purposes. The local memory included in modern FPGA architectures enables the buffering of relevant image information in order to minimize the communication with external memories, which can form a potential bottleneck.

*3) Control engineering:* As with fuzzy logic the main contribution FPGAs have to offer is their ability to implement controller as a hard real-time system. Therefore, it is possible to react to any time critical changes in the controlling environment. Another aspect is the possibility to reconfigure the FPGA during run time, which allows an adaptation to a changing environment by choosing the best fitting controller, while reducing the necessary logic resources. Besides monetary savings due to smaller devices, the energy consumption of the complete system can be reduced. In [4] the field of control engineering tasks is further divided into six categories, whereas motor control, power electronics, and motion control form 72 % of the evaluated implementations.

*4) Networks:* Analyzing network traffic without decreasing the overall network performance demands the real-time capabilities that are offered by FPGAs. On the other hand, the energy costs of large configurable switching knots can be reduced compared to CPU based implementations. With the introduction of PCIe hard-macros within the FPGA fabric an integration in a common server infrastructure can be achieved which allows an on-time reconfigurable architecture. The flexibility of FPGAs is the main reason stated for choosing them to implement even uncommon switching behavior, like single to broadcast transmissions.

*5) Cryptography:* Massive parallelism and the possibility to configure the computational units to the bit-width needed are the main reasons for using FPGAs in the fields of both encrypting / decrypting and breaking the encryption of encrypted data. The level of parallelism, especially for brute force dictionary attacks, often exceeds the logic resources of a single FPGA. Clustering multiple FPGAs in one system leads to new high performance computing architectures.

*6) Mathematics:* Dedicated DSP blocks within the FPGA fabric allow the port of mathematical models from CPUs or

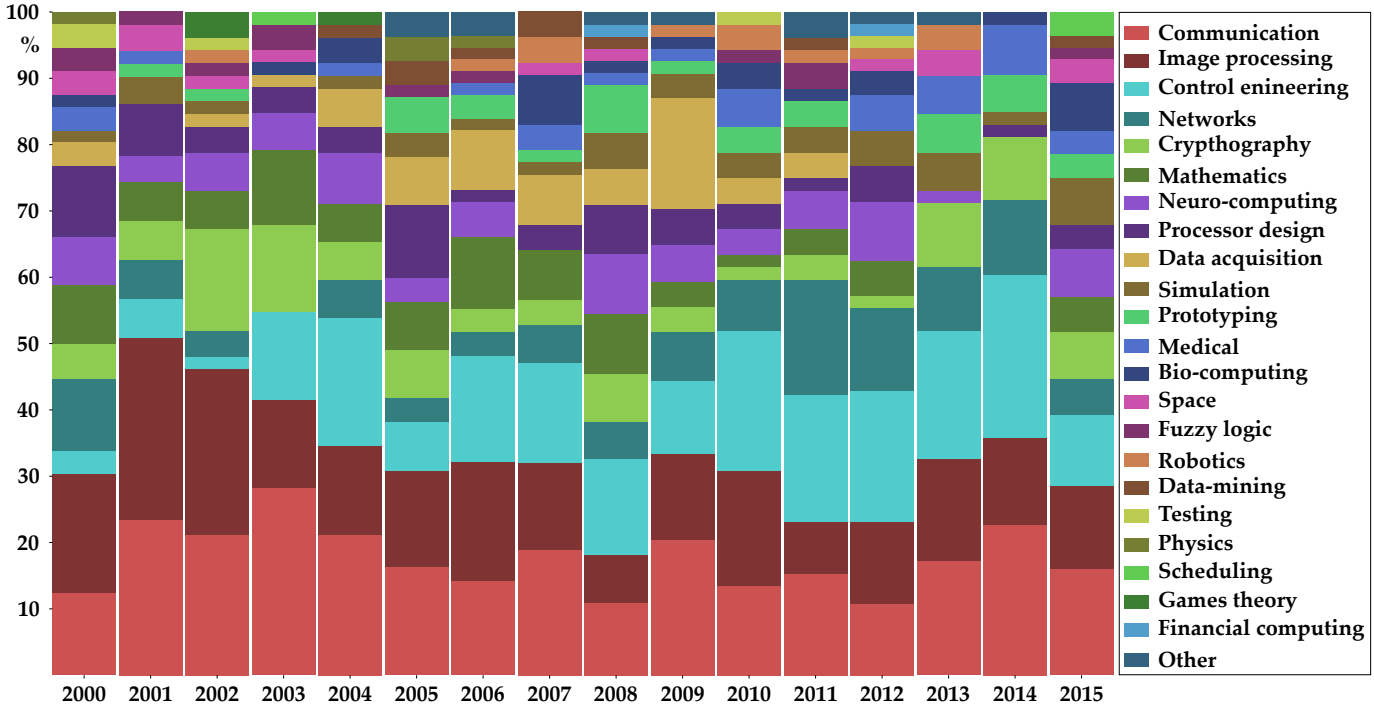


Fig. 2. FPGA applications in the period 2000 - 2015

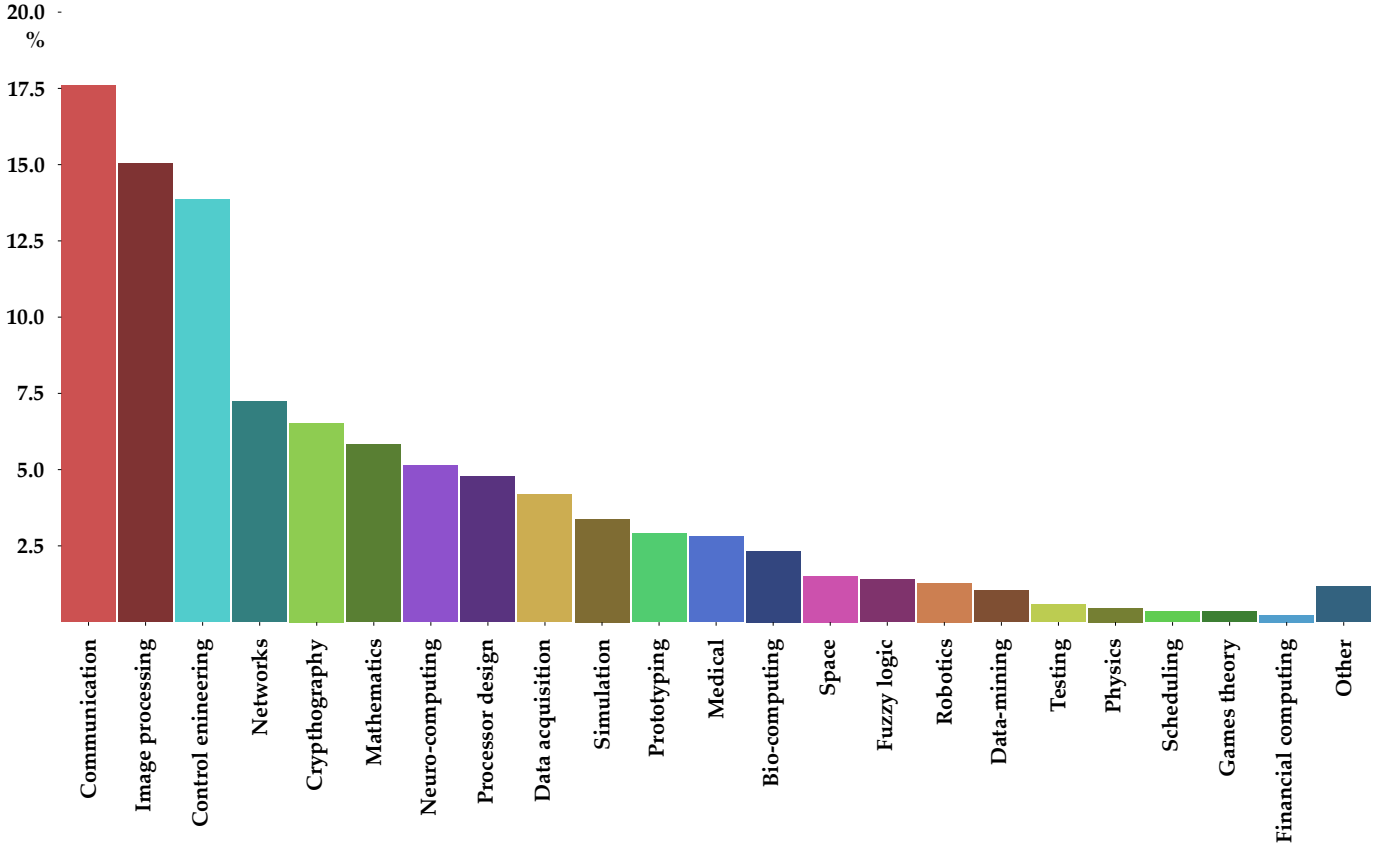


Fig. 3. Distribution of FPGA applications

GPGPUs, although floating point arithmetic is rather complex to implement, vendor and third party tools offer configurable soft macros of various floating point computations. The acceleration of calculations is the most important aspect for the implementation on FPGAs.

*7) Neuro-computing:* Different digital approaches to artificial neural networks benefit from the given parallelism of FPGAs. The memory resources available in the FPGA can be used to implement local independent neurons, which can be connected in various forms. The overall acceleration of the implementation is the main aspect of using FPGAs. Deep-learning currently gains an increased popularity with multinational companies like Microsoft [7] pushing the research.

*8) Processor design:* Using FPGAs as an implementation plattform for processors allows for an highly flexible system design. While discrete solutions necessarily lead to a more complex system, with potential communication bottlenecks between the components implemented in the FPGA and the processor, the integration of a whole specialized or general purpose processor architecture in the FPGA fabric enables a tight coupling of all components. Besides, completely new architecture approaches including different hardware acceleration engines could be evaluated in a closed environment before moving onward to prototyping.

*9) Data acquisition:* Besides configuring, receiving, and transporting data from sources like ADCs, FPGAs themselves can become a part of a sensor setup to acquire information about certain events. E.g. the regular structure of the FPGA fabric allows the creation of high precision time-to-digital converter. Part of the data acquisition can also be the separation of invalid data fragments or the compression of the data to be transmitted in order to use a communication infrastructure with limited bandwidth.

*10) Simulation:* The acceleration through parallelism of large scale simulation is one aspect for the use of FPGAs in this field. A second aspect is the real-time capability when the simulation directly interacts with the surrounding environment, e.g. the implementation of a hardware in-the-loop simulator, which emulates the sensor inputs of a processing unit and reacts to the unit's outgoing signals.

*11) Prototyping:* One of the main application fields for FPGAs right from the start of their usage has been the functional prototyping of future ASICs. Since the design flow of FPGA implementations and ASIC logic description is similar in many aspects, ASIC designs can be translated to a FPGA configuration with only minor adaptations. Therefore, it is possible to examine the functional behavior of the future ASIC although the FPGA design will most likely run at a lower speed. The speed-up gained by implementing the functional prototype compared to software based simulations is the main reason mentioned for using FPGAs in prototyping.

*12) Medical:* Besides the acceleration of the evaluation of acquired data like the surveillance of vital functions, FPGAs are used in medical teaching simulators to generate a real-time response to tactile instruments. Like in control engineering a real-time response to any input is most important for a realistic feedback.

*13) Bio-computing:* Computational challenging tasks like sequencing of genetic structures can be paralleled and therefore accelerated in regard to a single thread computation. A typical task is the characterization of genetic sets. Since this is a data intensive task which can be computed independently from one another, modern FPGA structures with local memory to store the required data directly in the FPGA fabric allow a high level of parallelism.

*14) Space:* In order to ensure a reliable response under harsh radiation conditions, a given design can be triplicated so that errors in the computation can be detected and corrected. Furthermore, the part of the design which produces faulty results can be reconfigured during run-time and therefore recovered to a normal state of operation. Another aspect is the limited power and communication bandwidth on-board of extra terrestrial vehicles, e.g. satellites, which enforces the pre-processing and the compression of the data before the transmission to the ground station.

*15) Fuzzy logic:* The fixed latency during the decision making of the implemented algorithm results in a hard real-time environment and allows therefore the realization of controller tasks. Since the mechanisms of fuzzy logic are completely different from classic control units, fuzzy logic is introduced as a distinctive application field, although both fields might be subsumed as control applications.

*16) Robotics:* The applications in the field of robotics implemented on FPGAs are a collection of tasks from several application fields presented in this paper. Realizations of optical flow systems and tracking of objects based on the data of multiple sensor inputs are the main categories. Like in control engineering, real-time requirements when controlling the movement of the robot were also mentioned as a reason for using reconfigurable architectures. Mobile platforms gain from the reduced power consumption of FPGAs compared to other computational systems. Furthermore, the mechanisms of dynamic reconfiguration are used in order to not only adapt to changing conditions but also to reduce the power consumption without limiting the robot's abilities.

*17) Data-Mining:* Data-mining applications try to identify or extract specific characteristics out of a given large set of data. Like in the field of bio-computing the computational tasks are data intensive and therefore benefit from the parallelism and local memory of the FPGAs. Furthermore, new system architectures combining persistent memories and FPGAs eliminate potential bandwidth bottlenecks. The methods often used include artificial neural networks, which is also an independent application field in this work.

*18) Testing:* Creating stimuli and evaluating the response of a device under test by using an FPGA allow a higher count of tested devices in a given amount of time, compared to software based test setups. The complexity of the test scenario can include the design of a whole system level environment in order to ensure the correct behavior of the tested device. The level of parallelism offered by the FPGAs enables the

generation of multiple test signals with various characteristics, ranging from standard digital commands to complex wave form generation by using PWM signals or controlling external digital-to-analog converter.

*19) Physics:* Accelerating physical simulations by utilizing the parallel FPGA structure is the main application in physics. A typical simulation scenario is particle movement in e.g. fluid mechanics. Besides that, combined data acquisition and pre-processing units are implemented in FPGAs in large scale experimental physical installations. Those units are necessary to process the high amount of incoming data in real-time to ensure that no relevant information gets lost while filtering and compressing the data for further investigations.

*20) Scheduling:* The real-time response to a changing environment is the main reason for using FPGAs in the field of dynamic task scheduling or resource scheduling. High-speed interconnects offered by the IO technology of the FPGAs allow a tight coupling of secondary components to the FPGA. Reducing the workload of a CPU by moving the task scheduling to a FPGA co-processor increases the overall efficiency of the system.

*21) Games theory:* Corresponding to implementations from the field of financial computations, decision prediction at a highly reliable level is a task which can be accelerated by FPGAs. Artificial intelligence implementations for games like Go or Chess benefit from the possibilities FPGAs offer by allowing the parallel computation of multiple variations of the current progress and future scenarios.

*22) Financial computing:* As studies showed that high-performance FPGA systems are more energy efficient, while the precision of a simulation can be adapted to the desired error ratio, the usage of FPGAs also leads to energy savings in high performance computing. Another important argument for using FPGAs in financial simulations and for market prediction is the real-time capability which allows a response with a fixed timing to any observed changes in the stock market.

*23) Other:* Other applications include glue logic functions which benefit from the FPGA's pinout flexibility. The generation of arbitrary wave forms or digital delay lines make use of the reliable signal timing behavior of the FPGA architecture.

## III. Conclusion

This paper demonstrates that the main contribution FPGAs offer to almost all fields of applications is their ability to meet hard real-time requirements, which is supported by their reconfigurable fine granular architecture. This distinctive architecture in regard to CPUs and GPGPUs elaborates the parallelism down to the bit-level of each implementation. While not matching the clock frequencies of the two other ones, FPGAs allow adjustments to the pipelining structure and can therefore easily match up in terms of data throughput.

In topics with a lower publication count the main reason for using FPGAs is to achieve an acceleration of specific computations. Again, the high level of parallelism offered by FPGAs enable applications to gain a significant speed-up, especially in comparison to even modern multi-core architecture CPUs. FPGA implementations are able to achieve or at least get near the degree of speed-up defined by Amdahls law [8].

As the homogeneous configurable logic block matrix paradigm is becoming obsolete with every new generation of FPGAs, more and more applications relying on typical DSP computations have been ported to FPGAs. By introducing hard encoded dedicated macros like multiply-accumulate units and divider units, the problems FPGAs face with floating point computation could be overcome.

Another aspect mentioned in numerous publications is the energy efficiency compared to general purpose architectures like CPUs and GPGPUs. Several applications make direct use of the possibilities introduced through partial reconfiguration to reduce the active chip area in order to minimize the power consumption. Besides that, even high performance computing systems are mentioned to save power when using FPGAs as an additional or exclusive component for computations.

A totally different and therefore noteworthy view on FPGAs comes from the field of space engineering. Although it can be brought down to exploit the parallel architecture of FPGAs, the concept of making excessive use of the ability of partial runtime reconfiguration in order to achieve a fault tolerant system is almost unique in this application field.

## IV. Reviewed Literature

Table I lists all examined research papers used for the comparison presented in this paper. Besides the matching category and the year of publication a brief information on the actual topic is given.

## References


[1] W. S. Carter, K. Duong, R. H. Freeman, H.-C. Hsieh, J. Y. Ja, J. E. Mahoney, L. T. Ngo, and S. L. Sze, "A user programmable reconfigurable logic array," in *Proceedings of the IEEE Custom Integrated Circuits Conference*. IEEE, May 1986, pp. 233 – 235, cited.

[2] R. Tessier, K. Pocek, and A. DeHon, "Reconfigurable computing architectures," *Proceedings of the IEEE*, vol. 103, no. 3, pp. 332 – 354, Mar. 2015, cited.

[3] N. Sulaiman, Z. A. Obaid, M. H. Marhaban, and M. N. Hamidon, "Design and implementation of fpga-based systems - a review," in *Australian Journal of Basic and Applied Sciences 3(4)*, 2009, pp. 3575 – 3596.

[4] C. Paiz and M. Porrmann, "The utilization of reconfigurable hardware to implement digital controllers: a review," in *Industrial Electronics, 2007. ISIE 2007. IEEE International Symposium on*, Jun. 2007, pp. 2380 – 2385, digital controller.

[5] I. Kuon, R. Tessier, and J. Rose, "Fpga architecture: Survey and challenges," vol. 2, no. 2, pp. 135 – 253, 2007.

[6] R. Nane, V. M. Sima, C. Pilato, J. Choi, B. Fort, A. Canis, Y. T. Chen, H. Hsiao, S. Brown, F. Ferrandi, J. Anderson, and K. Bertels, "A survey and evaluation of fpga high-level synthesis tools," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 35, no. 10, pp. 1591–1604, Oct 2016.

[7] J. Qiu, J. Wang, S. Yao, K. Guo, B. Li, E. Zhou, J. Yu, T. Tang, N. Xu, S. Song *et al.*, "Going deeper with embedded fpga platform for convolutional neural network," in *Proceedings of the 2016 ACM/SIGDA International Symposium on Field-Programmable Gate Arrays*. ACM, 2016, pp. 26–35.

[8] G. M. Amdahl, "Validity of the single processor approach to achieving large scale computing capabilities," in *Proceedings of the April 18-20, 1967, spring joint computer conference*, ser. AFIPS '67 (Spring). New York, NY, USA: ACM, 1967, pp. 483 – 485, cited.

TABLE I. Research overview

| Field | Description | Year | Reference |
|---|---|---|---|
| Processor design / Cryptography | Elliptic curve cryptography (ECC) | 2000 | [9] |
| Space / Physics | Event identification and centroiding for a photon counting detector | 2000 | [10] |
| Networks | 64 bit, 66 MHz PCI bus interface | 2000 | [11] |
| Data acquisition | Characters recognition and database word search | 2000 | [12] |
| Image processing | Orthonormal discrete wavelet transforms | 2000 | [13] |
| Communication | Block transmission decision feedback equalizer (DFE) based on Cholesky factorization | 2000 | [14] |
| Control engineering | Space Vector Pulse Width Modulator (SVPWM) for voltage source inverter | 2000 | [15] |
| Medical / Image processing | Image processing for electronic endoscope | 2000 | [16] |
| Cryptography | Data Encryption Standard (DES) encryption algorithm | 2000 | [17] |
| Data acquisition | Radar target detection under jamming condition | 2000 | [18] |
| Mathematics | Parallel/serial wavepipelined (WP) convolver | 2000 | [19] |
| Processor design | Java microprocessor core | 2000 | [20] |
| Networks | Internet protocol (IP) firewall | 2000 | [21] |
| Communication | Multiplierless, narrow transition width FIR filters | 2000 | [22] |
| Communication | Polyphase filter for sample rate conversion | 2000 | [23] |
| Image processing | Parallel Huffman decoder for JPEG and MPEG encoding | 2000 | [24] |
| Simulation | Gaussian noise generator using Box-Muller method for communication channel emulation | 2000 | [25] |
| Mathematics | 2D-discrete cosine transform (DCT) and 2D-inverse discrete cosine transform (IDCT) | 2000 | [26] |
| Processor design | Self-reconfigurable mesh array system | 2000 | [27] |
| Neuro-computing | Cellular Neural Network (CNN) simulator | 2000 | [28] |
| Image processing | Background elimination for scanned text string extraction | 2000 | [29] |
| Fuzzy logic | Fuzzy logic controller for DC/DC converter | 2000 | [30] |
| Image processing | Handwritten-digit recognition | 2000 | [31] |
| Networks | Asynchronous Transfer Mode (ATM) layer functions of an ATM switch | 2000 | [32] |
| Networks | Asynchronous Transfer Mode (ATM) traffic classifier for quality of service management | 2000 | [33] |
| Image processing | Image segmentation | 2000 | [34] |
| Image processing | Iterative image restoration algorithm | 2000 | [35] |
| Mathematics | Distributed arithmetic for DSP algorithms | 2000 | [36] |
| Communication | Signal processing using sigma-delta modulation | 2000 | [37] |
| Test | Re-configurable functional tester for memory chips | 2000 | [38] |
| Space | Demultiplexer for Eutelsat Hot-Bird satellites | 2000 | [39] |
| Networks | IP routing table lookup | 2000 | [40] |
| Mathematics | Bit-level matrix product based on the Baugh-Wooley algorithm | 2000 | [41] |
| Mathematics | General SATisfiability (SAT) problem solver | 2000 | [42] |
| Test | Emulator environment for functional verification of a multimedia processor | 2000 | [43] |
| Networks | Medium Access Control (MAC) transmitter for fiber distributed data interface (FDDI) | 2000 | [44] |
| Fuzzy logic | Fuzzy logic controller (FLC) | 2000 | [45] |
| Processor design / Image processing | Image Processing Coprocessor (IPC) | 2000 | [46] |
| Neuro-computing | Scalar processing and a neural network | 2000 | [47] |
| Neuro-computing | Cerebellar Model Arithmetic Computer (CMAC) modelling using bacterial evolutionary algorithm (BEA) | 2000 | [48] |
| Processor design | Context-free grammar parsing co-processor | 2000 | [49] |
| Neuro-computing | Networked Flexible Adaptable-Size Topology (FAST) architecture | 2000 | [50] |
| Communication | Multiplier-block based FIR filter | 2000 | [51] |
| Processor design / Cryptography | Systolic array architecture for RSA public-key cryptographic coprocessor | 2000 | [52] |
| Communication | Time-multiplexed downlink Rake receiver complying with the IS-95 CDMA standard | 2000 | [53] |
| Image processing | Image compression by Discrete Wavelet Transformations (DWT) and embedded zerotree encoding (EZT) | 2000 | [54] |
| Communication | Full rate and half rate Global System for Mobile (GSM) vocoders | 2000 | [55] |
| Image processing | Video compressor for H.263 | 2000 | [56] |
| Control engineering | PWM signal for a three-phase inverter | 2000 | [57] |
| Bio-computing / Medical | Kidney blood-pressure regulation mechanism model | 2000 | [58] |

| Field | Description | Year | Reference |
|---|---|---|---|
| Networks | Hybrid error code correction counter for telecommunication | 2001 | [59] |
| Control engineering | PWM generator to modulate gating pulses for Insulated-Gate Bipolar Transistor (IGBT) switches | 2001 | [60] |
| Communication | MRC (Maximal Ratio Combine) beamformer | 2001 | [61] |
| Fuzzy logic | Proportional-Differential (PD) fuzzy Look-Up Table (LUT) controller | 2001 | [62] |
| Image processing | H.263 video decoder | 2001 | [63] |
| Simulation | Fault injector for dependability evaluation of VLSI circuits | 2001 | [64] |
| Image processing | Object classification stages of an object detection system | 2001 | [65] |
| Processor design | Discrete wavelet transforms (DWT) coprocessor | 2001 | [66] |
| Communication | Fast Hadamard transforms using Baugh-Wooley multiplication for systolic architecture and distributed arithmetic | 2001 | [67] |
| Processor design | Reconfigurable processor core based on an RISC architecture | 2001 | [68] |
| Mathematics | Moore test for nonlinear equations | 2001 | [69] |
| Image processing | Inverse discrete wavelet transforms based on time-interleaved FIR filters | 2001 | [70] |
| Communication | Residue Number System (RNS) arithmetic for FIR digital filter | 2001 | [71] |
| Communication | $\sigma - \delta$ modulator and demodulator | 2001 | [72] |
| Mathematics | WSAT algorithm to solve boolean satisfiability problems | 2001 | [73] |
| Image processing | Contours extraction utilising a rapid wavelet transforms algorithm | 2001 | [74] |
| Networks / Image processing | MPEG-2 TS (transport stream) generation system with real-time PID filter | 2001 | [75] |
| Image processing | Improved watershed algorithm for image segmentation | 2001 | [76] |
| Communication | Adaptive antenna array receiver on a software radio platform | 2001 | [77] |
| Image processing | Fast Walsh-Hadamard transform using distributed arithmetic | 2001 | [78] |
| Cryptography | Message Diges 5 (MD5) hash algorithm for IPSED | 2001 | [79] |
| Image processing | Separable 2-D biorthogonal Discrete Wavelet Transform (DWT) decomposition | 2001 | [80] |
| Control engineering | Digital protective relays in power distribution system | 2001 | [81] |
| Image processing | Real-time color conversion from RGB to YUV | 2001 | [82] |
| Processor design | FLIX processor extensions | 2001 | [83] |
| Image processing | Frame filter-decimator for the Geostationary Imaging Fourier Transform Spectrometer (GIFTS) | 2001 | [84] |
| Communication | Fast Hadamard transforms using Baugh-Wooley multiplication for systolic architecture and distributed arithmetic | 2001 | [85] |
| Communication | Half-band filter | 2001 | [86] |
| Communication | Pulse-shaping filter for IS-95 Code Division Multiple Access (CDMA) | 2001 | [87] |
| Image processing | 3D laser micro-sensor | 2001 | [88] |
| Networks | Mid-value select architecture (HMVSA) control logic | 2001 | [89] |
| Communication | Non-linear auto-regressive (AR) filter structures for a chaos-based frequency hopping sequence generator | 2001 | [90] |
| Neuro-computing | Hopfield neural network mapped into a 2-D systolic array | 2001 | [91] |
| Communication | Real-time generation of trajectories of chaotic mappings for an FM-DCSK radio transmitter | 2001 | [92] |
| Communication | CRC | 2001 | [93] |
| Image processing | Convolution operation for real-time image processing | 2001 | [94] |
| Medical | Lyon and Mead's electronic cochlea filter | 2001 | [95] |
| Communication | IIR pulse-shaping filter for digital microwave radio | 2001 | [96] |
| Image processing | Real-time video multiplexer and processor for video surveillance | 2001 | [97] |
| Cryptography | Rijndael encryption | 2001 | [98] |
| Image processing | Volterra series based non-linear filters for image interpolation | 2001 | [99] |
| Control engineering | Vector modulation technique for pulse width modulation (PWM) signals for IGBT inverter | 2001 | [100] |
| Processor design | Reduced Instruction Set Computer (RISC) | 2001 | [101] |
| Prototyping | Wavelet transform to the fast fault detection and location on a transmission line | 2001 | [102] |
| Cryptography | Advanced encryption standard candidate algorithms | 2001 | [103] |
| Space | Fault-tolerant adder | 2001 | [104] |
| Mathematics | 2D discrete cosine transform (DCT) | 2001 | [105] |
| Neuro-computing | Toroidal mesh based toroidal neural processor (TNP) | 2001 | [106] |
| Simulation | Fault injector for dependability evaluation of processor-based system | 2001 | [107] |
| Space | Fault-tolerant redundant multistage interconnection network (MIN) | 2001 | [108] |
| Communication | Power estimation of digital filter | 2002 | [109] |
| Image processing | Real-time multi-oject tracking and depth estimation | 2002 | [110] |
| Neuro-computing | Feed-forward neural network | 2002 | [111] |
| Image processing | MPEG-compliant entropy decoding | 2002 | [112] |
| Cryptography | Redundant Residue Number System (RRNS) Quasi-Chaotic (QC) encoder/decoder | 2002 | [113] |
| Cryptography | Elliptic curve cryptography | 2002 | [114] |

| Field | Description | Year | Reference |
|---|---|---|---|
| Image processing | FPGA image co-processor | 2002 | [115] |
| Control engineering | Torsion vibration in a marine engine shaft-gear system | 2002 | [116] |
| Mathematics | Addition and multiply-accumulate blocks | 2002 | [117] |
| Communication | Radix-4 butterflies for HIPERLAN 2 | 2002 | [118] |
| Cryptography | 128 bit Rijndael algorithm | 2002 | [119] |
| Communication | Sample rate conversion subsystems for UMTS (MAX/TC algorithm) and GSM | 2002 | [120] |
| Image processing | H.263 video coder | 2002 | [121] |
| Communication | Cascaded integrator comb filter for software defined radio | 2002 | [122] |
| Simulation | Readback signal generator for hard-drive read channel simulator | 2002 | [123] |
| Prototyping | Microcomputersystem | 2002 | [124] |
| Cryptography | Rijndael algorithm | 2002 | [125] |
| Communication | Chaotic generators based on Lorenz chaotic system | 2002 | [126] |
| Image processing | PAL TV ghost canceller FIR filter | 2002 | [127] |
| Communication | Real-time calibration for digital beamforming | 2002 | [128] |
| Cryptography | Improvement in AES cipher text randomization | 2002 | [129] |
| Cryptography | Ombinatorial multiplier over canonical base GF(16) | 2002 | [130] |
| Image processing | 3D vision for moblie robot positioning | 2002 | [131] |
| Processor design | Fault-tolerant processor by degrading strategy of single cores | 2002 | [132] |
| Image processing | Real-time video processing | 2002 | [133] |
| Image processing | H.263 video coding | 2002 | [134] |
| Cryptography | Microcoded elliptic curve processor | 2002 | [135] |
| Communication | Quadrature direct digital synthesizers | 2002 | [136] |
| Neuro-computing | Multi-layer neural networks | 2002 | [137] |
| Processor design | IEEE-754 FPUs | 2002 | [138] |
| Networks | Data streaming mux and demux with CRC | 2002 | [139] |
| Image processing | Generic shape-based object detection | 2002 | [140] |
| Communication | Turbocodes and Viterbi coding for 8-PSK | 2002 | [141] |
| Communication | (3, k)-regular LDPC code partly parallel decoder | 2002 | [142] |
| Communication | Beamforming | 2002 | [143] |
| Mathematics | Population based ant colony optimization | 2002 | [144] |
| Neuro-computing | Bidirectional associative memory | 2002 | [145] |
| Games theory | Chess movement calculation | 2002 | [146] |
| Communication | Viterbi decoder converting pre-processed speech data into words or sub-word units | 2002 | [147] |
| Image processing | Adaptive genetic algorithm for image enhancement eliminating unknown distortion | 2002 | [148] |
| Test | Error injection System | 2002 | [149] |
| Space | CCSDS compatible command and telemetry collection hardware, BCH error detection and correction, level-0 command capability | 2002 | [150] |
| Image processing | 3D triangle mesh decompressor | 2002 | [151] |
| Games theory | Shogi AI | 2002 | [152] |
| Data acquisition | Parallel and serial parallel correlation using random pulse representation | 2002 | [153] |
| Robotics | Image processing and robotic vision platform | 2002 | [154] |
| Networks / Cryptography | IPSec triple-DES accelerator | 2002 | [155] |
| Fuzzy logic | Fuzzy computation accelerator | 2002 | [156] |
| Image processing | H.263 video coder | 2002 | [157] |
| Mathematics | Irregular computation problem of evaluating y = Ax when the matrix A is sparse | 2002 | [158] |
| Image processing | Iterativer image restoration | 2003 | [159] |
| Control engineering | Stepper motor controller | 2003 | [160] |
| Control engineering | AC/DC converter controller | 2003 | [161] |
| Control engineering | Powerinverter controller | 2003 | [162] |
| Neuro-computing | Pulse density NN using the simultaneous perturbation method | 2003 | [163] |
| Communication | Hebbian Algorithm Eigenfilter | 2003 | [164] |
| Communication | Turbo decoder | 2003 | [165] |
| Image processing | Multidimensional binary morphological image processing | 2003 | [166] |
| Communication | Numerically inverse Laplace transformation | 2003 | [167] |
| Cryptography | Finite field multiplicaiton | 2003 | [168] |
| Communication | Adaptiver Viterbi decoder | 2003 | [169] |
| Image processing | Block truncation code video compression | 2003 | [170] |

| Field | Description | Year | Reference |
|---|---|---|---|
| Neuro-computing / Image processing | Kohonen self-organizing map for digital color still imaging | 2003 | [171] |
| Communication | Canonic sign digit multiplier for adaptive digital filters | 2003 | [172] |
| Neuro-computing | Digital multilayer cellular neural network for 3D nonlinear spatio-temporal dynamics | 2003 | [173] |
| Mathematics | Two's complement serial / parallel multiplication | 2003 | [174] |
| Image processing | Color space conversion for MPEG decoding | 2003 | [175] |
| Cryptography | IDEA block cipher | 2003 | [176] |
| Communication | Genetic algorithm for seperation of wave signals | 2003 | [177] |
| Communication | Transversal filter | 2003 | [178] |
| Data acquisition | ADC data acquistion, compression, and memory rewriting | 2003 | [179] |
| Mathematics | Parallel block-diagonal-bordered for linear equations | 2003 | [180] |
| Cryptography | Block cipher MISTY1 | 2003 | [181] |
| Image processing | Filtering, correlation and transformation of 256x256 Pixel images | 2003 | [182] |
| Control engineering | Fixed-frequency quasisliding control algorithm for N parallel-connected single-phase inverters | 2003 | [183] |
| Cryptography | High and low modulo multiplier for International Data Encryption Algorithm (IDEA) | 2003 | [184] |
| Communication | FIR filter | 2003 | [185] |
| Control engineering | Space vector modulator for a voltage inverter | 2003 | [186] |
| Cryptography | AES encryptor/decryptor | 2003 | [187] |
| Control engineering | Three-phase Inverter power-factor correction PFC | 2003 | [188] |
| Bio-computing | PALM network | 2003 | [189] |
| Mathematics | FFT | 2003 | [190] |
| Mathematics | Discrete Hartley transforms using Booth-encoder-Wallace trees multiplication (MBWM) | 2003 | [191] |
| Processor design | SPIHT for mobile environments | 2003 | [192] |
| Communication / Control engineering | Fixed point recursive least square algorithm MMSE adaptive array antenna | 2003 | [193] |
| Fuzzy logic | Inverted pendulum car | 2003 | [194] |
| Image processing | Video compression using block truncation coding | 2003 | [195] |
| Communication | Multiplier-based complex mixer | 2003 | [196] |
| Scheduling | Fair Weighted Fair Queuing (WF2Q+) | 2003 | [197] |
| Communication | 64-QAM modem | 2003 | [198] |
| Fuzzy logic | Single disk of an ECP torsional plant | 2003 | [199] |
| Cryptography | Random number generation TRNG, BBS | 2003 | [200] |
| Communication | Generic 2D orthogonal discrete wavelet transform | 2003 | [201] |
| Processor design / Cryptography | Single instruction multiple data stream processor for key search | 2003 | [202] |
| Mathematics | 3D-finite-difference time-domain solver | 2003 | [203] |
| Communication / Space | Digital Matched-Filter (DMF) for Low-Earth Orbit (LEO) satellite communication | 2003 | [204] |
| Communication | Two bit error correction based on a modified step-by-step decoding algorithm | 2003 | [205] |
| Mathematics | Systolic array for Singular Value Decomposition (SVD) | 2003 | [206] |
| Communication | Least Mean Square (LMS) adaptive filter | 2003 | [207] |
| Image processing | Discrete Hartley transforms using Baugh-Wooley algorithm for a systolic architecture and distributed arithmetic | 2003 | [208] |
| Medical | Real-time blind source separation of fetal ECG signals | 2004 | [209] |
| Networks | Network intrusion detection system (NIDS) | 2004 | [210] |
| Control engineering | Optimal Total Harmonic Distortion (THD) control algorithm for cascaded H-bridges multilevel converter | 2004 | [211] |
| Communication | Complex sign Doppler estimator for real-time synthetic aperture radar (SAR) Doppler center frequency estimation | 2004 | [212] |
| Games theory | Chess program | 2004 | [213] |
| Communication | Subspace tracker based on a recursive unitary ESPRIT algorithm | 2004 | [214] |
| Networks | Digital transmitter for OFDM based WLAN systems | 2004 | [215] |
| Neuro-computing | TotemNC3003 Twinchip | 2004 | [216] |
| Neuro-computing | Spiking neural network for tangible collaborative autonomous agents | 2004 | [217] |
| Bio-computing | DNA sequence matching processor | 2004 | [218] |
| Control engineering | Dead time compensation for SVM inverters | 2004 | [219] |
| Mathematics | QR decomposition based recursive least squares (RLS) algorithm | 2004 | [220] |
| Communication | Interpolator and control mechanism for arbitary resampling | 2004 | [221] |
| Image processing | Real-time video smoothing | 2004 | [222] |
| Networks | Intermediate frequency transceiver for OFDM-based WLAN | 2004 | [223] |

| Field | Description | Year | Reference |
|---|---|---|---|
| Cryptography | Camellia encryption algorithm | 2004 | [224] |
| Image processing | 3D median filtering using word-parallel systolic arrays | 2004 | [225] |
| Communication | Blind source separation for audio signals using independent component analysis (ICA) | 2004 | [226] |
| Control engineering | Sliding-DFT based power-line phase measurement algorithm | 2004 | [227] |
| Control engineering | PID controller as distributed arithmetic | 2004 | [228] |
| Image processing | Real-time image feature extraction using gray level cooccurrence matrix | 2004 | [229] |
| Communication | Parallel and nonparallel stack filters | 2004 | [230] |
| Control engineering | Multilevel modulator for H-bridge-based converter | 2004 | [231] |
| Communication | Adaptive processing of noisy signals for target detection based on Constant False Alarm Rate (CFAR) algorithms | 2004 | [232] |
| Image processing | JPEG2000 MQ-decoder and arithmetic decoder | 2004 | [233] |
| Communication | Kalman band pass sigma-delta filter for FM demodulation | 2004 | [234] |
| Processor design | IEEE-754 single precision exponential unit | 2004 | [235] |
| Image processing | JPEG2000 decoder | 2004 | [236] |
| Image processing | Template tracking | 2004 | [237] |
| Communication | Distributed arithmetic multiplier-free FIR adaptive filter | 2004 | [238] |
| Control engineering | Rotor position estimator | 2004 | [239] |
| Communication | Digit-serial N-tap FIR filter with programmable coefficients | 2004 | [240] |
| Image processing | JPEG2000 MQ-decoder and arithmetic decoder | 2004 | [241] |
| Control engineering | Automated rail transit train controller | 2004 | [242] |
| Mathematics / Cryptography | Modular multiplication and inversion/division for Elliptic Curve Public Key Cryptosystems (ECPKC) | 2004 | [243] |
| Control engineering | Railway interlocking safety system | 2004 | [244] |
| Communication | Space-time block coder | 2004 | [245] |
| Data acquisition | Four channel data acquisition for for high resolution spectroscopy | 2004 | [246] |
| Data acquisition | Radio astronomy data acquisition with accurate time tagging | 2004 | [247] |
| Control engineering | Motion control system with load decoder | 2004 | [248] |
| Neuro-computing | Self-organizing map neural network for classification of vigilance states in humans EEG signals | 2004 | [249] |
| Communication | Distributed arithmetic multiplier-free FIR adaptive filter | 2004 | [250] |
| Bio-computing | Bat inspired biomimetic cochlear model | 2004 | [251] |
| Cryptography / Processor design | symmetric-key and message authentication co-processor | 2004 | [252] |
| Mathematics | Modulo M multiplication-addition | 2004 | [253] |
| Control engineering | Permanent magnet AC (PMAC) motor controller | 2004 | [254] |
| Data-Mining | Independent component analysis for dimensionality reduction in hyperspectral image | 2004 | [255] |
| Neuro-computing | Probabilistic neural network (PNN) for a bioelectric human interface | 2004 | [256] |
| Data acquisition | Data filtering and compression for a ultrasonic measuring system for pipelines | 2004 | [257] |
| Simulation | Received signal generator for a 44 MIMO transmission | 2004 | [258] |
| Communication | Parity-check convolutional decoders | 2005 | [259] |
| Communication | Structured binary (arary) Low Density Parity Check (LDPC) codes | 2005 | [260] |
| Image processing | 2-D shift-variant convolvers | 2005 | [261] |
| Communication | CDMA source coding and modulation | 2005 | [262] |
| Prototyping | Digital signal processing systems | 2005 | [263] |
| Communication | Parity sharing Reed Solomon codecs | 2005 | [264] |
| Other | Tri-state based shifters | 2005 | [265] |
| Processor design | Floating-point computation environment for SoCs | 2005 | [266] |
| Communication | Irregular Low-Density Parity-Check (LDPC) | 2005 | [267] |
| Image processing | Particle graphics simulations for real-time panicle graphics in video games | 2005 | [268] |
| Mathematics | Greedy algorithm for set covering | 2005 | [269] |
| Neuro-computing | Neural networks controller | 2005 | [270] |
| Other | Time-multiplexing of signal using selectable digital delays | 2005 | [271] |
| Communication | Viterbi decoder for wireless LANs | 2005 | [272] |
| Networks | CAN controller | 2005 | [273] |
| Communication | Evolutionary Digital Filter (EDF) | 2005 | [274] |
| Image processing | Multiplierless JPEG compressor for gray scale images | 2005 | [275] |
| Data acquisition / Physics | Off-shore readout system of the ANTARES neutrino experiment and CMS electromagnetic calorimeter at LHC | 2005 | [276] |
| Control engineering | Control for power converters | 2005 | [277] |
| Cryptography | ”PYRAMIDS” block cipher | 2005 | [278] |

| Field | Description | Year | Reference |
|---|---|---|---|
| Image processing | 2-D shift-variant convolvers | 2005 | [279] |
| Cryptography | AES-128 Encryption | 2005 | [280] |
| Mathematics | Higher radix floating-point computation | 2005 | [281] |
| Data acquisition | Real-time sensor fusion for automotive safety systems | 2005 | [282] |
| Simulation | Emulation test bed for powerline channels | 2005 | [283] |
| Data acquisition | Pulse-height analyzer for high resolution X-ray spectroscopy | 2005 | [284] |
| Mathematics | CORDIC algorithm for circular and linear coordinates | 2005 | [285] |
| Image processing | Image segmantation using logarithmic arithmetic for computer vision | 2005 | [286] |
| Communication | Kalman band-pass sigma-delta ($\sigma - \delta$) demodulator | 2005 | [287] |
| Cryptography | Rijndael AES encryption | 2005 | [288] |
| Neuro-computing | Interface to cellular nonlinear networks | 2005 | [289] |
| Simulation / Physics | Lattice quantum chromodynamics simulation | 2005 | [290] |
| Processor design | Intermediate code to machine code assembler | 2005 | [291] |
| Processor design | General purpose hidden Markov model (HMM) processor | 2005 | [292] |
| Data acquisition | Architecture for data acquisition | 2005 | [293] |
| Control engineering | Buffering interface of multi task motion control system | 2005 | [294] |
| Processor design | Real-time FFT processor | 2005 | [295] |
| Prototyping / Processor design | Perceptron-based branch predictor | 2005 | [296] |
| Control engineering | Low Level RF control for the Debuncher, readout of transfer-line Beam Position Monitors, and narrow-band spectral analysis of diagnostic signals from Schottky pickups | 2005 | [297] |
| Control engineering | Zero-current-switching single-phase high power factor boost rectifier controller | 2005 | [298] |
| Image processing | Distributed Arithmetic (DA) video processing | 2005 | [299] |
| Networks | IP lookup | 2005 | [300] |
| Prototyping / Processor design | Fast path-based neural branch predictor | 2005 | [301] |
| Communication | IQ-imbalances corrector in quadrature receivers | 2005 | [302] |
| Mathematics | Real-time histogram equalization | 2005 | [303] |
| Cryptography | Sequential implementation of advanced encryption standard (AES) | 2005 | [304] |
| Image processing | Real-time adaptive background model | 2005 | [305] |
| Data-Mining | XCS (accuracy-based learning classifier system) | 2005 | [306] |
| Data-Mining / Fuzzy logic | Data Fusion including Kalman filtering and fuzzy logic covariance matrix | 2005 | [307] |
| Image processing | Active contour models (snakes) | 2005 | [308] |
| Fuzzy logic | Fuzzy controller for multiphase DC-DC converters | 2006 | [309] |
| Robotics | Weak chaos control for action-oriented perception and navigation | 2006 | [310] |
| Neuro-computing | Path-based neural branch prediction algorithm | 2006 | [311] |
| Networks | Network interface for software router | 2006 | [312] |
| Simulation | Thermal emulation framework for multi-processor system-on-chip | 2006 | [313] |
| Image processing | H.264/AVC inverse transforms and quantization | 2006 | [314] |
| Control engineering | N-motor speed control system of brushless DC motors | 2006 | [315] |
| Image processing | Main profile H.264/AVC decoder | 2006 | [316] |
| Image processing | DCT/IDCT algorithm for MPEG or H.26x video compression | 2006 | [317] |
| Mathematics | Pseudo-random number generator based on cellular automata | 2006 | [318] |
| Data acquisition / Physics | Data acquisition and analysis for ANTARES neutrino experiment and CMS electromagnetic calorimeter at LHC | 2006 | [319] |
| Communication | Real-time wireless digital signal processing | 2006 | [320] |
| Other | Video arousal content modeling system | 2006 | [321] |
| Neuro-computing / Control engineering | Neural network-based controller for power electronic applications | 2006 | [322] |
| Control engineering | Real-time detection for creepage of power supply and person's getting an electric shock | 2006 | [323] |
| Mathematics | Simplex algorithm for linear programming | 2006 | [324] |
| Communication | Fixed-throughput sphere decoder for MIMO systems | 2006 | [325] |
| Data acquisition | Data stream zero suppression and word recoding | 2006 | [326] |
| Medical | Sleep apnea screening | 2006 | [327] |
| Image processing | Retinex image processing algorithm | 2006 | [328] |
| Control engineering | Variable structure controller slide-mode (VSC-SM) for DC/DC converters | 2006 | [329] |
| Image processing | Two-dimensional discrete wavelet transform for JPEG2000 compression | 2006 | [330] |
| Control engineering | 3-sinusoidal PWM (SPWM) controller | 2006 | [331] |

| Field | Description | Year | Reference |
|---|---|---|---|
| Control engineering | Phase-shift control for variable frequency multi-cells interleaved boost pre-regulator | 2006 | [332] |
| Neuro-computing | Time Adaptive Clustering (TAC) for Logical Story Unit (LSU) segmentation | 2006 | [333] |
| Data acquisition | Multi-rate interpolator with real-time rate change for a JET test-bench system | 2006 | [334] |
| Data acquisition | Multi-sensor data acquisition module with broadcasting capabilities and environment compensation | 2006 | [335] |
| Control engineering | Single-phase shunt Active Power Filter (APF) | 2006 | [336] |
| Communication | Digital blocks of a DAB receiver | 2006 | [337] |
| Communication | Digital IIR filter | 2006 | [338] |
| Other | Audiodecoding for multimedia player | 2006 | [339] |
| Data-Mining | Support vector machines with pseudo-logarithmic number representation | 2006 | [340] |
| Control engineering | Variable frequency interleaved zero-current-switching boost rectifier controller | 2006 | [341] |
| Mathematics / Cryptography | Exponentiation accelerator | 2006 | [342] |
| Communication | Dynamic Threshold Sphere Detection (DTSD) | 2006 | [343] |
| Processor design | Custom instruction accelerator | 2006 | [344] |
| Mathematics / Cryptography | Moduli multiplier for public-key cryptographic | 2006 | [345] |
| Communication | Multi-standard reconfigurable viterbi decoder for UMTS and GPRS | 2006 | [346] |
| Mathematics | All-Pairs Shortest-Paths (APSP) solver for directed graph | 2006 | [347] |
| Image processing | H.264/AVC decoder | 2006 | [348] |
| Control engineering / Prototyping | Second order Time Delay Tanlock Loop (TDTL) | 2006 | [349] |
| Image processing | Learning OCR system using short/long-term memory approach | 2006 | [350] |
| Image processing | License plate recognition SoC | 2006 | [351] |
| Communication | Canonical signed digit multiplier-less based FFT for wireless communication | 2006 | [352] |
| Mathematics | All-Pairs Shortest-Paths (APSP) solver for directed graph | 2006 | [353] |
| Data acquisition / Communication | Power-spectrum analysis | 2006 | [354] |
| Image processing | Color space conversion | 2006 | [355] |
| Prototyping | Packet switching algorithm for networks on chip | 2006 | [356] |
| Image processing | 2-D shift-variant convolvers | 2006 | [357] |
| Networks | Switch performance testbed for optical links | 2006 | [358] |
| Control engineering | Power Factor Correction (PFC) based on average current mode control | 2007 | [359] |
| Communication | Dirty paper precoder | 2007 | [360] |
| Medical | Communication controller with RF transceiver for health monitoring | 2007 | [361] |
| Mathematics | Multivariate PieceWise Linear (PWL) function | 2007 | [362] |
| Bio-computing / Processor design | Median-based phylogenetic reconstruction co-processor | 2007 | [363] |
| Image processing | Context-based Adaptive Binary Arithmetic Coding (CABAC) decoder | 2007 | [364] |
| Mathematics | Fast Fourier (FFT) and Inverse Fast Fourier Transform (IFFT) algorithms | 2007 | [365] |
| Image processing | Edge detection | 2007 | [366] |
| Cryptography | SAFER 64 (secure and fast encryption routine) algorithm for data and voice encryption | 2007 | [367] |
| Robotics | Autopilot platform for unmanned vehicle designs | 2007 | [368] |
| Communication | Receiver diversity combining for SIMO systems | 2007 | [369] |
| Prototyping | Gated clock based globally asynchronous locally synchronous wrapper circuits | 2007 | [370] |
| Medical | High resolution phase shift beamformer for 2D and 3D ultrasound real time imaging | 2007 | [371] |
| Image processing | Color space transformation RGB to YIQ and YCbCr | 2007 | [372] |
| Communication | Digital carrier synchronizer | 2007 | [373] |
| Cryptography | Elliptic Curve Cryptographic (ECC) | 2007 | [374] |
| Networks | Network-On-FPGA (NoFPGA) router | 2007 | [375] |
| Communication | Digital carrier synchronizer | 2007 | [376] |
| Bio-computing | Pairwise biological sequence alignment (Smith-Waterman and Needleman-Wunsch) | 2007 | [377] |
| Communication | CTC turbo decoder | 2007 | [378] |
| Image processing | Automatic meter reading of a fluid meter digit display | 2007 | [379] |
| Simulation | Sensor simulation | 2007 | [380] |
| Bio-computing | Molecular dynamics simulation | 2007 | [381] |
| Data acquisition | Power measuring for induction heating appliances | 2007 | [382] |
| Control engineering | Single-carrier Multilevel PWM | 2007 | [383] |
| Data acquisition / Processor design | Particle detector monitoring SoC | 2007 | [384] |

| Field | Description | Year | Reference |
|---|---|---|---|
| Control engineering | Vector PI (VPI) regulator controller | 2007 | [385] |
| Mathematics | Floating-point matrix multiplier for 3D affine transformations | 2007 | [386] |
| Data acquisition | Trigger and readout electronics for the CERN ALICE experiment | 2007 | [387] |
| Control engineering | Split-phase control current source multi-level inverter | 2007 | [388] |
| Data-Mining | Matched filter for hyperspectral data | 2007 | [389] |
| Control engineering | Controller for a NPC (Neutral Point Clamped) (three-level) multilevel converter | 2007 | [390] |
| Mathematics | Cyclotomic Fast Fourier Transform (FFT) over finite fields GF (2m) | 2007 | [391] |
| Networks | High-speed serial address-event representation | 2007 | [392] |
| Control engineering | Motor side active filter | 2007 | [393] |
| Communication | Chaos-based Code Division Multiple Access (CDMA) transceiver | 2007 | [394] |
| Image processing | Motion estimation | 2007 | [395] |
| Communication | Quadrature mirror filter bank | 2007 | [396] |
| Control engineering | Switching power converter controller | 2007 | [397] |
| Networks | Lookup circuit for session-based IP packet classification | 2007 | [398] |
| Data-Mining | Fingerprint verification and matching system | 2007 | [399] |
| Space / Communication | Reed-Solomon encoder | 2007 | [400] |
| Image processing | Low-level vision algorithm | 2007 | [401] |
| Data acquisition | Time-to-digital converter | 2007 | [402] |
| Image processing | Fast Hadamard transform | 2007 | [403] |
| Communication | Multi-standard software radio receiver | 2007 | [404] |
| Bio-computing | Maximum-Parsimony (MP) phylogenies reconstruction | 2007 | [405] |
| Control engineering | Power Factor Correction (PFC) based on average current mode control | 2007 | [406] |
| Robotics | Extended Kalman Filter (EKF) for localization and mapping | 2007 | [407] |
| Control engineering | Input current and DC link voltage of a single-phase voltage-doubler boost PFC | 2008 | [408] |
| Financial computing | Pseudo random number generators for monte carlo methods in quantitative finance | 2008 | [409] |
| Other | High-resolution programmable delay lines | 2008 | [410] |
| Processor design | 8-bit simple processor | 2008 | [411] |
| Cryptography | Hybrid additive programmable cellular automata encryption | 2008 | [412] |
| Cryptography | AES-CCM for IEEE 802.16e and IEEE 802.11i | 2008 | [413] |
| Communication | Decoder for long structured or unstructured LDPC codes | 2008 | [414] |
| Networks | Multiplexing and demultiplexing deep-sea hydrophone array signals | 2008 | [415] |
| Cryptography / Processor design | Tate Pairing coprocessor | 2008 | [416] |
| Control engineering | Digital pulse width modulator | 2008 | [417] |
| Communication | Vector SISO algorithm decoder for extended Hamming code and extended Bose, Chaudhri, and Hocquenghem code | 2008 | [418] |
| Mathematics | 2D-discrete cosine transform | 2008 | [419] |
| Control engineering | Control of a PFC converter | 2008 | [420] |
| Simulation | Rayleigh and Rician fading channels for MIMO | 2008 | [421] |
| Communication | Space time block encoder | 2008 | [422] |
| Image processing | Rotationally invariant sparse patch matching | 2008 | [423] |
| Data acquisition | Time-to-digital converters | 2008 | [424] |
| Mathematics | Linear, non-linear, and hybrid pseudo-random number generators | 2008 | [425] |
| Space | Floating point signal processing for MATMOS Fourier Transform InfraRed (FTIR) spectrometer | 2008 | [426] |
| Mathematics | Left to right serial multiplier for large numbers | 2008 | [427] |
| Networks | Crossbar for NoC | 2008 | [428] |
| Mathematics | CORDIC algorithm for cosine calculation | 2008 | [429] |
| Neuro-computing | Isolated digit recognition system using self organizing feature map | 2008 | [430] |
| Image processing | Robust Evolutionary Controlled (REC) filter for radar image enhancement | 2008 | [431] |
| Simulation | Real-time simulator for electrical system | 2008 | [432] |
| Control engineering | Controller for laboratory scale air levitation system | 2008 | [433] |
| Data acquisition | Trigger and readout electronics for the CERN ALICE experiment | 2008 | [434] |
| Control engineering / Processor design | Full speed real-time motor control drive algorithm based MPSoC | 2008 | [435] |
| Communication | Viterbi decoder using Register Exchange Algorithm (REA) for digital video broadcasting for terrestrial networks (DVB-T) | 2008 | [436] |

| Field | Description | Year | Reference |
|---|---|---|---|
| Data acquisition | Automatic Censored Cell Averaging (ACCA) Constant False Alarm Rate (CFAR) detection algorithm for RADAR | 2008 | [437] |
| Communication | CoOrdinate Rotation DIgital Computer (CORDIC) for OFDM | 2008 | [438] |
| Processor design | SIMD SoC parallel reduction algorithm | 2008 | [439] |
| Neuro-computing | Serial, partial parallel, and full parallel artificial neuron model | 2008 | [440] |
| Prototyping | Alamouti space-time coding with 64-QAM for LTE | 2008 | [441] |
| Neuro-computing | Artificial neural network for Cetane number prediction form liquid chromatography and gas chromatography | 2008 | [442] |
| Image processing | Spatial-temporal implementation of sobel filters and anisotropic diffusion | 2008 | [443] |
| Mathematics | Wide integer multiplier | 2008 | [444] |
| Simulation / Control engineering | Real-time motor emulator linked to its controller drive | 2008 | [445] |
| Control engineering | Multilevel inverter controller | 2008 | [446] |
| Neuro-computing / Control engineering | Neural multi-layer network for DC motor speed control | 2008 | [447] |
| Cryptography | AES-CCM for IEEE 802.16e and IEEE 802.11i | 2008 | [448] |
| Medical / Prototyping | Transcutaneous electrical nerve stimulator | 2008 | [449] |
| Image processing | Stereo vision on gray scaled Bayer patterned images | 2008 | [450] |
| Communication | Second Order Volterra Filter (SOVF) for decomposing pulse echo ultrasonic Radio-Frequency (RF) signals | 2008 | [451] |
| Bio-computing | Smith-Waterman algorithm for DNA sequence alignments | 2008 | [452] |
| Data-Mining | Sixphase pulse compression sequences for radar signal processing | 2008 | [453] |
| Prototyping | Circuit model emulation of quantum algorithms | 2008 | [454] |
| Networks | Universal Serial Bus (USB) transceiver macro cell interface (UTMI) | 2008 | [455] |
| Neuro-computing | Biologically inspired spike timing-dependent plasticity | 2008 | [456] |
| Prototyping | Quantum cellular automata | 2008 | [457] |
| Data acquisition | Non-linear least squares for digital spectroscopy | 2009 | [458] |
| Data acquisition | Time-to-digital converter | 2009 | [459] |
| Data acquisition | Direct resistance and capacitance measurement | 2009 | [460] |
| Communication | FFT for infinite complex field C and Galois finite field GF | 2009 | [461] |
| Control engineering | Power Factor Correction (PFC) of a single-phase voltage doubler rectifier | 2009 | [462] |
| Data acquisition | Rigger architecture for high-resolution spectroscopy | 2009 | [463] |
| Communication | Digital up converter for Wideband Code Division Multiple Access (WCDMA) | 2009 | [464] |
| Communication | SNR estimation for Direct Sequence Spread Spectrum (DSSS) signal of space borne secondary radar | 2009 | [465] |
| Neuro-computing / Image processing | Discrete time cellular neural network for image processing | 2009 | [466] |
| Control engineering | Space vector pulse width modulation based induction motor speed control | 2009 | [467] |
| Communication | Multiple Signal Classification (MUSIC) and Direction Of Arrival (DOA) estimation of smart antenna array | 2009 | [468] |
| Communication | CRC engine | 2009 | [469] |
| Networks | Zigbee CRC block | 2009 | [470] |
| Medical / Neuro-computing | Cardiac arrhythmias recognition by means of Kohonen self-organizing map | 2009 | [471] |
| Neuro-computing | Binary self organizing map | 2009 | [472] |
| Image processing | Multimodal Sigma-Delta background estimation for moving objects extraction | 2009 | [473] |
| Image processing / Cryptography | Chaos-based image encryption | 2009 | [474] |
| Control engineering | Time domain deadbeat algorithm for DC motor control | 2009 | [475] |
| Communication | CRC engine for error detection in data transmission | 2009 | [476] |
| Communication | Bit Error Rate Tester (BERT) for hardware-based verification of the physical layer of emerging wireless systems | 2009 | [477] |
| Data acquisition | Least mean squares to correct the mismatch errors in time interleaved ADCs | 2009 | [478] |
| Communication | Multi-rate signal processing for Software Defined Radio (SDR) | 2009 | [479] |
| Control engineering | Pulse shape discrimination for positron emission tomography | 2009 | [480] |
| Image processing | Optical-flow estimation | 2009 | [481] |
| Communication | Variable step-size normalized least-mean-square acoustic echo canceller | 2009 | [482] |
| Mathematics | Linear equation solver | 2009 | [483] |
| Data acquisition | Time-to-digital converter | 2009 | [484] |
| Bio-computing | SSEARCH35 Smith-Waterman implementation | 2009 | [485] |
| Prototyping | Verification of broadband MIMO wireless systems | 2009 | [486] |

| Field | Description | Year | Reference |
|---|---|---|---|
| Processor design | Coordinate Rotation Digital Computer (CORDIC) trigonometric algorithm | 2009 | [487] |
| Processor design | 1D linear MPSoC architecture for invasive computing | 2009 | [488] |
| Cryptography | Micro crypto-functions | 2009 | [489] |
| Other | Extending GPS with inertial navigation system (INS) | 2009 | [490] |
| Networks | Zigbee bit-to-symbol block and the symbol-to-chip block for an acknowledgement frame | 2009 | [491] |
| Data acquisition | Time To Digital converter (TDC) for Positron Emission Tomography (PET) | 2009 | [492] |
| Processor design / Networks | Packet classification coprocessor | 2009 | [493] |
| Communication | Carrier Frequency Offset (CFO) estimation and correction for WiMAX OFDM receiver | 2009 | [494] |
| Image processing | Stable Euler-number based algorithm for image binarization | 2009 | [495] |
| Simulation | Pulse generator circuit that produces a stream of pulses at pseudo-random time intervals | 2009 | [496] |
| Networks | Zigbee CRC block | 2009 | [497] |
| Robotics | Control of a sailing Robot | 2009 | [498] |
| Control engineering | Solid state pulsed power generator controller | 2009 | [499] |
| Communication | Intermediate frequency filter for GSM systems | 2009 | [500] |
| Image processing | CCD scanning and detecting defects of crossing-linkable polyethylene unsulation | 2009 | [501] |
| Simulation | Emulation of GLink chip set with serial transceivers for the ATLAS Level-1 Muon Trigger | 2009 | [502] |
| Control engineering | Phase Locked Loop (PLL) controller | 2009 | [503] |
| Data acquisition | Multihit time-to-digital converter | 2009 | [504] |
| Image processing | Real-time stereo imaging system | 2009 | [505] |
| Mathematics | Multivariate polynomial evaluation | 2009 | [506] |
| Data acquisition | Fast control and timing distribution system | 2009 | [507] |
| Communication | Direct sequence code division multiple access receiver | 2010 | [508] |
| Neuro-computing / Robotics | Discrete Time Cellular Neural Network (DTCNN) for robot guiding | 2010 | [509] |
| Data acquisition | Trigger and dead-time free DAQ System for the KAOS Spectrometer at MAMI | 2010 | [510] |
| Communication | Bartlett direction of arrival algorithm for a 5.8ghz circular antenna array | 2010 | [511] |
| Medical | Real-time measurement of ventricular volumes | 2010 | [512] |
| Image processing | Sobel algorithm for adaptive edge detection | 2010 | [513] |
| Networks | Successive interference cancellation detector | 2010 | [514] |
| Image processing | Iris biometic recognition | 2010 | [515] |
| Robotics | Object seeking and tracking | 2010 | [516] |
| Cryptography | Secure Hash Alogrithm (SHA) | 2010 | [517] |
| Control engineering | Pulse Width Modulation (PWM)-Pulse Frequency Modulation (PFM) for DC-DC converter | 2010 | [518] |
| Prototyping | Cluster-based multiprocessor system-on-chip (MPSoC) | 2010 | [519] |
| Image processing | CVBS to SDI conversion | 2010 | [520] |
| Communication | Matched filtering algorithm for impact signal processing | 2010 | [521] |
| Image processing | Video capturing system for plate-profile information and spatial domain image processing | 2010 | [522] |
| Communication | 8-point Slantlet transform based polynomial cancellation coding-OFDM | 2010 | [523] |
| Control engineering | Pulsed-power generators controller | 2010 | [524] |
| Simulation | Stochastic spatial MIMO channel simulation | 2010 | [525] |
| Networks | Public telephone remote control system | 2010 | [526] |
| Image processing | Message displaying system using scanning technique | 2010 | [527] |
| Control engineering | Brushless DC motor speed controller | 2010 | [528] |
| Control engineering | Space vector modulated trigger controller for a frequency converter | 2010 | [529] |
| Image processing | Serial Digital Interface (SDI) video interface | 2010 | [530] |
| Networks | Full duplex implementation of Internet Protocol version 4 | 2010 | [531] |
| Networks | UDP/IP core | 2010 | [532] |
| Image processing | Vehicle recognition for speed limit enforcement systems | 2010 | [533] |
| Control engineering | Pulse generator for stepper motor | 2010 | [534] |
| Medical / Image processing | Finite RAdon Transform (FRAT) for medical image de-noising | 2010 | [535] |
| Neuro-computing | Multilayer perceptron artificial neural network | 2010 | [536] |
| Simulation | Emulation of GLink chip set with serial transceivers for the ATLAS Level-1 Muon Trigger | 2010 | [537] |
| Mathematics | Integer division | 2010 | [538] |
| Control engineering | Unipolar sinusoidal pulse width modulation (SPWM) for single phase full bridge inverter | 2010 | [539] |
| Medical | ECG signal FIR filter for diagnosis of cardiovascular disease | 2010 | [540] |
| Data acquisition | Levenberg-Marquardt algorithm for non-linear least-squares for digital spectroscopy | 2010 | [541] |
| Processor design | FFT processor for orthogonal frequency division multiple access system | 2010 | [542] |

| Field | Description | Year | Reference |
|---|---|---|---|
| Test | Multiport equipment testing through relay matrix control | 2010 | [543] |
| Image processing | Zernike Moments based near-field laser imaging detector | 2010 | [544] |
| Fuzzy logic | Fuzzy logic controller | 2010 | [545] |
| Processor design | Direct frequency synthesis (DDS), down-sampling filter (CIC) and low pass filter (FIR) | 2010 | [546] |
| Communication | Acoustic localization | 2010 | [547] |
| Control engineering | Trapezoidal modulated cyclo-inverter | 2010 | [548] |
| Control engineering | Calculation of the azimuth angle and altitude angle for a two axis solar tracking system | 2010 | [549] |
| Communication | High Density Bipolar codec (HDB3) encoder and decoder | 2010 | [550] |
| Communication | OFDM Baseband WiMAX transmitter | 2010 | [551] |
| Bio-computing | DNA Sequence Alignment | 2010 | [552] |
| Bio-computing | HMMER to identify homologous protein or nucleotide sequences | 2010 | [553] |
| Control engineering | Blowout expert control system | 2010 | [554] |
| Control engineering | Adaptive binary integrator | 2010 | [555] |
| Control engineering | Brushless DC motor speed controller | 2010 | [556] |
| Prototyping | Higher order moving target indication for radar | 2010 | [557] |
| Communication | DS/FH communication intermediate frequency $\frac{\pi}{4}$ DQPSK modulation | 2011 | [558] |
| Fuzzy logic | Stator condition monitoring | 2011 | [559] |
| Control engineering | Third-order SPWM inverter controller | 2011 | [560] |
| Communication | Pseudo-random m-sequence error detection for OFDM channel | 2011 | [561] |
| Networks | LDPC channel coding for digital video broadcasting | 2011 | [562] |
| Networks | Serial communication interface bridge | 2011 | [563] |
| Mathematics | Negative logarithmic function | 2011 | [564] |
| Communication | Viterbi decoder | 2011 | [565] |
| Mathematics | Traveling salesman problem solver using genetic algorithms | 2011 | [566] |
| Networks | Bus interface unit for ARINC 659 backplane | 2011 | [567] |
| Networks | Downlink PDSCH architecture for LTE | 2011 | [568] |
| Communication | Coefficient multiplier for FIR filter | 2011 | [569] |
| Other | Extending GPS navigation with motion sensor information, accelerometer, and gyroscope | 2011 | [570] |
| Communication | QR-decomposition algorithm for a LTE MIMO detector | 2011 | [571] |
| Simulation | One-dimensional Euler equations for fluid dynamics | 2011 | [572] |
| Data acquisition | Trigger and dead-time free DAQ System for the KAOS spectrometer at MAMI | 2011 | [573] |
| Control engineering | Sinusoidal PWM waveform generation for a five-phase five-level converter | 2011 | [574] |
| Data acquisition | Accurate frame interleaved sampling | 2011 | [575] |
| Prototyping | Shared memory system for high bandwidth communication | 2011 | [576] |
| Control engineering | Space Vector Modulated (SVM) trigger controller for frequency converter | 2011 | [577] |
| Control engineering | Delta modulated single-phase matrix converter | 2011 | [578] |
| Control engineering | Trapezoidal pulse width modulation for cyclo-inverter | 2011 | [579] |
| Image processing | Viola Jones algorithm face detection for car theft detection | 2011 | [580] |
| Communication | Offset quadrature phase shift keying (OQPSK)-pulse-shaping block | 2011 | [581] |
| Networks | ARINC 659 Host | 2011 | [582] |
| Cryptography | AES for data storage encryption | 2011 | [583] |
| Image processing / Networks | VGA data communication | 2011 | [584] |
| Networks | Hardware packet filter for network gateways | 2011 | [585] |
| Networks | Hardware packet filter for network gateways | 2011 | [586] |
| Communication | CRC generation | 2011 | [587] |
| Neuro-computing / Fuzzy logic | Multi-stage condition monitoring of induction motors | 2011 | [588] |
| Control engineering | Pulsed power generator controller | 2011 | [589] |
| Bio-computing | Phylogenetic parsimony function for reconstructing evolutionary trees | 2011 | [590] |
| Robotics | PID controller for robot navigation | 2011 | [591] |
| Control engineering | Permanent magnet synchronous motor (PMSM) speed controller | 2011 | [592] |
| Control engineering | 5 step modified space vector modulation algorithm for AC drive control | 2011 | [593] |
| Control engineering | Space vector modulation algorithm for current control of three phase electric machines | 2011 | [594] |
| Control engineering | 6 channels pulse width modulator for three phase AC drives control | 2011 | [595] |
| Neuro-computing | Learning vector quantization for movement prediction of electromyogram signals | 2011 | [596] |
| Simulation | Generic simulator for instruction set architectures | 2011 | [597] |
| Prototyping | Replacement of timing trigger and control receiver for the LHC | 2011 | [598] |

| Field | Description | Year | Reference |
|---|---|---|---|
| Data-Mining | Parallel sorting algorithm for OS-CFAR radar algorithms | 2011 | [599] |
| Other | 7-segment displays interface logic | 2011 | [600] |
| Cryptography | Elliptic curve cryptography | 2011 | [601] |
| Processor design | Streaming and vector computations processor | 2011 | [602] |
| Communication | Viterbi decoder | 2011 | [603] |
| Image processing | RVC MPEG-4 SP intra decoder | 2011 | [604] |
| Networks | Network port scan detection | 2011 | [605] |
| Image processing | 2D discrete cosine transform for image compression | 2011 | [606] |
| Neuro-computing | Auto-associative memory based on a spiking neural network (SNN) | 2011 | [607] |
| Networks | Network-on-chip structure | 2012 | [608] |
| Networks | Serial link communication for SuperB asymmetric e+e – colider | 2012 | [609] |
| Image processing | Canny edge detection | 2012 | [610] |
| Control engineering / Space | Micro-stepping scheme for stepper motor in space-based solar power systems | 2012 | [611] |
| Other | Arbitrary waveform generator | 2012 | [612] |
| Neuro-computing | Time-derivative cellular neural networks for spatiotemporal transfer functions for linear filtering | 2012 | [613] |
| Networks | Bluetooth Medium Access Control (MAC) with Universal Asynchronous Receiver/Transmitter (UART) | 2012 | [614] |
| Mathematics | Matrix inversion using single, double and custom floating-point precision | 2012 | [615] |
| Bio-computing | DNA sequence data minimization | 2012 | [616] |
| Medical | Discrete wavelet transformation for noise filtering of EEG data | 2012 | [617] |
| Control engineering | Permanent magnet synchronous motor (PMSM) speed controller | 2012 | [618] |
| Mathematics | Radix square root unit with prescaling | 2012 | [619] |
| Control engineering | Numerically controlled oscillator | 2012 | [620] |
| Neuro-computing | Neural networks for environment/noise classification and removal | 2012 | [621] |
| Control engineering | High brightness light emitting diode array controller | 2012 | [622] |
| Networks | Wake-up radio receiver for wireless sensor networks | 2012 | [623] |
| Networks | Physical downlink control channel (PDCCH) for LTE | 2012 | [624] |
| Simulation | Simulation environment for FPGA based embedded controller | 2012 | [625] |
| Communication | Emulator for low-density-parity-check-codes evaluation | 2012 | [626] |
| Mathematics / Financial computing | Decimal digit adders and multipliers | 2012 | [627] |
| Neuro-computing | Auto-associative memory based on a spiking neural network | 2012 | [628] |
| Communication | Digital down conversion with high signal-to-noise (SNR) gain | 2012 | [629] |
| Image processing | Real-time linear blending vision reconstruction for a spherical light field camera | 2012 | [630] |
| Simulation | Intermediate frequency GPS signal source | 2012 | [631] |
| Processor design / Medical | Processor for real-time interlaced co-registered ultrasound and photoacoustic imaging for tumor dynamic response | 2012 | [632] |
| Control engineering | 2nd and higher order systems controller using Graham Lathrop optimal polynomials and Left Hand Side zero | 2012 | [633] |
| Image processing / Networks | Data processing for a video surveillance system with large network of cameras | 2012 | [634] |
| Communication | Conditioned adaptive post detection integration for radar | 2012 | [635] |
| Control engineering | Cyclo-converter and Cyclo-inverter using non-sinusoidal carrier-based PWM | 2012 | [636] |
| Control engineering | Data acquisition and antenna guidance to achieve maximum signal strength | 2012 | [637] |
| Image processing | Color histogram based Particle filter for video object tracking | 2012 | [638] |
| Networks | Gigabit Ethernet UDP/IP core | 2012 | [639] |
| Communication | PLL-based quarter-rate clock and data recovery circuit | 2012 | [640] |
| Bio-computing | DNA sequence data minimization | 2012 | [641] |
| Communication | Cyclic Redundancy Check (CRC) accelerators | 2012 | [642] |
| Robotics / Image processing | Image processing of a low-cost camera sensor | 2012 | [643] |
| Control engineering | Synchronized Sinusoidal Pulse Width Modulation (SPWM) for medium voltage inverters | 2012 | [644] |
| Test | Embedded instrument for board system test | 2012 | [645] |
| Medical / Image processing | 3-D Daubechies with transpose-based method for medical image compression | 2012 | [646] |
| Control engineering | 1-degree-of-freedom discrete PID for buck converter | 2012 | [647] |
| Control engineering | Modulator for a five level hybrid multilevel inverter | 2012 | [648] |
| Control engineering | Measurement and control system for laser cladding | 2012 | [649] |
| Simulation | Signal generator for power quality analysis | 2012 | [650] |

| Field | Description | Year | Reference |
|---|---|---|---|
| Processor design | Virtual Processing Integrated Grid (VPIG) with one MCU and four cells for bio-inspired hardware applications | 2012 | [651] |
| Processor design | 8 bit RISC controller IP core | 2012 | [652] |
| Neuro-computing | Controlling reconfigurable antennas via neural network | 2012 | [653] |
| Cryptography | 128 bit AES | 2012 | [654] |
| Image processing | Eye tracking | 2012 | [655] |
| Neuro-computing | Tri-state logic self-organizing map | 2012 | [656] |
| Communication | Digital down converter for multi-standard radio communication | 2013 | [657] |
| Simulation | Isotropic and non-isotropic fading channel simulator for wireless communication | 2013 | [658] |
| Robotics | Servomotor controller for a six-legged robot | 2013 | [659] |
| Control engineering / Space | Microstepping stepper motor drive controller for solar array drive assembly | 2013 | [660] |
| Simulation | HIL simulation of a linear system block for strongly coupled system applications | 2013 | [661] |
| Cryptography | Trusted cryptography module | 2013 | [662] |
| Robotics / Image processing | Harris edge detection for colored stereo images | 2013 | [663] |
| Control engineering | PID controller of a MATLAB modelled DC motor | 2013 | [664] |
| Image processing | Laplace filter for 40 x 40 pixel grey scale video signals | 2013 | [665] |
| Communication | Digital pre-distortion linearisation for wide-band waveforms | 2013 | [666] |
| Communication | Finite impulse response and infinite impulse response filters | 2013 | [667] |
| Networks | Junction based router for NoCs | 2013 | [668] |
| Medical | Pulse encoder for optoelectronic neural stimulation | 2013 | [669] |
| Control engineering | PLL and signal processing for a 60 GHz radar distance measurement system | 2013 | [670] |
| Cryptography | Blake-256 cryptographic hash implementation | 2013 | [671] |
| Cryptography | JH cryptographic hash function | 2013 | [672] |
| Communication | Reconfigurable 4 / 8 / 16 / 32 / 64 Quadrature Amplitude Modulation (QAM) demodulator | 2013 | [673] |
| Space | Support vector machine for 128-dimensional feature space data | 2013 | [674] |
| Image processing | Real-time traffic sign recognition | 2013 | [675] |
| Neuro-computing | Spiking neural network of 117 Izhikevich neurons | 2013 | [676] |
| Networks | Low latency interface to a HPC-GPU farm | 2013 | [677] |
| Image processing | Stereo matching system for 3D-TV meeting HDMI 1.4a requirements | 2013 | [678] |
| Control engineering | Controller for a single-stage grid connected solar Photo-Voltaic systems | 2013 | [679] |
| Prototyping | Network-On-Chip parameter simulation | 2013 | [680] |
| Cryptography | Polynomial multiplication with the number theoretic transform for lattice-based cryptography | 2013 | [681] |
| Communication | Multiplier for FFT for OFDM transmission | 2013 | [682] |
| Communication | Quickest detection algorithm and energy detection algorithm as spectrum sensing technique for cognitive radio networks | 2013 | [683] |
| Cryptography | Advanced encryption standard (AES) | 2013 | [684] |
| Control engineering | Three phase inverter modulation with sinusoidal pulse width with zero sequence injection modulation and space vector modulation | 2013 | [685] |
| Other | Reconstruction of the energy-deposition peak in the NA62 liquid krypton electromagnetic calorimeter at CERN | 2013 | [686] |
| Image processing | Real-time filter for spatial and temporal parallelism | 2013 | [687] |
| Communication | distributed algorithm FIR filter | 2013 | [688] |
| Communication | Adaptive fractionally spaced blind equalizer for 2x2 Multi-Input Multi-Output (MIMO) 16-QAM channel | 2013 | [689] |
| Networks | Transmission Control Protocol based industry automation | 2013 | [690] |
| Communication | Digital frequency synthesis for OFDM software defined radio | 2013 | [691] |
| Image processing | DAQ System for a mercury imaging X-ray spectrometer | 2013 | [692] |
| Medical | Even power distributor for optoelectronic neural stimulation | 2013 | [693] |
| Control engineering | Unified one-cycle controller for single phase boost power factor compensation | 2013 | [694] |
| Control engineering | Control and gate signal generation for a multilevel current-source inverter | 2013 | [695] |
| Prototyping | Round-Robin-arbiter for Network-On-Chip designs | 2013 | [696] |
| Prototyping | Code compression/decompressor for embedded system processors | 2013 | [697] |
| Control engineering | Delta modulation and trapezoidal modulation for cycloinverter | 2013 | [698] |
| Control engineering | Controller for digital pulse width modulation for single-phase cascaded H-bridge multilevel inverter | 2013 | [699] |
| Medical | Electrical impedance tomography image reconstruction | 2013 | [700] |
| Image processing | Spatial binary filtering and euclidean distance calculation for a fingerprint recognition system | 2013 | [701] |
| Networks | Remote DMA virtual to physical address translator | 2013 | [702] |
| Image processing | Fractional wavelet transformation to reduce image sizes | 2013 | [703] |

| Field | Description | Year | Reference |
|---|---|---|---|
| Networks | USB 3.0 controller at $3\,\mathrm{Gbit/s}$ | 2013 | [704] |
| Simulation | Floating-point solver for HIL simulation of electric and power electronic circuits | 2013 | [705] |
| Control engineering | MEMS inclinometer controller | 2013 | [706] |
| Communication | Adaptive noise cancellation with LMS algorithm | 2014 | [707] |
| Image processing | Median filter | 2014 | [708] |
| Communication | Orthogonal frequency division multiplexing (OFDM) pipeline | 2014 | [709] |
| Networks | low-density parity-check decoder | 2014 | [710] |
| Image processing | Quality control and palletization | 2014 | [711] |
| Control engineering | Sliding mode controller and sliding mode observer for DC/DC converter | 2014 | [712] |
| Communication | Quasi-cyclic irregular LDPC decoder | 2014 | [713] |
| Communication | $\frac{\pi}{4}$-DQPSK complex wavelet packet modulation CWPM transceiver | 2014 | [714] |
| Prototyping | Cyberphysical-system-on-chip | 2014 | [715] |
| Networks | SQL query acceleration | 2014 | [716] |
| Cryptography | $128\,\mathrm{bit}$-key AES cipher | 2014 | [717] |
| Image processing / Medical | Ultrasonic image enhancement | 2014 | [718] |
| Control engineering | System identification based on re-sampling of periodic signals for open-loop control | 2014 | [719] |
| Communication | Spatial multiplexing blocks for 3GPP-LTE | 2014 | [720] |
| Control engineering | Least mean square beamforming for terrestrial radar | 2014 | [721] |
| Cryptography | PRINCE block cipher | 2014 | [722] |
| Control engineering | Field oriented control algorithm for speed control of a permanent magnet synchronous motor | 2014 | [723] |
| Communication | Short-time Fourier-transform for speech applications | 2014 | [724] |
| Control engineering | Digital phase locked loop for resonant converter | 2014 | [725] |
| Networks | Robust and redundant data capturing for ATLAS | 2014 | [726] |
| Processor design | Asynchronous ALU based on modified 4 phase handshaking protocol with tapered buffers | 2014 | [727] |
| Communication | Carrier recovery and timing synchronization | 2014 | [728] |
| Cryptography | SHA-3 (Keccak) cryptographic hash algorithm | 2014 | [729] |
| Control engineering | FMCW radar liquid level measurement system signal processing | 2014 | [730] |
| Networks / Prototyping | cut-through and store-and-forward ethernet switch | 2014 | [731] |
| Control engineering | Fractional position estimation for optical incremental encoder | 2014 | [732] |
| Communication | Huffman decoder for seismic data decompression | 2014 | [733] |
| Communication | Multiple constant multiplication for FIR filter | 2014 | [734] |
| Simulation | Acceleration of MATLAB simulations | 2014 | [735] |
| Control engineering | PID controller | 2014 | [736] |
| Control engineering | Time measurement | 2014 | [737] |
| Prototyping | Triple modular redundancy voter | 2014 | [738] |
| Communication | Constant modulus algorithm for adaptive array antennas | 2014 | [739] |
| Communication | QR Processors for MIMO wireless communications | 2014 | [740] |
| Control engineering | Finite-state predictive speed and current control for a permanent magnet synchronous motor | 2014 | [741] |
| Cryptography | ChaCha, BLAKE, Threefish, and Skein | 2014 | [742] |
| Image processing | Runway boundary recognition for aircrafts | 2014 | [743] |
| Communication / Networks | Channel estimation in MIMO-OFDM system | 2014 | [744] |
| Control engineering | Z-source inverter controller | 2014 | [745] |
| Medical | Ultrasound digital beamformer with dynamic focusing | 2014 | [746] |
| Cryptography | Commutative RSA public key cryptography | 2014 | [747] |
| Medical | Processing of fast-scan cyclic voltammetry data for monitoring of brain neurochemistry | 2014 | [748] |
| Image processing | Real-time video stabilizer | 2014 | [749] |
| Image processing | PAL to XGA format conversion | 2014 | [750] |
| Networks | Data acquisition of a FDML Lasers for FBG accelerometer interrogation | 2014 | [751] |
| Image processing | Harris corner algorithms | 2014 | [752] |
| Medical | RFID identification | 2014 | [753] |
| Control engineering | Dedicated self control strategy for a delta inverter fed BDCM drive | 2014 | [754] |
| Bio-computing | Phylogenetic tree reconstruction | 2014 | [755] |
| Control engineering | Current feedback control for Pulse Width Modulation (PWM) inverter | 2014 | [756] |
| Prototyping | Uplink Transceiver for interleaved frequency domain multiple access passive optical network system | 2015 | [757] |
| Space / Image processing | HySime algorithm for spectral unmixing | 2015 | [758] |

| Field | Description | Year | Reference |
|---|---|---|---|
| Cryptography | AES algorithm | 2015 | [759] |
| Cryptography | Elliptic curve cryptography and authentication | 2015 | [760] |
| Image processing | Ultrasound imaging beamforming | 2015 | [761] |
| Bio-computing | Bowtie | 2015 | [762] |
| Control engineering | Delayed signal cancellation phase locked loop | 2015 | [763] |
| Networks | FlexRay communication controller | 2015 | [764] |
| Fuzzy logic | Direct torque control of an induction machine | 2015 | [765] |
| Cryptography | Weakening of AES and 3DES through bitstream modification | 2015 | [766] |
| Processor design | FFT-CoProcessor | 2015 | [767] |
| Communication / Networks | Finite Impulse Response (FIR) filter | 2015 | [768] |
| Communication | Finite impulse repsonse filter | 2015 | [769] |
| Cryptography | AES algorithm | 2015 | [770] |
| Neuro-computing | feed-forward neural network which employs backpropagation algorithm | 2015 | [771] |
| Image processing | Harris-Laplace variant of scale-invariant feature detection | 2015 | [772] |
| Medical | Non-invasive fetal heart rate monitoring | 2015 | [773] |
| Neuro-computing | Machine learning double arbiter-based physically unclonable function | 2015 | [774] |
| Image processing | Stereo vision system | 2015 | [775] |
| Bio-computing | SNP Arrays for detecting epistasis | 2015 | [776] |
| Processor design | WLAN channel specific ALU using GTL IO standard | 2015 | [777] |
| Communication | Flight termination system for software defined radio | 2015 | [778] |
| Networks | Recovery from multiple failures in multicore fiber links using FPGA-based optical switch units | 2015 | [779] |
| Mathematics | Fixed-width modified Baugh-Wooley multiplier | 2015 | [780] |
| Communication | Kernel least mean square algorithmus | 2015 | [781] |
| Space | Wavelet trigger in radio detection of cosmic rays | 2015 | [782] |
| Mathematics | 16-bit Vedic multiplier | 2015 | [783] |
| Control engineering | Real-time bearing fault diagnosis using ultrasampling rate acoustic emission signals | 2015 | [784] |
| Communication | Data-aided single-carrier frequency-domain equalizer for format-flexible receivers | 2015 | [785] |
| Control engineering | Modular multilevel converter pulse generation and capacitor voltage balance method | 2015 | [786] |
| Bio-computing | Basic Local Alignment Search Tool (BLASTN) wordmatching | 2015 | [787] |
| Control engineering / Communication | Voltage and current dual drive system for high frame rate electrical impedance tomography | 2015 | [788] |
| Neurocomputing / Image processing | Deep belief network architecture for character recognition using stochastic computation | 2015 | [789] |
| Biocomputing | BLESS implementation for DNA error correction | 2015 | [790] |
| Mathematics | Redundant basis (RB) multipliers over Galois field | 2015 | [791] |
| Image processing | COordinate Rotation DIgital Computer (CORDIC) algorithm for QR decomposition | 2015 | [792] |
| Image processing | Robert, Prewitt, Sobel operator based edge detection | 2015 | [793] |
| Medical | Communication infrastructure for electrocardiograms | 2015 | [794] |
| Control engineering | Data-driven predictive gearshift control | 2015 | [795] |
| Communication | measurements of AM/AM and AM-PM distortion curves | 2015 | [796] |
| Scheduling | Task scheduler for real-time soft-core processor base computing systems | 2015 | [797] |
| Simulation | Simulation of a chip-multiprocessor consisting of real and pseudo cores | 2015 | [798] |
| Communication | ear field inductive communication using frequency splitting and MIMO configuration | 2015 | [799] |
| Prototyping / Communication | De/Scrambler and De/Interleaver for digital video broadcasting satellite standard | 2015 | [800] |
| Neurocomputing | SOM and Hebbian network for hand sign recognition | 2015 | [801] |
| Data-Mining | Decision tree classification | 2015 | [802] |
| Control engineering | Linearised torque actuation for magnetorheological clutches | 2015 | [803] |
| Simulation | Real-time simulation of power electronic converters and electric drives | 2015 | [804] |
| Simulation / Scheduling | Performance analysis of various scheduling algorithms for a crossbar switch | 2015 | [805] |
| Simulation | Analytical space harmonic model of permanent magnet machines for hardware-in-the-loop simulation | 2015 | [806] |

[9] K. Leung, K. Ma, W. Wong, and P. Leong, "Fpga implementation of a microcoded elliptic curve cryptographic processor," in *Field-Programmable Custom Computing Machines, 2000 IEEE Symposium on*, 2000, pp. 68–76.

[10] M. Alderighi, S. D'Angelo, and G. Sechi, "Evidence: an fpga-based system for photon event identification and centroiding," in *Field-Programmable Custom Computing Machines, 2000 IEEE Symposium on*, 2000, pp. 259–266.

[11] C. Brueggen and H. J. Pottinger, "A novel fpga-based master/slave pci interface core," in *Circuits and Systems, 2000. Proceedings of the 43rd IEEE Midwest Symposium on*, vol. 1, 2000, pp. 162–163 vol.1.

[12] L. Carro and D. Franco, "Fpga based systems with linear and non-linear signal processing capabilities," in *Euromicro Conference, 2000. Proceedings of the 26th*, vol. 1, 2000, pp. 260–264 vol.1.

[13] M. Nibouche, A. Bouridane, O. Nibouche, D. Crookes, and S. Boussekta, "Design and fpga implementation of orthonormal discrete wavelet transforms," in *Electronics, Circuits and Systems, 2000. ICECS 2000. The 7th IEEE International Conference on*, vol. 1, 2000, pp. 312–315 vol.1.

[14] Y.-T. Hwang and J.-C. Han, "A novel fpga design of a wireless block transmission channel equalizer," in *ASICs, 2000. AP-ASIC 2000. Proceedings of the Second IEEE Asia Pacific Conference on*, 2000, pp. 119–122.

[15] C. Moreira, R. Freire, E. Melcher, G. Deep, S. Catunda, and R. Alves, "Fpga-based svpwm trigger generator for a 3 phi; voltage source inverter," in *Instrumentation and Measurement Technology Conference, 2000. IMTC 2000. Proceedings of the 17th IEEE*, vol. 1, 2000, pp. 174–178 vol.1.

[16] J. Jiang, D. Yu, and Z. Sun, "Real-time image processing system based on fpga for electronic endoscope," in *Circuits and Systems, 2000. IEEE APCCAS 2000. The 2000 IEEE Asia-Pacific Conference on*, 2000, pp. 682–685.

[17] M. McLoone and J. McCanny, "A high performance fpga implementation of des," in *Signal Processing Systems, 2000. SiPS 2000. 2000 IEEE Workshop on*, 2000, pp. 374–383.

[18] E. Elsehely and M. Sobhy, "Real time radar target detection under jamming conditions using wavelet transform on fpga device," in *Circuits and Systems, 2000. Proceedings. ISCAS 2000 Geneva. The 2000 IEEE International Symposium on*, vol. 4, 2000, pp. 545–548 vol.4.

[19] G. Lakshminarayanan, B. Venkataramani, K. Senthilkumar, and M. Kottapalli, "Design and implementation of fpga based wavepipelined fast convolver," in *TENCON 2000. Proceedings*, vol. 3, 2000, pp. 212–217 vol.3.

[20] A. Kim and M. Chang, "Designing a java microprocessor core using fpga technology," *Computing Control Engineering Journal*, vol. 11, no. 3, pp. 135–141, June 2000.

[21] A. Kayssi, L. Harik, R. Ferzli, and M. Fawaz, "Fpga-based internet protocol firewall chip," in *Electronics, Circuits and Systems, 2000. ICECS 2000. The 7th IEEE International Conference on*, vol. 1, 2000, pp. 316–319 vol.1.

[22] Y. Lian, "Fpga implementation of high speed multiplierless frequency response masking fir filters," in *Signal Processing Systems, 2000. SiPS 2000. 2000 IEEE Workshop on*, 2000, pp. 317–325.

[23] C. Ang, R. Turner, T. Courtney, and R. Woods, "Virtex fpga implementation of a polyphase filter for sample rate conversion," in *Signals, Systems and Computers, 2000. Conference Record of the Thirty-Fourth Asilomar Conference on*, vol. 1, Oct 2000, pp. 365–369 vol.1.

[24] Z. Aspar, Z. Yusof, and I. Suleiman, "Parallel huffman decoder with an optimized look up table option on fpga," in *TENCON 2000. Proceedings*, vol. 1, 2000, pp. 73–76 vol.1.

[25] J.-L. Danger, A. Ghazel, E. Boutillon, and H. Laamari, "Efficient fpga implementation of gaussian noise generator for communication channel emulation," in *Electronics, Circuits and Systems, 2000. ICECS 2000. The 7th IEEE International Conference on*, vol. 1, 2000, pp. 366–369 vol.1.

[26] Z. Mohd-Yusof, I. Suleiman, and Z. Aspar, "Implementation of two dimensional forward dct and inverse dct using fpga," in *TENCON 2000. Proceedings*, vol. 3, 2000, pp. 242–245 vol.3.

[27] M. Fukushi and S. Horiguchi, "Self-reconfigurable mesh array system on fpga," in *Defect and Fault Tolerance in VLSI Systems, 2000. Proceedings. IEEE International Symposium on*, 2000, pp. 240–248.

[28] M. Perko, I. Fajfar, T. Tuma, and J. Puhan, "Low-cost, high-performance cnn simulator implemented in fpga," in *Cellular Neural Networks and Their Applications, 2000. (CNNA 2000). Proceedings of the 2000 6th IEEE International Workshop on*, 2000, pp. 277–282.

[29] N. Ratha, A. Jain, and D. Rover, "Fpga-based coprocessor for text string extraction," in *Computer Architectures for Machine Perception, 2000. Proceedings. Fifth IEEE International Workshop on*, 2000, pp. 217–221.

[30] R. Ramos, X. Roset, and A. Manuel, "Implementation of fuzzy logic controller for dc/dc converters using field programmable gate array (fpga)," in *Instrumentation and Measurement Technology Conference, 2000. IMTC 2000. Proceedings of the 17th IEEE*, vol. 1, 2000, pp. 160–163 vol.1.

[31] R. Levy, S. Lepri, E. Sanchez, G. Ritter, and M. Sipper, "State of the art: an evolving fpga-based board for handwritten-digit recognition," in *Evolvable Hardware, 2000. Proceedings. The Second NASA/DoD Workshop on*, 2000, pp. 237–243.

[32] J. Gomes de Lima, E. Melchier, and H. Soares da Silva, "An fpga implementation of the atm layer," in *Integrated Circuits and Systems Design, 2000. Proceedings. 13th Symposium on*, 2000, pp. 185–190.

[33] S. Holgado, S. Lopez-Buedo, and A. Pearmain, "Fpga implementation of an atm traffic classifier for quality of service management," in *Electrotechnical Conference, 2000. MELECON 2000. 10th Mediterranean*, vol. 1, 2000, pp. 210–212 vol.1.

[34] D. Demigny, L. Kessal, R. Bourguiba, and N. Boudouani, "How to use high speed reconfigurable fpga for real time image processing?" in *Computer Architectures for Machine Perception, 2000. Proceedings. Fifth IEEE International Workshop on*, 2000, pp. 240–246.

[35] S. Ogrenci, K. Bazargan, and M. Sarrafzadeh, "Image analysis and partitioning for fpga implementation of image restoration," in *Signal Processing Systems, 2000. SiPS 2000. 2000 IEEE Workshop on*, 2000, pp. 346–355.

[36] H. Jianjun and L. Shuqin, "An alternative approach to using an fpga to implement dsp algorithms," in *Signal Processing Proceedings, 2000. WCCC-ICSP 2000. 5th International Conference on*, vol. 1, 2000, pp. 623–626 vol.1.

[37] C. Dick and F. Harris, "Fpga signal processing using sigma-delta modulation," *Signal Processing Magazine, IEEE*, vol. 17, no. 1, pp. 20–35, Jan 2000.

[38] J. Huang, C. Ong, K.-T. Cheng, and C. Wu, "An fpga-based reconfigurable functional tester for memory chips," in *Test Symposium, 2000. (ATS 2000). Proceedings of the Ninth Asian*, 2000, pp. 51–57.

[39] M. Re, G. Cardarilli, A. Del Re, and R. Lojacono, "Fpga implementation of a demux based on a multirate filter bank," in *Circuits and Systems, 2000. Proceedings. ISCAS 2000 Geneva. The 2000 IEEE International Symposium on*, vol. 5, 2000, pp. 353–356 vol.5.

[40] I. Y.-L. Hsiao and C.-W. Jen, "A new hardware design and fpga implementation for internet routing towards ip over wdm and terabit routers," in *Circuits and Systems, 2000. Proceedings. ISCAS 2000 Geneva. The 2000 IEEE International Symposium on*, vol. 1, 2000, pp. 387–390 vol.1.

[41] A. Amira, A. Bouridane, P. Milligan, and P. Sage, "A high throughput fpga implementation of a bit-level matrix product," in *Signal Processing Systems, 2000. SiPS 2000. 2000 IEEE Workshop on*, 2000, pp. 356–364.

[42] T. Pagarani, F. Kocan, D. Saab, and J. Abraham, "Parallel and scalable architecture for solving satisfiability on reconfigurable fpga," in *Custom Integrated Circuits Conference, 2000. CICC. Proceedings of the IEEE 2000*, 2000, pp. 147–150.

[43] K.-S. Oh, S.-Y. Yoon, and S.-I. Chae, "Emulator environment based on an fpga prototyping board," in *Rapid System Prototyping, 2000. RSP 2000. Proceedings. 11th International Workshop on*, 2000, pp. 72–77.

[44] L. Chaari, N. Masmoudi, and L. Kammoun, "Implementation on fpga of the mac transceiver in fddi system," in *Microelectronics, 1999. ICM '99. The Eleventh International Conference on*, Nov 2000, pp. 235–241.

[45] D. Kim, "An implementation of fuzzy logic controller on the reconfigurable fpga system," *Industrial Electronics, IEEE Transactions on*, vol. 47, no. 3, pp. 703–715, Jun 2000.

[46] D. Crookes, K. Benkrid, A. Bouridane, K. Alotaibi, and A. Benkrid, "Design and implementation of a high level programming environment for fpga-based image processing," *Vision, Image and Signal Processing, IEE Proceedings* -, vol. 147, no. 4, pp. 377–384, Aug 2000.

[47] D. Franco and L. Carro, "Fpga architecture comparison for non-conventional signal processing," in *Neural Networks, 2000. IJCNN*

*2000, Proceedings of the IEEE-INNS-ENNS International Joint Conference on*, vol. 2, 2000, pp. 55–58 vol.2.

[48] M. Miwa, T. Furuhashi, M. Matsuzaki, and S. Okuma, "Cmac modeling using bacterial evolutionary algorithm (bea) on field programmable gate array (fpga)," in *Industrial Electronics Society, 2000. IECON 2000. 26th Annual Confjerence of the IEEE*, vol. 1, 2000, pp. 644–650 vol.1.

[49] C. Ciressan, E. Sanchez, M. Rajman, and J.-C. Chappelier, "An fpga-based coprocessor for the parsing of context-free grammars," in *Field-Programmable Custom Computing Machines, 2000 IEEE Symposium on*, 2000, pp. 236–245.

[50] H. Restrepo, R. Hoffmann, A. Perez-Uribe, C. Teuscher, and E. Sanchez, "A networked fpga-based hardware implementation of a neural network application," in *Field-Programmable Custom Computing Machines, 2000 IEEE Symposium on*, 2000, pp. 337–338.

[51] S. Demirsoy, A. Dempster, and I. Kale, "Transition analysis on fpga for multiplier-block based fir filter structures," in *Electronics, Circuits and Systems, 2000. ICECS 2000. The 7th IEEE International Conference on*, vol. 2, 2000, pp. 862–865 vol.2.

[52] M. Khalil Hani, T. S. Lin, and N. Shaikh-Husin, "Fpga implementation of rsa public-key cryptographic coprocessor," in *TENCON 2000. Proceedings*, vol. 3, 2000, pp. 6–11 vol.3.

[53] O. Leung, C. ying Tsui, and R. Cheng, "Vlsi implementation of rake receiver for is-95 cdma testbed using fpga," in *Design Automation Conference, 2000. Proceedings of the ASP-DAC 2000. Asia and South Pacific*, June 2000, pp. 3–4.

[54] J. Ritter and P. Molitor, "A partitioned wavelet-based approach for image compression using fpga's," in *Custom Integrated Circuits Conference, 2000. CICC. Proceedings of the IEEE 2000*, 2000, pp. 547–550.

[55] H. Noori, H. Pedram, A. Akbari, and S. Sheidaei, "Fpga implementation of a dsp core for full rate and half rate gsm vocoders," in *Microelectronics, 2000. ICM 2000. Proceedings of the 12th International Conference on*, Oct 2000, pp. 273–276.

[56] G. Lienhart, R. Lay, K. Noffz, and R. Manner, "An fpga-based video compressor for h.263 compatible bitstreams," in *Consumer Electronics, 2000. ICCE. 2000 Digest of Technical Papers. International Conference on*, June 2000, pp. 320–321.

[57] J. Lima, J. Corleta, A. Medeiros, V. Canalli, F. Antunes, F. Libano, and F. Dos Reis, "A pic controller for grid connected pv system using a fpga based inverter," in *Industrial Electronics, 2000. ISIE 2000. Proceedings of the 2000 IEEE International Symposium on*, vol. 1, 2000, pp. 169–173 vol.1.

[58] N. Botros, "Modeling and realizing biological mechanisms on fpga chip," in *Engineering in Medicine and Biology Society, 2000. Proceedings of the 22nd Annual International Conference of the IEEE*, vol. 3, 2000, pp. 1921–1922 vol.3.

[59] J. J.-L. Kuo, C.-C. Tsai, L. Lai, T. Chen, and T. Ding, "Integrated fpga based asic design on error code correction counter for ups telecommunication," in *Power Electronics and Drive Systems, 2001. Proceedings., 2001 4th IEEE International Conference on*, vol. 2, Oct 2001, pp. 512–516 vol.2.

[60] D. Deng, S. Chen, and G. Joos, "Fpga implementation of pwm pattern generators," in *Electrical and Computer Engineering, 2001. Canadian Conference on*, vol. 2, 2001, pp. 1279–1284 vol.2.

[61] M. Kim, K. Ichige, and H. Arai, "Fpga-based dsp implementation of simple mrc beamformer," in *Microwave Conference, 2001. APMC 2001. 2001 Asia-Pacific*, vol. 2, Dec 2001, pp. 589–592 vol.2.

[62] J. Bonilla, V. Grisales, and M. Melgarejo, "Genetic tuned fpga based pd fuzzy lut controller," in *Fuzzy Systems, 2001. The 10th IEEE International Conference on*, vol. 3, 2001, pp. 1084–1087.

[63] J. Gause, C. Reuter, H. Kropp, P. Cheung, and W. Luk, "The effect of fpga granularity on video codec implementations," in *Field-Programmable Custom Computing Machines, 2001. FCCM '01. The 9th Annual IEEE Symposium on*, March 2001, pp. 287–288.

[64] P. Civera, L. Macchiarulo, M. Rebaudengo, M. Sonza Reorda, and M. Violante, "Exploiting fpga-based techniques for fault injection campaigns on vlsi circuits," in *Defect and Fault Tolerance in VLSI Systems, 2001. Proceedings. 2001 IEEE International Symposium on*, 2001, pp. 250–258.

[65] P. McCurry, F. Morgan, and L. Kilmartin, "Xilinx fpga implementation of an image classifier for object detection applications," in *Image Processing, 2001. Proceedings. 2001 International Conference on*, vol. 3, 2001, pp. 346–349 vol.3.

[66] M. Nibouche, A. Bouridane, D. Crookes, and O. Nibouche, "An fpga-based wavelet transforms coprocessor," in *Image Processing, 2001. Proceedings. 2001 International Conference on*, vol. 3, 2001, pp. 194–197 vol.3.

[67] A. Amira, A. Bouridane, P. Milligan, and M. Roula, "An fpga implementation of walsh-hadamard transforms for signal processing," in *Acoustics, Speech, and Signal Processing, 2001. Proceedings. (ICASSP '01). 2001 IEEE International Conference on*, vol. 2, 2001, pp. 1105–1108 vol.2.

[68] M. Gschwind, V. Salapura, and D. Maurer, "Fpga prototyping of a risc processor core for embedded applications," *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on*, vol. 9, no. 2, pp. 241–250, April 2001.

[69] T. Hisakado, T. Nishimura, and K. Okumura, "Hardware implementation of moore test on fpga," in *Circuits and Systems, 2002. ISCAS 2002. IEEE International Symposium on*, vol. 1, 2002, pp. I–653–I–656 vol.1.

[70] M. Nibouche, A. Bouridane, O. Nibouche, and A. Belatreche, "Design and fpga implementation of orthonormal inverse discrete wavelet transforms," in *Wireless Communications, 2001. (SPAWC '01). 2001 IEEE Third Workshop on Signal Processing Advances in*, 2001, pp. 356–359.

[71] K. Kaluri, W. F. Leong, K.-H. Tan, L. Johnson, and M. Soderstrand, "Comparison of rns and optimized fir digital filters in xilinx fpga's," in *Circuits and Systems, 2001. MWSCAS 2001. Proceedings of the 44th IEEE 2001 Midwest Symposium on*, vol. 1, 2001, pp. 438–441 vol.1.

[72] S. Abeysekera and C. Charoensak, "Performance evaluation of 3rd order sigma-delta ( sigma;- utri;) modulators via fpga implementation," in *ASIC/SOC Conference, 2001. Proceedings. 14th Annual IEEE International*, 2001, pp. 13–17.

[73] P. Leong, C. Sham, W. Wong, H. Wong, W. Yuen, and M. Leong, "A bitstream reconfigurable fpga implementation of the wsat algorithm," *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on*, vol. 9, no. 1, pp. 197–201, Feb 2001.

[74] S. Laggoune, "Establishment of an algorithm for detecting the multi-scale contours in the forms of fpga circuits," in *Electrical and Computer Engineering, 2001. Canadian Conference on*, vol. 2, 2001, pp. 1205–1210 vol.2.

[75] D. Guan, S. Yu, C. Liang, and X. Wang, "Mpeg-2 ts generate system and its implementation with fpga," in *ASIC, 2001. Proceedings. 4th International Conference on*, 2001, pp. 510–513.

[76] C. Kuo, S. Odeh, and M. Huang, "Image segmentation with improved watershed algorithm and its fpga implementation," in *Circuits and Systems, 2001. ISCAS 2001. The 2001 IEEE International Symposium on*, vol. 2, May 2001, pp. 753–756 vol. 2.

[77] S. Korah and S. McDonald, "Towards the implementation of a wcdma aaa receiver on an fpga software radio platform," in *Vehicular Technology Conference, 2001. VTC 2001 Spring. IEEE VTS 53rd*, vol. 3, 2001, pp. 1917–1921 vol.3.

[78] A. Amira, A. Bouridane, and P. Milligan, "An fpga based walsh hadamard transforms," in *Circuits and Systems, 2001. ISCAS 2001. The 2001 IEEE International Symposium on*, vol. 2, May 2001, pp. 569–572 vol. 2.

[79] J. Deepakumara, H. Heys, and R. Venkatesan, "Fpga implementation of md5 hash algorithm," in *Electrical and Computer Engineering, 2001. Canadian Conference on*, vol. 2, 2001, pp. 919–924 vol.2.

[80] A. Benkrid, D. Crookes, and K. Benkrid, "Design and implementation of a generic 2-d biorthogonal discrete wavelet transform on an fpga," in *Field-Programmable Custom Computing Machines, 2001. FCCM '01. The 9th Annual IEEE Symposium on*, March 2001, pp. 190–198.

[81] Z. Guiqing, F. Tao, Z. Hang, W. Jianhua, XuHong, G. Yingsan, and Z. Shiquan, "The implementation of digital protection in power system using fpga," in *ASIC, 2001. Proceedings. 4th International Conference on*, 2001, pp. 474–477.

[82] V. Hlukhov and A. Melnik, "The real-time digital color converter core for xilinx fpga," in *CAD Systems in Microelectronics, 2001. CADSM 2001. Proceedings of the 6th International Conference. The Experience of Designing and Application of*, Feb 2001, pp. 103–106.

[83] L. Limin, Z. Salcic, and L. Dong, "Fpga hardware devices with single-instruction driving for an embedded mobile computing platform," in *ASIC, 2001. Proceedings. 4th International Conference on*, 2001, pp. 514–517.

[84] S. Budge and C. O'Brien, "Design of an fpga-based high-speed filter-decimator for the gifts imaging interferometer," in *Signals, Systems*

*and Computers, 2001. Conference Record of the Thirty-Fifth Asilomar Conference on*, vol. 2, Nov 2001, pp. 1357–1361 vol.2.

[85] A. Amira, A. Bouridane, P. Milligan, and M. Roula, "Novel fpga implementations of walsh-hadamard transforms for signal processing," *Vision, Image and Signal Processing, IEE Proceedings* -, vol. 148, no. 6, pp. 377–383, Dec 2001.

[86] L. DeBrunner, V. DeBrunner, X. Hu, O. Demuynck, and A. Swartztrauber, "A reduced-space half-band filter design on an actel fpga," in *Signals, Systems and Computers, 2001. Conference Record of the Thirty-Fifth Asilomar Conference on*, vol. 2, Nov 2001, pp. 1237–1240 vol.2.

[87] Y. Lian and P. M. Hwee, "Fpga implementation of is-95 cdma baseband filter," in *ASIC, 2001. Proceedings. 4th International Conference on*, 2001, pp. 411–415.

[88] N. Arana-Arejolaleiba, M. Briot, C. Ganibal, A. Nketsa, and R. Prajoux, "A 3d laser micro-sensor integrating control and data processing in an fpga-based calculator," in *3-D Digital Imaging and Modeling, 2001. Proceedings. Third International Conference on*, 2001, pp. 107–114.

[89] M. Krstic and M. Stojcev, "Fpga implementation of hardware voter," in *Telecommunications in Modern Satellite, Cable and Broadcasting Service, 2001. TELSIKS 2001. 5th International Conference on*, vol. 2, 2001, pp. 401–404 vol.2.

[90] L. Cong and W. Xiaofu, "Design and realization of an fpga-based generator for chaotic frequency hopping sequences," *Circuits and Systems I: Fundamental Theory and Applications, IEEE Transactions on*, vol. 48, no. 5, pp. 521–532, May 2001.

[91] I. Mihu, R. Brad, and M. Breazu, "Specifications and fpga implementation of a systolic hopfield-type associative memory," in *Neural Networks, 2001. Proceedings. IJCNN '01. International Joint Conference on*, vol. 1, 2001, pp. 228–233 vol.1.

[92] A. Mozsary, L. Azzinari, K. Krol, and V. Porra, "Theoretical connection between pn-sequences and chaos makes simple fpga pseudo-chaos sources possible," in *Electronics, Circuits and Systems, 2001. ICECS 2001. The 8th IEEE International Conference on*, vol. 1, 2001, pp. 457–460 vol.1.

[93] F. Monteiro, A. Dandache, A. M'sir, and B. Lepley, "A fast crc implementation on fpga using a pipelined architecture for the polynomial division," in *Electronics, Circuits and Systems, 2001. ICECS 2001. The 8th IEEE International Conference on*, vol. 3, 2001, pp. 1231–1234 vol.3.

[94] E. Jamro and K. Wiatr, "Convolution operation implemented in fpga structures for real-time image processing," in *Image and Signal Processing and Analysis, 2001. ISPA 2001. Proceedings of the 2nd International Symposium on*, 2001, pp. 417–422.

[95] M. Leong, C. Jin, and P. Leong, "Parameterized module generator for an fpga-based electronic cochlea," in *Field-Programmable Custom Computing Machines, 2001. FCCM '01. The 9th Annual IEEE Symposium on*, March 2001, pp. 21–30.

[96] N. Batani, C. Thibeault, and C. Gargour, "An efficient fpga implementation of a pulse-shaping iir filter," in *Electrical and Computer Engineering, 2001. Canadian Conference on*, vol. 1, 2001, pp. 353–355 vol.1.

[97] L. Longfei and Y. Songyu, "Real-time duplex digital video surveillance system and its implementation with fpga," in *ASIC, 2001. Proceedings. 4th International Conference on*, 2001, pp. 471–473.

[98] M. McLoone and J. McCanny, "Rijndael fpga implementation utilizing look-up tables," in *Signal Processing Systems, 2001 IEEE Workshop on*, 2001, pp. 349–360.

[99] P. McWilliams, S. McLaughlin, D. Laurenson, W. Collis, M. Weston, and P. White, "Non-linear filtering for broadcast television: a real-time fpga implementation," in *Image Processing, 2001. Proceedings. 2001 International Conference on*, vol. 3, 2001, pp. 354–357 vol.3.

[100] M. Loulou, N. Masmoudi, and L. Kamoun, "Fpga-based ic design for inverter with vector modulation technique," in *Microelectronics, 2001. ICM 2001 Proceedings. The 13th International Conference on*, Oct 2001, pp. 185–188.

[101] J. Luker and V. Prasad, "Risc system design in an fpga," in *Circuits and Systems, 2001. MWSCAS 2001. Proceedings of the 44th IEEE 2001 Midwest Symposium on*, vol. 2, 2001, pp. 532–536 vol.2.

[102] T. Hisakado and K. Okumura, "An application of wavelet transform to fault location and its implementation on fpga," in *Circuits and Systems, 2001. MWSCAS 2001. Proceedings of the 44th IEEE 2001 Midwest Symposium on*, vol. 2, 2001, pp. 528–531 vol.2.

[103] A. Elbirt, W. Yip, B. Chetwynd, and C. Paar, "An fpga-based performance evaluation of the aes block cipher candidate algorithm finalists," *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on*, vol. 9, no. 4, pp. 545–557, Aug 2001.

[104] M. Alderighi, S. D'Angelo, C. Metra, and G. Sechi, "Novel fault-tolerant adder design for fpga-based systems," in *On-Line Testing Workshop, 2001. Proceedings. Seventh International*, 2001, pp. 54–58.

[105] G. Kiryukhin and M. Celenk, "Implementation of 2d-dct on xc4000 series fpga using dft-based dsfg and da architectures," in *Image Processing, 2001. Proceedings. 2001 International Conference on*, vol. 3, 2001, pp. 302–305 vol.3.

[106] J. Hudec and M. Hust'ava, "Design of the neural processor optimized for xilinx virtex fpga devices," in *Information Technology Interfaces, 2001. ITI 2001. Proceedings of the 23rd International Conference on*, June 2001, pp. A7–A8 vol. 2.

[107] P. Civera, L. Macchiarulo, M. Rebaudengo, M. Reorda, and M. Violante, "Fpga-based fault injection for microprocessor systems," in *Test Symposium, 2001. Proceedings. 10th Asian*, 2001, pp. 304–309.

[108] M. Alderighi, F. Casini, S. D'Angelo, D. Salvi, and G. Sechi, "A fault-tolerance strategy for an fpga-based multi-stage interconnection network in a multi-sensor system for space application," in *Defect and Fault Tolerance in VLSI Systems, 2001. Proceedings. 2001 IEEE International Symposium on*, 2001, pp. 191–199.

[109] G. Cardarilli, A. Del Re, A. Nannarelli, and M. Re, "Power characterization of digital filters implemented on fpga," in *Circuits and Systems, 2002. ISCAS 2002. IEEE International Symposium on*, vol. 5, 2002, pp. V–801–V–804 vol.5.

[110] T. Hamamoto, S. Nagao, and K. Aizawa, "Real-time objects tracking by using smart image sensor and fpga," in *Image Processing. 2002. Proceedings. 2002 International Conference on*, vol. 3, 2002, pp. III–441–III–444 vol.3.

[111] Y. Chen and W. du Plessis, "Neural network implementation on a fpga," in *Africon Conference in Africa, 2002. IEEE AFRICON. 6th*, vol. 1, Oct 2002, pp. 337–342 vol.1.

[112] M. Sima, S. Cotofana, S. Vassiliadis, J. van Eijndhoven, and K. Vissers, "Mpeg-compliant entropy decoding on fpga-augmented trimedia/cpu64," in *Field-Programmable Custom Computing Machines, 2002. Proceedings. 10th Annual IEEE Symposium on*, 2002, pp. 261–270.

[113] W. Wang, M. Swamy, and M. Ahmad, "A new architecture of rrns error-correcting qc encoder/decoder and its fpga implementation," in *Circuits and Systems, 2002. ISCAS 2002. IEEE International Symposium on*, vol. 5, 2002, pp. V–813–V–816 vol.5.

[114] M. Bednara, M. Daldrup, J. Teich, von zur Gathen, and J. Shokrollahi, "Tradeoff analysis of fpga based elliptic curve cryptography," in *Circuits and Systems, 2002. ISCAS 2002. IEEE International Symposium on*, vol. 5, 2002, pp. V–797–V–800 vol.5.

[115] D. Benitez, "Performance of remote fpga-based coprocessors for image-processing applications," in *Digital System Design, 2002. Proceedings. Euromicro Symposium on*, 2002, pp. 268–275.

[116] Y. Fu and W. Kinsner, "A marine engine torsion vibration measuring method and its implementation based on fpga," in *Electrical and Computer Engineering, 2002. IEEE CCECE 2002. Canadian Conference on*, vol. 1, 2002, pp. 488–493 vol.1.

[117] W. du Plessis, "Optimal mac structures in an fpga," in *Africon Conference in Africa, 2002. IEEE AFRICON. 6th*, vol. 1, Oct 2002, pp. 333–336 vol.1.

[118] A. Perez-Pascual, T. Sansaloni, and J. Valls, "Fpga-based radix-4 butterflies for hiperlan/2," in *Circuits and Systems, 2002. ISCAS 2002. IEEE International Symposium on*, vol. 3, 2002, pp. III–277–III–280 vol.3.

[119] C. Chitu, D. Chien, C. Chien, I. Verbauwhede, and F. Chang, "A hardware implementation in fpga of the rijndael algorithm," in *Circuits and Systems, 2002. MWSCAS-2002. The 2002 45th Midwest Symposium on*, vol. 1, Aug 2002, pp. I–507–10 vol.1.

[120] G. Baruffa, S. Caeopardi, and S. Soazzi, "Fpga implementation of a multimodal sample rate converter and synchronizer," in *Personal, Indoor and Mobile Radio Communications, 2002. The 13th IEEE International Symposium on*, vol. 1, Sept 2002, pp. 447–451 vol.1.

[121] M. Garrido, C. Sanz, M. Jimenez, and J. Meneses, "A flexible h.263 video coder prototype based on fpga," in *Rapid System Prototyping, 2002. Proceedings. 13th IEEE International Workshop on*, 2002, pp. 34–41.

[122] G. Girau, M. Martina, A. Molino, A. Terreno, and F. Vacca, "Fpga digital down converter ip for sdr terminals," in *Signals, Systems and Computers, 2002. Conference Record of the Thirty-Sixth Asilomar Conference on*, vol. 2, Nov 2002, pp. 1010–1014 vol.2.

[123] J. Chen, J. Moon, and K. Bazargan, "A reconfigurable fpga-based readback signal generator for hard-drive read channel simulator," in *Design Automation Conference, 2002. Proceedings. 39th*, 2002, pp. 349–354.

[124] I. Mezei and V. Malbasa, "Formal specification of an fpga based educational microprocessor," in *Microelectronics, 2002. MIEL 2002. 23rd International Conference on*, vol. 2, 2002, pp. 667–670.

[125] D. Tong, P. S. Lo, K. H. Lee, and P. Leong, "A system level implementation of rijndael on a memory-slot based fpga card," in *Field-Programmable Technology, 2002. (FPT). Proceedings. 2002 IEEE International Conference on*, Dec 2002, pp. 102–109.

[126] M. Aseeri, M. Sobhy, and P. Lee, "Lorenz chaotic model using filed programmable gate array (fpga)," in *Circuits and Systems, 2002. MWSCAS-2002. The 2002 45th Midwest Symposium on*, vol. 1, Aug 2002, pp. I–527–30 vol.1.

[127] W. Pora and P. Siriluangtong, "A tv ghost canceller using fpga-based fir filters," in *Circuits and Systems, 2002. APCCAS '02. 2002 Asia-Pacific Conference on*, vol. 2, 2002, pp. 289–292 vol.2.

[128] T. Nuteson, I. Clark, J.S., D. Haque, and G. Mitchell, "Digital beamforming and calibration for smart antennas using real-time fpga processing," in *Microwave Symposium Digest, 2002 IEEE MTT-S International*, vol. 1, June 2002, pp. 307–310 vol.1.

[129] M.-H. Jing, C. Hsu, T. Truong, Y. Chen, and Y. Chang, "The diversity study of aes on fpga application," in *Field-Programmable Technology, 2002. (FPT). Proceedings. 2002 IEEE International Conference on*, Dec 2002, pp. 390–393.

[130] V. Tomashau, "Efficient 4-input luts fpga implementation of combinatorial multiplier over canonical base gf(16)," in *Field-Programmable Technology, 2002. (FPT). Proceedings. 2002 IEEE International Conference on*, Dec 2002, pp. 318–321.

[131] I. Ibanez, M. Aguirre, A. Torralba, and L. Franquelo, "A low cost 3d vision system for positioning welding mobile robots using a fpga prototyping system," in *IECON 02 [Industrial Electronics Society, IEEE 2002 28th Annual Conference of the]*, vol. 2, Nov 2002, pp. 1590–1593 vol.2.

[132] Y. Nakamura and K. Hiraki, "Highly fault-tolerant fpga processor by degrading strategy," in *Dependable Computing, 2002. Proceedings. 2002 Pacific Rim International Symposium on*, Dec 2002, pp. 75–78.

[133] J. Martín-Langerwerf, C. Reuter, H. Kropp, and P. Pirsch, "Benefits of macro-based multi-fpga partitioning for video processing applications," in *Rapid System Prototyping, 2002. Proceedings. 13th IEEE International Workshop on*, 2002, pp. 60–65.

[134] M. Garrido, C. Sanz, M. Jimenez, and J. Meneses, "An fpga implementation of a flexible architecture for h.263 video coding," in *Consumer Electronics, 2002. ICCE. 2002 Digest of Technical Papers. International Conference on*, June 2002, pp. 274–275.

[135] P. Leong and I. Leung, "A microcoded elliptic curve processor using fpga technology," *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on*, vol. 10, no. 5, pp. 550–559, Oct 2002.

[136] F. Cardells-Tormo and J. Valls-Coquillat, "Optimized fpga-implementation of quadrature dds," in *Circuits and Systems, 2002. ISCAS 2002. IEEE International Symposium on*, vol. 5, 2002, pp. V–369–V–372 vol.5.

[137] T. Aoyama, Q. Wang, R. Suematsu, R. Shimizu, and U. Nagashima, "Learning algorithms for a neural network in fpga," in *Neural Networks, 2002. IJCNN '02. Proceedings of the 2002 International Joint Conference on*, vol. 1, 2002, pp. 1007–1012.

[138] B. Lee and N. Burgess, "Parameterisable floating-point operations on fpga," in *Signals, Systems and Computers, 2002. Conference Record of the Thirty-Sixth Asilomar Conference on*, vol. 2, Nov 2002, pp. 1064–1068 vol.2.

[139] S. Zhaoyan, D. Yonggui, G. Wenxiu, X. Xanping, M. Cheng, J. Huibo, and F. Guanping, "An fpga-based interface for recording high-speed data stream," in *Communications, Circuits and Systems and West Sino Expositions, IEEE 2002 International Conference on*, vol. 2, June 2002, pp. 1466–1470 vol.2.

[140] S. Hezel, A. Kugel, R. Manner, and D. Gavrila, "Fpga-based template matching using distance transforms," in *Field-Programmable Custom Computing Machines, 2002. Proceedings. 10th Annual IEEE Symposium on*, 2002, pp. 89–97.

[141] J.-C. Huang, M.-H. Chen, and J.-J. Shyu, "Implementation of the turbo-tcm and space-time code modulation with fpga in transceiver," in *Consumer Electronics, 2002. ICCE. 2002 Digest of Technical Papers. International Conference on*, June 2002, pp. 358–359.

[142] T. Zhang and K. Parhi, "A 54 mbps (3,6)-regular fpga ldpc decoder," in *Signal Processing Systems, 2002. (SIPS '02). IEEE Workshop on*, Oct 2002, pp. 127–132.

[143] T. Nuteson, J. Stocker, I. Clark, J.S., D. Haque, and G. Mitchell, "Performance characterization of fpga techniques for calibration and beamforming in smart antenna applications," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 50, no. 12, pp. 3043–3051, Dec 2002.

[144] M. Guntsch, M. Middendorf, B. Scheuermann, O. Diessel, H. ElGindy, H. Schmeck, and K. So, "Population based ant colony optimization on fpga," in *Field-Programmable Technology, 2002. (FPT). Proceedings. 2002 IEEE International Conference on*, Dec 2002, pp. 125–132.

[145] M. Wakamura and Y. Maeda, "Fpga implementation of bidirectional associative memory via simultaneous perturbation rule," in *SICE 2002. Proceedings of the 41st SICE Annual Conference*, vol. 3, Aug 2002, pp. 1631–1632 vol.3.

[146] M. Boulé and Z. Zilic, "An fpga based move generator for the game of chess," in *Custom Integrated Circuits Conference, 2002. Proceedings of the IEEE 2002*, 2002, pp. 71–74.

[147] S. Melnikoff, S. Quigley, and M. Russell, "Implementing a simple continuous speech recognition system on an fpga," in *Field-Programmable Custom Computing Machines, 2002. Proceedings. 10th Annual IEEE Symposium on*, 2002, pp. 275–276.

[148] J. H. Koo, T. S. Kim, S. S. Dong, and C. H. Lee, "Development of fpga based adaptive image enhancement filter system using genetic algorithms," in *Evolutionary Computation, 2002. CEC '02. Proceedings of the 2002 Congress on*, vol. 2, 2002, pp. 1480–1485.

[149] T. Chakraborty and C.-H. Chiang, "A novel fault injection method for system verification based on fpga boundary scan architecture," in *Test Conference, 2002. Proceedings. International*, 2002, pp. 923–929.

[150] M. Epperly, B. Walls, and M. Wasiewicz, "Fpga ccsds command decoder with bch edac and level-0 command execution," in *Aerospace Conference Proceedings, 2002. IEEE*, vol. 4, 2002, pp. 4–1909–4–1916 vol.4.

[151] T. Mitra and T. cker Chiueh, "An fpga implementation of triangle mesh decompression," in *Field-Programmable Custom Computing Machines, 2002. Proceedings. 10th Annual IEEE Symposium on*, 2002, pp. 22–31.

[152] Y. Hori, M. Sonoyama, and T. Maruyama, "An fpga-based processor for shogi mating problems," in *Field-Programmable Technology, 2002. (FPT). Proceedings. 2002 IEEE International Conference on*, Dec 2002, pp. 117–124.

[153] A. Al-Dhaher, E. Petriu, and M. Dostaler, "Fpga correlator architecture using random-pulse data representation," in *Instrumentation and Measurement Technology Conference, 2002. IMTC/2002. Proceedings of the 19th IEEE*, vol. 2, 2002, pp. 1061–1063 vol.2.

[154] P. Arribas and F.-H. Macia, "Fpga board for real time vision development systems," in *Devices, Circuits and Systems, 2002. Proceedings of the Fourth IEEE International Caracas Conference on*, 2002, pp. T021–1–T021–6.

[155] O. Cheung and P. Leong, "Implementation of an fpga based accelerator for virtual private networks," in *Field-Programmable Technology, 2002. (FPT). Proceedings. 2002 IEEE International Conference on*, Dec 2002, pp. 34–41.

[156] B. Umamaheswari, "Fpga based fuzzy computation accelerator," in *Fuzzy Systems, 2002. FUZZ-IEEE'02. Proceedings of the 2002 IEEE International Conference on*, vol. 1, 2002, pp. 352–357.

[157] M. Garrido, C. Sanz, M. Jimenez, and J. Menesses, "An fpga implementation of a flexible architecture for h.263 video coding," *Consumer Electronics, IEEE Transactions on*, vol. 48, no. 4, pp. 1056–1066, Nov 2002.

[158] H. Elgindy and Y.-L. Shue, "On sparse matrix-vector multiplication with fpga-based system," in *Field-Programmable Custom Computing Machines, 2002. Proceedings. 10th Annual IEEE Symposium on*, 2002, pp. 273–274.

[159] S. Memik, A. Katsaggelos, and M. Sarrafzadeh, "Analysis and fpga implementation of image restoration under resource constraints," *Computers, IEEE Transactions on*, vol. 52, no. 3, pp. 390–399, March 2003.

[160] D. Carrica, M. A. Funes, and S. Gonzalez, "Novel stepper motor controller based on fpga hardware implementation," *Mechatronics, IEEE/ASME Transactions on*, vol. 8, no. 1, pp. 120–124, March 2003.

[161] A. de Castro, P. Zumel, O. Garcia, T. Riesgo, and J. Uceda, "Concurrent and simple digital controller of an ac/dc converter with power factor correction based on an fpga," *Power Electronics, IEEE Transactions on*, vol. 18, no. 1, pp. 334–343, Jan 2003.

[162] R. Ramos, D. Biel, E. Fossas, and F. Guinjoan, "A fixed-frequency quasi-sliding control algorithm: application to power inverters design by means of fpga implementation," *Power Electronics, IEEE Transactions on*, vol. 18, no. 1, pp. 344–355, Jan 2003.

[163] Y. Maeda and T. Tada, "Fpga implementation of a pulse density neural network with learning ability using simultaneous perturbation," *Neural Networks, IEEE Transactions on*, vol. 14, no. 3, pp. 688–695, May 2003.

[164] K. Lam and S. Mak, "An fpga-based eigenfilter using fast hebbian learning," in *Acoustics, Speech, and Signal Processing, 2003. Proceedings. (ICASSP '03). 2003 IEEE International Conference on*, vol. 2, April 2003, pp. II–765–8 vol.2.

[165] S. Sharma, S. Attri, and F. Chauhan, "A simplified and efficient implementation of fpga-based turbo decoder," in *Performance, Computing, and Communications Conference, 2003. Conference Proceedings of the 2003 IEEE International*, April 2003, pp. 207–213.

[166] J. Velten and A. Kummert, "High-speed fpga-implementation of multi-dimensional binary morphological operations," in *Circuits and Systems, 2003. ISCAS '03. Proceedings of the 2003 International Symposium on*, vol. 3, May 2003, pp. III–706–III–709 vol.3.

[167] A. Yonemoto, T. Hisakado, and K. Okumura, "An implementation of numerical inversion of laplace transforms on fpga," in *Circuits and Systems, 2003. ISCAS '03. Proceedings of the 2003 International Symposium on*, vol. 4, May 2003, pp. IV–492–IV–495 vol.4.

[168] C. Grabbe, M. Bednara, J. Teich, von zur Gathen, and J. Shokrollahi, "Fpga designs of parallel high performance gf(2233) multipliers [cryptographic applications]," in *Circuits and Systems, 2003. ISCAS '03. Proceedings of the 2003 International Symposium on*, vol. 2, May 2003, pp. II–268–II–271 vol.2.

[169] M. Guo, M. Ahmad, M. Swamy, and C. Wang, "A low-power systolic array-based adaptive viterbi decoder and its fpga implementation," in *Circuits and Systems, 2003. ISCAS '03. Proceedings of the 2003 International Symposium on*, vol. 2, May 2003, pp. II–276–II–279 vol.2.

[170] S. Saif, H. Abbas, and S. Nassar, "Fpga implementation of block truncation coding algorithm for gray scale images," in *Circuits and Systems, 2003. ISCAS '03. Proceedings of the 2003 International Symposium on*, vol. 2, May 2003, pp. II–448–II–451 vol.2.

[171] M. Shibu, C.-H. Chang, and R. Xiao, "Fpga implementation of a frequency adaptive learning sofm for digital color still imaging," in *Circuits and Systems, 2003. ISCAS '03. Proceedings of the 2003 International Symposium on*, vol. 2, May 2003, pp. II–452–II–455 vol.2.

[172] M. A. Soderstrand, "Csd multipliers for fpga dsp applications," in *Circuits and Systems, 2003. ISCAS '03. Proceedings of the 2003 International Symposium on*, vol. 5, May 2003, pp. V–469–V–472 vol.5.

[173] Z. Nagy and P. Szolgay, "Configurable multilayer cnn-um emulator on fpga," *Circuits and Systems I: Fundamental Theory and Applications, IEEE Transactions on*, vol. 50, no. 6, pp. 774–778, June 2003.

[174] J. Valls and E. Boemo, "Efficient fpga-implementation of two's complement digit-serial/parallel multipliers," *Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on*, vol. 50, no. 6, pp. 317–322, June 2003.

[175] M. Sima, S. Vassiliadis, S. Cotofana, and J. van Eijndhoven, "Color space conversion for mpeg decoding on fpga-augmented trimedia processor," in *Application-Specific Systems, Architectures, and Processors, 2003. Proceedings. IEEE International Conference on*, June 2003, pp. 250–259.

[176] J.-L. Beuchat, "Modular multiplication for fpga implementation of the idea block cipher," in *Application-Specific Systems, Architectures, and Processors, 2003. Proceedings. IEEE International Conference on*, June 2003, pp. 412–422.

[177] H. Emam, M. Ashour, H. Fekry, and A. Wahdan, "Introducing an fpga based genetic algorithms in the applications of blind signals separation," in *System-on-Chip for Real-Time Applications, 2003. Proceedings. The 3rd IEEE International Workshop on*, June 2003, pp. 123–127.

[178] A. Lin, K. Gugel, and J. Principe, "Feasibility of fixed-point transversal adaptive filters in fpga devices with embedded dsp blocks," in *System-on-Chip for Real-Time Applications, 2003. Proceedings. The 3rd IEEE International Workshop on*, June 2003, pp. 157–160.

[179] T. Lin and Z. Zhengou, "The implementation of 100mhz data acquisition based on fpga," in *System-on-Chip for Real-Time Applications, 2003. Proceedings. The 3rd IEEE International Workshop on*, June 2003, pp. 287–291.

[180] X. Wang and S. Ziavras, "Parallel direct solution of linear equations on fpga-based machines," in *Parallel and Distributed Processing Symposium, 2003. Proceedings. International*, April 2003, pp. 8 pp.–.

[181] G. Rouvroy, F.-X. Standaert, J.-J. Quisquater, and J. Legat, "Efficient fpga implementation of block cipher misty1," in *Parallel and Distributed Processing Symposium, 2003. Proceedings. International*, April 2003, pp. 7 pp.–.

[182] S. McBader and P. Lee, "An fpga implementation of a flexible, parallel image processing architecture suitable for embedded vision systems," in *Parallel and Distributed Processing Symposium, 2003. Proceedings. International*, April 2003, pp. 5 pp.–.

[183] R. Ramos, D. Biel, E. Fossas, and F. Guinjoan, "Control of single-phase parallel-connected inverters: fixed-frequency quasisliding mode control approach and fpga-based implementation," in *Power Electronics Specialist Conference, 2003. PESC '03. 2003 IEEE 34th Annual*, vol. 3, June 2003, pp. 1426–1431 vol.3.

[184] S. Elagooz, N. Hamdy, K. Shehata, and M. Helmy, "Design and implementation of high and low modulo (216 + 1) multiplier used in idea algorithm on fpga," in *Radio Science Conference, 2003. NRSC 2003. Proceedings of the Twentieth National*, March 2003, pp. C10–1–10.

[185] K. Vinger and J. Torresen, "Implementing evolution of fir-filters efficiently in an fpga," in *Evolvable Hardware, 2003. Proceedings. NASA/DoD Conference on*, July 2003, pp. 26–29.

[186] S. Berto, S. Bolognani, M. Ceschia, A. Paccagnella, and M. Zigliotto, "Fpga-based random pwm with real-time dead time compensation," in *Power Electronics Specialist Conference, 2003. PESC '03. 2003 IEEE 34th Annual*, vol. 2, June 2003, pp. 513–518 vol.2.

[187] F. Rodriguez-Henriquez, N. Saqib, and A. Diaz-Perez, "4.2 gbit/s single-chip fpga implementation of aes algorithm," *Electronics Letters*, vol. 39, no. 15, pp. 1115–1116, July 2003.

[188] S. Mekhilef and N. Rahim, "Fpga based asic power-factor control for three-phase inverter," in *Control Applications, 2003. CCA 2003. Proceedings of 2003 IEEE Conference on*, vol. 1, June 2003, pp. 594–597 vol.1.

[189] C. Gao and D. Hammerstrom, "Platform performance comparison of palm network on pentium 4 and fpga," in *Neural Networks, 2003. Proceedings of the International Joint Conference on*, vol. 2, July 2003, pp. 995–1000 vol.2.

[190] I. Uzun, A. Amira, A. Ahmedsaid, and F. Bensaali, "Towards a general framework for an fpga-based fft coprocessor," in *Signal Processing and Its Applications, 2003. Proceedings. Seventh International Symposium on*, vol. 1, July 2003, pp. 617–620 vol.1.

[191] A. Amira and A. Bouridane, "An fpga implementation of discrete hartley transforms," in *Signal Processing and Its Applications, 2003. Proceedings. Seventh International Symposium on*, vol. 1, July 2003, pp. 625–628 vol.1.

[192] M. Martina, A. Molino, A. Terreno, and F. Vacca, "Fpga implementation of a reconfigurable spiht coprocessor," in *Signal Processing and Its Applications, 2003. Proceedings. Seventh International Symposium on*, vol. 2, July 2003, pp. 605–606 vol.2.

[193] N. Matsumoto, K. Ichige, and H. Arai, "Fixed-point digital processing of recursive least-square algorithm toward fpga implementation of mmse adaptive array antenna," in *Signal Processing and Its Applications, 2003. Proceedings. Seventh International Symposium on*, vol. 2, July 2003, pp. 615–617 vol.2.

[194] J.-H. Li, T. Li, M.-C. Tsai, and S.-H. Lin, "Design and implementation of dynamic weighted fuzzy sliding-mode controller for an fpga-based inverted pendulum car," in *Advanced Intelligent Mechatronics, 2003. AIM 2003. Proceedings. 2003 IEEE/ASME International Conference on*, vol. 1, July 2003, pp. 628–633 vol.1.

[195] S. Saif, S. Nassar, H. Abbas, and A. Soliman, "Fpga implementation of block truncation coding algorithm for gray scale and color images," in *Electrical and Computer Engineering, 2003. IEEE CCECE 2003. Canadian Conference on*, vol. 1, May 2003, pp. 23–26 vol.1.

[196] Q. Liu, J. Langlois, D. Al-Khalili, V. Szwarc, and R. Inkol, "Synthesis of a 12-bit complex mixer for fpga implementation," in *Electrical*

*and Computer Engineering, 2003. IEEE CCECE 2003. Canadian Conference on*, vol. 1, May 2003, pp. 81–84 vol.1.

[197] M. Song, J. Song, and H. Li, "Implementing a high performance scheduling discipline wf2q+ in fpga," in *Electrical and Computer Engineering, 2003. IEEE CCECE 2003. Canadian Conference on*, vol. 1, May 2003, pp. 187–190 vol.1.

[198] Y. Wu and Y. Shayan, "Implementation of high-speed multi-level qam modems based on xilinx virtex-ii fpga," in *Electrical and Computer Engineering, 2003. IEEE CCECE 2003. Canadian Conference on*, vol. 1, May 2003, pp. 195–198 vol.1.

[199] S. Singh and K. Rattan, "Implementation of a fuzzy logic controller on an fpga using vhdl," in *Fuzzy Information Processing Society, 2003. NAFIPS 2003. 22nd International Conference of the North American*, July 2003, pp. 110–115.

[200] K. Tsoi, K. Leung, and P. Leong, "Compact fpga-based true and pseudo random number generators," in *Field-Programmable Custom Computing Machines, 2003. FCCM 2003. 11th Annual IEEE Symposium on*, April 2003, pp. 51–61.

[201] A. Benkrid, K. Benkrid, and D. Crookes, "Design and implementation of a generic 2d orthogonal discrete wavelet transform on fpga," in *Field-Programmable Custom Computing Machines, 2003. FCCM 2003. 11th Annual IEEE Symposium on*, April 2003, pp. 162–172.

[202] S. Li, G. Cheuk, K. Lee, and P. Leong, "Fpga-based simd processor," in *Field-Programmable Custom Computing Machines, 2003. FCCM 2003. 11th Annual IEEE Symposium on*, April 2003, pp. 267–268.

[203] J. Durbano, F. Ortiz, J. Humphrey, D. Prather, and M. Mirotznik, "Implementation of three-dimensional fpga-based fdtd solvers: an architectural overview," in *Field-Programmable Custom Computing Machines, 2003. FCCM 2003. 11th Annual IEEE Symposium on*, April 2003, pp. 269–270.

[204] T. Xiao-Heng and Y. Shi-Zhong, "The design and fpga realization of the long pn code acquisition circuit based on digital matched-filter," in *ASIC, 2003. Proceedings. 5th International Conference on*, vol. 2, Oct 2003, pp. 744–747 Vol.2.

[205] S. Abbasi, "Fpga based realization of a reduced complexity high speed decoder for error correction," in *Electronics, Circuits and Systems, 2003. ICECS 2003. Proceedings of the 2003 10th IEEE International Conference on*, vol. 3, Dec 2003, pp. 1002–1005 Vol.3.

[206] A. Ahmedsaid, A. Amira, and A. Bouridane, "Improved svd systolic array and implementation on fpga," in *Field-Programmable Technology (FPT), 2003. Proceedings. 2003 IEEE International Conference on*, Dec 2003, pp. 35–42.

[207] D. Allred, V. Krishnan, W. Huang, and D. Anderson, "Implementation of an lms adaptive filter on an fpga employing multiplexed multiplier architecture," in *Signals, Systems and Computers, 2004. Conference Record of the Thirty-Seventh Asilomar Conference on*, vol. 1, Nov 2003, pp. 918–921 Vol.1.

[208] A. Amira, "An fpga based system for discrete hartley transforms," in *Visual Information Engineering, 2003. VIE 2003. International Conference on*, July 2003, pp. 137–140.

[209] C. Chareonsak, F. Sana, Y. Wei, and X. Bing, "Design of fpga hardware for a real-time blind source separation of fetal ecg signals," in *Biomedical Circuits and Systems, 2004 IEEE International Workshop on*, Dec 2004, pp. S2/4–13–16.

[210] L. Bu and J. Chandy, "Fpga based network intrusion detection using content addressable memories," in *Field-Programmable Custom Computing Machines, 2004. FCCM 2004. 12th Annual IEEE Symposium on*, April 2004, pp. 316–317.

[211] Z. Du, L. Tolbert, and J. Chiasson, "Active harmonic elimination in multilevel converters using fpga control," in *Computers in Power Electronics, 2004. Proceedings. 2004 IEEE Workshop on*, Aug 2004, pp. 127–132.

[212] L. Bo, W. Zhensong, Y. Ping, and L. Minfeng, "A novel algorithm for fpga-based sar doppler center frequency estimation," in *Signal Processing, 2004. Proceedings. ICSP '04. 2004 7th International Conference on*, vol. 3, Aug 2004, pp. 2186–2189 vol.3.

[213] C. Donninger, A. Kure, and U. Lorenz, "Parallel brutus: the first distributed, fpga accelerated chess program," in *Parallel and Distributed Processing Symposium, 2004. Proceedings. 18th International*, April 2004, pp. 44–.

[214] P. Boonyanant and S. Tan-a ram, "Fpga implementation of a subspace tracker based on a recursive unitary esprit algorithm," in *TENCON 2004. 2004 IEEE Region 10 Conference*, vol. A, Nov 2004, pp. 547–550 Vol. 1.

[215] M. Canet, F. Vicedo, J. Valls, and V. Almenar, "Design of a digital front-end transmitter for ofdm-wlan systems using fpga," in *Control, Communications and Signal Processing, 2004. First International Symposium on*, 2004, pp. 503–506.

[216] M. Avogadro, M. Bera, G. Danese, F. Leporati, and A. Spelgatti, "The totem neurochip: an fpga implementation," in *Signal Processing and Information Technology, 2004. Proceedings of the Fourth IEEE International Symposium on*, Dec 2004, pp. 461–464.

[217] S. Bellis, K. Razeeb, C. Saha, K. Delaney, C. O'Mathuna, A. Pounds-Cornish, G. de Souza, M. Colley, H. Hagras, G. Clarke, V. Callaghan, C. Argyropoulos, C. Karistianos, and G. Nikiforidis, "Fpga implementation of spiking neural networks - an initial step towards building tangible collaborative autonomous agents," in *Field-Programmable Technology, 2004. Proceedings. 2004 IEEE International Conference on*, Dec 2004, pp. 449–452.

[218] B. Brown, M.-L. Yin, and Y. Cheng, "Dna sequence matching processor using fpga and java interface," in *Engineering in Medicine and Biology Society, 2004. IEMBS '04. 26th Annual International Conference of the IEEE*, vol. 2, Sept 2004, pp. 3043–3046.

[219] S. Bolognani, M. Ceschia, P. Mattavelli, A. Paccagnella, and M. Zigliotto, "Improved fpga-based dead time compensation for svm inverters," in *Power Electronics, Machines and Drives, 2004. (PEMD 2004). Second International Conference on (Conf. Publ. No. 498)*, vol. 2, March 2004, pp. 662–667 Vol.2.

[220] D. Boppana, K. Dhanoa, and J. Kempa, "Fpga based embedded processing architecture for the qrd-rls algorithm," in *Field-Programmable Custom Computing Machines, 2004. FCCM 2004. 12th Annual IEEE Symposium on*, April 2004, pp. 330–331.

[221] C. Dick and F. Harris, "Options for arbitrary resamplers in fpga-based modulators," in *Signals, Systems and Computers, 2004. Conference Record of the Thirty-Eighth Asilomar Conference on*, vol. 1, Nov 2004, pp. 777–781 Vol.1.

[222] R. Djemal, D. Demigny, and R. Tourki, "A real time video smoothing implementation inside an fpga-based system," in *Microelectronics, 2004. ICM 2004 Proceedings. The 16th International Conference on*, Dec 2004, pp. 152–156.

[223] M. Canet, F. Vicedo, V. Almenar, and J. Valls, "Fpga implementation of an if transceiver for ofdm-based wlan," in *Signal Processing Systems, 2004. SIPS 2004. IEEE Workshop on*, Oct 2004, pp. 227–232.

[224] D. Denning, J. Irvine, and M. Devlin, "Compact iterative fpga camellia algorithm implementations," in *Field-Programmable Technology, 2004. Proceedings. 2004 IEEE International Conference on*, Dec 2004, pp. 311–314.

[225] C. Castro-Pareja, J. Jagadeesh, S. Venugopal, and R. Shekhar, "Fpga-based 3d median filtering using word-parallel systolic arrays," in *Circuits and Systems, 2004. ISCAS '04. Proceedings of the 2004 International Symposium on*, vol. 3, May 2004, pp. III–157–60 Vol.3.

[226] C. Charoensak and F. Sattar, "System-level design of low-cost fpga hardware for real-time ica-based blind source separation," in *SOC Conference, 2004. Proceedings. IEEE International*, Sept 2004, pp. 139–140.

[227] B. Ahn, B. Kim, and T. Chang, "A sliding-dft based power-line phase measurement algorithm and its fpga implementation," in *Developments in Power System Protection, 2004. Eighth IEE International Conference on*, vol. 1, April 2004, pp. 44–47 Vol.1.

[228] Y. Chan, M. Moallem, and W. Wang, "Efficient implementation of pid control algorithm using fpga technology," in *Decision and Control, 2004. CDC. 43rd IEEE Conference on*, vol. 5, Dec 2004, pp. 4885–4890 Vol.5.

[229] D. Bariamis, D. Iakovidis, D. Maroulis, and S. Karkanis, "An fpga-based architecture for real time image feature extraction," in *Pattern Recognition, 2004. ICPR 2004. Proceedings of the 17th International Conference on*, vol. 1, Aug 2004, pp. 801–804 Vol.1.

[230] D. Diaz and J. Paredes, "Fpga implementation of a new family of stack filters," in *Devices, Circuits and Systems, 2004. Proceedings of the Fifth IEEE International Caracas Conference on*, vol. 1, Nov 2004, pp. 152–157.

[231] C. Cecati, A. Dell'Aquila, A. Lecci, M. Liserre, and V. Monopoli, "Fpga-based multilevel modulations for h-bridge-based converters," in *Industrial Electronics, 2004 IEEE International Symposium on*, vol. 2, May 2004, pp. 957–962 vol. 2.

[232] R. Cumplido, C. Torres, and S. Lopez, "On the implementation of an efficient fpga-based cfar processor for target detection," in *Electrical*

*and Electronics Engineering, 2004. (ICEEE). 1st International Conference on*, Sept 2004, pp. 214–218.

[233] S. Bouchoux, E.-B. Bourennane, J. Miteran, and M. Paindavoine, "Implementation of jpeg2000 arithmetic decoder on a dynamically reconfigurable atmel fpga," in *VLSI, 2004. Proceedings. IEEE Computer society Annual Symposium on*, Feb 2004, pp. 237–238.

[234] C. Charoensak and S. Abeysekera, "Fpga implementation of efficient kalman band-pass sigma-delta filter for application in fm demodulation," in *SOC Conference, 2004. Proceedings. IEEE International*, Sept 2004, pp. 137–138.

[235] C. Doss and J. Riley, R.L., "Fpga-based implementation of a robust ieee-754 exponential unit," in *Field-Programmable Custom Computing Machines, 2004. FCCM 2004. 12th Annual IEEE Symposium on*, April 2004, pp. 229–238.

[236] A. Descampe, F. Devaux, G. Rouvroy, B. Macq, and J.-D. Legat, "An efficient fpga implementation of a flexible jpeg2000 decoder for digital cinema," in *Signal Processing Conference, 2004 12th European*, Sept 2004, pp. 2019–2022.

[237] P. Chalimbaud and F. Berry, "Design of an imaging system based on fpga technology and cmos imager," in *Field-Programmable Technology, 2004. Proceedings. 2004 IEEE International Conference on*, Dec 2004, pp. 407–411.

[238] D. Allred, W. Huang, V. Krishnan, H. Yoo, and D. Anderson, "An fpga implementation for a high throughput adaptive filter using distributed arithmetic," in *Field-Programmable Custom Computing Machines, 2004. FCCM 2004. 12th Annual IEEE Symposium on*, April 2004, pp. 324–325.

[239] Z. Zhao-Yong, X. Zheng, and L. Tie-Cai, "Fpga implementation of a new hybrid rotor position estimation scheme based on three symmetrical locked hall effect position sensors," in *Power Electronics and Motion Control Conference, 2004. IPEMC 2004. The 4th International*, vol. 3, Aug 2004, pp. 1592–1596 Vol.3.

[240] D. Dawoud and S. Masupe, "Design and fpga implementation of digit-serial fir filters," in *AFRICON, 2004. 7th AFRICON Conference in Africa*, vol. 1, Sept 2004, pp. 203–209 Vol.1.

[241] S. Bouchoux, E.-B. Bourennane, and M. Paindavoine, "Implementation of jpeg2000 arithmetic decoder using dynamic reconfiguration of fpga," in *Image Processing, 2004. ICIP '04. 2004 International Conference on*, vol. 4, Oct 2004, pp. 2841–2844 Vol. 4.

[242] W. Chia, L. Jeganathan, M. Ibne-Reaz, and F. Mohd-Yasin, "The fpga approach in the design and development of an automated rail transit system controller," in *Semiconductor Electronics, 2004. ICSE 2004. IEEE International Conference on*, Dec 2004, pp. 5 pp.–.

[243] G. de Dormale, P. Bulens, and J.-J. Quisquater, "An improved montgomery modular inversion targeted for efficient implementation on fpga," in *Field-Programmable Technology, 2004. Proceedings. 2004 IEEE International Conference on*, Dec 2004, pp. 441–444.

[244] R. Dobias and H. Kubatova, "Fpga based design of the railway's interlocking equipments," in *Digital System Design, 2004. DSD 2004. Euromicro Symposium on*, Aug 2004, pp. 467–473.

[245] M. Baghaie A, S. Kuo, and I. McLoughlin, "Fpga implementation of space-time block coding systems," in *Emerging Technologies: Frontiers of Mobile and Wireless Communication, 2004. Proceedings of the IEEE 6th Circuits and Systems Symposium on*, vol. 2, May 2004, pp. 591–594 Vol.2.

[246] S. Buzzetti, M. Capou, C. Guazzoni, A. Longoni, R. Mariani, and S. Moser, "Multichannel data acquisition system based on fpga for high resolution spectroscopy," in *Nuclear Science Symposium Conference Record, 2004 IEEE*, vol. 3, Oct 2004, pp. 1458–1462 Vol. 3.

[247] Y. Abhyankar, C. Sajish, P. Kulkarni, and C. Subrahmanya, "Design of a fpga based data acquisition system for radio astronomy applications," in *Microelectronics, 2004. ICM 2004 Proceedings. The 16th International Conference on*, Dec 2004, pp. 555–557.

[248] S. Cooper, A. Kuperman, and R. Rabinovici, "Controlling an electrical motion system by a load instruction decoding algorithm using fpga," in *Electronics, Circuits and Systems, 2004. ICECS 2004. Proceedings of the 2004 11th IEEE International Conference on*, Dec 2004, pp. 443–446.

[249] K. Ben Khalifa, B. Girau, F. Alexandre, and M. Bedoui, "Parallel fpga implementation of self-organizing maps," in *Microelectronics, 2004. ICM 2004 Proceedings. The 16th International Conference on*, Dec 2004, pp. 709–712.

[250] D. Allred, H. Yoo, V. Krishnan, W. Huang, and D. Anderson, "A novel high performance distributed arithmetic adaptive filter implementation on an fpga," in *Acoustics, Speech, and Signal Processing, 2004. Proceedings. (ICASSP '04). IEEE International Conference on*, vol. 5, May 2004, pp. V–161–4 vol.5.

[251] C. Clarke and L. Qiang, "Bat on an fpga: a biomimetic implementation of a highly parallel signal processing system," in *Signals, Systems and Computers, 2004. Conference Record of the Thirty-Eighth Asilomar Conference on*, vol. 1, Nov 2004, pp. 456–460 Vol.1.

[252] F. Crowe, A. Daly, T. Kerins, and W. Marnane, "Single-chip fpga implementation of a cryptographic co-processor," in *Field-Programmable Technology, 2004. Proceedings. 2004 IEEE International Conference on*, Dec 2004, pp. 279–285.

[253] J.-L. Beuchat and J.-M. Muller, "Modulo m multiplication-addition: algorithms and fpga implementation," *Electronics Letters*, vol. 40, no. 11, pp. 654–655, May 2004.

[254] R. Dubey, P. Agarwal, and M. Vasantha, "Fpga based pmac motor control for system-on-chip applications," in *Power Electronics Systems and Applications, 2004. Proceedings. 2004 First International Conference on*, Nov 2004, pp. 194–200.

[255] H. Du and H. Qi, "An fpga implementation of parallel ica for dimensionality reduction in hyperspectral images," in *Geoscience and Remote Sensing Symposium, 2004. IGARSS '04. Proceedings. 2004 IEEE International*, vol. 5, Sept 2004, pp. 3257–3260 vol.5.

[256] N. Bu, T. Hamamoto, T. Tsuji, and O. Fukuda, "Fpga implementation of a probabilistic neural network for a bioelectric human interface," in *Circuits and Systems, 2004. MWSCAS '04. The 2004 47th Midwest Symposium on*, vol. 3, July 2004, pp. iii–29–32 vol.3.

[257] M. Balzer and H. Stripf, "Blackfin-fpga multiprocessor system for ultrasonic-data reduction," in *Control, Communications and Signal Processing, 2004. First International Symposium on*, March 2004, pp. 841–844.

[258] M. Cui, H. Murata, and K. Araki, "Fpga implementation of 4 times;4 mimo test-bed for spatial multiplexing systems," in *Personal, Indoor and Mobile Radio Communications, 2004. PIMRC 2004. 15th IEEE International Symposium on*, vol. 4, Sept 2004, pp. 3045–3048 Vol.4.

[259] S. Bates and G. Block, "A memory-based architecture for fpga implementations of low-density parity-check convolutional decoders," in *Circuits and Systems, 2005. ISCAS 2005. IEEE International Symposium on*, May 2005, pp. 336–339 Vol. 1.

[260] P. Bhagawat, M. Uppal, and G. Choi, "Fpga based implementation of decoder for array low-density parity-check codes," in *Acoustics, Speech, and Signal Processing, 2005. Proceedings. (ICASSP '05). IEEE International Conference on*, vol. 5, March 2005, pp. v/29–v/32 Vol. 5.

[261] F. Cardells-Tormo, P.-L. Molinet, J. Sempere-Agullo, L. Baldez, and M. Bautista-Palacios, "Area-efficient 2d shift-variant convolvers for fpga-based digital image processing," in *Field Programmable Logic and Applications, 2005. International Conference on*, Aug 2005, pp. 578–581.

[262] M. Boukadourn, K. Tabari, A. Bensaoula, D. Starikov, and E. Aboulhamid, "Fpga implementation of a cdma source coding and modulation subsystem for a multiband fluorometer with pattern recognition capabilities," in *Circuits and Systems, 2005. ISCAS 2005. IEEE International Symposium on*, May 2005, pp. 4767–4770 Vol. 5.

[263] K. Banovic, M. Khalid, and E. Abdel-Raheem, "Fpga-based rapid prototyping of digital signal processing systems," in *Circuits and Systems, 2005. 48th Midwest Symposium on*, Aug 2005, pp. 647–650 Vol. 1.

[264] G. Cardarilli, S. Pontarelli, M. Re, and A. Salsano, "Fpga oriented design of parity sharing rs codecs," in *Defect and Fault Tolerance in VLSI Systems, 2005. DFT 2005. 20th IEEE International Symposium on*, Oct 2005, pp. 259–265.

[265] M. Baig, F. Niaz, and A. Mukhtar, "Tri-state based shifters in fpga: Comparison and optimization," in *Microelectronics, 2005. ICM 2005. The 17th International Conference on*, Dec 2005, pp. 247–250.

[266] C. Brunelli, F. Garzia, J. Nurmi, C. Mucci, F. Campi, and D. Rossi, "A fpga implementation of an open-source floating-point computation system," in *System-on-Chip, 2005. Proceedings. 2005 International Symposium on*, Nov 2005, pp. 29–32.

[267] Z. Cao, J. Kang, and P. Fan, "An fpga implementation of a structured irregular ldpc decoder," in *Microwave, Antenna, Propagation and EMC Technologies for Wireless Communications, 2005. MAPE 2005. IEEE International Symposium on*, vol. 2, Aug 2005, pp. 1050–1053 Vol. 2.

[268] J. Beeckler and W. Gross, "Fpga particle graphics hardware," in *Field-Programmable Custom Computing Machines, 2005. FCCM 2005. 13th Annual IEEE Symposium on*, April 2005, pp. 85–94.

[269] A. Aloisio, V. Izzo, and S. Rampone, "Fpga implementation of a greedy algorithm for set covering," in *Real Time Conference, 2005. 14th IEEE-NPSS*, June 2005, pp. 5 pp.–.

[270] A. Ben Salem, S. Ben Othman, and S. Ben Saoud, "Design and implementation of a neural command rule on a fpga circuit," in *Electronics, Circuits and Systems, 2005. ICECS 2005. 12th IEEE International Conference on*, Dec 2005, pp. 1–4.

[271] V. Bocci, G. Chiodi, F. Iacoangeli, R. Nobrega, D. Pinci, and W. Rinaldi, "Time-multiplexing of signal using highly integrated digital delay: an fpga implementation," in *Nuclear Science Symposium Conference Record, 2005 IEEE*, vol. 1, Oct 2005, pp. 398–402.

[272] F. Angarita, A. Perez-Pascual, T. Sansaloni, and J. Valls, "Efficient mapping on fpga of a viterbi decoder for wireless lans," in *Signal Processing Systems Design and Implementation, 2005. IEEE Workshop on*, Nov 2005, pp. 710–715.

[273] F. Carvalho, I. Jansch-Porto, E. Freitas, and C. Pereira, "The tinycan: an optimized can controller ip for fpga-based platforms," in *Emerging Technologies and Factory Automation, 2005. ETFA 2005. 10th IEEE Conference on*, vol. 1, Sept 2005, pp. 4 pp.–374.

[274] M. Abe, H. Arai, and M. Kawamata, "Design and fpga implementation of a structure of evolutionary digital filters for hardware implementation," in *Circuits and Systems, 2005. ISCAS 2005. IEEE International Symposium on*, May 2005, pp. 528–531 Vol. 1.

[275] L. Agostini, R. Porto, S. Bampi, and I. Silva, "A fpga based design of a multiplierless and fully pipelined jpeg compressor," in *Digital System Design, 2005. Proceedings. 8th Euromicro Conference on*, Aug 2005, pp. 210–213.

[276] S. Anvar, O. Gachelin, P. Kestener, H. Le Provost, and I. Mandjavidze, "Fpga-based system-on-chip designs for real-time applications in particle physics," in *Real Time Conference, 2005. 14th IEEE-NPSS*, June 2005, pp. 5 pp.–.

[277] J. Bastos, L. Farronato, H. Figueroa, D. Franzoni, S. Lentijo, A. Monti, A. Smith, and X. Wu, "Fpga-based control of power converter: Comparing alternative solutions," in *Applied Power Electronics Conference and Exposition, 2005. APEC 2005. Twentieth Annual IEEE*, vol. 3, Mar. 2005, pp. 1983 – 1989.

[278] A. AlKalbany, H. Al Hassan, and M. Saeb, "Fpga implementation of the "pyramids" block cipher," in *SOC Conference, 2005. Proceedings. IEEE International*, Sept 2005, pp. 271–275.

[279] F. Cardells-Tormo and P. Molinet, "Area-efficient 2-d shift-variant convolvers for fpga-based digital image processing," in *Signal Processing Systems Design and Implementation, 2005. IEEE Workshop on*, Nov 2005, pp. 209–213.

[280] A. Brokalakis, A. Kakarountas, and C. Goutis, "A high-throughput area efficient fpga implementation of aes-128 encryption," in *Signal Processing Systems Design and Implementation, 2005. IEEE Workshop on*, Nov 2005, pp. 116–121.

[281] B. Catanzaro and B. Nelson, "Higher radix floating-point representations for fpga-based arithmetic," in *Field-Programmable Custom Computing Machines, 2005. FCCM 2005. 13th Annual IEEE Symposium on*, April 2005, pp. 161–170.

[282] S. Chappell, A. Macarthur, D. Preston, D. Olmstead, B. Flint, and C. Sullivan, "Exploiting real-time fpga based adaptive systems technology for real-time sensor fusion in next generation automotive safety systems," in *Design, Automation and Test in Europe, 2005. Proceedings*, March 2005, pp. 180–185 Vol. 3.

[283] M. Babic and K. Dostert, "An fpga-based high-speed emulation system for powerline channels," in *Power Line Communications and Its Applications, 2005 International Symposium on*, April 2005, pp. 290–294.

[284] S. Buzzetti, M. Capou, C. Guazzoni, A. Longoni, R. Mariani, and S. Moser, "High-speed fpga-based pulse-height analyzer for high resolution x-ray spectroscopy," *Nuclear Science, IEEE Transactions on*, vol. 52, no. 4, pp. 854–860, Aug 2005.

[285] F. Angarita, A. Perez-Pascual, T. Sansaloni, and J. Vails, "Efficient fpga implementation of cordic algorithm for circular and linear coordinates," in *Field Programmable Logic and Applications, 2005. International Conference on*, Aug 2005, pp. 535–538.

[286] R. Bannister, D. Gregg, S. Wilson, and A. Nisbet, "Fpga implementation of an image segmentation algorithm using logarithmic arithmetic," in *Circuits and Systems, 2005. 48th Midwest Symposium on*, Aug 2005, pp. 810–813 Vol. 1.

[287] C. Charoensak and S. Abeysekera, "System on chip fpga design of an fm demodulator using a kalman band-pass sigma-delta architecture," in *Circuits and Systems, 2005. ISCAS 2005. IEEE International Symposium on*, May 2005, pp. 33–36 Vol. 1.

[288] M. Abdelhalim, H. Aslan, and H. Farouk, "A design for an fpga-based implementation of rijndael cipher," in *Information and Communications Technology, 2005. Enabling Technologies for the New Knowledge Society: ITI 3rd International Conference on*, Dec 2005, pp. 897–912.

[289] P. Arena, L. Fortuna, G. Vagliasindi, and A. Basile, "Cnn chip and fpga to explore complexity," in *Cellular Neural Networks and Their Applications, 2005 9th International Workshop on*, May 2005, pp. 154–157.

[290] O. Callanan, A. Nisbet, E. Ozer, J. Sexton, and D. Gregg, "Fpga implementation of a lattice quantum chromodynamics algorithm using logarithmic arithmetic," in *Parallel and Distributed Processing Symposium, 2005. Proceedings. 19th IEEE International*, April 2005, pp. 146b–146b.

[291] G. Acher, C. Trinitis, and R. Buchty, "Cpu-independent assembler in an fpga," in *Field Programmable Logic and Applications, 2005. International Conference on*, Aug 2005, pp. 519–522.

[292] D. Bianchi, G. Cardarilli, A. Del Re, A. Malatesta, and M. Re, "Fpga implementation of a general purpose hmm processor based on token passing algorithm," in *Circuit Theory and Design, 2005. Proceedings of the 2005 European Conference on*, vol. 1, Aug 2005, pp. I/285–I/288 vol. 1.

[293] M. Bautista-Palacios, L. Baldez, J. Sempere-Agullo, F. Cardells-Tormo, P. Molinet, and A. Herms-Berenguer, "Configurable hardware/software architecture for data acquisition implementation on fpga," in *Field Programmable Logic and Applications, 2005. International Conference on*, Aug 2005, pp. 241–246.

[294] O. Al-Ayasrah, T. Alukaidey, and G. Pissanidis, "Mixed signal dsp based multi task motion control system using external fpga structural design," in *INDICON, 2005 Annual IEEE*, Dec 2005, pp. 419–422.

[295] C. Chad, Z. Qin, X. Yingke, and H. Chengde, "Design of a high performance fft processor based on fpga," in *Design Automation Conference, 2005. Proceedings of the ASP-DAC 2005. Asia and South Pacific*, vol. 2, Jan 2005, pp. 920–923 Vol. 2.

[296] O. Cadenas, G. Megson, and D. Jones, "A new organization for a perceptron-based branch predictor and its fpga implementation," in *VLSI, 2005. Proceedings. IEEE Computer Society Annual Symposium on*, May 2005, pp. 305–306.

[297] W. Ashmanskas, S. Hansen, T. Kiper, and D. Peterson, "Fpga-based instrumentation for the fermilab antiproton source," in *Particle Accelerator Conference, 2005. PAC 2005. Proceedings of the*, May 2005, pp. 1159–1161.

[298] C. Canesin and F. Gonçalves, "A 2kw interleaved zcs-fm boost rectifier digitally controlled by fpga device," in *Power Electronics Specialists Conference, 2005. PESC '05. IEEE 36th*, June 2005, pp. 513–518.

[299] Z. Abid, W. Wang, and Y. Chen, "Low-power fpga implementation for da-based video processing," in *VLSI Design and Video Technology, 2005. Proceedings of 2005 IEEE International Workshop on*, May 2005, pp. 361–364.

[300] D. Bemmann, "Ip lookup on a platform fpga: A comparative study," in *Parallel and Distributed Processing Symposium, 2005. Proceedings. 19th IEEE International*, April 2005, pp. 166a–166a.

[301] O. Cadenas, G. Megson, and D. Jones, "Fpga organization for the fast path-based neural branch predictor," in *Field-Programmable Technology, 2005. Proceedings. 2005 IEEE International Conference on*, Dec 2005, pp. 251–257.

[302] E. Cetin, S. Demirsoy, I. Kale, and R. Morling, "Efficient fpga implementation of an adaptive iq-imbalance corrector for communication receivers using reduced range multipliers," in *Signal Processing Conference, 2005 13th European*, Sept 2005, pp. 1–4.

[303] A. Alsuwailem and S. Alshebeili, "A new approach for real-time histogram equalization using fpga," in *Intelligent Signal Processing and Communication Systems, 2005. ISPACS 2005. Proceedings of 2005 International Symposium on*, Dec 2005, pp. 397–400.

[304] A. Aziz and N. Ikram, "An efficient fpga based sequential implementation of advanced encryption standard," in *Information and Communications Technology, 2005. Enabling Technologies for the New Knowledge Society: ITI 3rd International Conference on*, Dec 2005, pp. 875–882.

[305] K. Appiah and A. Hunter, "A single-chip fpga implementation of real-time adaptive background model," in *Field-Programmable Technology, 2005. Proceedings. 2005 IEEE International Conference on*, Dec 2005, pp. 95–102.

[306] C. Bolchini, P. Ferrandi, P. Lanzi, and F. Salice, "Toward an fpga implementation of xcs," in *Evolutionary Computation, 2005. The 2005 IEEE Congress on*, vol. 3, Sept 2005, pp. 2053–2060 Vol. 3.

[307] A. Al-Dhaher, E. Farsi, and D. Mackesy, "Data fusion architecture - an fpga implementation," in *Instrumentation and Measurement Technology Conference, 2005. IMTC 2005. Proceedings of the IEEE*, vol. 3, May 2005, pp. 1985–1990.

[308] A. Ahmadi, H. Mattausch, and T. Koide, "Parallel hardware design for snake models with an fpga architecture," in *Nonlinear Signal and Image Processing, 2005. NSIP 2005. Abstracts. IEEE-Eurasip*, May 2005, pp. 13–.

[309] J. Alvarez, A. Lago, A. Nogueiras, C. Martinez-Penalver, J. Marcos, J. Doval, and O. Lopez, "Fpga implementation of a fuzzy controller for automobile dc-dc converters," in *Field Programmable Technology, 2006. FPT 2006. IEEE International Conference on*, Dec 2006, pp. 237–240.

[310] P. Arena, S. De Fiore, L. Fortuna, M. Frasca, L. Patane, and G. Vagliasindi, "Weak chaos control for action-oriented perception: Real time implementation via fpga," in *Biomedical Robotics and Biomechatronics, 2006. BioRob 2006. The First IEEE/RAS-EMBS International Conference on*, Feb 2006, pp. 555–560.

[311] O. Cadenas and G. Megson, "Verification and fpga circuits of a block-2 fast path-based predictor," in *Field Programmable Logic and Applications, 2006. FPL '06. International Conference on*, Aug 2006, pp. 1–6.

[312] A. Bianco, R. Birke, G. Botto, M. Chiaberge, J. Finochietto, G. Galante, M. Mellia, F. Neri, and M. Petracca, "Boosting the performance of pc-based software routers with fpga-enhanced network interface cards," in *High Performance Switching and Routing, 2006 Workshop on*, 2006, pp. 6 pp.–.

[313] D. Atienza, P. Del Valle, G. Paci, F. Poletti, L. Benini, G. De Micheli, and J. Mendias, "A fast hw/sw fpga-based thermal emulation framework for multi-processor system-on-chip," in *Design Automation Conference, 2006 43rd ACM/IEEE*, 2006, pp. 618–623.

[314] L. Agostini, M. Porto, J. L. Guntzel, R. Porto, and S. Bampi, "High throughput fpga based architecture for h. 264/avc inverse transforms and quantization," in *Circuits and Systems, 2006. MWSCAS '06. 49th IEEE International Midwest Symposium on*, vol. 1, Aug 2006, pp. 281–285.

[315] O. Al-Ayasrah, T. Alukaidey, and G. Pissanidis, "Dsp based n-motor speed control of brushless dc motors using external fpga design," in *Industrial Technology, 2006. ICIT 2006. IEEE International Conference on*, Dec 2006, pp. 627–631.

[316] L. Agostini, A. Azevedo Filho, V. Rosa, E. Berriel, T. Santos, S. Bampi, and A. Susin, "Fpga design of a h.264/avc main profile decoder for hdtv," in *Field Programmable Logic and Applications, 2006. FPL '06. International Conference on*, Aug 2006, pp. 1–6.

[317] A. Atitallah, P. Kadionik, F. Ghozzi, P. Nouel, N. Masmoudi, and P. Marchegay, "Optimization and implementation on fpga of the dct/idct algorithm," in *Acoustics, Speech and Signal Processing, 2006. ICASSP 2006 Proceedings. 2006 IEEE International Conference on*, vol. 3, May 2006, pp. III–III.

[318] P. Anghelescu, E. Sofron, S. Ionita, and L. Ionescu, "Fpga implementations of cellular automata for pseudo-random number generation," in *International Semiconductor Conference, 2006*, vol. 2, Sept 2006, pp. 371–374.

[319] S. Anvar, O. Gachelin, P. Kestener, H. Le Provost, and I. Mandjavidze, "Fpga-based system-on-chip designs for real-time applications in particle physics," *Nuclear Science, IEEE Transactions on*, vol. 53, no. 3, pp. 682–687, June 2006.

[320] R. Brodersen, A. Tkachenko, and H. Kwok-Hay So, "A unified hardware/software runtime environment for fpga-based reconfigurable computers using borph," in *Hardware/Software Codesign and System Synthesis, 2006. CODES+ISSS '06. Proceedings of the 4th International Conference*, Oct 2006, pp. 259–264.

[321] S. Arifin and P. Cheung, "Towards affective level video applications: A novel fpga-based video arousal content modeling system," in *Field Programmable Logic and Applications, 2006. FPL '06. International Conference on*, Aug 2006, pp. 1–4.

[322] J. Bastos, H. Figueroa, and A. Monti, "Fpga implementation of neural network-based controllers for power electronics applications," in *Applied Power Electronics Conference and Exposition, 2006. APEC '06. Twenty-First Annual IEEE*, March 2006, pp. 6 pp.–.

[323] L. Bi, X. Wei, and Z. Sun, "A high-voltage safety protection method for electric vehicle based on fpga," in *Vehicular Electronics and Safety, 2006. ICVES 2006. IEEE International Conference on*, Dec 2006, pp. 26–31.

[324] S. Bayliss, C. Bouganis, G. Constantinides, and W. Luk, "An fpga implementation of the simplex algorithm," in *Field Programmable Technology, 2006. FPT 2006. IEEE International Conference on*, Dec 2006, pp. 49–56.

[325] L. Barbero and J. Thompson, "Fpga design considerations in the implementation of a fixed-throughput sphere decoder for mimo systems," in *Field Programmable Logic and Applications, 2006. FPL '06. International Conference on*, Aug 2006, pp. 1–6.

[326] V. Bocci, F. Iacoangeli, and R. Nobrega, "Data stream zero suppression and word recoding using an accordion pipeline, an fpga implementation," in *Nuclear Science Symposium Conference Record, 2006. IEEE*, vol. 1, Oct 2006, pp. 341–344.

[327] K. Al-Ashmouny, H. Hamed, and A. Morsy, "Fpga-based sleep apnea screening device for home monitoring," in *Engineering in Medicine and Biology Society, 2006. EMBS '06. 28th Annual International Conference of the IEEE*, Aug 2006, pp. 5948–5951.

[328] T. Balercia, A. Zitti, H. Francesconi, S. Orcioni, and M. Conti, "Fpga implementations of a simplified retinex image processing algorithm," in *Electronics, Circuits and Systems, 2006. ICECS '06. 13th IEEE International Conference on*, Dec 2006, pp. 176–179.

[329] B. Al-Hadithi, J. Muro, and A. Garcia, "Fpga based variable structure control for switched d.c/d.c converters," in *Electrotechnical Conference, 2006. MELECON 2006. IEEE Mediterranean*, May 2006, pp. 413–416.

[330] S. Borgio, D. Bosisio, F. Ferrandi, M. Monchiero, M. Santambrogio, D. Sciuto, and A. Tumeo, "Hardware dwt accelerator for multiprocessor system-on-chip on fpga," in *Embedded Computer Systems: Architectures, Modeling and Simulation, 2006. IC-SAMOS 2006. International Conference on*, July 2006, pp. 107–114.

[331] C. Guo-Xiang, W. Cheng-Yuan, G. Dian-Ling, X. Jia-Kuan, and L. Xiu-Ling, "Design of an fpga-based 3-phase sinusoidal pwm controller," in *Control Conference, 2006. CCC 2006. Chinese*, Aug 2006, pp. 1886–1889.

[332] C. Canesin and F. Gonçalves, "A phase-shifting control for variable frequency multi-cells interleaved boost pre-regulator based on fpga device," in *Industrial Electronics, 2006 IEEE International Symposium on*, vol. 2, July 2006, pp. 1432–1435.

[333] S. Arifin and P. Cheung, "A novel fpga-based implementation of time adaptive clustering for logical story unit segmentation," in *Design, Automation and Test in Europe, 2006. DATE '06. Proceedings*, vol. 2, March 2006, pp. 1–6.

[334] A. Batista, D. Alves, N. Cruz, J. Sousa, C. Varandas, E. Joffrin, R. Felton, J. Farthing, and J.-E. Contributors, "An fpga-based multi-rate interpolator with real-time rate change for a jet test-bench system," *Nuclear Science, IEEE Transactions on*, vol. 53, no. 3, pp. 756–760, June 2006.

[335] R. Carneiro Martins, H. Ramos, and P. Proenca, "A fpga-based general purpose multi-sensor data acquisition system with nonlinear sensor characteristic and environment compensation," in *Instrumentation and Measurement Technology Conference, 2006. IMTC 2006. Proceedings of the IEEE*, April 2006, pp. 563–567.

[336] J. Acosta, A. Gonzalez, and Z. Martinez, "Fpga based control scheme for active power filter," in *Transmission Distribution Conference and Exposition: Latin America, 2006. TDC '06. IEEE/PES*, Aug 2006, pp. 1–4.

[337] R. Cabral, S. Escarigo, H. Neto, and H. Sarmento, "Implementation of a dab receiver with fpga technology," in *Consumer Electronics, 2006. ICCE '06. 2006 Digest of Technical Papers. International Conference on*, Jan 2006, pp. 397–398.

[338] T. Brich, K. Novacek, and A. Khateb, "The digital signal processing using fpga," in *Electronics Technology, 2006. ISSE '06. 29th International Spring Seminar on*, May 2006, pp. 322–324.

[339] J. Castillo, P. Huerta, C. Pedraza, and J. Martinez, "A self-reconfigurable multimedia player on fpga," in *Reconfigurable Computing and FPGA's, 2006. ReConFig 2006. IEEE International Conference on*, Sept 2006, pp. 1–6.

[340] A. Boni and A. Zorat, "Fpga implementation of support vector machines with pseudo-logarithmic number representation," in *Neural Networks, 2006. IJCNN '06. International Joint Conference on*, 2006, pp. 618–624.

[341] C. Canesin and F. Gonçalves, "A multi-cell variable frequency interleaved zcs boost rectifier digitally controlled by fpga," in *Industrial Electronics, 2006 IEEE International Symposium on*, vol. 2, July 2006, pp. 1382–1387.

[342] T. Alho, P. Hamalainen, M. Hannikainen, and T. Hamalainen, "Design of a compact modular exponentiation accelerator for modern fpga devices," in *Automation Congress, 2006. WAC '06. World*, July 2006, pp. 1–7.

[343] K. Amiri and J. Cavallaro, "Fpga implementation of dynamic threshold sphere detection for mimo systems," in *Signals, Systems and Computers, 2006. ACSSC '06. Fortieth Asilomar Conference on*, Oct 2006, pp. 94–98.

[344] Y. Aoudni, G. Gogniat, M. Abid, and J.-L. Philippe, "Custom instruction integration method within reconfigurable soc and fpga devices," in *Microelectronics, 2006. ICM '06. International Conference on*, Dec 2006, pp. 131–134.

[345] O. Al-Khaleel, C. Papachristou, F. Wolff, and K. Pekmestzi, "Fpga-based design of a large moduli multiplier for public-key cryptographic systems," in *Computer Design, 2006. ICCD 2006. International Conference on*, Oct 2006, pp. 314–319.

[346] L. Bissi, P. Placidi, G. Baruffa, and A. Scorzoni, "A multi-standard reconfigurable viterbi decoder using embedded fpga blocks," in *Digital System Design: Architectures, Methods and Tools, 2006. DSD 2006. 9th EUROMICRO Conference on*, 2006, pp. 146–154.

[347] U. Bondhugula, A. Devulapalli, J. Fernando, P. Wyckoff, and P. Sadayappan, "Parallel fpga-based all-pairs shortest-paths in a directed graph," in *Parallel and Distributed Processing Symposium, 2006. IPDPS 2006. 20th International*, April 2006, pp. 10 pp.–.

[348] L. Agostini and S. Bampi, "Fpga based architectures for h. 264/avc video compression standard," in *Field Programmable Logic and Applications, 2006. FPL '06. International Conference on*, Aug 2006, pp. 1–2.

[349] M. Al-Qutayri, S. Al-Araji, and N. Al-Moosa, "Second order tdtl performance analysis and fpga implementation," in *Electrotechnical Conference, 2006. MELECON 2006. IEEE Mediterranean*, May 2006, pp. 514–517.

[350] A. Ahmadi, M. Ritonga, M. Abedin, H. Mattausch, and T. Koide, "A learning ocr system using short/long-term memory approach and hardware implementation in fpga," in *Evolutionary Computation, 2006. CEC 2006. IEEE Congress on*, 2006, pp. 687–693.

[351] N. Bellas, S. Chai, M. Dwyer, and D. Linzmeier, "Fpga implementation of a license plate recognition soc using automatically generated streaming accelerators," in *Parallel and Distributed Processing Symposium, 2006. IPDPS 2006. 20th International*, April 2006, pp. 8 pp.–.

[352] M. Benhamid and M. Othman, "Fpga implementation of a canonical signed digit multiplier-less based fft processor for wireless communication applications," in *Semiconductor Electronics, 2006. ICSE '06. IEEE International Conference on*, Oct 2006, pp. 641–645.

[353] U. Bondhugula, A. Devulapalli, J. Dinan, J. Fernando, P. Wyckoff, E. Stahlberg, and P. Sadayappan, "Hardware/software integration for fpga-based all-pairs shortest-paths," in *Field-Programmable Custom Computing Machines, 2006. FCCM '06. 14th Annual IEEE Symposium on*, April 2006, pp. 152–164.

[354] Y. Abhyankar, C. Sajish, Y. Agarwal, C. Subrahmanya, and P. Prasad, "High performance power spectrum analysis using a fpga based reconfigurable computing platform," in *Reconfigurable Computing and FPGA's, 2006. ReConFig 2006. IEEE International Conference on*, Sept 2006, pp. 1–5.

[355] F. Bensaali, A. Amira, and S. Chandrasekaran, "Power modeling and efficient fpga implementation of color space conversion," in *Electronics, Circuits and Systems, 2006. ICECS '06. 13th IEEE International Conference on*, Dec 2006, pp. 164–167.

[356] J. Becker, C. Bieser, J. Becker, and K.-D. Mueller-Glase, "Evaluation of a packet switching algorithm for network on chip topologies using a xilinx virtex-ii fpga based rapid prototyping system," in *Industrial Electronics, 2006 IEEE International Symposium on*, vol. 4, July 2006, pp. 3184–3189.

[357] F. Cardells-Tormo and P. Molinet, "Area-efficient 2-d shift-variant convolvers for fpga-based digital image processing," *Circuits and Systems II: Express Briefs, IEEE Transactions on*, vol. 53, no. 2, pp. 105–109, Feb 2006.

[358] A. Abdo and T. Hall, "Fpga-based testbed for packet switch performance measurement," in *Instrumentation and Measurement Technology Conference, 2006. IMTC 2006. Proceedings of the IEEE*, April 2006, pp. 347–352.

[359] A. Alcalde, F. D'aquino, M. Ortmann, H. Mohr, and S. Mussa, "Fpga-based control of a pfc converter," in *Industrial Electronics, 2007. ISIE 2007. IEEE International Symposium on*, June 2007, pp. 959–963.

[360] P. Bhagawat, W. Wang, M. Uppal, G. Choi, Z. Xiong, M. Yeary, and A. Harris, "An fpga implementation of dirty paper precoder," in *Communications, 2007. ICC '07. IEEE International Conference on*, June 2007, pp. 2761–2766.

[361] K. Arshak, E. Jafer, and C. Ibala, "Fpga based system design suitable for wireless health monitoring employing intelligent rf module," in *Sensors, 2007 IEEE*, Oct 2007, pp. 276–279.

[362] A. Boggiano, S. Delfitto, T. Poggi, and M. Storace, "Fpga implementation of a new scheme for the circuit realization of pwl functions," in *Circuit Theory and Design, 2007. ECCTD 2007. 18th European Conference on*, Aug 2007, pp. 874–877.

[363] J. Bakos, P. Elenis, and J. Tang, "Fpga acceleration of phylogeny reconstruction for whole genome data," in *Bioinformatics and Bioengineering, 2007. BIBE 2007. Proceedings of the 7th IEEE International Conference on*, Oct 2007, pp. 888–895.

[364] X. Mei-Hua, C. Yu-Lan, R. Feng, and C. Zhang-Jin, "Optimizing design and fpga implementation for cabac decoder," in *High Density packaging and Microsystem Integration, 2007. HDP '07. International Symposium on*, June 2007, pp. 1–5.

[365] I. Az, S. Sahin, and M. Cavuslu, "Implementation of fast fourier and inverse fast fourier transforms in fpga," in *Signal Processing and Communications Applications, 2007. SIU 2007. IEEE 15th*, June 2007, pp. 1–4.

[366] M. Bin Mohamed Shukor, L. H. Hiung, and P. Sebastian, "Implementation of real-time simple edge detection on fpga," in *Intelligent and Advanced Systems, 2007. ICIAS 2007. International Conference on*, Nov 2007, pp. 1404–1406.

[367] I. Ashour, "On line data and voice encryption system based on fpga technology," in *Radio Science Conference, 2007. NRSC 2007. National*, March 2007, pp. 1–7.

[368] W. Alvis, S. Murthy, K. Valavanis, W. Moreno, M. Fields, and S. Katkoori, "Fpga based flexible autopilot platform for unmanned systems," in *Control Automation, 2007. MED '07. Mediterranean Conference on*, June 2007, pp. 1–9.

[369] R. Ayoubi, J. Dubois, and O. Abdul-Latif, "Fpga implementation of a novel receiver diversity combining technique for wireless simo systems," in *Signal Processing and Communications, 2007. ICSPC 2007. IEEE International Conference on*, Nov 2007, pp. 37–40.

[370] E. Amini, M. Najibi, Z. Jeddi, and H. Pedram, "Fpga implementation of gated clock based globally asynchronous locally synchronous wrapper circuits," in *Signals, Circuits and Systems, 2007. ISSCS 2007. International Symposium on*, vol. 1, July 2007, pp. 1–4.

[371] A. Abche, A. Maalouf, R. Ayoubi, E. Karam, and A. Alameddine, "An fpga implementation of a high resolution phase shift beamformer," in *Signal Processing and Communications, 2007. ICSPC 2007. IEEE International Conference on*, Nov 2007, pp. 1319–1322.

[372] B. Ahirwal, M. Khadtare, and R. Mehta, "Fpga based system for color space transformation rgb to yiq and ycbcr," in *Intelligent and Advanced Systems, 2007. ICIAS 2007. International Conference on*, Nov 2007, pp. 1345–1349.

[373] A. Ahmed, S. Rahman, G. Al-Sammane, and O. Mohamed, "Fpga emulation environment of different digital carrier synchronizers," in *Circuits and Systems, 2007. NEWCAS 2007. IEEE Northeast Workshop on*, Aug 2007, pp. 510–513.

[374] O. Al-Khaleel, C. Papachristou, F. Wolff, and K. Pekmestzi, "An elliptic curve cryptosystem design based on fpga pipeline folding," in *On-Line Testing Symposium, 2007. IOLTS 07. 13th IEEE International*, July 2007, pp. 71–78.

[375] N. Alaraje, J. DeGroat, and H. Jasani, "Sofpga (sysytem-on-fpga) architecture: Performance analysis," in *Electro/Information Technology, 2007 IEEE International Conference on*, May 2007, pp. 551–556.

[376] A. Ahmed, S. Rahman, and O. Mohamed, "Fpga implementation and performance evaluation of a digital carrier synchronizer using different numerically controlled oscillators," in *Electrical and Computer Engi-*

*neering, 2007. CCECE 2007. Canadian Conference on*, April 2007, pp. 1243–1246.

[377] K. Benkrid, Y. Liu, and A. Benkrid, "Design and implementation of a highly parameterised fpga-based skeleton for pairwise biological sequence alignment," in *Field-Programmable Custom Computing Machines, 2007. FCCM 2007. 15th Annual IEEE Symposium on*, April 2007, pp. 275–278.

[378] C. Anghel, A. Enescu, O. Bugiugan, and C. Cacoveanu, "Fpga implementation of a ctc decoder for h-arq compliant wimax systems," in *Design Technology of Integrated Systems in Nanoscale Era, 2007. DTIS. International Conference on*, Sept 2007, pp. 82–86.

[379] N. Benitez, G. Bellanco, C. Amuchastegui, G. Alvarez, I. Laniella, H. Cepeda, N. Ayuso, and A. Guerendiain, "Low power amr system based on fpga," in *Programmable Logic, 2007. SPL '07. 2007 3rd Southern Conference on*, Feb 2007, pp. 177–182.

[380] V. Aggarwal, "Sensor simulation on fpga hardware," in *Autotestcon, 2007 IEEE*, Sept 2007, pp. 167–173.

[381] S. Alam, P. Agarwal, M. Smith, J. Vetter, and D. Caliga, "Using fpga devices to accelerate biomolecular simulations," *Computer*, vol. 40, no. 3, pp. 66–73, March 2007.

[382] J. Acero, D. Navarro, L. Barragan, I. Garde, J. Artigas, and J. Burdio, "Fpga-based power measuring for induction heating appliances using sigma – delta a/d conversion," *Industrial Electronics, IEEE Transactions on*, vol. 54, no. 4, pp. 1843–1852, Aug 2007.

[383] N. Azli, L. Teng, and P. Lim, "Implementation of a single-carrier multilevel pwm technique using field programmable gate array (fpga)," in *Power Electronics and Drive Systems, 2007. PEDS '07. 7th International Conference on*, Nov 2007, pp. 836–841.

[384] A. Aloisio, F. Cevenini, R. Giordano, and V. Izzo, "A vlsi-fpga system-on-chip for detectors monitoring," in *Nuclear Science Symposium Conference Record, 2007. NSS '07. IEEE*, vol. 1, Oct 2007, pp. 468–473.

[385] M. Abdellatif, M. Naouar, I. Slama-Belkhodja, and E. Monmasson, "Fpga-based vector pi regulator for electrical drives control," in *Power Electronics and Applications, 2007 European Conference on*, Sept 2007, pp. 1–9.

[386] F. Bensaali, A. Amira, and R. Sotudeh, "Floating-point matrix product on fpga," in *Computer Systems and Applications, 2007. AICCSA '07. IEEE/ACS International Conference on*, May 2007, pp. 466–473.

[387] J. Alme, R. Campagnolo, D. Fehlker, C. Gutierrez, H. Helstrup, P. Hille, H. Muller, M. Munkejord, L. Musa, A. Karlsson, R. Pimenta, M. Richter, A. Rossebo, K. Roed, D. Rohrich, T. Skaali, A. Stangeland, and K. Ullaland, "Radiation-tolerant, sram-fpga based trigger and readout electronics for the alice experiment," in *Real-Time Conference, 2007 15th IEEE-NPSS*, April 2007, pp. 1–7.

[388] W. Cheng-Yuan, C. Guo-Xiang, L. Xiu-Ling, and M. Xin, "A novel current source multilevel controller based on fpga," in *Electrical Machines and Systems, 2007. ICEMS. International Conference on*, Oct 2007, pp. 1799–1801.

[389] Z. Baker, M. Gokhale, and J. Tripp, "Matched filter computation on fpga, cell and gpu," in *Field-Programmable Custom Computing Machines, 2007. FCCM 2007. 15th Annual IEEE Symposium on*, April 2007, pp. 207–218.

[390] M. Alonso, F. Huerta, C. Girón, E. Bueno, A. Hernandez, F. Rodriguez, and S. Cobreces, "Industrial control system for a back-to-back multilevel npc converter based on dsp and fpga," in *Industrial Electronics, 2007. ISIE 2007. IEEE International Symposium on*, June 2007, pp. 2358–2363.

[391] A. Al Ghouwayel, Y. Louet, A. Nafkha, and J. Palicot, "On the fpga implementation of the fourier transform over finite fields gf(2m)," in *Communications and Information Technologies, 2007. ISCIT '07. International Symposium on*, Oct 2007, pp. 146–151.

[392] H. Berge and P. Hafliger, "High-speed serial aer on fpga," in *Circuits and Systems, 2007. ISCAS 2007. IEEE International Symposium on*, May 2007, pp. 857–860.

[393] C. Attaianese and V. Tomasso, "Fpga based control system for motor side active filter (msaf)," in *Power Electronics Specialists Conference, 2007. PESC 2007. IEEE*, June 2007, pp. 527–533.

[394] S. Berber and C.-C. Wei, "Theoretical analysis, design and prototyping of a chaos-based cdma system based on fpga technology," in *Ultra-Wideband, 2007. ICUWB 2007. IEEE International Conference on*, Sept 2007, pp. 535–539.

[395] A. Ben AtItallah, P. Kadionik, N. Masmoudi, and H. Levi, "Hw/sw fpga architecture for a flexible motion estimation," in *Electronics, Circuits and Systems, 2007. ICECS 2007. 14th IEEE International Conference on*, Dec 2007, pp. 30–33.

[396] A. Al-Haj, "Fpga-based quadrature mirror filters for dsp applications," in *Signal-Image Technologies and Internet-Based System, 2007. SITIS '07. Third International IEEE Conference on*, Dec 2007, pp. 581–584.

[397] L. Barragán, I. Urriza, D. Navarro, J. Artigas, J. Acero, and J. Burdio, "Comparing simulation alternatives of fpga-based controllers for switching converters," in *Industrial Electronics, 2007. ISIE 2007. IEEE International Symposium on*, June 2007, pp. 419–424.

[398] M. Abdelghani, S. Sezer, E. Garcia, J. Mu, and C. Toal, "Fpga-based lookup circuit for session-based ip packet classification," in *Adaptive Hardware and Systems, 2007. AHS 2007. Second NASA/ESA Conference on*, Aug 2007, pp. 619–624.

[399] M. Barrenechea, J. Altuna, and M. San Miguel, "A low-cost fpga-based embedded fingerprint verification and matching system," in *Intelligent Solutions in Embedded Systems, 2007 Fifth Workshop on*, June 2007, pp. 250–261.

[400] G. Almeida, E. Bezerra, L. Cargnini, R. Fagundes, and D. Mesquita, "A reed-solomon algorithm for fpga area optimization in space applications," in *Adaptive Hardware and Systems, 2007. AHS 2007. Second NASA/ESA Conference on*, Aug 2007, pp. 243–249.

[401] D. Baumgartner, P. Rossler, and W. Kubinger, "Performance benchmark of dsp and fpga implementations of low-level vision algorithms," in *Computer Vision and Pattern Recognition, 2007. CVPR '07. IEEE Conference on*, June 2007, pp. 1–8.

[402] A. Aloisio, P. Branchini, R. Cicalese, R. Giordano, V. Izzo, and S. Loffredo, "Fpga implementation of a high-resolution time-to-digital converter," in *Nuclear Science Symposium Conference Record, 2007. NSS '07. IEEE*, vol. 1, Oct 2007, pp. 504–507.

[403] A. Amira and S. Chandrasekaran, "Power modeling and efficient fpga implementation of fht for signal processing," *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on*, vol. 15, no. 3, pp. 286–295, March 2007.

[404] M.-u.-R. Awan, M. Alam, P. Koch, and N. Behjou, "Design and implementation of an fpga-based multi-standard software radio receiver," in *Norchip, 2007*, Nov 2007, pp. 1–5.

[405] J. Bakos, "Fpga acceleration of gene rearrangement analysis," in *Field-Programmable Custom Computing Machines, 2007. FCCM 2007. 15th Annual IEEE Symposium on*, April 2007, pp. 85–94.

[406] A. Alcalde, F. D'aquino, H. Mohr, and S. Mussa, "Implementation of a control strategy for pfc with fpga," in *Power Electronics and Applications, 2007 European Conference on*, Sept 2007, pp. 1–9.

[407] V. Bonato, R. Peron, D. Wolf, J. de Holanda, E. Marques, and J. Cardoso, "An fpga implementation for a kalman filter with application to mobile robotics," in *Industrial Embedded Systems, 2007. SIES '07. International Symposium on*, July 2007, pp. 148–155.

[408] A. Alcalde, D. Borgonovo, and S. Mussa, "An fpga control application: Self-control of current and linear control of dc link of pfc," in *Industrial Electronics, 2008. IECON 2008. 34th Annual Conference of IEEE*, Nov 2008, pp. 2387–2392.

[409] S. Banks, P. Beadling, and A. Ferencz, "Fpga implementation of pseudo random number generators for monte carlo methods in quantitative finance," in *Reconfigurable Computing and FPGAs, 2008. ReConFig '08. International Conference on*, Dec 2008, pp. 271–276.

[410] E. Bergeron, M. Feeley, M. Daigneault, and J. David, "Using dynamic reconfiguration to implement high-resolution programmable delays on an fpga," in *Circuits and Systems and TAISA Conference, 2008. NEWCAS-TAISA 2008. 2008 Joint 6th International IEEE Northeast Workshop on*, June 2008, pp. 265–268.

[411] E. Ayeh, K. Agbedanu, Y. Morita, O. Adamo, and P. Guturu, "Fpga implementation of an 8-bit simple processor," in *Region 5 Conference, 2008 IEEE*, April 2008, pp. 1–5.

[412] P. Anghelescu, S. Ionita, and E. Sofron, "Fpga implementation of hybrid additive programmable cellular automata encryption algorithm," in *Hybrid Intelligent Systems, 2008. HIS '08. Eighth International Conference on*, Sept 2008, pp. 96–101.

[413] I. Algredo-Badillo, C. Feregrino-Uribe, R. Cumplido, and M. Morales-Sandoval, "Fpga implementation and performance evaluation of aes-ccm cores for wireless networks," in *Reconfigurable Computing and FPGAs, 2008. ReConFig '08. International Conference on*, Dec 2008, pp. 421–426.

[414] C. Beuschel and H.-J. Pfleiderer, "Fpga implementation of a flexible decoder for long ldpc codes," in *Field Programmable Logic and*

*Applications, 2008. FPL 2008. International Conference on*, Sept 2008, pp. 185–190.

[415] M. Abdillahi-Said and C. Park, "Designing and implementing a system of multiplexing and demultiplexing on fpga using matlab/simulink for the detection of acoustic signals," in *OCEANS 2008*, Sept 2008, pp. 1–6.

[416] A. Barenghi, G. Bertoni, L. Breveglieri, and G. Pelosi, "A fpga coprocessor for the cryptographic tate pairing over fp," in *Information Technology: New Generations, 2008. ITNG 2008. Fifth International Conference on*, April 2008, pp. 112–119.

[417] M. Batarseh, W. Al-Hoor, L. Huang, C. Iannello, and I. Batarseh, "Segmented digital clock manager- fpga based digital pulse width modulator technique," in *Power Electronics Specialists Conference, 2008. PESC 2008. IEEE*, June 2008, pp. 3036–3042.

[418] A.-R. Abdul-Shakoor, R. Kerr, J. Lodge, and V. Szwarc, "An fpga implementation of a soft-in soft-out decoder for block codes," in *Communications, 2008 24th Biennial Symposium on*, June 2008, pp. 226–230.

[419] S. An and C. Wang, "Recursive algorithm, architectures and fpga implementation of the two-dimensional discrete cosine transform," *Image Processing, IET*, vol. 2, no. 6, pp. 286–294, December 2008.

[420] A. Alcalde, M. Ortmann, and S. Mussa, "Nios ii processor implemented in fpga: An application on control of a pfc converter," in *Power Electronics Specialists Conference, 2008. PESC 2008. IEEE*, June 2008, pp. 4446–4451.

[421] A. Alimohammad, S. Fard, B. Cockburn, and C. Schlegel, "A single-fpga multipath mimo fading channel simulator," in *Circuits and Systems, 2008. ISCAS 2008. IEEE International Symposium on*, May 2008, pp. 308–311.

[422] R. Anguiano, G. Galaviz, and A. Andrade, "On the implementation of a space time block coded transmitter in an fpga platform," in *Wireless Telecommunications Symposium, 2008. WTS 2008*, April 2008, pp. 324–328.

[423] Z. Baker and R. Porter, "Rotationally invariant sparse patch matching on gpu and fpga," in *Parallel and Distributed Processing, 2008. IPDPS 2008. IEEE International Symposium on*, April 2008, pp. 1–8.

[424] A. Aloisio, P. Branchini, R. Cicalese, R. Giordano, V. Izzo, and S. Loffredo, "High-precision time-to-digital converters in a fpga device," in *Nuclear Science Symposium Conference Record, 2008. NSS '08. IEEE*, Oct 2008, pp. 2114–2118.

[425] A. Alimohammad, S. Fard, B. Cockburn, and C. Schlegel, "On the efficiency and accuracy of hybrid pseudo-random number generators for fpga-based simulations," in *Parallel and Distributed Processing, 2008. IPDPS 2008. IEEE International Symposium on*, April 2008, pp. 1–8.

[426] D. Bekker, M. Lukowiak, M. Shaaban, J.-F. Blavier, and P. Pingree, "A hybrid-fpga system for on-board data processing targeting the matmos ftir instrument," in *Aerospace Conference, 2008 IEEE*, March 2008, pp. 1–15.

[427] H. Bessalah, K. Messaoudi, M. Issad, N. Anane, and M. Anane, "Left to right serial multiplier for large numbers on fpga," in *Design and Test Workshop, 2008. IDT 2008. 3rd International*, Dec 2008, pp. 288–293.

[428] D. Bafumba-Lokilo, Y. Savaria, and J.-P. David, "Generic crossbar network on chip for fpga mpsocs," in *Circuits and Systems and TAISA Conference, 2008. NEWCAS-TAISA 2008. 2008 Joint 6th International IEEE Northeast Workshop on*, June 2008, pp. 269–272.

[429] G. Amruta, P. Yogita, P. Puja, and P. Sriniwas Shastry, "Low latency and high accuracy archtectures of cordic algorithm for cosine calculation on fpga," in *Electronics, Circuits and Systems, 2008. ICECS 2008. 15th IEEE International Conference on*, Aug 2008, pp. 478–481.

[430] V. Amudha, B. Venkataramani, and J. Manikandan, "Fpga implementation of isolated digit recognition system using modified back propagation algorithm," in *Electronic Design, 2008. ICED 2008. International Conference on*, Dec 2008, pp. 1–6.

[431] A. Atoche, J. Aguilar, and J. Castillo, "Fpga based radar image enhanced: A robust evolutionary controlled filter approach," in *Devices, Circuits and Systems, 2008. ICCDCS 2008. 7th International Caribbean Conference on*, April 2008, pp. 1–5.

[432] I. Bahri, M.-W. Naouar, E. Monmasson, I. Slama-Belkhodja, and L. Charaabi, "Design of an fpga-based real-time simulator for electrical system," in *Power Electronics and Motion Control Conference, 2008. EPE-PEMC 2008. 13th*, Sept 2008, pp. 1365–1370.

[433] T. Barlas and M. Moallem, "Next generation of embedded controllers: Developing fpga-based reconfigurable controllers using matlab/simulink," in *Emerging Technologies and Factory Automation, 2008. ETFA 2008. IEEE International Conference on*, Sept 2008, pp. 1055–1058.

[434] J. Alme, R. Campagnolo, O. Djuvsland, D. Fehlker, C. Gutierrez, H. Helstrup, P. Hille, O. Hland, H. Muller, M. Munkejord, L. Musa, A. Oltean Karlsson, R. Pimenta, M. Richter, A. Rossebo, K. Roed, D. Rohrich, T. Skaali, A. Stangeland, and K. Ullaland, "Radiation-tolerant, sram-fpga based trigger and readout electronics for the alice experiment," *Nuclear Science, IEEE Transactions on*, vol. 55, no. 1, pp. 76–83, Feb 2008.

[435] S. Ben Othman, A. Ben Salem, and S. Ben Saoud, "Mpsoc design of rt control applications based on fpga softcore processors," in *Electronics, Circuits and Systems, 2008. ICECS 2008. 15th IEEE International Conference on*, Aug 2008, pp. 404–409.

[436] A. Abdellatif, S. Ismail, and D. Korzec, "Fpga implementation of a multi-rate punctured viterbi decoder compatible with the dvb-t standard," in *Signal Processing and Information Technology, 2008. ISSPIT 2008. IEEE International Symposium on*, Dec 2008, pp. 100–105.

[437] A. Alsuwailem, S. Alshebeili, M. Alhowaish, and S. Qasim, "Hardware realization of a novel automatic censored cell averaging cfar detection algorithm using fpga," in *Signal Processing, 2008. ICSP 2008. 9th International Conference on*, Oct 2008, pp. 398–401.

[438] O. Alim, N. Elboghdadly, M. Ashour, and A. Elaskary, "Fpga implementation for an optimized cordic module for ofdm system," in *Computer Engineering Systems, 2008. ICCES 2008. International Conference on*, Nov 2008, pp. 21–26.

[439] M. Baklouti, P. Marquet, M. Abid, and J. Dekeyser, "Impact of interconnection networks in a massively parallel fpga architecture on a parallel reduction algorithm," in *Design and Test Workshop, 2008. IDT 2008. 3rd International*, Dec 2008, pp. 209–214.

[440] S. Al-Kazzaz and R. Khalil, "Fpga implementation of artificial neurons: Comparison study," in *Information and Communication Technologies: From Theory to Applications, 2008. ICTTA 2008. 3rd International Conference on*, April 2008, pp. 1–6.

[441] D. Bates, S. Henriksen, B. Ninness, and S. R. Weller, "A $4 \times 4$ fpga-based wireless testbed for lte applications," in *Personal, Indoor and Mobile Radio Communications, 2008. PIMRC 2008. IEEE 19th International Symposium on*, Sept 2008, pp. 1–5.

[442] G. Alizadeh, J. Frounchi, M. Baradaran Nia, M. Zarifi, and S. Asgarifar, "An fpga implementation of an artificial neural network for prediction of cetane number," in *Computer and Communication Engineering, 2008. ICCCE 2008. International Conference on*, May 2008, pp. 605–608.

[443] W. Atabany and P. Degenaar, "Parallelism to reduce power consumption on fpga spatiotemporal image processing," in *Circuits and Systems, 2008. ISCAS 2008. IEEE International Symposium on*, May 2008, pp. 1476–1479.

[444] J. Athow and A. Al-Khalili, "Implementation of large-integer hardware multiplier in xilinx fpga," in *Electronics, Circuits and Systems, 2008. ICECS 2008. 15th IEEE International Conference on*, Aug 2008, pp. 1300–1303.

[445] S. Ben Othman, M. Ghrissi, A. Ben Salem, and S. Ben Saoud, "Fpga hardcore single processor implementation of rt control applications," in *Design and Technology of Integrated Systems in Nanoscale Era, 2008. DTIS 2008. 3rd International Conference on*, March 2008, pp. 1–4.

[446] M. Ahmad, Z. Husin, R. Ahmad, H. Rahim, M. Abu Hassan, and M. Md Isa, "Fpga based control ic for multilevel inverter," in *Computer and Communication Engineering, 2008. ICCCE 2008. International Conference on*, May 2008, pp. 319–322.

[447] C. Benbouchama, S. Sakhi, M. Tadjine, and A. Bouridane, "Design of an fpga based neural controller," in *Human System Interactions, 2008 Conference on*, May 2008, pp. 516–521.

[448] I. Algredo-Badillo, C. Feregrino-Uribe, R. Cumplido, and M. Morales-Sandoval, "Fpga implementation cost and performance evaluation of the ieee 802.16e and ieee 802.11i security architectures based on aes-ccm," in *Electrical Engineering, Computing Science and Automatic Control, 2008. CCE 2008. 5th International Conference on*, Nov 2008, pp. 304–309.

[449] W. Benzaba, A. Allam, L. Bendaouia, R. Boutaleb, F. Ykhlef, and Y. Boucetta, "Anti pain stimulator using fpga circuit," in *Signals, Circuits and Systems, 2008. SCS 2008. 2nd International Conference on*, Nov 2008, pp. 1–5.

[450] K. Ambrosch, M. Humenberger, W. Kubinger, and A. Steininger, "Extending two non-parametric transforms for fpga based stereo matching using bayer filtered cameras," in *Computer Vision and Pattern Recognition Workshops, 2008. CVPRW '08. IEEE Computer Society Conference on*, June 2008, pp. 1–8.

[451] M. Al-Mistarihi, "Separable implementation of the second order volterra filter (sovf) in xilinx virtex-e fpga," in *Field Programmable Logic and Applications, 2008. FPL 2008. International Conference on*, Sept 2008, pp. 531–534.

[452] S. Al Junid, Z. Majid, and A. Halim, "High speed dna sequencing accelerator using fpga," in *Electronic Design, 2008. ICED 2008. International Conference on*, Dec 2008, pp. 1–4.

[453] N. Balaji, K. Rao, and M. Rao, "Generation of six phase pulse compression sequences using fpga," in *Computer Science and Information Technology, 2008. ICCSIT '08. International Conference on*, Aug 2008, pp. 829–835.

[454] M. Aminian, M. Saeedi, M. Zamani, and M. Sedighi, "Fpga-based circuit model emulation of quantum algorithms," in *Symposium on VLSI, 2008. ISVLSI '08. IEEE Computer Society Annual*, April 2008, pp. 399–404.

[455] K. Babulu and K. Rajan, "Fpga implementation of usb transceiver macrocell interface with usb2.0 specifications," in *Emerging Trends in Engineering and Technology, 2008. ICETET '08. First International Conference on*, July 2008, pp. 966–970.

[456] B. Belhadj, J. Tomas, O. Malot, G. N'Kaoua, Y. Bornat, and S. Renaud, "Fpga-based architecture for real-time synaptic plasticity computation," in *Electronics, Circuits and Systems, 2008. ICECS 2008. 15th IEEE International Conference on*, Aug 2008, pp. 93–96.

[457] M. Amiri, M. Mahdavi, and S. Mirzakuchaki, "Qca implementation of a mux-based fpga clb," in *Nanoscience and Nanotechnology, 2008. ICONN 2008. International Conference on*, Feb 2008, pp. 141–144.

[458] A. Abba, A. Manenti, A. Suardi, A. Geraci, and G. Ripamonti, "Non-linear least squares fitting in fpga devices for digital spectroscopy," in *Nuclear Science Symposium Conference Record (NSS/MIC), 2009 IEEE*, Oct 2009, pp. 563–568.

[459] A. Aloisio, P. Branchini, R. Giordano, V. Izzo, and S. Loffredo, "High-precision time-to-digital converter in a fpga device," in *Nuclear Science Symposium Conference Record (NSS/MIC), 2009 IEEE*, Oct 2009, pp. 290–294.

[460] L. Ares, J. Rodriguez-Andina, and J. Farina, "Fpga-based direct resistance and capacitance measurements," in *Industrial Electronics, 2009. IECON '09. 35th Annual Conference of IEEE*, Nov 2009, pp. 2837–2841.

[461] A. Al Ghouwayel and Y. Louet, "Fpga implementation of a reconfigurable fft for multi-standard systems in software radio context," in *Consumer Electronics, 2009. ICCE '09. Digest of Technical Papers International Conference on*, Jan 2009, pp. 1–2.

[462] A. Alcalde, H. Mohr, D. Borgonovo, and S. Mussa, "Experimental validation of the nios ii processor-fpga on the digital control of pfc converter," in *Power Electronics Conference, 2009. COBEP '09. Brazilian*, Sept 2009, pp. 895–900.

[463] A. Abba, A. Manenti, A. Suardi, S. Riboldi, and A. Geraci, "Adaptive digital trigger architecture in fpga," in *Nuclear Science Symposium Conference Record (NSS/MIC), 2009 IEEE*, Oct 2009, pp. 569–572.

[464] L. Fei-Yu, Q. Wei-Ming, J. Xi-Xiang, J. Lan, and M. Yun-Hai, "Efficient design of digital up converter for wcdma in fpga using system generator," in *Information Engineering and Computer Science, 2009. ICIECS 2009. International Conference on*, Dec 2009, pp. 1–4.

[465] W. Yong-Qing, Q. Yuan, F. Hong-Lun, and W. Si-Liang, "Fpga implementation of snr estimation for dsss signal of space borne secondary radar," in *Radar Conference, 2009 IET International*, April 2009, pp. 1–4.

[466] J. Albo-Canals, J. Villasante-Bembibre, J. Riera-Babures, N. Fernandez-Garcia, and V. Brea, "An efficient fpga implementation of a dt-cnn for small image gray-scale pre-processing," in *Circuit Theory and Design, 2009. ECCTD 2009. European Conference on*, Aug 2009, pp. 839–842.

[467] R. Arulmozhiyal, K. Baskaran, N. Devarajan, and J. Kanagaraj, "Space vector pulse width modulation based induction motor speed control using fpga," in *Emerging Trends in Engineering and Technology (ICETET), 2009 2nd International Conference on*, Dec 2009, pp. 742–747.

[468] S. Wen-Miao and Z. Jing-Ying, "Research and fpga implementation of music doa of smart antenna array," in *Networks Security, Wireless Communications and Trusted Computing, 2009. NSWCTC '09. International Conference on*, vol. 2, April 2009, pp. 189–192.

[469] C. Anton, L. Ionescu, I. Tutanescu, A. Mazare, and G. Serban, "Fpga-implemented crc algorithm," in *Applied Electronics, 2009. AE 2009*, Sept 2009, pp. 25–29.

[470] R. Ahmad, O. Sidek, and S. Mohd, "Development of the crc block for zigbee standard on fpga," in *Technical Postgraduates (TECHPOS), 2009 International Conference for*, Dec 2009, pp. 1–4.

[471] A. Armato, E. Nardini, A. Lanata, G. Valenza, C. Mancuso, E. Scilingo, and D. De Rossi, "An fpga based arrhythmia recognition system for wearable applications," in *Intelligent Systems Design and Applications, 2009. ISDA '09. Ninth International Conference on*, Nov 2009, pp. 660–664.

[472] K. Appiah, A. Hunter, H. Meng, S. Yue, M. Hobden, N. Priestley, P. Hobden, and C. Pettit, "A binary self-organizing map and its fpga implementation," in *Neural Networks, 2009. IJCNN 2009. International Joint Conference on*, June 2009, pp. 164–171.

[473] M. Abutaleb, A. Hamdy, M. Abuelwafa, and E. Saad, "Fpga-based object-extraction based on multimodal $\sigma - \delta$ background estimation," in *Computer, Control and Communication, 2009. IC4 2009. 2nd International Conference on*, Feb 2009, pp. 1–7.

[474] M. Azzaz, C. Tanougast, S. Sadoudi, A. Bouridane, and A. Dandache, "Fpga implementation of new real-time image encryption based switching chaotic systems," in *Signals and Systems Conference (ISSC 2009), IET Irish*, June 2009, pp. 1–6.

[475] B. Alecsa and A. Onea, "An fpga implementation of the time domain deadbeat algorithm for control applications," in *NORCHIP, 2009*, Nov 2009, pp. 1–4.

[476] C. Anton, L. Ionescu, I. Tutanescu, A. Mazare, and G. Serban, "Detecting errors in digital communications with crc codes implemented with fpga," in *Internet Technology and Secured Transactions, 2009. ICITST 2009. International Conference for*, Nov 2009, pp. 1–6.

[477] A. Alimohammad, S. Fard, and B. Cockburn, "Fpga-based accelerator for the verification of leading-edge wireless systems," in *Design Automation Conference, 2009. DAC '09. 46th ACM/IEEE*, July 2009, pp. 844–847.

[478] A. Abbaszadeh and K. Dabbagh-Sadeghipour, "A new fpga-based postprocessor architecture for channel mismatch correction of time interleaved adcs," in *Signal Processing Systems, 2009. SiPS 2009. IEEE Workshop on*, Oct 2009, pp. 202–207.

[479] Z. De-An, L. Xian-Guo, and Y. Ping, "Multi-rate signal processing for software defined radio (sdr) and realize on fpga," in *Computer Science-Technology and Applications, 2009. IFCSTA '09. International Forum on*, vol. 1, Dec 2009, pp. 251–254.

[480] A. Arafa, H. Saleh, M. Ashour, and A. Salem, "Fft- and dwt-based fpga realization of pulse shape discrimination in pet system," in *Design Technology of Integrated Systems in Nanoscal Era, 2009. DTIS '09. 4th International Conference on*, April 2009, pp. 299–302.

[481] M. Abutaleb, A. Hamdy, M. Abuelwafa, and E. Saad, "A reliable fpga-based real-time optical-flow estimation," in *Radio Science Conference, 2009. NRSC 2009. National*, March 2009, pp. 1–8.

[482] C. Anghel, C. Paleologu, J. Benesty, and S. Ciochina, "Fpga implementation of an acoustic echo canceller using a vss-nlms algorithm," in *Signals, Circuits and Systems, 2009. ISSCS 2009. International Symposium on*, July 2009, pp. 1–4.

[483] R. Alonso and D. Lucio, "Parallel architecture for the solution of linear equation systems implemented in fpga," in *Electronics, Robotics and Automotive Mechanics Conference, 2009. CERMA '09.*, Sept 2009, pp. 275–280.

[484] A. Aloisio, P. Branchini, R. Giordano, V. Izzo, and S. Loffredo, "High-precision time-to-digital converter in a fpga device," in *Real Time Conference, 2009. RT '09. 16th IEEE-NPSS*, May 2009, pp. 283–286.

[485] J. Allred, J. Coyne, W. Lynch, V. Natoli, J. Grecco, and J. Morrissette, "Smith-waterman implementation on a fsb-fpga module using the intel accelerator abstraction layer," in *Parallel Distributed Processing, 2009. IPDPS 2009. IEEE International Symposium on*, May 2009, pp. 1–4.

[486] A. Alimohammad, S. Fard, and B. Cockburn, "Fpga-accelerated baseband design and verification of broadband mimo wireless systems," in *Advances in System Testing and Validation Lifecycle, 2009. VALID '09. First International Conference on*, Sept 2009, pp. 135–140.

[487] T. Adiono and R. Purba, "Scalable pipelined cordic architecture design and implementation in fpga," in *Electrical Engineering and Informatics, 2009. ICEEI '09. International Conference on*, vol. 02, Aug 2009, pp. 646–649.

[488] A. Amouri, F. Arifin, F. Hannig, and J. Teich, "Fpga implementation of an invasive computing architecture," in *Field-Programmable Technology, 2009. FPT 2009. International Conference on*, Dec 2009, pp. 135–142.

[489] W. Adi, N. Ouertani, A. Hanoun, and B. Soudan, "Deploying fpga self-configurable cell structure for micro crypto-functions," in *Computers and Communications, 2009. ISCC 2009. IEEE Symposium on*, July 2009, pp. 348–354.

[490] V. Agarwal, H. Arya, and S. Bhaktavatsala, "Design and development of a real-time dsp and fpga-based integrated gps-ins system for compact and low power applications," *Aerospace and Electronic Systems, IEEE Transactions on*, vol. 45, no. 2, pp. 443–454, April 2009.

[491] R. Ahmad, O. Sidek, and S. Mohd, "Development of bit-to-chip block for zigbee transmitter on fpga," in *Computer and Electrical Engineering, 2009. ICCEE '09. Second International Conference on*, vol. 1, Dec 2009, pp. 492–496.

[492] L. Arpin, M. Bergeron, M.-A. Tetrault, R. Lecomte, and R. Fontaine, "A sub-nanosecond edge detection system using embedded fpga fabrics," in *Real Time Conference, 2009. RT '09. 16th IEEE-NPSS*, May 2009, pp. 299–303.

[493] W. Yong-Gang, Z. Tau, Z. Yu-Feng, and Y. Yang, "Realization of fpga-based packet classification in embedded system," in *Instrumentation and Measurement Technology Conference, 2009. I2MTC '09. IEEE*, May 2009, pp. 938–942.

[494] O. Abdel Alim, N. Elboghdadly, M. Ashour, and A. Elaskary, "Fpga implementation and simulink integration of cfo module in wimax receiver model," in *Advances in Computational Tools for Engineering Applications, 2009. ACTEA '09. International Conference on*, July 2009, pp. 137–141.

[495] N. Abbasi, J. Athow, and A. Amer, "Real-time fpga architecture of modified stable euler-number algorithm for image binarization," in *Image Processing (ICIP), 2009 16th IEEE International Conference on*, Nov 2009, pp. 3253–3256.

[496] A. Amiri, A. Khouas, and M. Boukadoum, "Pseudorandom stimuli generation for testing time-to-digital converters on an fpga," *Instrumentation and Measurement, IEEE Transactions on*, vol. 58, no. 7, pp. 2209–2215, July 2009.

[497] R. Ahmad, O. Sidek, and S. Mohd, "Development of crc block onn fpga for zigbee standard," in *Microsystems, Packaging, Assembly and Circuits Technology Conference, 2009. IMPACT 2009. 4th International*, Oct 2009, pp. 282–285.

[498] J. Alves and N. Cruz, "An fpga-based embedded system for a sailing robot," in *Digital System Design, Architectures, Methods and Tools, 2009. DSD '09. 12th Euromicro Conference on*, Aug 2009, pp. 830–837.

[499] M. Akiyama, K. Kouno, K. Kawamoto, T. Sakugawa, H. Akiyama, K. Suematsu, A. Kouda, and M. Watanabe, "Compact all solid state pulsed power generator driven by fpga," in *Pulsed Power Conference, 2009. PPC '09. IEEE*, June 2009, pp. 1223–1226.

[500] Z. Pei-Zhi and H. Shi-Zhen, "If filter design and implementation of fpga," in *Information Science and Engineering (ICISE), 2009 1st International Conference on*, Dec 2009, pp. 2634–2636.

[501] X. Guo-Sheng, "The study on real-time data processing based on ccd scanning and detecting device on fpga," in *Intelligent Computing and Intelligent Systems, 2009. ICIS 2009. IEEE International Conference on*, vol. 3, Nov 2009, pp. 81–84.

[502] A. Aloisio, F. Cevenini, R. Giordano, and V. Izzo, "Emulating the glink chip-set with fpga serial transceivers in the atlas level-1 muon trigger," in *Real Time Conference, 2009. RT '09. 16th IEEE-NPSS*, May 2009, pp. 84–88.

[503] B. Alecsa and A. Onea, "An fpga implementation of an all digital phase locked loop for control applications," in *Intelligent Computer Communication and Processing, 2009. ICCP 2009. IEEE 5th International Conference on*, Aug 2009, pp. 365–368.

[504] A. Amiri, M. Boukadoum, and A. Khouas, "A multihit time-to-digital converter architecture on fpga," *Instrumentation and Measurement, IEEE Transactions on*, vol. 58, no. 3, pp. 530–540, March 2009.

[505] I. Andorko, P. Corcoran, and P. Bigioi, "Fpga based stereo imaging system with applications in computer gaming," in *Games Innovations Conference, 2009. ICE-GIC 2009. International IEEE Consumer Electronics Society's*, Aug 2009, pp. 239–245.

[506] M. Allard, P. Grogan, and J.-P. David, "A scalable architecture for multivariate polynomial evaluation on fpga," in *Reconfigurable Computing and FPGAs, 2009. ReConFig '09. International Conference on*, Dec 2009, pp. 107–112.

[507] A. Aloisio, R. Giordano, and V. Izzo, "Fast control and timing distribution based on fpga-embedded serial transceivers," in *Nuclear Science Symposium Conference Record (NSS/MIC), 2009 IEEE*, Oct 2009, pp. 1147–1151.

[508] D. Zhuo-Zhi, W. Hao-Xian, S. Ying-Hong, M. Xing-Peng, and L. Ai-Ying, "The fpga implementation of high-speed ds-cdma receiver," in *Pervasive Computing Signal Processing and Applications (PCSPA), 2010 First International Conference on*, Sept 2010, pp. 751–754.

[509] J. Albo-Canals, J. Villasante-Bembibre, J. Riera-Babures, and X. Vilasis-Cardona, "8-bit gray-scale dtcnn implementation over an fpga for robot guiding algorithm," in *Cellular Nanoscale Networks and Their Applications (CNNA), 2010 12th International Workshop on*, Feb 2010, pp. 1–2.

[510] P. Achenbach, "A large-scale fpga-based trigger and dead-time free daq system for the kaos spectrometer at mami," in *Real Time Conference (RT), 2010 17th IEEE-NPSS*, May 2010, pp. 1–7.

[511] M. Abusultan, S. Harkness, B. LaMeres, and Y. Huang, "Fpga implementation of a bartlett direction of arrival algorithm for a 5.8ghz circular antenna array," in *Aerospace Conference, 2010 IEEE*, March 2010, pp. 1–10.

[512] M. de los Á Gómez López, J. Olivera, and M. Herrera, "Real time conductance catheter system based on fpga," in *Engineering in Medicine and Biology Society (EMBC), 2010 Annual International Conference of the IEEE*, Aug 2010, pp. 2525–2528.

[513] S. Ting-Qiang, "Fpga design and simulation of the adaptive edge detection pre-processor," in *Information Processing (ISIP), 2010 Third International Symposium on*, Oct 2010, pp. 296–300.

[514] T. Alshawi, A. Bentrcia, M. Elnamaky, and S. Alshebeili, "Low complexity fpga-implementation of a reconfigurable sic multiuser detector for wireless applications," in *Signal Processing and Communication Systems (ICSPCS), 2010 4th International Conference on*, Dec 2010, pp. 1–6.

[515] Z. Hu-Lin and X. Mei, "Iris biometic processor enhanced module fpga-based design," in *Computer Modeling and Simulation, 2010. ICCMS '10. Second International Conference on*, vol. 2, Jan 2010, pp. 259–262.

[516] A. Al-Omary, "Autonomous object seeking robot based on fpga and a single chip microcontroller," in *Computer and Communication Engineering (ICCCE), 2010 International Conference on*, May 2010, pp. 1–6.

[517] C. Xiao-Hui and D. Jian-Zhi, "Design of sha-1 algorithm based on fpga," in *Networks Security Wireless Communications and Trusted Computing (NSWCTC), 2010 Second International Conference on*, vol. 1, April 2010, pp. 532–534.

[518] P. Agnihotri, N. Kaabouch, H. Salehfar, and W. chen Hu, "Fpga-based combined pwm-pfm technique to control dc-dc converters," in *North American Power Symposium (NAPS), 2010*, Sept 2010, pp. 1–6.

[519] G. Luo-Feng, Z. Duo-Li, and G. Ming-Lun, "Performance evaluation of cluster-based homogeneous multiprocessor system-on-chip using fpga device," in *Computer Engineering and Technology (ICCET), 2010 2nd International Conference on*, vol. 4, April 2010, pp. V4–144–V4–147.

[520] N. Li-Pi, Y. Ying-Yun, Y. Yan-Si, and J. Xiu-Hua, "Conversion from cvbs to sdi based on fpga," in *Computer Science and Information Technology (ICCSIT), 2010 3rd IEEE International Conference on*, vol. 8, July 2010, pp. 345–347.

[521] L. Xiao-Feng, L. Ming-Jie, C. Long, and W. Shi-Hu, "Fpga processing technology on impact signal," in *Advanced Computer Theory and Engineering (ICACTE), 2010 3rd International Conference on*, vol. 5, Aug 2010, pp. V5–32–V5–35.

[522] X. Hong-Zhe, W. Jian-Xin, and C. Lu-Meng, "The design and implementation of plate-profile information collecting and processing system based on fpga," in *Computer Science and Information Technology (ICCSIT), 2010 3rd IEEE International Conference on*, vol. 3, July 2010, pp. 541–545.

[523] H. Abdullah and S. Ali, "Implementation of 8-point slantlet transform based polynomial cancellation coding-ofdm system using fpga," in *Systems Signals and Devices (SSD), 2010 7th International Multi-Conference on*, June 2010, pp. 1–6.

[524] M. Akiyama, T. Sakugawa, S. Hosseini, E. Shiraishi, T. Kiyan, and H. Akiyama, "High-performance pulsed-power generator controlled by fpga," *Plasma Science, IEEE Transactions on*, vol. 38, no. 10, pp. 2588–2592, Oct 2010.

[525] L. Guo-Dong and R. Jian, "The spatial mimo channel implement on fpga," in *Electrical and Control Engineering (ICECE), 2010 International Conference on*, June 2010, pp. 2443–2446.

[526] L. Xue-Mei, W. Wu-Chen, H. Li-Gang, and L. Zhao-Chun, "Implementation of telephone remote control system based on fpga," in *Microelectronics and Electronics (PrimeAsia), 2010 Asia Pacific Conference on Postgraduate Research in*, Sept 2010, pp. 37–40.

[527] M. Ali, S. Ahmad, and M. Karim, "Development of an fpga based low power message displaying system using scanning technique," in *Electrical and Computer Engineering (ICECE), 2010 International Conference on*, Dec 2010, pp. 112–115.

[528] B. Alecsa and A. Onea, "Design, validation and fpga implementation of a brushless dc motor speed controller," in *Electronics, Circuits, and Systems (ICECS), 2010 17th IEEE International Conference on*, Dec 2010, pp. 1112–1115.

[529] P. Agarwal, A. Agarwal, and V. Agarwal, "Fpga based space vector modulated trigger controller for a frequency converter," in *Power, Control and Embedded Systems (ICPCES), 2010 International Conference on*, Nov 2010, pp. 1–4.

[530] N. Li-Pi, J. Xiu-Hua, S. Dong-Xin, and Z. Wen-Hui, "Design and implementation of sdi based on fpga," in *Networking and Information Technology (ICNIT), 2010 International Conference on*, June 2010, pp. 429–431.

[531] P. de Aguirre, L. Teixeira, C. Muller, F. Herrmann, L. Pieper, J. de Freitas, G. Dessbesell, and J. Martins, "A full duplex implementation of internet protocol version 4 in an fpga device," in *Programmable Logic Conference (SPL), 2010 VI Southern*, March 2010, pp. 159–162.

[532] N. Alachiotis, S. Berger, and A. Stamatakis, "Efficient pc-fpga communication over gigabit ethernet," in *Computer and Information Technology (CIT), 2010 IEEE 10th International Conference on*, June 2010, pp. 1727–1734.

[533] F. Jian-Qun and S. Zhong-Ke, "Fpga-based embedded speed limit enforcement system on freeway," in *Advanced Computer Theory and Engineering (ICACTE), 2010 3rd International Conference on*, vol. 6, Aug 2010, pp. V6–498–V6–502.

[534] L. Cai-Hong, J. Jin-Shui, and C. Xiu-Ping, "Control module for stepper motor based on fpga," in *E-Product E-Service and E-Entertainment (ICEEE), 2010 International Conference on*, Nov 2010, pp. 1–3.

[535] A. Ahmad, A. Amira, H. Rabah, and Y. Berviller, "Fpga-based architectures of finite radon transform for medical image de-noising," in *Circuits and Systems (APCCAS), 2010 IEEE Asia Pacific Conference on*, Dec 2010, pp. 20–23.

[536] A. do A.Ferreira and E. da S Barros, "A high performance full pipelined arquitecture of mlp neural networks in fpga," in *Electronics, Circuits, and Systems (ICECS), 2010 17th IEEE International Conference on*, Dec 2010, pp. 742–745.

[537] A. Aloisio, F. Cevenini, R. Giordano, and V. Izzo, "Emulating the glink chip set with fpga serial transceivers in the atlas level-1 muon trigger," *Nuclear Science, IEEE Transactions on*, vol. 57, no. 2, pp. 467–471, April 2010.

[538] B. Alecsa and A. Ioan, "Fpga implementation of a matrix structure for integer division," in *Electrical and Electronics Engineering (ISEEE), 2010 3rd International Symposium on*, Sept 2010, pp. 238–243.

[539] A. Afarulrazi, M. Zarafi, W. Utomo, and A. Zar, "Fpga implementation of unipolar spwm for single phase inverter," in *Computer Applications and Industrial Electronics (ICCAIE), 2010 International Conference on*, Dec 2010, pp. 671–676.

[540] L. Nian-Qiang, H. Si-Yu, and C. Shi-Yao, "Application of distributed fir filter based on fpga in the analyzing of ecg signal," in *Intelligent System Design and Engineering Application (ISDEA), 2010 International Conference on*, vol. 1, Oct 2010, pp. 335–338.

[541] A. Abba, F. Caponio, A. Geraci, and G. Ripamonti, "Implementation of high efficiency non-linear least-squares in fpga devices for digital spectroscopy," in *Nuclear Science Symposium Conference Record (NSS/MIC), 2010 IEEE*, Oct 2010, pp. 1371–1376.

[542] W. Xiu-Fang and H. Zhen-Long, "Design and implement of fft processor for ofdma system using fpga," in *Mechanical and Electronics Engineering (ICMEE), 2010 2nd International Conference on*, vol. 2, Aug 2010, pp. V2–297–V2–299.

[543] Z. Zhi Xian, Y. Jian, and Z. Zheng Ji, "Design of relay matrix network control based on fpga," in *Advanced Computer Theory and Engineering (ICACTE), 2010 3rd International Conference on*, vol. 6, Aug 2010, pp. V6–563–V6–565.

[544] L. Li-Feng, M. Hui-Min, and L. Ming-Quan, "A fpga and zernike moments based near-field laser imaging detector multi-scale real-time target recognition algorithm," in *Information Science and Engineering (ISISE), 2010 International Symposium on*, Dec 2010, pp. 370–374.

[545] A. Abu-Khudhair, R. Muresan, and S. X. Yang, "Fpga based real-time adaptive fuzzy logic controller," in *Automation and Logistics (ICAL), 2010 IEEE International Conference on*, Aug 2010, pp. 539–544.

[546] Z. Fei and Z. Hai Shao, "Efficient implementation of intermediate frequency signal processor based on fpga," in *Computational Problem-Solving (ICCP), 2010 International Conference on*, Dec 2010, pp. 316–318.

[547] I. Aleksi, Z. Hocenski, and P. Horvat, "Acoustic localization based on fpga," in *MIPRO, 2010 Proceedings of the 33rd International Convention*, May 2010, pp. 656–658.

[548] A. Agarwal, M. Karmakar, and V. Agarwal, "Design of fpga based controller for trapezoidal modulated cycloinverter," in *Information and Automation for Sustainability (ICIAFs), 2010 5th International Conference on*, Dec 2010, pp. 479–483.

[549] F. Al-Naima and B. Al-Taee, "An fpga based stand-alone solar tracking system," in *Energy Conference and Exhibition (EnergyCon), 2010 IEEE International*, Dec 2010, pp. 513–518.

[550] Z. Chang-Sen and X. Qi, "A design of hdb3 codec based on fpga," in *Advanced Computer Control (ICACC), 2010 2nd International Conference on*, vol. 3, March 2010, pp. 75–78.

[551] S. Abbas, W. Khan, T. Khan, and S. Ahmed, "Implementation of ofdm baseband trasmitter compliant ieee std 802.16d on fpga," in *Communication Software and Networks, 2010. ICCSN '10. Second International Conference on*, Feb 2010, pp. 22–26.

[552] S. Al Junid, M. Haron, Z. Abd Majid, F. Osman, H. Hashim, M. Idros, and M. Dohad, "Optimization of dna sequences data to accelerate dna sequence alignment on fpga," in *Mathematical/Analytical Modelling and Computer Simulation (AMS), 2010 Fourth Asia International Conference on*, May 2010, pp. 231–236.

[553] N. Abbas, S. Derrien, S. Rajopadhye, and P. Quinton, "Accelerating hmmer on fpga using parallel prefixes and reductions," in *Field-Programmable Technology (FPT), 2010 International Conference on*, Dec 2010, pp. 37–44.

[554] M. Da-Cheng and L. Yu-Hai, "Design of a blowout expert control system based on fpga," in *Computer and Automation Engineering (ICCAE), 2010 The 2nd International Conference on*, vol. 4, Feb 2010, pp. 402–405.

[555] F. Ahmed, K. Moustafa, A. Fouad, and A. Fahmy, "Fpga based design and implementation of an adaptive binary integrator," in *Signal Processing and Information Technology (ISSPIT), 2010 IEEE International Symposium on*, Dec 2010, pp. 409–413.

[556] B. Alecsa and A. Onea, "An fpga implementation of a brushless dc motor speed controller," in *Design and Technology in Electronic Packaging (SIITME), 2010 IEEE 16th International Symposium for*, Sept 2010, pp. 99–102.

[557] Z. Ali, A. Arshad, and U. Razzaq, "An fpga based semi-parallel architecture for higher order moving target indication (mti) processing," in *Rapid System Prototyping (RSP), 2010 21st IEEE International Symposium on*, June 2010, pp. 1–7.

[558] H. Guo-Qing and Q. Tian-Xi, "Implementation of ds/fh communication intermediate frequency $\frac{\pi}{4}$ dqpsk modulation based on fpga," in *Intelligent Control and Information Processing (ICICIP), 2011 2nd International Conference on*, vol. 1, July 2011, pp. 233–237.

[559] L. Jing-Kui, "A fast fuzzy stator condition monitoring algorithm using fpga," in *Communication Software and Networks (ICCSN), 2011 IEEE 3rd International Conference on*, May 2011, pp. 267–272.

[560] L. Shu-Lin and L. De-Fang, "Research on spwm inverter controller based on fpga," in *Electrical and Control Engineering (ICECE), 2011 International Conference on*, Sept 2011, pp. 4915–4918.

[561] L. Yi-Long and Z. Jie, "Ofdm channel error detection and fpga implementation," in *Cross Strait Quad-Regional Radio Science and Wireless Technology Conference (CSQRWC), 2011*, vol. 2, July 2011, pp. 914–916.

[562] M. Ming-Chuan, W. Jun-Jun, and S. Jia-Lin, "Design of channel coding in digital video broadcasting system based on fpga," in *Electric Information and Control Engineering (ICEICE), 2011 International Conference on*, April 2011, pp. 4096–4099.

[563] P. Hui-Ling and N. Ya-Lin, "Design of serial communication interface based on fpga," in *Computer Science and Automation Engineering*

*(CSAE), 2011 IEEE International Conference on*, vol. 4, June 2011, pp. 410–414.

[564] R. Wei-Hua, "The realization of the negative logarithmic function based on fpga," in *Electronics, Communications and Control (ICECC), 2011 International Conference on*, Sept 2011, pp. 565–568.

[565] Y. Min, "Design optimization of fpga based viterbi decoder," in *Electric Information and Control Engineering (ICEICE), 2011 International Conference on*, April 2011, pp. 4129–4131.

[566] Z. Yan-Cong, G. Jun-Hua, D. Yong-Feng, and H. Huan-Ping, "Implementation of genetic algorithm for tsp based on fpga," in *Control and Decision Conference (CCDC), 2011 Chinese*, May 2011, pp. 2226–2231.

[567] G. Abbas, Y. Zhu, A. Muhammad, A. Waqar, and J. An, "Backplane bus controller implementation in fpga for hard real time control systems," in *Communication Software and Networks (ICCSN), 2011 IEEE 3rd International Conference on*, May 2011, pp. 451–456.

[568] S. Abbas, P. Sheeba, and S. Thiruvengadam, "Design of downlink pdsch architecture for lte using fpga," in *Recent Trends in Information Technology (ICRTIT), 2011 International Conference on*, June 2011, pp. 947–952.

[569] A. Abbaszadeh and K. Sadeghipour, "A new hardware efficient reconfigurable fir filter architecture suitable for fpga applications," in *Digital Signal Processing (DSP), 2011 17th International Conference on*, July 2011, pp. 1–4.

[570] W. Abdelfatah, J. Georgy, U. Iqbal, and A. Noureldin, "2d mobile multi-sensor navigation system realization using fpga-based embedded processors," in *Electrical and Computer Engineering (CCECE), 2011 24th Canadian Conference on*, May 2011, pp. 001 218–001 221.

[571] M. Abels, T. Wiegand, and S. Paul, "Efficient fpga implementation of a high throughput systolic array qr-decomposition algorithm," in *Signals, Systems and Computers (ASILOMAR), 2011 Conference Record of the Forty Fifth Asilomar Conference on*, Nov 2011, pp. 904–908.

[572] M. Abu Talip and H. Amano, "A design of one-dimensional euler equations for fluid dynamics on fpga," in *Access Spaces (ISAS), 2011 1st International Symposium on*, June 2011, pp. 170–173.

[573] P. Achenbach, C. Gayoso, J. Bernauer, R. Bohm, D. Bosnar, L. Debenjak, M. Distler, A. Esser, I. Friscic, M. Gomez Rodriguez de la Paz, J. Hoffmann, M. Makek, H. Merkel, S. Minami, U. Muller, L. Nungesser, W. Ott, J. Pochodzalla, M. Potokar, I. Rusanov, T. Saito, S. Sanchez Majos, B. Schlimme, S. Sirca, S. Voltz, K. Weindel, and M. Weinriefer, "A large-scale fpga-based trigger and dead-time free daq system for the kaos spectrometer at mami," *Nuclear Science, IEEE Transactions on*, vol. 58, no. 4, pp. 1677–1684, Aug 2011.

[574] P. Adhikari and M. Okaro, "Five-level five-phase pwm signal generation using fpga," in *North American Power Symposium (NAPS), 2011*, Aug 2011, pp. 1–5.

[575] A. Afaneh, H. Yin, and A. Kalashnikov, "Implementation of accurate frame interleaved sampling in a low cost fpga-based data acquisition system," in *Intelligent Data Acquisition and Advanced Computing Systems (IDAACS), 2011 IEEE 6th International Conference on*, vol. 1, Sept 2011, pp. 20–25.

[576] M. Afzal, S. Plaga, and A. Grzemba, "Implementation of a fpga based shared memory system for high bandwidth communication between microprocessor and microcontroller," in *Applied Electronics (AE), 2011 International Conference on*, Sept 2011, pp. 1–4.

[577] P. Agarwal, A. Agarwal, and V. Agarwal, "Implementation of space vector modulation for fpga based frequency converter," in *Telecommunications Energy Conference (INTELEC), 2011 IEEE 33rd International*, Oct 2011, pp. 1–4.

[578] V. Agarwal and A. Agarwal, "Fpga based delta modulated cycloconverter," in *Power Engineering and Optimization Conference (PEOCO), 2011 5th International*, June 2011, pp. 301–305.

[579] ——, "Fpga controlled cyclo-inverter," in *Power Engineering and Optimization Conference (PEOCO), 2011 5th International*, June 2011, pp. 111–115.

[580] A. Ahilan and E. James, "Design and implementation of real time car theft detection in fpga," in *Advanced Computing (ICoAC), 2011 Third International Conference on*, Dec 2011, pp. 353–358.

[581] R. Ahmad, O. Sidek, W. Hassin, and S. Mohd, "Implementation of ieee 802.15.4-based oqpsk-pulse-shaping block on fpga," in *Computer Applications and Industrial Electronics (ICCAIE), 2011 IEEE International Conference on*, Dec 2011, pp. 459–464.

[582] W. Ahmad, Z. Shengbing, H. Amjad, G. Gillani, and A. Jianfeng, "Fpga based real time implementation scheme for arinc 659 backplane data bus," in *Computer Research and Development (ICCRD), 2011 3rd International Conference on*, vol. 4, March 2011, pp. 478–482.

[583] S. Ahmed, K. Samsudin, A. Ramli, and F. Rokhani, "Effective implementation of aes-xts on fpga," in *TENCON 2011 - 2011 IEEE Region 10 Conference*, Nov 2011, pp. 184–186.

[584] W. Aihua, L. Dong, and W. Zhen, "The design of vga data communication based on fpga," in *IT in Medicine and Education (ITME), 2011 International Symposium on*, vol. 1, Dec 2011, pp. 649–651.

[585] R. Ajami and A. Dinh, "Embedded network firewall on fpga," in *Information Technology: New Generations (ITNG), 2011 Eighth International Conference on*, April 2011, pp. 1041–1043.

[586] ——, "Design a hardware network firewall on fpga," in *Electrical and Computer Engineering (CCECE), 2011 24th Canadian Conference on*, May 2011, pp. 000 674–000 678.

[587] A. Akagic and H. Amano, "Performance evaluation of multiple lookup tables algorithms for generating crc on an fpga," in *Access Spaces (ISAS), 2011 1st International Symposium on*, June 2011, pp. 164–169.

[588] E. Akin, I. Aydin, and M. Karakose, "Fpga based intelligent condition monitoring of induction motors: Detection, diagnosis, and prognosis," in *Industrial Technology (ICIT), 2011 IEEE International Conference on*, March 2011, pp. 373–378.

[589] M. Akiyama, T. Goh, Y. Nakagawa, M. Suematsu, T. Sakamoto, and H. Akiyama, "Pulsed power generator driven by fpga and pc," in *Pulsed Power Conference (PPC), 2011 IEEE*, June 2011, pp. 927–929.

[590] N. Alachiotis and A. Stamatakis, "Fpga acceleration of the phylogenetic parsimony kernel?" in *Field Programmable Logic and Applications (FPL), 2011 International Conference on*, Sept 2011, pp. 417–422.

[591] R. Alba-Flores, F. Rios-Gutierrez, and C. Jeanniton, "Qualitative evaluation of a pid controller for autonomous mobile robot navigation implemented in an fpga card," in *Natural Computation (ICNC), 2011 Seventh International Conference on*, vol. 3, July 2011, pp. 1753–1757.

[592] B. Alecsa, M. Cirstea, and A. Onea, "Holistic modeling and fpga implementation of a pmsm speed controller," in *IECON 2011 - 37th Annual Conference on IEEE Industrial Electronics Society*, Nov 2011, pp. 4009–4014.

[593] B. Alecsa and A. Onea, "An optimized fpga implementation of the modified space vector modulation algorithm for ac drives control," in *Field Programmable Logic and Applications (FPL), 2011 International Conference on*, Sept 2011, pp. 393–395.

[594] B. Alecsa, A. Onea, and M. Cirstea, "An efficient fpga implementation of the space vector modulation algorithm," in *Signals, Circuits and Systems (ISSCS), 2011 10th International Symposium on*, June 2011, pp. 1–4.

[595] B. Alecsa, A. Tisan, and M. Cirstea, "High resolution 6 channels pulse width modulator for fpga-based ac motor control," in *Applied Electronics (AE), 2011 International Conference on*, Sept 2011, pp. 1–4.

[596] E. Alkim and E. Kilic, "Chip design for intelligent data classification algorithms and implementation on an fpga: A case study to classify emg signals," in *Signal Processing and Communications Applications (SIU), 2011 IEEE 19th Conference on*, April 2011, pp. 307–310.

[597] I. Almasri, G. Abandah, A. Shhadeh, and A. Shahrour, "Universal isa simulator with soft processor fpga implementation," in *Applied Electrical Engineering and Computing Technologies (AEECT), 2011 IEEE Jordan Conference on*, Dec 2011, pp. 1–6.

[598] A. Aloisio, F. Ameli, V. Bocci, M. Della Pietra, R. Giordano, and V. Izzo, "A fpga-based emulation of the timing trigger and control receiver for the lhc experiments," in *Nuclear Science Symposium and Medical Imaging Conference (NSS/MIC), 2011 IEEE*, Oct 2011, pp. 794–799.

[599] F. Alquaied, A. Almudaifer, and M. AlShaya, "A novel high-speed parallel sorting algorithm based on fpga," in *Electronics, Communications and Photonics Conference (SIECPC), 2011 Saudi International*, April 2011, pp. 1–4.

[600] T. Al-Sabbagh, "Classification and control system for achieving client documents with an fpga interfacing circuit," in *Innovation in Information Communication Technology (ISIICT), 2011 Fourth International Symposium on*, Nov 2011, pp. 137–141.

[601] T. Al-Somani and H. Houssain, "Implementation of gf(2m) elliptic curve cryptoprocessor on a nano fpga," in *Internet Technology and Secured Transactions (ICITST), 2011 International Conference for*, Dec 2011, pp. 7–12.

[602] J. Alves and P. Diniz, "Custom fpga-based micro-architecture for streaming computing," in *Programmable Logic (SPL), 2011 VII Southern Conference on*, April 2011, pp. 51–56.

[603] S. Ameen, M. Al-Jammas, and A. Alenezi, "Fpga implementation of modified architecture for adaptive viterbi decoder," in *Electronics, Communications and Photonics Conference (SIECPC), 2011 Saudi International*, April 2011, pp. 1–9.

[604] H. Amer, A. Rahman, I. Amer, C. Lucarz, and M. Mattavelli, "Methodology and technique to improve throughput of fpga-based cal dataflow programs: Case study of the rvc mpeg-4 sp intra decoder," in *Signal Processing Systems (SiPS), 2011 IEEE Workshop on*, Oct 2011, pp. 186–191.

[605] T. Anand, Y. Waghela, and K. Varghese, "A scalable network port scan detection system on fpga," in *Field-Programmable Technology (FPT), 2011 International Conference on*, Dec 2011, pp. 1–6.

[606] H. Anas, S. Belkouch, M. El Aakif, and N. Chabini, "Fpga implementation of a pipelined 2d-dct and simplified quantization for real-time applications," in *Multimedia Computing and Systems (ICMCS), 2011 International Conference on*, April 2011, pp. 1–6.

[607] C. Ang, C. Jin, P. Leong, and A. van Schaik, "Spiking neural network-based auto-associative memory using fpga interconnect delays," in *Field-Programmable Technology (FPT), 2011 International Conference on*, Dec 2011, pp. 1–4.

[608] M. Abdelfattah and V. Betz, "Design tradeoffs for hard and soft fpga-based networks-on-chip," in *Field-Programmable Technology (FPT), 2012 International Conference on*, Dec 2012, pp. 95–103.

[609] A. Aloisio, V. Bocci, R. Giordano, V. Izzo, L. Sterpone, and M. Violante, "Fpga-based serial links for superb: Design issues vs. radiation tolerance," in *Nuclear Science Symposium and Medical Imaging Conference (NSS/MIC), 2012 IEEE*, Oct 2012, pp. 1595–1596.

[610] A. Amaricai, O. Boncalo, M. Iordate, and B. Marinescu, "A moving window architecture for a hw/sw codesign based canny edge detection for fpga," in *Microelectronics (MIEL), 2012 28th International Conference on*, May 2012, pp. 393–396.

[611] N. Anish, D. Krishnan, S. Moorthi, and M. Selvan, "Fpga based microstepping scheme for stepper motor in space-based solar power systems," in *Industrial and Information Systems (ICIIS), 2012 7th IEEE International Conference on*, Aug 2012, pp. 1–5.

[612] T. Alpert, M. Werz, F. Lang, D. Ferenci, M. Masini, M. Groezing, and M. Berroth, "Arbitrary waveform generator based on fpga and high-speed dac with real-time interface," in *Ph.D. Research in Microelectronics and Electronics (PRIME), 2012 8th Conference on*, June 2012, pp. 1–4.

[613] J. Albo-Canals and G. Pazienza, "Implementing time-derivative cnns on a xilinx spartan fpga," in *Cellular Nanoscale Networks and Their Applications (CNNA), 2012 13th International Workshop on*, Aug 2012, pp. 1–4.

[614] R. Aneesh, B. Sreekumari, and K. Jiju, "Design and implementation of bluetooth mac core with rfcomm on fpga," in *India Conference (INDICON), 2012 Annual IEEE*, Dec 2012, pp. 422–426.

[615] J. Arias-Garcia, C. Llanos, M. Ayala-Rincon, and R. Jacobi, "Fpga implementation of large-scale matrix inversion using single, double and custom floating-point precision," in *Programmable Logic (SPL), 2012 VIII Southern Conference on*, March 2012, pp. 1–6.

[616] S. Al Junid, N. Md Tahir, Z. Abd Majid, Z. Othman, and K. Mohd Shariff, "Reducing memory complexity using data minimization technique on fpga," in *Computer Information Science (ICCIS), 2012 International Conference on*, vol. 1, June 2012, pp. 431–434.

[617] L. Nian-qiang, N. Yun-jie, and Z. Wei, "The application of fpga-based discrete wavelet transform system in eeg analysis," in *Intelligent System Design and Engineering Application (ISDEA), 2012 Second International Conference on*, Jan 2012, pp. 1306–1309.

[618] B. Alecsa, M. Cirstea, and A. Onea, "Simulink modeling and design of an efficient hardware-constrained fpga-based pmsm speed controller," *Industrial Informatics, IEEE Transactions on*, vol. 8, no. 3, pp. 554–562, Aug 2012.

[619] A. Amaricai and O. Boncalo, "Fpga implementation of very high radix square root with prescaling," in *Electronics, Circuits and Systems (ICECS), 2012 19th IEEE International Conference on*, Dec 2012, pp. 221–224.

[620] G. P. Ao, "The basic principle and fpga implementation of nco," in *Instrumentation, Measurement, Computer, Communication and Control (IMCCC), 2012 Second International Conference on*, Dec 2012, pp. 90–94.

[621] N. Ambasana and M. Zaveri, "Analysis of increased parallelism in fpga implementation of neural networks for environment/noise classification and removal," in *Engineering (NUiCONE), 2012 Nirma University International Conference on*, Dec 2012, pp. 1–5.

[622] A. Abu-Aisheh, S. Khader, and O. Hasan, "Sustainable pv-powered fpga-controlled high brightness led illumination systems," in *Global Engineering Education Conference (EDUCON), 2012 IEEE*, April 2012, pp. 1–5.

[623] A. Al-Uraiby, K. Yoshigoe, R. Seker, R. Babiceanu, and N. Yilmazer, "Fpga implementation of low-profile wake-up radio receiver for wireless sensor networks," in *Consumer Electronics (GCCE), 2012 IEEE 1st Global Conference on*, Oct 2012, pp. 20–24.

[624] S. Abbas, K. Geethu, and S. Thiruvengadam, "Implementation of physical downlink control channel (pdcch) for lte using fpga," in *Devices, Circuits and Systems (ICDCS), 2012 International Conference on*, March 2012, pp. 335–339.

[625] M. Agarwal and L. Vachhani, "Development of simulation environment for controllers based on fpga," in *Industrial Electronics and Applications (ICIEA), 2012 7th IEEE Conference on*, July 2012, pp. 349–354.

[626] F. Angarita, V. Torres, A. Perez-Pascual, and J. Valls, "High-throughput fpga-based emulator for structured ldpc codes," in *Electronics, Circuits and Systems (ICECS), 2012 19th IEEE International Conference on*, Dec 2012, pp. 404–407.

[627] O. Al-Khaleel, N. Tulic, and K. Mhaidat, "Fpga implementation of binary coded decimal digit adders and multipliers," in *Mechatronics and its Applications (ISMA), 2012 8th International Symposium on*, April 2012, pp. 1–5.

[628] C. Ang, A. McEwan, A. van Schaik, C. Jin, and P. Leong, "Fpga implementation of biologically-inspired auto-associative memory," *Electronics Letters*, vol. 48, no. 3, pp. 148–149, February 2012.

[629] Z. Zhi-Hai, L. Shan-Ge, L. Wen-Guang, L. Ben-Lu, and Z. Ze-Chao, "Implementation of high-performance multi-structure digital down converter based on fpga," in *Signal Processing (ICSP), 2012 IEEE 11th International Conference on*, vol. 1, Oct 2012, pp. 31–35.

[630] H. Afshari, A. Akin, V. Popovic, A. Schmid, and Y. Leblebici, "Real-time fpga implementation of linear blending vision reconstruction algorithm using a spherical light field camera," in *Signal Processing Systems (SiPS), 2012 IEEE Workshop on*, Oct 2012, pp. 49–54.

[631] G. Yue-yun, L. Yong-hong, F. Qiao-ling, and W. Yu-Long, "Research of intermediate frequency gps signal simulator based on fpga," in *Computer Science Service System (CSSS), 2012 International Conference on*, Aug 2012, pp. 1095–1098.

[632] U. Alqasemi, H. Li, A. Aguirre, and Q. Zhu, "Fpga-based reconfigurable processor for ultrafast interlaced ultrasound and photoacoustic imaging," *Ultrasonics, Ferroelectrics, and Frequency Control, IEEE Transactions on*, vol. 59, no. 7, pp. 1344–1353, July 2012.

[633] A. Adhikary, M. Khanra, and K. Biswas, "Design of fpga based digital controller for 2nd and higher order systems," in *Engineering and Systems (SCES), 2012 Students Conference on*, March 2012, pp. 1–5.

[634] M. Alias, E. Karuppiah, C. P. Kit, and S. Tahir, "Real-time multiple video streams processing on pc-based fpga platform," in *Computer Science and Network Technology (ICCSNT), 2012 2nd International Conference on*, Dec 2012, pp. 391–395.

[635] F. Ahmed, H. Kamel, A. Fahmy, and I. Salem, "Design and fpga implementation of novel radar adaptive post detection integration algorithm," in *Radar Conference (RADAR), 2012 IEEE*, May 2012, pp. 0128–0132.

[636] A. Agarwal and V. Agarwal, "Fpga realization of trapezoidal pwm for generalized frequency converter," *Industrial Informatics, IEEE Transactions on*, vol. 8, no. 3, pp. 501–510, Aug 2012.

[637] R. Adhikary, M. Chakraborty, B. Dara, A. Bharti, and S. Mukherjee, "Fpga based data acquisition and data monitoring system," in *Radar, Communication and Computing (ICRCC), 2012 International Conference on*, Dec 2012, pp. 250–253.

[638] S. Agrawal, P. Engineer, R. Velmurugan, and S. Patkar, "Fpga implementation of particle filter based object tracking in video," in *Electronic System Design (ISED), 2012 International Symposium on*, Dec 2012, pp. 82–86.

[639] N. Alachiotis, S. Berger, and A. Stamatakis, "A versatile udp/ip based pc ¡−¿ fpga communication platform," in *Reconfigurable Computing and FPGAs (ReConFig), 2012 International Conference on*, Dec 2012, pp. 1–6.

[640] M. Alser, M. Assaad, F. Hussin, and I. Yohannes, "Design and fpga implementation of pll-based quarter-rate clock and data recovery circuit," in *Intelligent and Advanced Systems (ICIAS), 2012 4th International Conference on*, vol. 2, June 2012, pp. 825–830.

[641] S. Al Junid, N. Tahir, Z. Majid, F. Osman, and K. Mohd Shariff, "Comparative study for dna data minimization technique on fpga," in *Intelligent and Advanced Systems (ICIAS), 2012 4th International Conference on*, vol. 2, June 2012, pp. 765–767.

[642] A. Akagic and H. Amano, "Performance analysis of fully-adaptable crc accelerators on an fpga," in *Field Programmable Logic and Applications (FPL), 2012 22nd International Conference on*, Aug 2012, pp. 575–578.

[643] J. Albo-Canals, S. Ortega, S. Perdices, A. Badalov, and X. Vilasis-Cardona, "Embedded low-power low-cost camera sensor based on fpga and its applications in mobile robots," in *Electronics, Circuits and Systems (ICECS), 2012 19th IEEE International Conference on*, Dec 2012, pp. 336–339.

[644] M. Aravind and T. Bhattacharya, "Fpga based synchronized sinusoidal pulse width modulation with smooth transition into overmodulation and six step modes of operation for three phase ac motor drives," in *Power Electronics, Drives and Energy Systems (PEDES), 2012 IEEE International Conference on*, Dec 2012, pp. 1–6.

[645] I. Aleksejev, A. Jutman, S. Devadze, S. Odintsov, and T. Wenzel, "Fpga-based synthetic instrumentation for board test," in *Test Conference (ITC), 2012 IEEE International*, Nov 2012, pp. 1–10.

[646] A. Ahmad, N. Ja'afar, and A. Amira, "Fpga-based implementation of 3-d daubechies for medical image compression," in *Biomedical Engineering and Sciences (IECBES), 2012 IEEE EMBS Conference on*, Dec 2012, pp. 683–688.

[647] G. Abbas, U. Farooq, and M. Asad, "Design and fpga implementation of 1-degree-of-freedom discrete pid controller for power switching converter," in *Industrial Electronics and Applications (ICIEA), 2012 7th IEEE Conference on*, July 2012, pp. 1070–1074.

[648] R. Alencar Leao e Silva, L. Barreto, A. Barbosa, D. Joca, and P. Praca, "Digital implementation of a modulation technique for a multilevel inverter on fpga," in *Industry Applications (INDUSCON), 2012 10th IEEE/IAS International Conference on*, Nov 2012, pp. 1–6.

[649] J. Araujo, J. Rodriguez-Andina, J. Farina, F. Vidal, J. Mato, and M. Montealegre, "Fpga-based laser cladding system with increased robustness to optical defects," in *IECON 2012 - 38th Annual Conference on IEEE Industrial Electronics Society*, Oct 2012, pp. 4688–4693.

[650] A. Aprigliano, M. Caciotta, S. Giarnetti, and F. Leccese, "Digital signal generator for real-time fpga power quality alghoritm test," in *Environment and Electrical Engineering (EEEIC), 2012 11th International Conference on*, May 2012, pp. 931–934.

[651] Z. Kai-Feng, T. Hua-Min, and X. Shan-Zhu, "A novel fpga based virtual-pig: Cell matrix with embedded processor," in *Adaptive Hardware and Systems (AHS), 2012 NASA/ESA Conference on*, June 2012, pp. 239–245.

[652] R. Aneesh and K. Jiju, "Design of fpga based 8-bit risc controller ip core using vhdl," in *India Conference (INDICON), 2012 Annual IEEE*, Dec 2012, pp. 427–432.

[653] E. Al Zuraiqi, Y. Tawk, L. Pollard, and C. Christodoulou, "Controlling reconfigurable antennas via neural network embedded into an fpga," in *Antennas and Propagation Society International Symposium (APSURSI), 2012 IEEE*, July 2012, pp. 1–2.

[654] N. Anitha Christy and P. Karthigaikumar, "Fpga implementation of aes algorithm using composite field arithmetic," in *Devices, Circuits and Systems (ICDCS), 2012 International Conference on*, March 2012, pp. 713–717.

[655] T. Ando, V. Moshnyaga, and K. Hashimoto, "A low-power fpga implementation of eye tracking," in *Acoustics, Speech and Signal Processing (ICASSP), 2012 IEEE International Conference on*, March 2012, pp. 1573–1576.

[656] K. Appiah, A. Hunter, P. Dickinson, and H. Meng, "Implementation and applications of tri-state self-organizing maps on fpga," *Circuits and Systems for Video Technology, IEEE Transactions on*, vol. 22, no. 8, pp. 1150–1160, Aug 2012.

[657] A. Agarwal, L. Boppana, and R. Kodali, "A factorization method for fpga implementation of sample rate converter for a multi-standard radio communications," in *TENCON Spring Conference, 2013 IEEE*, April 2013, pp. 530–534.

[658] A. Alimohammad and S. Fard, "Fpga implementation of isotropic and nonisotropic fading channels," *Circuits and Systems II: Express Briefs, IEEE Transactions on*, vol. 60, no. 11, pp. 796–800, Nov 2013.

[659] N. Ali, S. Salim, R. Rahim, S. Anas, Z. Noh, and S. Samsudin, "Pwm controller design of a hexapod robot using fpga," in *Control System, Computing and Engineering (ICCSCE), 2013 IEEE International Conference on*, Nov 2013, pp. 310–314.

[660] S. Angadi, V. Saikumar, and B. Satyanarayana Kumari, "A novel digital controller for microstepping stepper motor drive using fpga for solar array drive assembly in satellites-a comparison with alternative schemes," in *Advances in Computing, Communications and Informatics (ICACCI), 2013 International Conference on*, Aug 2013, pp. 1724–1729.

[661] J. Arias-Garcia, A. Braga, C. Llanos, M. Ayala-Rincon, R. Pezzuol Jacobi, and A. Foltran, "Fpga hil simulation of a linear system block for strongly coupled system applications," in *Industrial Technology (ICIT), 2013 IEEE International Conference on*, Feb 2013, pp. 1017–1022.

[662] Y. An, B. Zhao, and H. Li, "Extension implementation of tcm in the embedded system based on fpga," in *Computer Sciences and Applications (CSA), 2013 International Conference on*, Dec 2013, pp. 749–752.

[663] M. Aydogdu, M. Demirci, and C. Kasnakoglu, "Pipelining harris corner detection with a tiny fpga for a mobile robot," in *Robotics and Biomimetics (ROBIO), 2013 IEEE International Conference on*, Dec 2013, pp. 2177–2184.

[664] C. Agarwal and A. Gupta, "Modeling, simulation based dc motor speed control by implementing pid controller on fpga," in *Confluence 2013: The Next Generation Information Technology Summit (4th International Conference)*, Sept 2013, pp. 467–471.

[665] Z. P. Ang, A. Kumar, and Y. Ha, "High speed video processing using fine-grained processing on fpga platform," in *Field-Programmable Custom Computing Machines (FCCM), 2013 IEEE 21st Annual International Symposium on*, April 2013, pp. 85–88.

[666] K. Arun Kumar, "An implementation of dpd in fpga with a soft proceesor using partial re-configuration for wireless radios," in *Information Communication Technologies (ICT), 2013 IEEE Conference on*, April 2013, pp. 860–864.

[667] M. Aykenar, "Analysis of fpga based recursive and non-recursive digital filters according to hardware cost and performance," in *Signal Processing and Communications Applications Conference (SIU), 2013 21st*, April 2013, pp. 1–4.

[668] M. Aslam, S. Kumar, and R. Holsmark, "An efficient router architecture and its fpga prototyping to support junction based routing in noc platforms," in *Digital System Design (DSD), 2013 Euromicro Conference on*, Sept 2013, pp. 297–300.

[669] M. Al Yaman, A. Ghani, A. Bystrov, P. Degenaar, and P. Maaskant, "Fpga design of a pulse encoder for optoelectronic neural stimulation and recording arrays," in *Biomedical Circuits and Systems Conference (BioCAS), 2013 IEEE*, Oct 2013, pp. 190–193.

[670] R. Agethen, M. PourMousavi, P. Mengs, R. Weigel, and D. Kissinger, "Fpga-based signal control for highly integrated 60 ghz radar distance measurements," in *Radar Conference (EuRAD), 2013 European*, Oct 2013, pp. 121–124.

[671] M. Arsalan, M. Ata-ur Rehman, N. Mehmood, and A. Aziz, "Compact hardware implementation of sha-3 finalist blake on fpga," in *Emerging Technologies (ICET), 2013 IEEE 9th International Conference on*, Dec 2013, pp. 1–5.

[672] G. Athanasiou, H. Michail, G. Theodoridis, and C. Goutis, "High-performance fpga implementations of the cryptographic hash function jh," *Computers Digital Techniques, IET*, vol. 7, no. 1, pp. 29–40, Jan 2013.

[673] K. Arun Kumar, "Fpga implementation of qam modems using pr for reconfigurable wireless radios," in *Emerging Research Areas and 2013 International Conference on Microelectronics, Communications and Renewable Energy (AICERA/ICMiCR), 2013 Annual International Conference on*, June 2013, pp. 1–6.

[674] Y. Ago, K. Nakano, and Y. Ito, "A classification processor for a support vector machine with embedded dsp slices and block rams in the fpga," in *Embedded Multicore Socs (MCSoC), 2013 IEEE 7th International Symposium on*, Sept 2013, pp. 91–96.

[675] N. Aguirre-Dobernack, H. Guzman-Miranda, and M. Aguirre, "Implementation of a machine vision system for real-time traffic sign recognition on fpga," in *Industrial Electronics Society, IECON 2013 - 39th Annual Conference of the IEEE*, Nov 2013, pp. 2285–2290.

[676] M. Ambroise, T. Levi, Y. Bornat, and S. Saighi, "Biorealistic spiking neural network on fpga," in *Information Sciences and Systems (CISS), 2013 47th Annual Conference on*, March 2013, pp. 1–6.

[677] R. Ammendola, A. Biagionil, O. Frezza, F. Cicero, A. Lonardo, P. Paolucci, D. Rossetti, F. Simula, L. Tosoratto, and P. Vicini, "Design and implementation of a modular, low latency, fault-aware, fpga-based network interface," in *Reconfigurable Computing and FPGAs (ReConFig), 2013 International Conference on*, Dec 2013, pp. 1–6.

[678] A. Aysu, M. Sayinta, and C. Cigla, "Low cost fpga design and implementation of a stereo matching system for 3d-tv applications," in *Very Large Scale Integration (VLSI-SoC), 2013 IFIP/IEEE 21st International Conference on*, Oct 2013, pp. 204–209.

[679] N. Anish, M. Chakravarthi, B. Dastagiri Reddy, S. Moorthi, and M. Selvan, "Fpga based control scheme for a single-stage grid-connected solar photovoltaic system," in *AFRICON, 2013*, Sept 2013, pp. 1–4.

[680] S. Abba and J.-A. Lee, "Examining the performance impact of noc parameters for scalable and adaptive fpga-based network-on-chips," in *Computational Intelligence, Modelling and Simulation (CIMSim), 2013 Fifth International Conference on*, Sept 2013, pp. 364–372.

[681] A. Aysu, C. Patterson, and P. Schaumont, "Low-cost and area-efficient fpga implementations of lattice-based cryptography," in *Hardware-Oriented Security and Trust (HOST), 2013 IEEE International Symposium on*, June 2013, pp. 81–86.

[682] M. Aboelaze, "An fpga based low power multiplier for fft in ofdm systems using precomputations," in *ICT Convergence (ICTC), 2013 International Conference on*, Oct 2013, pp. 24–29.

[683] A. Badawy and T. Khattab, "Efficient fpga-based implementation of a novel dual mode spectrum sensing technique," in *Communications, Computers and Signal Processing (PACRIM), 2013 IEEE Pacific Rim Conference on*, Aug 2013, pp. 237–241.

[684] A. Abed and A. Jawad, "Fpga implementation of a modified advanced encryption standard algorithm," in *Electrical, Communication, Computer, Power, and Control Engineering (ICECCPCE), 2013 International Conference on*, Dec 2013, pp. 46–51.

[685] B. Alecsa and A. Onea, "Hardware implementation on fpga of two modulation techniques for three phase inverters," in *Intelligent Computer Communication and Processing (ICCP), 2013 IEEE International Conference on*, Sept 2013, pp. 287–293.

[686] D. Badoni, M. Bizzarri, V. Bonaiuto, B. Checcucci, N. De Simone, L. Federici, A. Fucci, G. Paoluzzi, A. Papi, M. Piccini, A. Salamon, G. Salina, E. Santovetti, F. Sargeni, and S. Venditti, "Fast cluster reconstruction in the na62 liquid krypton electromagnetic calorimeter by using soft core embedded processors in fpga," in *Nuclear Science Symposium and Medical Imaging Conference (NSS/MIC), 2013 IEEE*, Oct 2013, pp. 1–3.

[687] M. AlAli, K. Mhaidat, and I. Aljarrah, "Implementing image processing algorithms in fpga hardware," in *Applied Electrical Engineering and Computing Technologies (AEECT), 2013 IEEE Jordan Conference on*, Dec 2013, pp. 1–5.

[688] C. Guowei and W. Fengying, "The implementation of fir low-pass filter based on fpga and da," in *Intelligent Control and Information Processing (ICICIP), 2013 Fourth International Conference on*, June 2013, pp. 604–608.

[689] S. Alrumaih, A. Alghaihab, A. Ragheb, T. Alshawi, S. Alshebeili, and H. Fathallah, "Fpga-based implementation of channel-blind adaptive equalizers," in *Computer Engineering Systems (ICCES), 2013 8th International Conference on*, Nov 2013, pp. 208–213.

[690] N. Anish, B. Kowshick, and S. Moorthi, "Ethernet based industry automation using fpga," in *AFRICON, 2013*, Sept 2013, pp. 1–4.

[691] H. Ali, X. Zhou, and K. Iqbal, "Fpga architecture for ofdm software defined radio with an optimized direct digital frequency synthesizer," in *Electronics, Communications and Photonics Conference (SIECPC), 2013 Saudi International*, April 2013, pp. 1–5.

[692] F. Aschauer, W. Stechele, and J. Treis, "Fpga based real-time data processing daq system for the mercury imaging x-ray spectrometer," in *Digital System Design (DSD), 2013 Euromicro Conference on*, Sept 2013, pp. 535–542.

[693] M. Al Yaman and P. Degenaar, "Fpga design of an even power distributor for optoelectronic neural stimulation," in *Applied Electrical Engineering and Computing Technologies (AEECT), 2013 IEEE Jordan Conference on*, Dec 2013, pp. 1–4.

[694] A. Antunes Soares and A. Alves de Melo Bento, "Fpga-based unified one-cycle controller for single phase boost pfc," in *Power Electronics Conference (COBEP), 2013 Brazilian*, Oct 2013, pp. 290–297.

[695] M. Aguirre, L. Calvino, and M. Valla, "Multilevel current-source inverter with fpga control," *Industrial Electronics, IEEE Transactions on*, vol. 60, no. 1, pp. 3–10, Jan 2013.

[696] M. Abdelrasoul, M. Ragab, and V. Goulart, "Evaluation of the scalability of round robin arbiters for noc routers on fpga," in *Embedded Multicore Socs (MCSoC), 2013 IEEE 7th International Symposium on*, Sept 2013, pp. 61–66.

[697] W. Azevedo Dias, E. Moreno, and I. Nattan Palmeira, "A new code compression algorithm and its decompressor in fpga-based hardware," in *Integrated Circuits and Systems Design (SBCCI), 2013 26th Symposium on*, Sept 2013, pp. 1–6.

[698] A. Agarwal and V. Agarwal, "A comparative study of fpga based cycloinverter with two modulation techniques," in *Energy Conversion Congress and Exposition (ECCE), 2013 IEEE*, Sept 2013, pp. 5301–5305.

[699] A. Ahmad and R. Gupta, "Digital pwm of cascaded multilevel voltage source inverter using fpga," in *Engineering and Systems (SCES), 2013 Students Conference on*, April 2013, pp. 1–5.

[700] P. Artem and S. Dmitry, "Fpga technologies in medical equipment: Electrical impedance tomography," in *Design Test Symposium, 2013 East-West*, Sept 2013, pp. 1–4.

[701] A. Alilla, M. Faccio, T. Vali, G. Marotta, and L. DeSantis, "A new low cost fingerprint recognition system on fpga," in *Industrial Technology (ICIT), 2013 IEEE International Conference on*, Feb 2013, pp. 988–993.

[702] R. Ammendola, A. Biagioni, O. Frezza, F. Cicero, A. Lonardo, P. Paolucci, D. Rossetti, F. Simula, L. Tosoratto, and P. Vicini, "Virtual-to-physical address translation for an fpga-based interconnect with host and gpu remote dma capabilities," in *Field-Programmable Technology (FPT), 2013 International Conference on*, Dec 2013, pp. 58–65.

[703] J. Abdul-Jabbar and S. Abboodi, "Fpga implementation of modified fractional wavelet transforms," in *Electrical, Communication, Computer, Power, and Control Engineering (ICECCPCE), 2013 International Conference on*, Dec 2013, pp. 95–100.

[704] A. Abba, F. Caponio, A. Cusimano, and A. Geraci, "Implementation of usb 3.0 bus controller in fpga for data transfer in multi-channel applications," in *Nuclear Science Symposium and Medical Imaging Conference (NSS/MIC), 2013 IEEE*, Oct 2013, pp. 1–4.

[705] S. Abourida, S. Cense, C. Dufour, and J. Belanger, "Hardware-in-the-loop simulation of electric systems and power electronics on fpga using physical modeling," in *Power Engineering, Energy and Electrical Drives (POWERENG), 2013 Fourth International Conference on*, May 2013, pp. 775–780.

[706] F. Alves, R. Dias, J. Cabral, L. Rocha, and J. Monteiro, "Fpga controlled mems inclinometer," in *Industrial Electronics (ISIE), 2013 IEEE International Symposium on*, May 2013, pp. 1–4.

[707] D. Bhoyar, C. Dethe, S. Bera, and M. Mushrif, "Fpga implementation of adaptive filter for noise cancellation," in *Electronics and Communication Systems (ICECS), 2014 International Conference on*, Feb 2014, pp. 1–5.

[708] V. Balaji and R. Krishnaveni, "Fpga based low complexity multipurpose reconfigurable image processor," in *Information Communication and Embedded Systems (ICICES), 2014 International Conference on*, Feb 2014, pp. 1–6.

[709] J. Chacko, C. Sahin, D. Nguyen, D. Pfeil, N. Kandasamy, and K. Dandekar, "Fpga-based latency-insensitive ofdm pipeline for wireless research," in *High Performance Extreme Computing Conference (HPEC), 2014 IEEE*, Sept 2014, pp. 1–6.

[710] C. Ceroici and V. Gaudet, "Fpga implementation of a clockless stochastic ldpc decoder," in *Signal Processing Systems (SiPS), 2014 IEEE Workshop on*, Oct 2014, pp. 1–5.

[711] A. Ashir, A. Ata, and M. Salman, "Fpga-based image processing system for quality control and palletization applications," in *Autonomous Robot Systems and Competitions (ICARSC), 2014 IEEE International Conference on*, May 2014, pp. 285–290.

[712] P. Bhartiya, N. Rathore, and D. Fulwani, "A tutorial on implementation of sliding mode observer for dc/dc power converters using fpga," in *Industrial Electronics Society, IECON 2014 - 40th Annual Conference of the IEEE*, Oct 2014, pp. 4153–4159.

[713] O. Boncalo, A. Amaricai, A. Hera, and V. Savin, "Cost-efficient fpga layered ldpc decoder with serial ap-llr processing," in *Field Programmable Logic and Applications (FPL), 2014 24th International Conference on*, Sept 2014, pp. 1–6.

[714] H. Abdullah, F. Sahib, and A. Valenzuela, "Fpga based pi/4-dqpsk complex wavelet packet modulation," in *Communications and Vehicular Technology in the Benelux (SCVT), 2014 IEEE 21st Symposium on*, Nov 2014, pp. 85–89.

[715] S. Sarma and N. Dutt, "Fpga emulation and prototyping of a cyberphysical-system-on-chip (cpsoc)," in *Rapid System Prototyping (RSP), 2014 25th IEEE International Symposium on*, Oct 2014, pp. 121–127.

[716] A. Becher, F. Bauer, D. Ziener, and J. Teich, "Energy-aware sql query acceleration through fpga-based dynamic partial reconfiguration," in *Field Programmable Logic and Applications (FPL), 2014 24th International Conference on*, Sept 2014, pp. 1–8.

[717] J. Balamurugan and E. Logashanmugam, "High speed low cost implementation of advanced encryption standard on fpga," in *Current Trends in Engineering and Technology (ICCTET), 2014 2nd International Conference on*, July 2014, pp. 371–375.

[718] V. Akkala, P. Rajalakshmi, P. Kumar, and U. Desai, "Fpga based ultrasound backend system with image enhancement technique," in *Biosignals and Biorobotics Conference (2014): Biosignals and Robotics for Better and Safer Living (BRC), 5th ISSNIP-IEEE*, May 2014, pp. 1–5.

[719] P. Ayala, P. Bernal, S. Guerra-Jimenez, and A. Fernandez-Correa, "System identification based on re-sampling of periodic signals implemented in fpga," in *Central America and Panama Convention (CONCAPAN XXXIV), 2014 IEEE*, Nov 2014, pp. 1–7.

[720] S. Abbas, D. Selvathi, V. Nandhini, and S. Thiruvengadam, "Synthesis and implementation of spatial multiplexing blocks for 3gpp-lte using fpga," in *Communication and Network Technologies (ICCNT), 2014 International Conference on*, Dec 2014, pp. 243–248.

[721] D. Anjitha and S. Shanmugha, "Fpga implementation of beamforming algorithm for terrestrial radar application," in *Communications and Signal Processing (ICCSP), 2014 International Conference on*, April 2014, pp. 453–457.

[722] Y. Abbas, R. Jidin, N. Jamil, M. Z'aba, M. Rusli, and B. Tariq, "Implementation of prince algorithm in fpga," in *Information Technology and Multimedia (ICIMU), 2014 International Conference on*, Nov 2014, pp. 1–4.

[723] M. Bevilaqua, A. Nied, and J. de Oliveira, "Labview fpga foc implementation for synchronous permanent magnet motor speed control," in *Industry Applications (INDUSCON), 2014 11th IEEE/IAS International Conference on*, Dec 2014, pp. 1–8.

[724] S. Amornwongpeeti, N. Ono, and M. Ekpanyapong, "Design of fpga-based rapid prototype spectral subtraction for hands-free speech applications," in *Asia-Pacific Signal and Information Processing Association, 2014 Annual Summit and Conference (APSIPA)*, Dec 2014, pp. 1–6.

[725] E. Asa, K. Colak, M. Bojarski, and D. Czarkowski, "Fpga based d-pll control technique of cll resonant converter for ev battery chargers," in *Transportation Electrification Conference and Expo (ITEC), 2014 IEEE*, June 2014, pp. 1–6.

[726] H. Akerstedt, S. Muschter, G. Drake, K. Anderson, C. Bohm, M. Oreglia, and F. Tang, "Reliable and redundant fpga based readout design in the atlas tilecal demonstrator," in *Real Time Conference (RT), 2014 19th IEEE-NPSS*, May 2014, pp. 1–3.

[727] N. Bhandari and S. Chowdhury, "Fpga based high performance asynchronous alu based on modified 4 phase handshaking protocol with tapered buffers," in *Devices, Circuits and Communications (ICDCCom), 2014 International Conference on*, Sept 2014, pp. 1–6.

[728] B. Bhatti, M. Umer, W. Ahmed, M. Tariq, and U. Ali, "Carrier and symbol synchronization in digital receivers using feedback compensation loop and early late gate on fpga," in *Robotics and Emerging Allied Technologies in Engineering (iCREATE), 2014 International Conference on*, April 2014, pp. 146–150.

[729] G. Athanasiou, G.-P. Makkas, and G. Theodoridis, "High throughput pipelined fpga implementation of the new sha-3 cryptographic hash algorithm," in *Communications, Control and Signal Processing (ISCCSP), 2014 6th International Symposium on*, May 2014, pp. 538–541.

[730] Z. Zengrong and Q. Yaohui, "The design of fmcw radar liquid level measuring system based on fpga," in *Advanced Research and Technology in Industry Applications (WARTIA), 2014 IEEE Workshop on*, Sept 2014, pp. 536–538.

[731] A. Astarloa, J. Lazaro, U. Bidarte, J. Araujo, and N. Moreira, "Fpga implemented cut-through vs store-and-forward switches for reliable ethernet networks," in *Design of Circuits and Integrated Circuits (DCIS), 2014 Conference on*, Nov 2014, pp. 1–6.

[732] J. Canseco, V. Cruz-Sanchez, A. Flores-Abad, O. Vergara-Villegas, and M. Nandayapa, "Fractional position estimation for optical incremental encoder based on fpga," in *Central America and Panama Convention (CONCAPAN XXXIV), 2014 IEEE*, Nov 2014, pp. 1–6.

[733] A. Carlos, F. Carlos, O. Reyes, and C. Javier, "Fpga implementation of a huffman decoder for high speed seismic data decompression," in *Data Compression Conference (DCC), 2014*, March 2014, pp. 396–396.

[734] L. Aksoy, P. Flores, and J. Monteiro, "Efficient design of fir filters using hybrid multiple constant multiplications on fpga," in *Computer Design (ICCD), 2014 32nd IEEE International Conference on*, Oct 2014, pp. 42–47.

[735] M. Al Kadi, M. Ferger, V. Stegemann, and M. Hubner, "Multi-fpga reconfigurable system for accelerating matlab simulations," in *Field Programmable Logic and Applications (FPL), 2014 24th International Conference on*, Sept 2014, pp. 1–4.

[736] S. Akkaya, O. Akbati, and H. Gorgun, "Multiple closed loop system control with digital pid controller using fpga," in *Control, Decision and Information Technologies (CoDIT), 2014 International Conference on*, Nov 2014, pp. 764–769.

[737] P. Broulim, J. Broulim, V. Georgiev, and J. Moldaschl, "Very high resolution time measurement in fpga," in *Telecommunications Forum Telfor (TELFOR), 2014 22nd*, Nov 2014, pp. 745–748.

[738] J. Anwer, M. Platzner, and S. Meisner, "Fpga redundancy configurations: An automated design space exploration," in *Parallel Distributed Processing Symposium Workshops (IPDPSW), 2014 IEEE International*, May 2014, pp. 275–280.

[739] A. Boonpoonga, P. Sirisuk, and M. Krairiksh, "On fpga implementation of blind adaptive antenna," in *Electrical Engineering Congress (iEECON), 2014 International*, March 2014, pp. 1–4.

[740] K. Boonyi, J. Tagapanij, and A. Boonpoonga, "Fpga-based hardware/software implementation for mimo wireless communications," in *Electrical Engineering Congress (iEECON), 2014 International*, March 2014, pp. 1–4.

[741] M. Carraro, M. Zigliotto, and L. Peretti, "Fpga-based hierarchical finite-states predictive control for pmsm drives," in *Power Electronics, Machines and Drives (PEMD 2014), 7th IET International Conference on*, April 2014, pp. 1–6.

[742] N. At, J.-L. Beuchat, E. Okamoto, I. San, and T. Yamazaki, "Compact hardware implementations of chacha, blake, threefish, and skein on fpga," *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol. 61, no. 2, pp. 485–498, Feb 2014.

[743] S. Blokzyl, M. Vodel, and W. Hardt, "Fpga-based approach for runway boundary detection in high-resolution colour images," in *Sensors Applications Symposium (SAS), 2014 IEEE*, Feb 2014, pp. 59–64.

[744] D. Bhoyar, C. Dethe, and M. Mushrif, "Fpga implementation of modified leaky least mean square channel estimation algorithm," in *Devices, Circuits and Systems (ICDCS), 2014 2nd International Conference on*, March 2014, pp. 1–5.

[745] A. Ahmad, A. Gupta, and P. Samuel, "Embedded system design for digital control of single phase z-source inverter using fpga," in *Environment and Electrical Engineering (EEEIC), 2014 14th International Conference on*, May 2014, pp. 402–407.

[746] M. Almekkawy, J. Xu, and M. Chirala, "An optimized ultrasound digital beamformer with dynamic focusing implemented on fpga," in *Engineering in Medicine and Biology Society (EMBC), 2014 36th Annual International Conference of the IEEE*, Aug 2014, pp. 3296–3299.

[747] R. Ambika, S. Ramachandran, and K. Kashwan, "Data security using serial commutative rsa core for multiple fpga system," in *Devices, Circuits and Systems (ICDCS), 2014 2nd International Conference on*, March 2014, pp. 1–5.

[748] B. Bozorgzadeh, D. Covey, B. Heidenreich, P. Garris, and P. Mohseni, "Real-time processing of fast-scan cyclic voltammetry (fscv) data using a field-programmable gate array (fpga)," in *Engineering in Medicine and Biology Society (EMBC), 2014 36th Annual International Conference of the IEEE*, Aug 2014, pp. 2036–2039.

[749] L. Araneda and M. Figueroa, "Real-time digital video stabilization on an fpga," in *Digital System Design (DSD), 2014 17th Euromicro Conference on*, Aug 2014, pp. 90–97.

[750] F. Amiel, B. Barry, and M. Trocan, "A contour preserving fpga architecture for pal to xga format conversion," in *New Circuits and*

*Systems Conference (NEWCAS), 2014 IEEE 12th International*, June 2014, pp. 205–208.

[751] M. Ben Abdallah, G. Laffont, N. Roussel, and P. Ferdinand, "High-speed tunable fdml laser, interfaced to a continuous fpga acquisition system, for fbg accelerometer interrogation," in *SENSORS, 2014 IEEE*, Nov 2014, pp. 29–31.

[752] A. Amaricai, C.-E. Gavriliu, and O. Boncalo, "An fpga sliding window-based architecture harris corner detector," in *Field Programmable Logic and Applications (FPL), 2014 24th International Conference on*, Sept 2014, pp. 1–4.

[753] J. Bag, S. Roy, and S. Sarkar, "Fpga implementation of advanced health care system using zig-bee enabled rfid technology," in *Advance Computing Conference (IACC), 2014 IEEE International*, Feb 2014, pp. 899–904.

[754] A. Alouane, A. Ben Rhouma, and A. Kheder, "Fpga implementation of a dedicated self control strategy for a delta inverter fed bdcm drive," in *Electrical Sciences and Technologies in Maghreb (CISTEM), 2014 International Conference on*, Nov 2014, pp. 1–8.

[755] H. Block and T. Maruyama, "An fpga hardware acceleration of the indirect calculation of tree lengths method for phylogenetic tree reconstruction," in *Field Programmable Logic and Applications (FPL), 2014 24th International Conference on*, Sept 2014, pp. 1–4.

[756] S. Amano and K. Akatsu, "Study on high frequency inverter with 100khz current feedback control by using fpga," in *Electrical Machines and Systems (ICEMS), 2014 17th International Conference on*, Oct 2014, pp. 3392–3397.

[757] K. Onohara, K. Ishii, Y. Akiyama, M. Noda, M. Nogami, T. Sugihara, T. Mizuochi, Y. Yoshida, A. Maruta, and K.-I. Kitayama, "Prototype of uplink transceiver for ifdma-pon system by fpga emulation," *Photonics Technology Letters, IEEE*, vol. 27, no. 1, pp. 81–84, Jan 2015.

[758] C. Gonzalez, S. Lopez, D. Mozos, and R. Sarmiento, "Fpga implementation of the hysime algorithm for the determination of the number of endmembers in hyperspectral data," *Selected Topics in Applied Earth Observations and Remote Sensing, IEEE Journal of*, vol. PP, no. 99, pp. 1–14, 2015.

[759] P. Khose and V. Raut, "Implementation of aes algorithm on fpga for low area consumption," in *Pervasive Computing (ICPC), 2015 International Conference on*, Jan 2015, pp. 1–4.

[760] P. Jilna, P. Deepthi, S. Sameer, P. Sathidevi, and A. Vijitha, "Fpga implementation of an elliptic curve based integrated system for encryption and authentication," in *Signal Processing, Informatics, Communication and Energy Systems (SPICES), 2015 IEEE International Conference on*, Feb 2015, pp. 1–6.

[761] J. Amaro, B. Yiu, G. Falcao, M. Gomes, and A. Yu, "Software-based high-level synthesis design of fpga beamformers for synthetic aperture imaging," *Ultrasonics, Ferroelectrics, and Frequency Control, IEEE Transactions on*, vol. 62, no. 5, pp. 862–870, May 2015.

[762] E. Fernandez, J. Villarreal, S. Lonardi, and W. Najjar, "Fhast: Fpga-based acceleration of bowtie in hardware," *Computational Biology and Bioinformatics, IEEE/ACM Transactions on*, vol. PP, no. 99, pp. 1–1, 2015.

[763] J. Jo, B.-M. Han, and H. Cha, "Fpga based dsc-pll for grid harmonics and voltage unbalance effect elimination," in *Applied Power Electronics Conference and Exposition (APEC), 2015 IEEE*, March 2015, pp. 2212–2216.

[764] S. Shreejith and S. Fahmy, "Extensible flexray communication controller for fpga-based automotive systems," *Vehicular Technology, IEEE Transactions on*, vol. 64, no. 2, pp. 453–465, Feb 2015.

[765] S. Gdaim, A. Mtibaa, and M. Mimouni, "Design and experimental implementation of dtc of an induction machine based on fuzzy logic control on fpga," *Fuzzy Systems, IEEE Transactions on*, vol. 23, no. 3, pp. 644–655, June 2015.

[766] P. Swierczynski, M. Fyrbiak, P. Koppe, and C. Paar, "Fpga trojans through detecting and weakening of cryptographic primitives," *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on*, vol. PP, no. 99, pp. 1–1, 2015.

[767] H. Giefers, R. Polig, and C. Hagleitner, "Accelerating arithmetic kernels with coherent attached fpga coprocessors," in *Design, Automation Test in Europe Conference Exhibition (DATE), 2015*, March 2015, pp. 1072–1077.

[768] D. Bhat, A. Kaur, and S. Singh, "Wireless sensor network specific low power fir filter design and implementation on fpga," in *Computing for Sustainable Global Development (INDIACom), 2015 2nd International Conference on*, March 2015, pp. 1534–1536.

[769] M. Kadam, K. Sawarkar, and S. Mande, "Investigation of suitable dsp architecture for efficient fpga implementation of fir filter," in *Communication, Information Computing Technology (ICCICT), 2015 International Conference on*, Jan 2015, pp. 1–4.

[770] O. Dhede and S. Shah, "A review: Hardware implementation of aes using minimal resources on fpga," in *Pervasive Computing (ICPC), 2015 International Conference on*, Jan 2015, pp. 1–3.

[771] R. Biradar, A. Chatterjee, P. Mishra, and K. George, "Fpga implementation of a multilayer artificial neural network using system-on-chip design methodology," in *Cognitive Computing and Information Processing (CCIP), 2015 International Conference on*, March 2015, pp. 1–6.

[772] H. Chang, I. Jiang, H. Hofstee, D. Jamsek, and G. Nam, "Feature detection for image analytics via fpga acceleration," *IBM Journal of Research and Development*, vol. 59, no. 2/3, pp. 8:1–8:10, March 2015.

[773] R. Rasu, P. Sundaram, and N. Santhiyakumari, "Fpga based non-invasive heart rate monitoring system for detecting abnormalities in fetal," in *Signal Processing And Communication Engineering Systems (SPACES), 2015 International Conference on*, Jan 2015, pp. 375–379.

[774] T. Machida, D. Yamamoto, M. Iwamoto, and K. Sakiyama, "Implementation of double arbiter puf and its performance evaluation on fpga," in *Design Automation Conference (ASP-DAC), 2015 20th Asia and South Pacific*, Jan 2015, pp. 6–7.

[775] W. Wang, J. YAN, N. Xu, Y. Wang, and F.-h. Hsu, "Real-time high-quality stereo vision system in fpga," *Circuits and Systems for Video Technology, IEEE Transactions on*, vol. PP, no. 99, pp. 1–1, 2015.

[776] J. Gonzalez, L. Wienbrandt, J. Kassens, D. Ellinghaus, M. Schimmler, and B. Schmidt, "Parallelizing epistasis detection in gwas on fpga and gpu-acceleratedcomputing systems," *Computational Biology and Bioinformatics, IEEE/ACM Transactions on*, vol. PP, no. 99, pp. 1–1, 2015.

[777] S. Verma, D. Gaba, and B. Pandey, "Gtl io standards based wlan specific low power alu design on fpga," in *Computing for Sustainable Global Development (INDIACom), 2015 2nd International Conference on*, March 2015, pp. 1484–1489.

[778] A. Panda, D. Mishra, and H. Ratha, "Fpga implementation of software defined radio-based flight termination system," *Industrial Informatics, IEEE Transactions on*, vol. 11, no. 1, pp. 74–82, Feb 2015.

[779] K. Tanaka, Y. Lee, E. Nomoto, T. Sugawara, and H. Arimoto, "Experimental evaluation of recovery from multiple failures in multicore fiber links using fpga-based optical switch units," *Lightwave Technology, Journal of*, vol. 33, no. 1, pp. 201–211, Jan 2015.

[780] A. Badawi, A. Alqarni, A. Aljuffri, M. S. BenSaleh, A. M. Obeid, and S. M. Qasim, "Fpga realization and performance evaluation of fixed-width modified baugh-wooley multiplier," in *Technological Advances in Electrical, Electronics and Computer Engineering (TAEECE), 2015 Third International Conference on*, April 2015, pp. 155–158.

[781] X. Ren, Y. Qihang, B. Chen, N. Zheng, and P. Ren, "A 128-way fpga platform for the acceleration of klms algorithm," in *Design Automation Conference (ASP-DAC), 2015 20th Asia and South Pacific*, Jan 2015, pp. 18–19.

[782] Z. Szadkowski, "An optimization of the fpga based wavelet trigger in radio detection of cosmic rays," *Nuclear Science, IEEE Transactions on*, vol. PP, no. 99, pp. 1–9, 2015.

[783] U. Narula, R. Tripathi, and G. Wakhle, "High speed 16-bit digital vedic multiplier using fpga," in *Computing for Sustainable Global Development (INDIACom), 2015 2nd International Conference on*, March 2015, pp. 121–124.

[784] M. Kang, J. Kim, and J.-M. Kim, "An fpga-based multicore system for real-time bearing fault diagnosis using ultrasampling rate ae signals," *Industrial Electronics, IEEE Transactions on*, vol. 62, no. 4, pp. 2319–2329, April 2015.

[785] R. Elschner, F. Frey, C. Schmidt-Langhorst, J. K. Fischer, and C. Schubert, "Fpga implementation of a data-aided single-carrier frequency-domain equalizer for format-flexible receivers," in *Photonic Networks; 16. ITG Symposium; Proceedings of*, May 2015, pp. 1–6.

[786] W. Li, L.-A. Gregoire, and J. Belanger, "A modular multilevel converter pulse generation and capacitor voltage balance method optimized for fpga implementation," *Industrial Electronics, IEEE Transactions on*, vol. 62, no. 5, pp. 2859–2867, May 2015.

[787] S. Bhalekar and P. Chilveri, "A review: Fpga based word matching stage of blastn," in *Pervasive Computing (ICPC), 2015 International Conference on*, Jan 2015, pp. 1–4.

[788] S. Khan, P. Manwaring, A. Borsic, and R. Halter, "Fpga-based voltage and current dual drive system for high frame rate electrical impedance tomography," *Medical Imaging, IEEE Transactions on*, vol. 34, no. 4, pp. 888–901, April 2015.

[789] K. Sanni, G. Garreau, J. Molin, and A. Andreou, "Fpga implementation of a deep belief network architecture for character recognition using stochastic computation," in *Information Sciences and Systems (CISS), 2015 49th Annual Conference on*, March 2015, pp. 1–5.

[790] A. Ramachandran, Y. Heo, W. mei Hwu, J. Ma, and D. Chen, "Fpga accelerated dna error correction," in *Design, Automation Test in Europe Conference Exhibition (DATE), 2015*, March 2015, pp. 1371–1376.

[791] J. Xie, P. Meher, and Z.-H. Mao, "High-throughput finite field multipliers using redundant basis for fpga and asic implementations," *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol. 62, no. 1, pp. 110–119, Jan 2015.

[792] S. Munoz and J. Hormigo, "High-throughput fpga implementation of qr decomposition," *Circuits and Systems II: Express Briefs, IEEE Transactions on*, vol. PP, no. 99, pp. 1–1, 2015.

[793] G. Chaple, R. Daruwala, and M. Gofane, "Comparisions of robert, prewitt, sobel operator based edge detection methods for real time uses on fpga," in *Technologies for Sustainable Development (ICTSD), 2015 International Conference on*, Feb 2015, pp. 1–4.

[794] T. Kumar, A. Memon, S. Musavi, F. Khan, and R. Kumar, "Fpga based energy efficient ecg machine design using different io standard," in *Computing for Sustainable Global Development (INDIACom), 2015 2nd International Conference on*, March 2015, pp. 1541–1545.

[795] X. Lu, H. Chen, B. Gao, Z. Zhang, and W. Jin, "Data-driven predictive gearshift control for dual-clutch transmissions and fpga implementation," *Industrial Electronics, IEEE Transactions on*, vol. 62, no. 1, pp. 599–610, Jan 2015.

[796] J. Nunez-Perez, J. Cardenas-Valdez, C. Gontrand, R. Jauregui-Duran, and J. Reynoso-Hernandez, "Test bed for low-cost measurement of am/am and am/pm effects in rf pas based on fpga," in *Electronics, Communications and Computers (CONIELECOMP), 2015 International Conference on*, Feb 2015, pp. 87–92.

[797] Y. Tang and N. Bergmann, "A hardware scheduler based on task queues for fpga-based embedded real-time systems," *Computers, IEEE Transactions on*, vol. 64, no. 5, pp. 1254–1267, May 2015.

[798] X. Chen, G. Zhang, H. Wang, R. Wu, P. Wu, and L. Zhang, "Mrp: Mix real cores and pseudo cores for fpga-based chip-multiprocessor simulation," in *Design, Automation Test in Europe Conference Exhibition (DATE), 2015*, March 2015, pp. 211–216.

[799] H. Nguyen, J. Agbinya, and J. Devlin, "Fpga-based implementation of multiple modes in near field inductive communication using frequency splitting and mimo configuration," *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol. 62, no. 1, pp. 302–310, Jan 2015.

[800] R. Palisetty, V. Sinha, S. Mallick, and K. Ray, "Fpga prototyping of energy dispersal and improved error efficiency techniques for dvb-satellite standard," in *VLSI Systems, Architecture, Technology and Applications (VLSI-SATA), 2015 International Conference on*, Jan 2015, pp. 1–5.

[801] H. Hikawa and K. Kaida, "Novel fpga implementation of hand sign recognition system with som – hebb classifier," *Circuits and Systems for Video Technology, IEEE Transactions on*, vol. 25, no. 1, pp. 153–166, Jan 2015.

[802] F. Saqib, A. Dutta, J. Plusquellic, P. Ortiz, and M. Pattichis, "Pipelined decision tree classification accelerator implementation in fpga (dt-caif)," *Computers, IEEE Transactions on*, vol. 64, no. 1, pp. 280–285, Jan 2015.

[803] W. Li, P. Yadmellat, and M. Kermani, "Linearized torque actuation using fpga-controlled magnetorheological actuators," *Mechatronics, IEEE/ASME Transactions on*, vol. 20, no. 2, pp. 696–704, April 2015.

[804] L. Herrera, C. Li, X. Yao, and J. Wang, "Fpga-based detailed real-time simulation of power converters and electric machines for ev hil applications," *Industry Applications, IEEE Transactions on*, vol. 51, no. 2, pp. 1702–1712, March 2015.

[805] L. Nazir and R. Mir, "Performance analysis of various scheduling algorithms using fpga platforms," in *VLSI Systems, Architecture, Technology and Applications (VLSI-SATA), 2015 International Conference on*, Jan 2015, pp. 1–4.

[806] N. Roshandel Tavana and V. Dinavahi, "Real-time fpga-based analytical space harmonic model of permanent magnet machines for hardware-in-the-loop simulation," *Magnetics, IEEE Transactions on*, vol. PP, no. 99, pp. 1–1, 2015.