(article begins on next page)

Optimization of Fully-Integrated Power Converter Circuits Comprising Tapered Inductor Layout and Temperature Effects

Piet Callemeyn, Dimitri De Jonghe, Georges Gielen and Michiel Steyaert
ESAT-MICAS, KU Leuven,
Kasteelpark Arenberg 10,
B-3001 Leuven, Belgium
Email: piet.callemeyn@esat.kuleuven.be

Abstract—**A technique for the optimization of fully-integrated inductive DC-DC converters is presented. An optimization framework is used to acquire an optimal converter, focusing on the on-chip inductor as well as on the accurate layout-based modeling of temperature effects. For the inductor in inductive DC-DC converters, a tapered topology is introduced. A fully-integrated DC-DC boost converter is designed and optimized in a $0.13\ \mu m$ CMOS technology. The power loss in the circuit is reduced with $27\ \%$ resulting in a $7\ \%$ efficiency improvement, compared to a fully-integrated DC-DC boost converter with a regular inductor topology.**

I. INTRODUCTION

Until recently, the analog and mixed-signal designer was seen as an "artist" capable of designing an optimal circuit, based on years of design experience and thorough circuit knowledge. Nowadays, promising techniques in the domain of artificial intelligence are emerging. These techniques can simplify the work of an analog designer. Tools have already been developed for the optimal sizing of circuits [1]. The combination of the circuit knowledge of the designer and the use of these tools enable the designer to determine the most optimal circuit in a short time. Using these tools, even inexperienced designers are now able to identify the trade-offs in a circuit.

State-of-the-art power management techniques require fully-integrated DC-DC converters, as it becomes more cost-efficient to integrate all the passive components on the same die [2]. The integration of these components is paramount for the overall performance of the monolithic solution. This high efficiency can be achieved by the use of design tools.

In this work, an optimization framework is used in order to optimize the complex trade-offs encountered in the design of DC-DC converters. The effect of the inductor topology as well as temperature effects are taken into account in this layout-aware framework. Moreover, a tapered on-chip inductor topology is presented. It enables an efficiency increase compared to the regular inductor topologies that are used, without adding an extra cost in the processing.

The optimization framework is described in section II. The architecture of the inductive DC-DC converter along with the tapered inductor topology and temperature effects is discussed
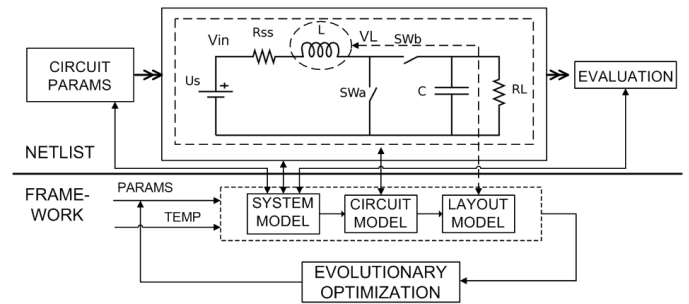

Fig. 1. The flow of the optimization framework (bottom part), integrating different high-level models for a DC-DC boost converter (top part).

in section III. Section IV gives an overview of the results and conclusions are drawn in section V.

II. OPTIMIZATION FRAMEWORK

An inductive DC-DC boost converter, as depicted in the top part of Figure 1 will be optimized. A high-level *system and circuit model* has been designed for this DC-DC boost converter in [3]. This high-level abstraction model enables a designer to perform an accurate evaluation (within 3% accuracy range of SPICE simulations) of the converter performance, using specified circuit parameters, without the need for time-intensive SPICE simulations. The existing model is adapted by the authors and enhanced in this paper to include temperature effects as well.

The inductor design has a major impact on the efficiency of a fully integrated DC-DC boost converter, due to the ever-present power losses in the inductor. Therefore it is important to have accurate simulations of this component. However, finite-element 3D-simulations of inductors are very time-intensive. The technique presented below will be incorporated into the model, hereby enabling highly accurate inductor optimization without extensive simulation times. In Figure 1 this is presented as the *layout model*.

The high-level DC-DC converter model and inductor

optimization technique are integrated in a global evolutionary framework. The framework uses a combination of existing evolutionary techniques, e.g. NSGA-II [4], SPEA [5] and ALPS [6]. This combination yields an efficient and robust framework, applicable for layout-aware optimization of a relatively large class of analog building blocks. The general flow is presented in the bottom part of Figure 1.

There are two simulation possibilities for the inductor layout. The first one is to perform fast evaluation using field-solvers. An example of such a tool for simulation of inductors is FastHenry [7]. On the other hand, when electromagnetic coupling effects need to be considered, expensive evaluations are needed. For instance, Momentum can generate accurate simulation results for 3D on-chip structures. In general, the expensive evaluations are more accurate than the fast evaluations. The total cost of the expensive simulations can be reduced using techniques as MC, DOE, LHS and active learning sampling selection, see [8] and [9].

In this optimization framework, a fast evaluation is chosen, where the simulated samples are stored in a database. These samples can be reused when similar design points occur. The loss in accuracy compared to the expensive evaluations is in this case irrelevant to consider the use of slightly more accurate expensive simulations. However, in power converters using on-chip transformers the use of expensive electromagnetic simulations is motivated and in such a case one would choose to follow this path. This is possible in the framework, but out of the scope of this paper.

To conclude, the temperature effects are considered in the optimization loop as well. As will be discussed in section III-C, the temperature effects will have a considerable influence on the overall converter performance.

III. ARCHITECTURE

A. Inductive DC-DC boost converter

The basic circuit for an inductive DC-DC boost converter is given in Figure 2 at the top right-hand side. The quality factor of the inductor determines the efficiency of the converter. Since all power to the load needs to be delivered through the inductor, the series resistance of the inductor will determine the efficiency of the complete circuit. Moreover, the parasitic capacitive coupling of the inductor to the substrate will lead to power losses.

Different approaches exist to increase the quality factor of inductors. One way to achieve this is to apply ferro-magnetic materials to metal-track inductors [10] or using bondwire inductors [11]. Another way is the addition of a thick metal-film on top of the chip [12], under-etching of the substrate [13] or even the use of an aluminium substrate [14]. However these are expensive methods. In the presented improved inductor topology, the standard CMOS process is used without the need for additional costly processing steps.

B. Inductor optimization

Two trends are identified in the design of an inductor. First, one wants to reduce the parasitic series resistance as much as
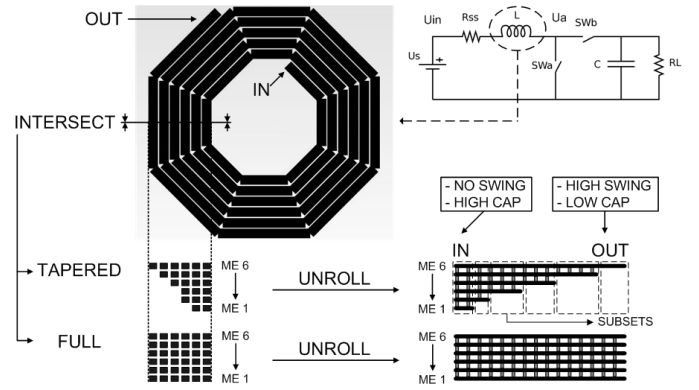

Fig. 2.   Intersection of an inductor with added tapered vs. full metal layers.

possible. Secondly, one wants the inductance to be as high as possible. The latter can be realized by increasing the number of windings. However, because of the increased length of the metal track, an increasing parasitic series resistance R_S arises (1). In (1), ρ and l denote the resistivity and length of the metal track respectively. A indicates the cross-section area of this metal track.

Furthermore, the inductor area will increase, yielding an increase of the parasitic substrate capacitance C_{sub} (2). In (2), ϵ_0 and ϵ_r indicate the absolute and relative permittivities of the oxide between the metal track and substrate, A_{ovl} indicates the overlapping area of metal track and substrate and d indicates the distance between the inductor metal track and substrate.

$$R_S = \frac{\rho * l}{A} \tag{1}$$

$$C_{sub} = \frac{\epsilon_0 * \epsilon_r * A_{ovl}}{d} \tag{2}$$

A solution to reduce the parasitic series resistance is the use of more parallel-connected metal layers, as indicated in the *full* intersection in Figure 2. However, since more metal layers are used, the distance of the lowest metal layer to the substrate decreases. This increases the total parasitic substrate capacitance C_{sub} (2) and hence the power losses in the substrate increase. This is indicated in (3), with input voltage U_S, average voltage drop ΔU over the inductor and switching frequency f_{SW}.

$$P_{loss,substrate} = C_{sub} * U_S * \Delta U * f_{sw} \tag{3}$$

In order to solve this problem, a tapered inductor topology is introduced. In this topology, an evenly increasing number of metal layers is used for the inductor metal tracks. The number increases along the length of the metal track, as indicated in the *tapered* intersection presented in Figure 2. This leads to an increase of series resistance, compared to a solution with added *full* metal. However, C_{sub} and the corresponding power losses are lower, because less metal is close to the substrate. Because of the continuous distribution of the metal layers, a trade-off is now determined between series resistance and parasitic substrate capacitance. This trade-off is presented in Figure 3. The horizontal axis presents
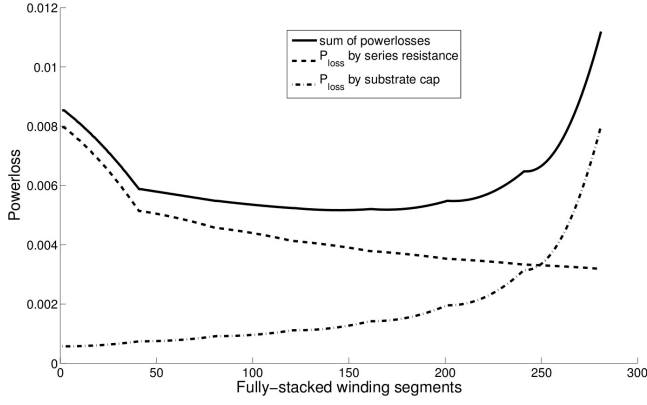
Fig. 3. Trade-off between power losses caused by series resistance vs. substrate capacitance. Number of segments indicates more added metal in layers.
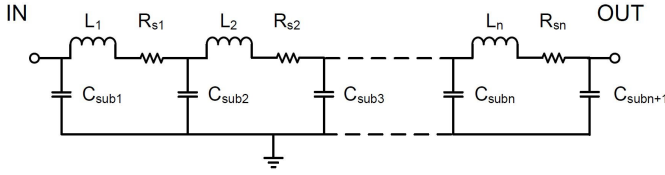

Fig. 4. The lumped inductor model.

Fig. 5. Temperature effect on efficiency for varying output power.

C. Temperature effects

As was determined in [15], the efficiency of the converter will go down with an increasing output power. This can be seen in Figure 5 for the designed optimal DC-DC converter that will be discussed in section IV.

In this figure, two trends can be observed. First, for both curves, a decrease of the efficiency is present with increasing output power. The reason for this behavior is the increasing energy loss in the parasitic series resistance of the inductor. A second trend is the decreasing efficiency when temperature effects are taken into account. The efficiency will decrease more and more with increasing output power, compared to the curve where no temperature effects are taken into account. At high output power, the circuit will heat up due to the increasing losses in the parasitic series resistance R_S of the inductor. Due to this heating, the series resistance will increase as well, now equaling $R_{S,temp}$. This has been modeled as follows:

$$R_{S,temp} = R_S * (1 + \alpha * \Delta T) \qquad (5)$$

Here, R_S is the initial parasitic series resistance of the inductor at $25°C$. ΔT is the temperature rise and α is the temperature coefficient of the resistivity of the inductor metal tracks. Also, with increasing temperature, the on-resistance of the transistors will increase. This will deteriorate efficiency as well. For an accurate modeling, these temperature effects have been integrated in the high-level model that is used in the optimization framework. Using this adaptation, the obtained results correspond to the real behavior of previously measured DC-DC converters, as discussed in [15].

IV. DISCUSSION OF RESULTS

An inductive DC-DC boost converter ($1.2\ V$ to $2.4\ V$) is designed in a $0.13\ \mu m$ CMOS technology using a tapered inductor. The properties of this design are summarized in Table I. These simulation results are compared for an inductor using the tapered topology; for an inductor with a regular topology, using only a thick top-metal layer and another regular inductor using eight metal layers. An inductor with 8 tapered metal

an increasing number of windings using a full stack of metal layers, leading to a more *full* inductor topology. From this trade-off curve, the most optimal design point for an inductor can be located. This is incorporated into the optimization loop.

Next to the intersections of the two inductor types in Figure 2, the unrolled versions of both inductors with *full* metal layers and with *tapered* metal layers are depicted as well. The latter thus has a decreasing number of windings with full metal stack, meaning that there are less metal layers closer to the substrate. An equivalent electrical lumped model is given in Figure 4. The subsets of this lumped model are shown in Figure 2 for the unrolled tapered inductor. Using (4), the total power loss in the substrate can now be calculated as in [3], with $U_{C,max}$ the average ΔU over all subsets and $C_{sub,i}$ the specific substrate capacitance of each subset. Using the factor $\frac{i}{n-1}$ the average voltage drop is translated into one that is applicable for a specific subset i of the n subsets.

$$P_{loss,substrate} = f_{sw} * U_S * \sum_{i=0}^{n-1} \left(i * \frac{U_{C,max} * C_{sub,i}}{n-1} \right) \quad (4)$$

For a boost converter topology, the voltage over the inductor will change frequently. The voltage at node U_a, as seen in Figure 2, will change with a full rail-to-rail swing (large ΔU), whereas the side of the inductor at node U_{in} is at DC-voltage ($\Delta U = 0$). The substrate capacitance at U_{in} will thus cause no significant power losses according to (3). At the U_a side, the number of metal layers is reduced yielding lower substrate capacitance of this subset and thus lower power losses.
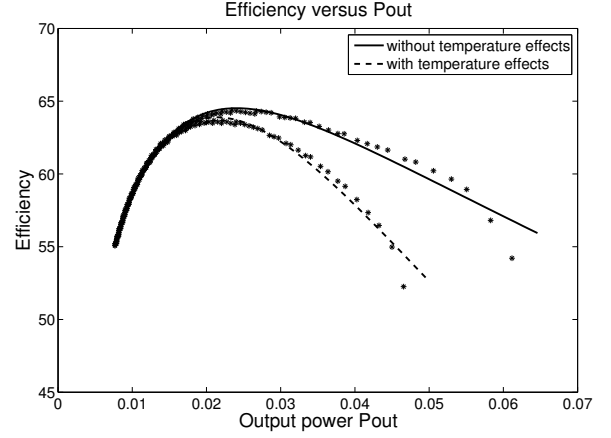
TABLE I

COMPARISON OF SIMULATION RESULTS FOR AN INDUCTIVE DC-DC CONVERTER DESIGN USING A REGULAR, FULL AND TAPERED INDUCTOR.

	Regular inductor (1 layer)	Full inductor (8 layers)	Tapered inductor
P_{out} at max efficiency	25.4 mW	25.7 mW	25.6 mW
P_{in} at max efficiency	43.3 mW	44.9 mW	39.7 mW
Max efficiency (with temperature effect)	**58**.7 % (58 %)	**57**.3 % (56.7 %)	**64**.5 % (64 %)
$P_{out,max}$ (with temperature effect)	47 mW @$\eta = 52$ % (35.3 mW @ 49 %)	59 mW @$\eta = 54$ % (44.2 mW @ 52 %)	63 mW @$\eta = 54$ % (46.6 mW @ 52 %)
Inductor inductance	49.74 nH (1 layer)	49.62 nH (full)	49.57 nH (tapered)
Inductor area	2.29 mm^2	2.29 mm^2	2.29 mm^2
Inductor series resistance	5.05 Ω	1.44 Ω	3.46 Ω
Switching frequency	76.8 MHz	76.8 MHz	76.8 MHz
C_{out}	0.89 nF	0.89 nF	0.89 nF
$P_{loss,inductor}$ (% of $P_{loss,total}$)	9.2 mW (**51** %)	11.4 mW (**59.4** %)	6.3 mW (**44** %)
$P_{loss,total}$	18 mW (100 %)	19.2 mW (100 %)	14 mW (100 %)

layers and resulting inductance of 49.57 nH is created with an area of 2.29 mm^2. As can be seen in Table I, only a small difference with the inductance of the regular inductors exists. The efficiency of the converter using a tapered inductor however is increased with 7 % giving a total efficiency of 64.5 % instead of 57.3 % for a converter with a *full* inductor. The temperature effects are considered as well. These have an influence on the maximum output power and should thus be taken into account. The total power loss is reduced with as much as 27 %, going from 19.2 mW to 14 mW. This implicitly presents the lower substrate capacitance in the tapered inductor. Also, the maximum output power has increased with 34 % from 47 mW to 63 mW (or 35.3 mW to 46.6 mW with temperature effects), compared to the regular inductor with one metal layer. The contribution of the inductor to the total power loss has dropped from 59 % to 44 %.

V. CONCLUSION

This paper proposes a technique for the optimization of fully-integrated inductive DC-DC converters. An optimization framework is used, focusing on the on-chip inductor as well as on the accurate layout-based modeling of temperature effects. A tapered inductor topology is introduced. This is applied in a design for a fully-integrated DC-DC boost converter in a 0.13 μm CMOS technology. The power loss in the circuit is reduced with 27 % which results in a 7 % efficiency improvement, compared to a fully-integrated DC-DC boost converter with a regular inductor topology.

REFERENCES

[1] T. McConaghy, "Variation-aware structural synthesis and knowledge extraction of analog circuits," Ph.D. dissertation, Katholieke Universiteit Leuven, Leuven, Belgium, 2008.

[2] M. Steyaert, T. Van Breussegem, H. Meyvaert, P. Callemeyn, and M. Wens, "Dc-dc converters: From discrete towards fully integrated cmos," in *ESSCIRC, 2011 Proceedings of the*, sept. 2011, pp. 42 –49.

[3] M. Wens and M. Steyaert, "A mathematical steady-state design model for fully-integrated boost and buck dcdc converters," *Analog Integrated Circuits and Signal Processing*, vol. 70, pp. 369–375, 19 april 2012.

[4] K. Deb, "A fast and elitist multiobjective genetic algorithm: Nsga-ii," *Transactions on Evolutionary Computation*, vol. 6 no. 2, april 2002.

[5] E. Zitzler and L. Thiele, *An evolutionary algorithm for multi-objective 0ptimization:The strength Pareto approach*. Zurich Computer Engineering and Networks Laboratory, Switzerland, May 1998, technical Report No. 43.

[6] G. S. Hornby, "Alps: The age-layered population structure for reducing the problem of premature convergence," *Proceedings of the Genetic and Evolutionary Computation Conference*, vol. 1, pp. 815–822, 2006.

[7] M. Kamon, M. Tsuk, and J. White, "Fasthenry: A multipole-accelerated 3-d inductance extraction program," in *Design Automation, 1993. 30th Conference on*, june 1993, pp. 678 – 683.

[8] D. Montgomery, *Design and analysis of experiments*. John Wiley & Sons Inc, 2008.

[9] E. Maricau, D. De Jonghe, and G. Gielen, "Hierarchical analog circuit reliability analysis using multivariate nonlinear regression and active learning sample selection," in *DATE, Proceedings of*, Dresden, 2012.

[10] D. Gardner, G. Schrom, F. Paillet, B. Jamieson, T. Karnik, and S. Borkar, "Review of on-chip inductor structures with magnetic films," *IEEE Transactions on Magnetics*, vol. 45 no. 10, pp. 4760–4766, Oct. 2009.

[11] J. Lu *et al.*, "Modeling, design, and characterization of multiturn bondwire inductors," *IEEE Transactions on Power Electronics*, vol. 25 no. 8, pp. 2010–2017, Aug. 2010.

[12] M. Prieto *et al.*, "Turn-coupling in thick-film integrated magnetic components for power converters," *IEEE Transactions on Components and Packaging Technologies*, vol. 31 no. 4, pp. 837–848, Dec. 2008.

[13] J. W u and M. Zaghloul, "Robust cmos micromachined inductors with structure supports for gilbert mixer matching circuits," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 56 no. 6, pp. 429–433, June 2009.

[14] K.-M. Kim, J.-H. Kim, and Y.-S. Kwon, "Micromachined bridge-shaped spiral inductor on anodised aluminium substrate," *Electronics Letters*, vol. 45 no. 6, pp. 311–313, March 12 2009.

[15] M. Wens, "An 800mw fully-integrated 130nm cmos dc-dc step-down multi-phase converter with on-chip spiral inductors and capacitors," *Energy Conversion Congress and Exposition*, pp. 3706–3709, 2009.