Technology and metrology of new electronic materials and devices

Scaling of the metal oxide semiconductor (MOS) field-effect transistor has been the basis of the semiconductor industry for nearly 30 years. Traditional materials have been pushed to their limits, which means that entirely new materials (such as high-κ gate dielectrics and metal gate electrodes), and new device structures are required. These materials and structures will probably allow MOS devices to remain competitive for at least another ten years. Beyond this timeframe, entirely new device structures (such as nanowire or molecular devices) and computational paradigms will almost certainly be needed to improve performance. The development of new nanoscale electronic devices and materials places increasingly stringent requirements on metrology.

ERIC M. VOGEL

The University of Texas at Dallas, Department of Electrical Engineering, 2601 North Floyd Road, Richardson, Texas 75083, USA; previously at the National Institute of Standards and Technology, Semiconductor Electronics Division, 100 Bureau Drive, MS 8120, Gaithersburg, Maryland 2089, USA.

e-mail: eric.vogel@utdallas.edu

For over 30 years, the planar silicon metal oxide semiconductor (MOS) field-effect transistor (FET) has been the basis of integrated circuits[1,2]. In 1970, integrated circuits contained thousands of MOSFETs, each having dimensions of tens of micrometres. Today's chips contain almost one billion MOSFETs, each having physical dimensions of tens of nanometres. The exponential increase of device density (Moore's Law[3]) and scaling of device dimension into the nanotechnology regime (see Fig. 1) have resulted in the vast improvements observed in numerous electronic devices, from PCs and mobile phones to control systems found in automobiles and jet airplanes. Although considerable innovation and investment was required to realize this rate of dimensional scaling, until recently very little has changed in the materials and design of the basic MOSFET. In the future, a variety of new materials and device structures will be required to continue MOSFET scaling[1,2,4–10]. Furthermore, as silicon MOSFET technology approaches its limits[11], entirely new device structures and computational paradigms will be required to replace and augment traditional MOSFETs. These possible emerging technologies span the realm from transistors made of silicon nanowires to devices made of nanoscale molecules.

Whether one is considering future nanoscale planar silicon MOSFETs or an emerging technology to replace the MOSFET, the electronic properties of all of these nanodevices are extremely susceptible to small perturbations in properties such as dimension, structure, roughness and defects, which means there is a significant need for precise metrology. Furthermore, the insertion of a variety of new materials into the conventional MOSFET and radically new materials and devices for potential emerging replacement technologies (for example, molecular and spin) present further challenges for metrology. Although the devices and materials being considered for future MOS technologies and beyond are broad, the overarching challenges to metrology remain. The ability to measure the physical, chemical and electronic properties that control final device electrical characteristics will be crucial to the research and development of future electronic devices.

TECHNOLOGY

TRADITIONAL MOS

As illustrated in Fig. 2a, the traditional MOSFET consists of a silicon substrate, a highly doped polysilicon gate electrode, a gate dielectric of SiO_2, and doped source and drain. In 1970, the MOSFET channel length was approximately 10 μm, the SiO_2 gate dielectric thickness was approximately 100 nm, and the operating voltage was approximately 10 V (refs 2,12). For over 30 years, the device density and speed of integrated circuits has been increased by reducing the MOSFET lateral dimension as shown in Fig. 1. To maintain, or improve, device performance when reducing channel length, most other device parameters need to be scaled: the substrate doping must be increased, the depth of the source/drain junction must be decreased, the supply voltage must be decreased and the capacitance of the SiO_2 gate dielectric must be increased (that is, SiO_2 thickness must be decreased).

Although there have been some changes of materials in the past 30 years (for example, moving from aluminium to highly doped polysilicon gate electrodes in the 1970s, the addition of lightly doped drain extensions in the 1980s, the addition of nitrogen to the SiO_2 gate dielectric to form silicon oxynitride in the late 1990s), the basic structure and materials of the traditional MOSFET have seen very little change. Today's MOSFET has an effective channel length of approximately 30 nm, a silicon oxynitride gate dielectric thickness of approximately 1.2 nm and a supply voltage of approximately 1.1 V. Although it may be possible to manufacture traditional MOS devices with a thinner layer of silicon oxynitride, tunnelling leakage current larger than that associated with the 1.2 nm gate dielectric ($\gtrsim$10 A cm^{-2}) results in unacceptably high power dissipation ($\gtrsim$10 W)

©2007 Nature Publishing Group

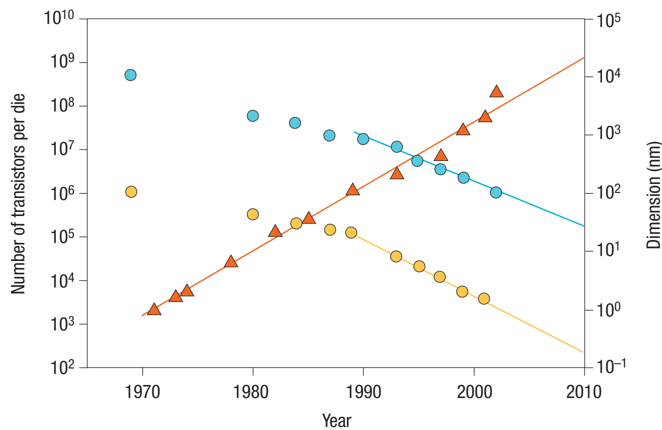

Figure 1 Moore's Law and scaling of transistor dimensions. The number of transistors (red triangles), transistor minimum lateral feature size (blue circles), and transistor minimum physical oxide thickness (yellow circles) as a function of time (data extracted from the Intel web site). The exponential increase in the number of transistors on an integrated circuit (Moore's Law[3]) requires the lateral dimensions of the transistor to scale downward. In order to improve the performance (speed) of the transistor, the physical oxide thickness must scale at approximately the same rate. Exponential fits to the data are shown as lines in the figure.

for the integrated circuit. Furthermore, because of high electric fields, the highly doped polysilicon no longer behaves as a metal and exhibits significant depletion, further limiting MOSFET performance. Owing to the fundamental limits associated with traditional MOSFET materials, new materials ('materials-limited MOS') and/or structures ('non-classical MOS') will be required to realize future improvements in MOSFET performance.

MATERIALS-LIMITED MOS

Insulators with high dielectric constant (for example, HfO_2) are being developed to replace silicon oxynitrde[9]. High-κ dielectrics allow a high capacitance with a thicker film so as to reduce the direct tunnelling leakage current. However, these dielectrics have a large number of technological problems, perhaps the worst of which is a generally poor interface with silicon. A wide variety of metals (for example, Ru, Ta, Pt, W, N and Si binaries and ternaries) are being considered as possible replacements to highly doped polysilicon[13,14]. The work function of the metal (minimum energy needed to remove an electron from the metal to vacuum) is critical in defining the threshold or turn-on voltage of the FET. Metal gate electrodes that have a work function similar to highly doped n-type silicon and highly doped p-type silicon must be found. The metal must have low resistance to current flow to ensure the speed of the device and be thermodynamically stable during subsequent processes, which can reach temperatures of ~1000 °C. Finally, the metal must not degrade the electrical properties of the underlying high-κ dielectric.

New materials for the substrate are also being developed and produced to directly improve the speed of the MOSFET without necessarily decreasing device dimensions. The most widely studied substrate material to date is strained silicon, formed either by growing silicon on top of relaxed $Si_{1-x}Ge_x$ or by introducing strain through the side using $Si_{1-x}Ge_x$ source/drains[2]. The smaller lattice constant of silicon as compared to $Si_{1-x}Ge_x$ results in strain and pronounced mobility enhancement for both holes and electrons. Because of their high mobility, III–V materials (for example, InGaAs, InSb) on a silicon platform are also being considered as future substrate materials[7].

NON-CLASSICAL MOS

To extend beyond the performance improvements found with dimensional scaling and new materials for planar MOSFETs, non-classical MOSFET structures are also being considered. The simplest is that of silicon-on-insulator (SOI), as shown in Fig. 2b, where the active silicon is on a layer of thick silicon dioxide, which decreases the parasitic junction capacitance from the source/drain to the substrate[5,10], thereby increasing the speed of the FET. In partially depleted (PD) SOI, the silicon depletion layer is less than the thickness of the silicon, whereas in fully depleted (FD) SOI, the silicon depletion layer is greater than the thickness of the silicon. FDSOI exhibits nearly ideal drain current–gate voltage characteristics (ideal sub-threshold slope) because the back substrate has little control over the channel.

A more radical non-classical device structure is the tri-gate or finFET as illustrated in Fig. 2c (refs 2,5,15–17). These devices exhibit good short-channel behaviour because the wrap-around gate can strongly control the channel but they pose a host of technological problems. For example, a high-quality gate oxide must be formed on an etched sidewall, the wire of silicon must typically be undoped to maintain a correct and controlled threshold voltage, and the fin height and width must be scaled appropriately[17].

BEYOND MOS

It is likely that MOSFET dimensional scaling with changes in both materials and device structure will enable necessary improvements in device performance well into the next decade. However, at some point, new 'beyond-MOS' devices will be needed to improve performance[11]. The devices being considered for beyond MOS can be roughly organized into four classifications: confined-dimension, molecular, strongly correlated and spin[1,18,19].

Confined-dimension devices include memories based on nanocrystals[20], thin semiconductors for resonant tunnelling diodes[21], quantum dots for cellular automata[22,23], carbon nanotube[24] or bottom-up nanowire transistors[25,26], and single-electron transistors[27]. The basis of molecular electronic devices is the behaviour of the electronic properties of single molecules or monolayers[28]. The potential for molecular electronics originates from its nanoscale dimension, the possibility of synthesizing very specific electronic properties, and the promise of fabrication through self-assembly. Although numerous molecular devices have been demonstrated, there is still significant controversy concerning the repeatability of measurements and the understanding of charge transport[29–31]. Forming ohmic but non-interacting metallic contacts to molecules is a specific problem.

Devices based on strongly correlated materials include ferroelectric memories[32] and ferromagnetic logic devices. Ferroelectric materials such as $(Ba,Sr)TiO_3$ exhibit memory function through spontaneous changes in dipole moment with the application of an electric field. Ferromagnetic devices formed of materials such as Fe, Ni, and Co have computational states based on local ferromagnetic orientation. The foundation of spin-based devices such as the spin MOSFET[33,34], spin-torque transistor[35], and spin-gain transistor[36] is the use of electron spin as the computational state. These devices are of interest because of their inherent low power dissipation as compared with charge-based devices. However, such devices are still in their infancy.

Silicon-based MOSFETs are approaching device densities of 10^9 devices per chip (with ten year reliability), lateral dimensions of 10 nm, and gate delays of 1 ps. Finding a technology with substantially better capabilities to simply replace the MOSFET in conventional architectures is highly unlikely[37]. Instead, these beyond-MOS technologies are more likely to be used as a modification to the MOS platform or in wholly different architectures (for example,

©2007 Nature Publishing Group

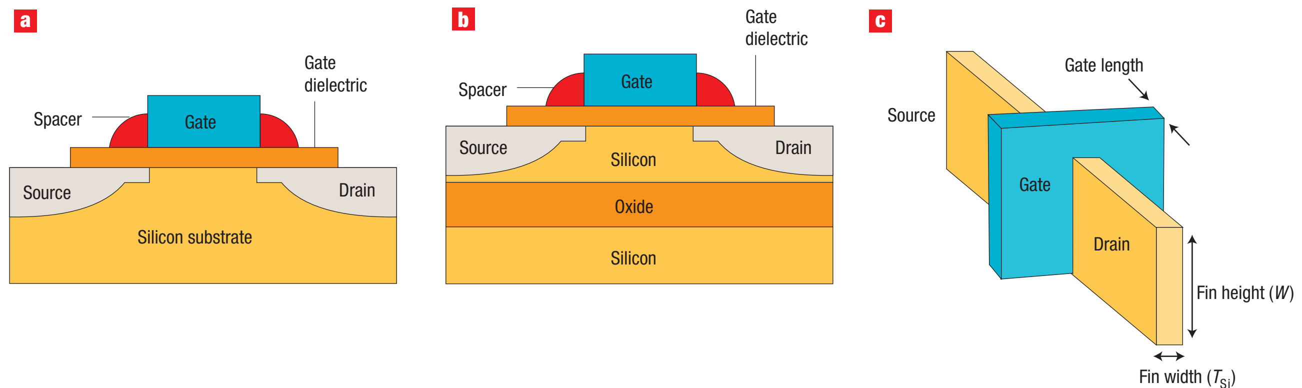

Figure 2 Illustrations of silicon transistors. **a**, A traditional n-channel MOSFET uses a highly doped n-type polysilicon gate electrode, a highly doped n-type source/drain, a p-type substrate, and a silicon dioxide or oxynitride gate dielectric. **b**, A silicon-on-insulator (SOI) MOSFET is similar to the traditional MOSFET except the active silicon is on a thick layer of silicon dioxide. This electrical isolation of the silicon reduces parasitic junction capacitance and improves device performance. **c**, A finFET is a three-dimensional version of a MOSFET. The gate electrode wraps around a confined silicon channel providing improved electrostatic control of the channel electrons.

quantum[38,39], defect tolerant[40] and biologically inspired[41]) aimed at applications that complement MOS. For example, one potential implementation of a quantum computer involves the use of dopants in silicon and single-electron transistors[38]. Quantum computers are exponentially more efficient than binary computers at applications such as searching a non-sorted database and number factorization. However, the probabilistic nature of quantum computing limits its applicability to more general computing.

METROLOGY REQUIREMENTS

Given the wide breadth of materials and devices being considered for future MOS and beyond, it is impossible to cover every measurement challenge adequately and it is not the purpose of this review to discuss all possible measurement tools and methods. However, there are important overarching measurement challenges that pervade most of these seemingly disparate technologies. The following describes these themes by illustrating the sensitivity of device behaviour to properties such as dimension, structure, and composition, and gives examples of solutions to these measurement challenges.

NANOMETRE DIMENSION

Perhaps the most fundamental measurement challenge for future MOSFETs and emerging devices is that of dimension, both horizontal (that is, critical dimension or linewidth) and vertical (film thickness). By 2010, the most recent edition of the International Technology Roadmap for Semiconductors (ITRS)[1] predicts that state-of-the-art MOSFETs in manufacturing will have physical gate lengths of approximately 20 nm controlled to within approximately 2 nm. In order to precisely measure a difference of 2 nm, the precision (3σ) of the critical dimension measurement must be much smaller — 0.37 nm (in the order of one atom) — by 2010. By 2020, the required precision drops to 0.12 nm. This is even more critical for devices such as finFETs or nanowire FETs that have extremely narrow channels. Figure 3 shows the drain current versus gate voltage characteristics for a finFET with different silicon fin widths. The off-state current (V_g = 0 V) varies by almost two orders of magnitude for a 2 nm change in the fin width (approximately one order of magnitude for every two atomic layers). This extreme sensitivity of electrical properties to nanoscale dimension illustrates the importance of dimensional metrology. Scanning electron microscopy (SEM), transmission electron microscopy (TEM) and atomic force microscopy are being developed to meet these needs[42–44]. As the dimensions of future devices approach the atomic scale, sample preparation, which can alter the dimension to be measured, becomes increasingly important.

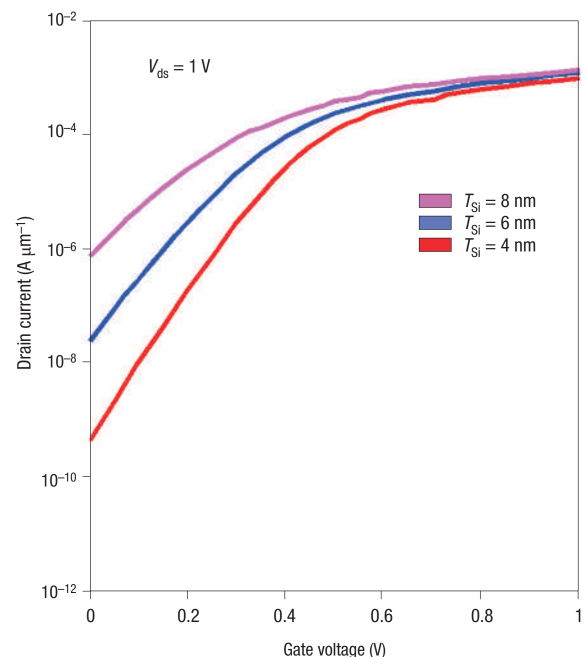

Figure 3 Simulation of a finFET. Drain current versus gate voltage characteristics of a finFET (illustrated in Fig. 2) for different values of fin width (T_{Si}) as defined in Fig. 2. The increase of the characteristic slope at low gate voltages with decreasing T_{Si} is due to increased electrostatic control of the gate over carriers in the channel. The strong sensitivity of the current at 0 V on T_{Si} (almost one order of magnitude in current for every 2 nm change in T_{Si}) illustrates the need for highly precise dimensional measurements with precision much less than 1 nm. Courtesy of T.-J. King, Univ. California, Berkeley.

©2007 Nature Publishing Group

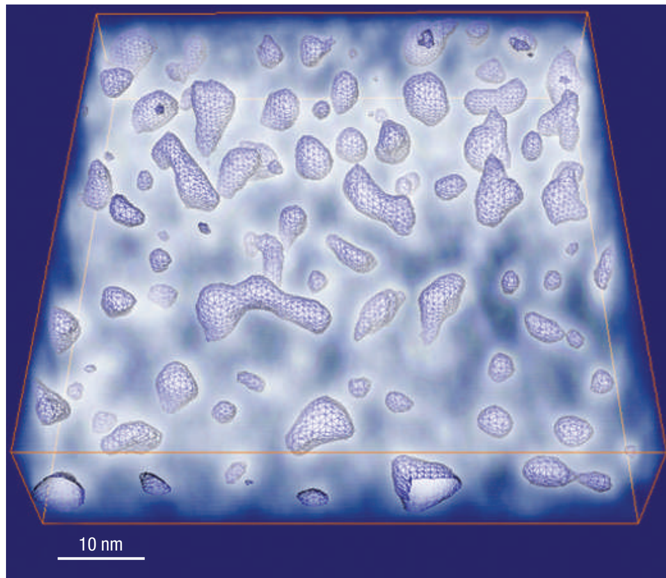

Figure 4 The structure of silicon quantum dots. Tomographic reconstruction of the silicon plasmon signal at 17 eV, visualized by volume rendering (white 'fog') and an iso-surface at fixed threshold (blue shapes) for silicon quantum dots embedded in SiO_2. In modelling and predicting the behaviour of devices based on silicon quantum dots, it is largely assumed that the quantum dots are perfectly spherical. These results indicate that the silicon dots are not perfectly spherical, illustrating the need for three-dimensional structural measurements at the nanoscale. Courtesy of A. Yurtserver and D. Muller, Cornell Univ.

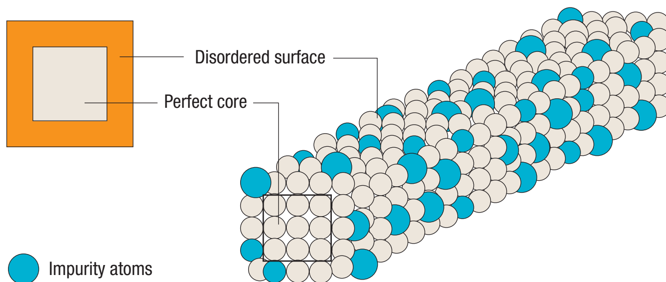

Figure 5 The importance of compositional metrology. Schematic illustration of a nanowire with surface disorder induced by shell doping. The mobility of electrons in silicon nanowires is a critical parameter that strongly impacts its measured electrical behaviour. Numerical results by Zhong[61] have suggested that doping of an outer shell of a silicon nanowire while keeping the core of the nanowire unperturbed may result in an increase in the electron mobility (in contrast to bulk silicon). There are currently no techniques capable of mapping the composition of nanowires at the spatial resolutions necessary to experimentally verify this result. Reprinted with permission from ref. 61. Copyright 2006 American Chemical Society.

The vertical dimension (thickness) of materials being considered for future devices is also critical[1, 45–47]. The thickness of silicon dioxide in today's MOSFET is approximately 1.2 nm controlled to within 0.04 nm[1,47]. This means that the precision (3σ) of the critical dimension measurement must be 0.0048 nm. Similar requirements are found for a wide variety of future devices and materials. FDSOI FETs will have silicon thicknesses approaching 15 nm and will require 0.0075 nm measurement precision by 2010. Resonant tunnelling diodes will have extremely thin quantum wells and self-assembled monolayers for molecular electronics have thicknesses in the order of nanometres.

Indirect techniques such as spectroscopic ellipsometry, X-ray reflectivity, and capacitance-based measurements are being used and developed to measure thickness in this regime[1,45–48]. These indirect techniques typically require some *a priori* knowledge of the fundamental properties and constants of the materials being measured. The breadth of materials being considered for future devices and the fact that their properties may change in the nanoscale complicates these indirect measurements. Furthermore, techniques available today to measure thickness to within 0.04 nm typically require large spot sizes or sample areas to achieve enough signal. For example, spectroscopic ellipsometers have a measurement diameter from micrometres to millimetres and capacitance–voltage measurements are typically made on test structures measuring tens of micrometres. Therefore, these techniques provide a measure of film thickness averaged over the probed sample. As device dimensions continue to scale into the nanometre regime, the assumption that thickness determined from large probes is relevant to the electrical device of interest (for example, a MOSFET with 30 nm channel length) is likely to become less valid. For example, the strain associated with a nanoscale MOSFET may have a strong impact on the growth and thickness of a dielectric. The value of thickness obtained from a large-area capacitor or optical measurement may not be relevant to the technology or device of interest. As the dimensions of future devices approach the atomic scale, technologically relevant measures of dimension become increasingly important.

THREE-DIMENSIONAL STRUCTURE

It is not only the lateral and vertical dimension of a nanodevice that is important or even necessarily relevant. The complete structure in multiple dimensions is critical for many devices and materials. For planar MOSFETs, line edge roughness (LER), line width roughness (LWR) and surface roughness is critical. By 2010, the ITRS predicts that LWR must be less than 1.4 nm and that the precision (3σ) of the LWR measurement must be 0.28 nm, in the order of one atom[1].

Furthermore, many of the devices being considered do not possess simple planar geometries. The exact shape, rather than simple dimension, of a nanowire has been shown to strongly influence its final electrical properties[49,50]. The thickness of a dielectric or film surrounding a nanowire is likely to be non-uniform. It is largely assumed that silicon quantum dots embedded in SiO_2 (for use in optical and memory applications) are spherical. However, as shown in Fig. 4, recent plasmon tomography measurements indicate that silicon particles have complex morphologies and high surface to volume ratios rather than the commonly assumed near-spherical structures. These complex morphologies would affect quantum-confined excitons and interface density of states, directly impacting final device properties[51,52]. A model that attempts to predict the electrical properties of devices based on spherical silicon quantum dots may be incorrect. Techniques such as TEM holography and tomography, aberration correction SEM, and STM have shown promise for measuring structure at the dimensions of interest[53–59].

ATOMIC COMPOSITION

The electrical properties of many devices are sensitive to small changes in composition or even the placement of small numbers of atoms. By 2010, the distribution of dopant atoms within the conventional MOSFET must be characterized with 3 nm spatial

©2007 Nature Publishing Group

resolution and 4% accuracy[1]. Characterizing the dopant distribution of nanowire devices is even more critical[60]. For example, it has been theoretically shown that shell-doping of nanowires, as illustrated in Fig. 5, results in enhanced electron mobility[61]. Rigorously confirming this prediction would require measurement of dopant profiles on the atomic scale.

Beyond dopants, another issue with bottom-up nanowires is that small amounts of metal catalyst used to grow the nanowires can migrate into the nanowire and affect the electrical properties[62]. It has also been shown that small numbers of bonded water molecules can change the conduction properties of carbon nanotubes from p-type to n-type[63,64] and the conductivity of single molecules has been shown to be strongly affected by single charged surface atoms[65]. One approach to quantum information processing proposes using single phosphorous atoms to make a quantum computer[38]. All of these technologies and issues point to the need for significant improvements in compositional metrology.

New characterization technology and understanding is needed for the problems described above, namely, characterizing compositions approaching single atoms with spatial resolution approaching angstroms. Common dopant profiling techniques such as secondary ion mass spectroscopy (SIMS) are not possible on these three-dimensional structures. Techniques for two-dimensional dopant profiling, such as scanning capacitance microscopy, are not easily performed on nanowires because the effective tip size is larger than the nanowire, but development is ongoing[66,67]. Techniques such as annular dark-field scanning transmission electron microscopy (ADF-STEM) have shown some success in detecting individual atoms[67–70]. ADF-STEM is a Z-contrast technique — the intensity scattered by an atom is approximately proportional to its atomic number (Z) squared. Achieving atomic resolution requires extremely sensitive cross-sectional sample preparation (~5-nm-thick samples with thickness variation less than the contrast associated with one atom). Further development of compositional metrology will be required for future electronic devices.

ELECTRONIC STRUCTURE AND PROPERTIES

Electronic density of states, dielectric function, bandgap, work function and density of electrically active defects are perhaps the properties most directly related to electrical-device behaviour. For example, future MOSFETs will likely have a complex stack of materials in which the density of states, work function and defect density will be critical. The metal gate electrode may consist of a thick top contact metal gate electrode and a thin layer of metal used to control effective work function[14]. It has been shown that, in the nanoscale regime, the thickness of this thin metal layer is a key parameter defining effective work function as measured from device characteristics[14]. The gate dielectric will consist of a high-permittivity material (such as HfO_2) on a very thin layer of SiO_2 to reduce the interfacial defect density near the substrate. The band offsets between these dielectrics, the substrate material and the gate electrode determine not only the tunnel current through the gate stack, but also the threshold voltage of the device[71,72]. Electrically active defects at the interfaces of these materials degrade device reliability as well as the effective mobility of carriers in the substrate[73–75].

Similar issues are present in beyond-MOS devices. An understanding of the local density of states of the molecules comprising the self-assembled monolayer is critical to understanding transport through the molecules[76]. The energy offsets and electrically active defects between the molecules and its electrodes are perhaps even more critical[30,76]. The bandgap and electronic structure (semiconducting versus metallic) of carbon nanotubes are critical to their electrical behaviour[77–80]. A low electrically active defect density is critical to achieving high negative differential resistance in resonant tunnelling diodes[81] and to charge offset stability in single electron devices[82]. Scattering is an important problem limiting spintronic devices[83].

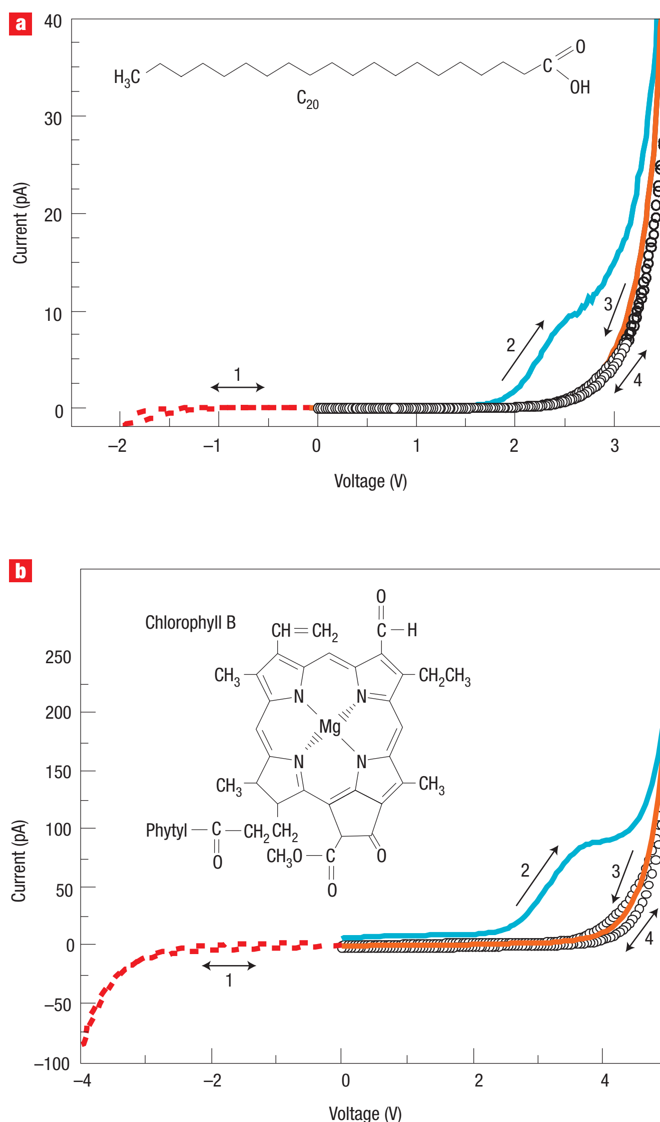

Figure 6 Does the molecule matter? Shown are typical experimental hysteretic current–voltage curves of Al/AlO$_x$/molecule/Ti/Al planar crossbar devices incorporating Langmuir–Blodgett organic monolayers of **a**, eicosanoic acid (C_{20}) and **b**, chlorophyll-B. The fact that the above hysterisis affect is observed for two very different molecular species suggests the importance of the interface of the metal electrodes with the molecule. The results illustrate the importance of performing compositional and structural measurements on the final device of interest since the entire device (molecule and electrodes) is critical to its final electrical properties. Reprinted with permission from ref. 30. Copyright (2005) Springer Science and Business Media.

Techniques such as photoelectron spectroscopy and inverse photoelectron spectroscopy have been used to map the valence and electron density of states in thin dielectric films[72,84]. One- and two-photon photoelectron spectroscopy has also been used to determine the electronic structure of self-assembled monolayers around the Fermi level[76]. These techniques are primarily applicable to planar thin films and monolayers and cannot typically be used to map the spatial dependence of properties. Scanned probe techniques such as scanning Kelvin probe microscopy[66] and versions of scanning tunnelling microscopy can provide information on local electronic structure[85].

©2007 Nature Publishing Group

However, the size of the probe tip is a limiting factor. Techniques such as fluorescence, Raman spectroscopy and Rayleigh scattering have been used to measure the bandgap of carbon nanotubes[79,80,86,87]. The ability to measure the electronic density of states, band offsets, and electrically active defect density as a function of energy and space provides valuable information for engineering the final electrical properties of MOS and beyond devices.

PROPERTIES OF DEVICE STRUCTURES

Measurement of electronic materials prior to their placement in a device structure is an important part of developing a new electronic device. However, the nanoscale dimension and the processing necessary to fabricate the device is critical to its final physical and electrical properties. For example, straining silicon by depositing it on $Si_{1-x}Ge_x$ is being used for enhancing carrier mobility. However, the final strain found in the device is determined not only by the lattice mismatch between the epitaxial silicon and $Si_{1-x}Ge_x$, but also by many other materials and processing steps associated with the final device such as sidewalls, capping layers and thermal processes[2,88]. Measuring properties such as composition, strain and structure within the final nanoscale device structure is crucial.

The final device structure can also dramatically change the intended electronic properties of the material of interest. For example, the interaction between the electrodes and molecules in molecular electronics is critical to the transport properties of the final device. The current–voltage characteristics of cross-bar device structures containing eicosanoic acid and chlorophyll B, respectively, are shown in Figs 6a and 6b (ref. 30). Eicosanoic acid is a simple molecule and is expected to act as a passive film with simple tunnelling current–voltage behaviour. The hysterisis observed for this simple molecule and its qualitatively similar characteristics to chlorophyll B (a very different molecular species) suggests that the final electrical properties are determined not only by the molecules, but also by the interaction of the molecule with its electrodes. Techniques such as inelastic tunnelling spectroscopy, which probe vibrational modes of the molecules through measurement of the device current–voltage behaviour, have been developed to determine which molecular species and bonds are present in the final device structure[31]. Techniques such as backside-incidence Fourier-transform infrared spectroscopy have been used to investigate the interaction of top-metallization with molecular monolayers[30]. The above molecular electronics example illustrates the importance of performing characterization of the full integrated device structure.

Electrical test structures can be used to characterize the physical properties of nanoscale materials. For example, electrically active defects in the gate dielectric of the MOSFET are at densities ($\sim 10^{10}$ cm^{-2}) that typically cannot be measured using physical characterization techniques. Methods such as charge pumping have been developed which permit sensitive extraction of both the energy and depth dependence of these defects[75]. This technique determines the electrically active defect density by measuring the amount of current associated with the capture of free carriers induced by applying periodic pulses to the gate of a FET. By comparing the depth and energy dependence of the extracted electrically active defect density from transistor measurements with physical measurements of composition and structure, important insights on the physical origin of the defects can be elucidated. This approach of integrated technology and measurement will be increasingly critical to future technological development (Box 1).

As another example, the ability of an injected spin-polarized current to retain its spin polarization (spin injection efficiency) is an important parameter in spin-based devices such as lateral spin valves. The spin injection efficiency of a spin valve can be deduced through measurement of the voltage induced by spin accumulation using separate detectors fabricated with the spin valve[89]. It has been shown that the exact configuration of the detector affects whether the measured value is due only to the signal of interest from the channel of the spin valve or includes other spurious affects[89]. The extreme sensitivity of the electrical properties of nanoscale devices on their physical properties can be exploited to precisely characterize many properties of nanoscale materials. However, care must be taken to ensure that the test structure and analysis of these indirect electrical measurements provide meaningful properties and do not

Box 1 Integrating metrology with technology development

The metrology requirements described in this review suggest that a single characterization tool is needed that can measure the location (to within 0.001 nm) and type of every atom within a three-dimensional device structure of interest (even if the structure is buried below 100 nm of material) and provide information on other parameters of interest such as electronic density of states and strain as a function of position. It is apparent that there will not be a characterization tool available to meet all of these challenges in time to have an impact on the development of new electronic materials and devices required by the semiconductor industry. Nevertheless, development continues at a rapid pace without the ability to physically measure every parameter of interest. For example, the semiconductor industry is developing uniaxial strain engineering through heteroexpitaxy or capping layers to enhance MOSFET performance[1,2,90]. As there are currently no metrology tools available that can measure strain magnitudes of interest within the nanoscale MOSFET, researchers are calibrating strain levels by applying known stress to a transistor while measuring drive current.

Furthermore, every characterization method has strengths and weaknesses. There is typically not one characterization method that provides all of the information necessary to describe a given property of a material. The complexity and dimensions of the materials and devices being considered often result in different measured values for nominally the same property of a given material. For example, the thickness of ultrathin silicon dioxide measured using transmission electron microscopy (TEM), spectroscopic ellipsometry (SE) and capacitance–voltage (C–V) can give results varying by as much as 20% (ref. 47). The thickness measured using TEM depends on sample preparation as well as the methodology used to define the interface. The thickness measured using SE and C–V depends dramatically on the model assumed in data interpretation[91].

Although developing a single metrology capability to provide increasingly accurate measurements is critical, it is also extremely important to develop a fundamental understanding of the interrelationship between measurements from many different physical characterization tools and measurements of the technology of interest. This approach may be the only way to obtain the information necessary to develop new electronic materials and devices.

©2007 Nature Publishing Group

include spurious effects that are not directly associated with the electronic material of interest.

OUTLOOK

The silicon transistor has been a technological and economic engine for over three decades. Metrology has been an important infrastructure enabling the exponential increase of device density and exponential decrease of device dimension. New nanoscale materials and devices will be required to sustain this technological revolution but the extreme sensitivity of the electronic properties of these devices to their nanoscale physical properties and the insertion of radically new materials present significant challenges to metrology. The ability to measure the physical, chemical and electronic properties of these new materials and devices will become even more critical in continuing the advance of the MOS and finding technologies to extend or replace it.

doi: 10.1038/nnano.2006.142

References

1. *International Technology Roadmap for Semiconductors* (Semiconductor Industry Association, 2005); www.itrs.net
2. Thompson, S. E. *et al.* In search of "forever," continued transistor scaling one new material at a time. *IEEE Trans. Semiconduct. M.* **18,** 26–36 (2005).
3. Moore, G. Cramming more components onto integrated circuits. *Electronics* **38,** 114–117 (1965).
4. Chang, L. L. *et al.* Extremely scaled silicon nano-CMOS devices. *Proc. IEEE* **91,** 1860–1873 (2003).
5. Chang, L. L. *et al.* Moore's law lives on: ultra-thin body SOI and FinFET CMOS transistors look to continue Moore's law for many years to come. *IEEE Circuits Device.* **19,** 35–42 (2003).
6. Chang, L. L., Ieong, M. & Yang, M. CMOS circuit performance enhancement by surface orientation optimization. *IEEE Trans. Electron. Dev.* **51,** 1621–1627 (2004).
7. Chau, R., Datta, S. & Majumdar, A. Opportunities and Challenges of III–V Nanoelectronics for Future High-Speed, Low-Power Logic Applications. *IEEE CSIC Symposium Technical Digest* 17–20 (2005).
8. Taur, Y. *et al.* CMOS scaling into the nanometer regime. *Proc. IEEE* **85,** 486–504 (1997).
9. Wilk, G. D., Wallace, R. M. & Anthony, J. M. High-kappa gate dielectrics: Current status and materials properties considerations. *J. Appl. Phys.* **89,** 5243–5275 (2001).
10. Wong, H. S. P., Frank, D. J., Solomon, P. M., Wann, C. H. J. & Welser, J. J. Nanoscale CMOS. *Proc. IEEE* **87,** 537–570 (1999).
11. Muller, D. A. A sound barrier for silicon? *Nature Mater.* **4,** 645–647 (2005).
12. Sah, C. T. Evolution Of The MOS-Transistor — from Conception To VLSI. *Proc. IEEE* **76,** 1280–1326 (1988).
13. Song, S. C. *et al.* Integration issues of high-k and metal gate into conventional CMOS technology. *Thin Solid Films* **504,** 170–173 (2006).
14. Jha, R., Lee, J., Majhi, P. & Misra, V. Investigation of work function tuning using multiple layer metal gate electrodes stacks for complementary metal-oxide-semiconductor applications. *Appl. Phys. Lett.* **87,** 223503 (2005).
15. Hisamoto, D. *et al.* FinFET — a self-aligned double-gate MOSFET scalable to 20 nm. *IEEE Trans. Electron. Dev.* **47,** 2320–2325 (2000).
16. Xiong, S. Y. & Bokor, J. Sensitivity of double-gate and finFET devices to process variations. *IEEE Trans. Electron. Dev.* **50,** 2255–2261 (2003).
17. Anil, K. G., Henson, K., Biesemans, S. & Collaert, N. Layout density analysis of finFETs. *Proc. 33rd ESSDERC* 139–142 (2003).
18. Hutchby, J. A., Bourianoff, G. L., Zhirnov, V. V. & Brewer, J. E. Emerging research memory and logic technologies. *IEEE Circuits Device.* **21,** 47–51 (2005).
19. Zhirnov, V. V., Hutchby, J. A., Bourianoff, G. I. & Brewer, J. E. Emerging research logic devices. *IEEE Circuits Device.* **21,** 37–46 (2005).
20. Hanafi, H. I., Tiwari, S. & Khan, I. Fast and long retention-time nano-crystal memory. *IEEE Trans. Electron. Dev.* **43,** 1553–1558 (1996).
21. Reed, M. A., Frensley, W. R., Matyi, R. J., Randall, J. N. & Seabaugh, A. C. Realization Of A 3-Terminal Resonant Tunneling Device: The Bipolar Quantum Resonant Tunneling Transistor. *Appl. Phys. Lett.* **54,** 1034–1036 (1989).
22. Lent, C. S. & Isaksen, B. Clocked molecular quantum-dot cellular automata. *IEEE Trans. Electron. Dev.* **50,** 1890–1896 (2003).
23. Lent, C. S., Isaksen, B. & Lieberman, M. Molecular quantum-dot cellular automata. *J. Am. Chem. Soc.* **125,** 1056–1063 (2003).
24. Chen, J., Klinke, C., Afzali, A. & Avouris, P. Self-aligned carbon nanotube transistors with charge transfer doping. *Appl. Phys. Lett.* **86,** 123108 (2005).
25. Chung, S. W., Yu, J. Y. & Heath, J. R. Silicon nanowire devices. *Appl. Phys. Lett.* **76,** 2068–2070 (2000).
26. Cui, Y., Zhong, Z. H., Wang, D. L., Wang, W. U. & Lieber, C. M. High performance silicon nanowire field effect transistors. *Nano Lett.* **3,** 149–152 (2003).
27. Chen, R. H., Korotkov, A. N. & Likharev, K. K. Single-electron transistor logic. *Appl. Phys. Lett.* **68,** 1954–1956 (1996).
28. Reed, M. A. Molecular-scale electronics. *Proc. IEEE* **87,** 652–658 (1999).
29. Reed, M. A. Molecular electronics: Back under control. *Nature Mater.* **3,** 286–287 (2004).
30. Richter, C. A., Stewart, D. R., Ohlberg, D. A. A. & Stanley Williams, R. Electrical characterization of Al/AlO_x/molecule/Ti/Al devices. *Appl. Phys. A* **80,** 1355–1362 (2005).
31. Wang, W. Y., Lee, T. H. & Reed, M. A. Electronic transport in molecular self-assembled monolayer devices. *Proc. IEEE* **93,** 1815–1824 (2005).
32. Arimoto, Y. & Ishiwara, H. Current status of ferroelectric random-access memory. *MRS Bull.* **29,** 823–828 (2004).
33. Datta, S. & Das, B. Electronic Analog Of The Electrooptic Modulator. *Appl. Phys. Lett.* **56,** 665–667 (1990).
34. Zutic, I., Fabian, J. & Das Sarma, S. Spintronics: Fundamentals and applications. *Rev. Mod. Phys.* **76,** 323–410 (2004).
35. Bauer, G. E. W., Brataas, A., Tserkovnyak, Y. & van Wees, B. J. Spin-torque transistor. *Appl. Phys. Lett.* **82,** 3928–3930 (2003).
36. Nikonov, D. E. & Bourianoff, G. I. Spin gain transistor in ferromagnetic semiconductors: The semiconductor Bloch-equations approach. *IEEE Trans. Nanotechnol.* **4,** 206–214 (2005).
37. Zhirnov, V. V., Cavin, R. K., Hutchby, J. A. & Bourianoff, G. I. Limits to binary logic switch scaling — a Gedanken model. *Proc. IEEE* **91,** 1934–1939 (2003).
38. Kane, B. E. A silicon-based nuclear spin quantum computer. *Nature* **393,** 133–137 (1998).
39. Shor, P. W. Polynomial-time algorithms for prime factorization and discrete logarithms on a quantum computer. *SIAM J. Comp.* **26,** 1484–1509 (1997).
40. Heath, J. R., Kuekes, P. J., Snider, G. S. & Williams, R. S. A defect-tolerant computer architecture: Opportunities for nanotechnology. *Science* **280,** 1716–1721 (1998).
41. Sarpeshkar, R. Analog versus digital: Extrapolating from electronics to neurobiology. *Neural Comput.* **10,** 1601–1638 (1998).
42. Diebold, A. C. Metrology technology for the 70-nm node: Process control through amplification and averaging microscopic changes. *IEEE Trans. Semiconduct. M.* **15,** 169–182 (2002).
43. Diebold, A. C. & Joy, D. A critical analysis of techniques and future CD metrology needs. *Solid State Technol.* **46,** 63 (2003).
44. Marchman, H. M. & Griffith, J. E. in *Handbook of Silicon Semiconductor Metrology* (ed. Diebold, A. C.) (Marcel Dekker, New York, 2001).
45. Diebold, A. C. *et al.* Characterization and production metrology of gate dielectric films. *Mat. Sci. Semicon. Proc.* **4,** 3–8 (2001).
46. Diebold, A. C. *et al.* Thin dielectric film thickness determination by advanced transmission electron microscopy. *Microscopy Microanal.* **9,** 493–508 (2003).
47. Ehrstein, J. *et al.* A comparison of thickness values for very thin SiO_2 films by using ellipsometric, capacitance-voltage, and HRTEM measurements. *J. Electrochem. Soc.* **153,** F12-F19 (2006).
48. Tompkins, H. H. & McGahan, W. A. *Spectroscopic Ellipsometry and Reflectometry* (Academic Press, New York, 1999).
49. Guo, J., Wang, J., Polizzi, E., Datta, S. & Lundstrom, M. Electrostatics of nanowire transistors. *IEEE Trans. Nanotechnol.* **2,** 329–334 (2003).
50. Vashaee, D. *et al.* Electrostatics of nanowire transistors with triangular cross sections. *J. Appl. Phys.* **99,** 054310 (2006).
51. Fonoberov, V. A., Pokatilov, E. P., Fomin, V. M. & Devreese, J. T. Photoluminescence of tetrahedral quantum-dot quantum wells. *Physica E* **26,** 63–66 (2005).
52. Tokura, Y., Sasaki, S., Austing, D. G. & Tarucha, S. Excitation spectra and exchange interactions in circular and elliptical quantum dots. *Physica B* **298,** 260–266 (2001).
53. Bals, S., Van Tendeloo, G. & Kisielowski, C. A new approach for electron tomography: Annular dark-field transmission electron microscopy. *Adv. Mater.* **18,** 892 (2006).
54. Cowley, J. M. Off-axis STEM or TEM holography combined with four-dimensional diffraction imaging. *Microscopy Microanal.* **10,** 9–15 (2004).
55. Cumings, J., Zettl, A., McCartney, M. R. & Spence, J. C. H. Electron holography of field-emitting carbon nanotubes. *Phys. Rev. Lett.* **88,** 056804 (2002).
56. Joy, D. C. The aberration corrected SEM. *AIP Conference Proceedings* **788,** 535–542 (2005).
57. Kim, M. J., Wallace, R. M. & Gnade, B. E. HRTEM for nano-electronic materials research. *Characterization and Metrology for ULSI Technology* **788,** 558–564 (2005).
58. Shekhawat, G. S. & Dravid, V. P. Nanoscale imaging of buried structures via scanning near-field ultrasound holography. *Science* **310,** 89–92 (2005).
59. Fallahi, P. *et al.* Imaging a single-electron quantum dot. *Nano Lett.* **5,** 223–226 (2005).
60. Garcia-Gutierrez, D. I. *et al.* Study of two-dimensional B doping profile in Si fin field-effect transistor structures by high angle annular dark field in scanning transmission electron microscopy mode. *J. Vac. Sci. Tech. B* **24,** 730–738 (2006).
61. Zhong, J. X. & Stocks, G. M. Localization/quasi-delocalization transitions and quasi-mobility-edges in shell-doped nanowires. *Nano Lett.* **6,** 128–132 (2006).
62. Hannon, J. B., Kodambaka, S., Ross, F. M. & Tromp, R. M. The influence of the surface migration of gold on the growth of silicon nanowires. *Nature* **440,** 69–71 (2006).
63. Cao, J., Wang, Q. & Dai, H. Electron transport in very clean, as-grown suspended carbon nanotubes. *Nature Mater.* **4,** 745–749 (2005).
64. Na, P. S. *et al.* Investigation of the humidity effect on the electrical properties of single-walled carbon nanotube transistors. *Appl. Phys. Lett.* 87 (2005).
65. Piva, P. G. *et al.* Field regulation of single-molecule conductivity by a charged surface atom. *Nature* **435,** 658–661 (2005).
66. Bonnell, D. A. & Shao, R. Local behavior of complex materials: scanning probes and nano structure. *Current Opin. Solid St. M.* **7,** 161–171 (2003).
67. Castell, M. R., Muller, D. A. & Voyles, P. M. Dopant mapping for the nanotechnology age. *Nature Mater.* **2,** 129–131 (2003).
68. Voyles, P. M., Grazul, J. L. & Muller, D. A. Imaging individual atoms inside crystals with ADF-STEM. *Ultramicroscopy* **96,** 251–273 (2003).
69. Voyles, P. M., Muller, D. A., Grazul, J. L., Citrin, P. H. & Gossmann, H. J. L. Atomic-scale imaging of individual dopant atoms and clusters in highly n-type bulk Si. *Nature* **416,** 826–829 (2002).
70. Voyles, P. M., Muller, D. A. & Kirkland, E. J. Depth-dependent imaging of individual dopant atoms in silicon. *Microscopy Microanal.* **10,** 291–300 (2004).
71. Sayan, S. *et al.* Band alignment issues related to HfO_2/SiO_2/p-Si gate stacks. *J. Appl. Phys.* **96,** 7485–7491 (2004).
72. Sayan, S. *et al.* Valence and conduction band offsets of a ZrO_2/SiO_xN_y/n-Si CMOS gate stack: A combined photoemission and inverse photoemission study. *Phys. Status Solidi B* **241,** 2246–2252 (2004).

©2007 Nature Publishing Group

73. Kerber, A. *et al.* Charge trapping in SiO_2/HfO_2 gate dielectrics: Comparison between charge-pumping and pulsed I-D.-V.-G. *Microelectron. Eng.* **72,** 267–272 (2004).
74. Han, J. P. *et al.* Asymmetric energy distribution of interface traps in n- and p-MOSFETs with HfO_2 gate dielectric on ultrathin SiON buffer layer. *IEEE Electron. Dev. Lett.* **25,** 126–128 (2004).
75. Heh, D. *et al.* Spatial distributions of trapping centers in HfO_2/SiO_2 gate stacks. *Appl. Phys. Lett.* **88,** 152907 (2006).
76. Zangmeister, C. D., Robey, S. W., van Zee, R. D., Yao, Y. & Tour, J. M. Fermi level alignment and electronic levels in "molecular wire" self-assembled monolayers on Au. *J. Phys. Chem. B* **108,** 16187–16193 (2004).
77. Kim, P., Odom, T. W., Jin-Lin, H. & Lieber, C. M. Electronic density of states of atomically resolved single-walled carbon nanotubes: van Hove singularities and end states. *Phys. Rev. Lett.* **82,** 1225–1228 (1999).
78. Reich, S., Thomsen, C. & Ordejon, P. Electronic band structure of isolated and bundled carbon nanotubes. *Phys. Rev. B* **65,** 155411 (2002).
79. Sfeir, M. Y. *et al.* Probing electronic transitions in individual carbon nanotubes by Rayleigh scattering. *Science* **306,** 1540–1543 (2004).
80. Wildoer, J. W. G., Venema, L. C., Rinzler, A. G., Smalley, R. E. & Dekker, C. Electronic structure of atomically resolved carbon nanotubes. *Nature* **391,** 59–62 (1998).
81. Lake, R., Brar, B., Wilk, G. D., Seabaugh, A. & Klimeck, G. in *Compound Semiconductors 1997 Institute of Physics Conference Series* 617–620 (1998).
82. Zimmerman, N. M., Huber, W. H., Fujiwara, A. & Takahashi, Y. Excellent charge offset stability in a Si-based single-electron tunneling transistor. *Appl. Phys. Lett.* **79,** 3188–3190 (2001).
83. Hong, C. *et al.* Spin-polarized reflection in a two-dimensional electron system. *Appl. Phys. Lett.* **86,** 32113 (2005).
84. Sayan, S. *et al.* Band alignment issues related to HfO_2/SiO_2/p-Si gate stacks. *J. Appl. Phys.* **96,** 7485–7491 (2004).
85. Bussmann, E., Zheng, N. & Williams, C. C. Single-electron manpulation to and from SiO_2 surface by electrostatic force microscopy. *Appl. Phys. Lett.* **86,** 163109 (2005).
86. Bachilo, S. M. *et al.* Structure-assigned optical spectra of single-walled carbon nanotubes. *Science* **298,** 2361–2366 (2002).
87. Odom, T. W., Jin-Lin, H., Kim, P. & Lieber, C. M. Atomic structure and electronic properties of single-walled carbon nanotubes. *Nature* **391,** 62–64 (1998).
88. Diebold, A. Introduction of stress requires stress metrology methods. *Solid State Technol.* **48,** 59 (2005).
89. Ku, J., Chang, J., Han, S., Ha, J. & Eom, J. Electrical spin injection and accumulation in ferromagnetic/Au/ferromagnetic lateral spin valves. *J. Appl. Phys.* **99,** 08H705 (2006).
90. Lin, H. N. *et al.* Correlating drain-current with strain-induced mobility in nanoscale strained CMOSFETs. *IEEE Electron. Dev. Lett.* **27,** 659–661 (2006).
91. Richter, C. A., Hefner, A. R. & Vogel, E. M. A comparison of quantum-mechanical capacitance-voltage simulators. *IEEE Electron. Dev. Lett.* **22,** 35–37 (2001).

Acknowledgments

The author acknowledges the support of the Jonsson School of Engineering at the University of Texas at Dallas, the NIST Office of Microelectronics Programs, and the NIST Semiconductor Electronics Division. Contribution of the National Institute of Standards and Technology is not subject to US copyright. The author would like to thank Curt Richter, Steve Knight, David Seiler and Erik Secula for careful reading of the manuscript.

Competing financial interests

The author declares no competing financial interests.

©2007 Nature Publishing Group