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# Routing multiterminal nets on a hexagonal grid

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#### Abstract

Channel routing is a vital task in the layout design of VLSI circuits. Multiterminal channel routing is different from two-terminal one. While the later is quite understood, the former still poses the difficulty. In this paper, we investigate the multiterminal channel routing problem in a hexagonal model, whose grid is composed of *horizontal tracks*, *right tracks* (with slope  $+60^{\circ}$ ), and *left tracks* (with slope  $-60^{\circ}$ ). We present an efficient algorithm for routing multiterminal nets on a channel of width d + 3, where d is the problem density. Furthermore, we can wire the layout produced by the router using four layers and there are no overlaps among different layers. This improves the previous known results [15, 19]. © 1999 Elsevier Science B.V. All rights reserved.

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# 1. Introduction

Channel routing plays an important role in the development of automated layout systems for integrated circuits [2, 10]. Many layout systems first place modules on a chip and then wire together terminals on different modules that should be electrically connected. This wiring problem is often solved by heuristically partitioning the given space into rectangular channels and then assigning to each such channel a set of wires that are to pass through it. This method reduces a "global" wiring problem to a set of disjoint "local" channel routing subproblems. For this reason, the channel routing problem has been intensively studied for over a decade, and numerous heuristics and approximation algorithms have been proposed [1, 7-9, 17].

The *Channel Routing Problem* consists of connecting terminals belonging to nets, which are displayed on two opposite sides (*entry and exit lines*) of a rectangular channel. The main objective is to complete the connections in a channel of minimum width. The solution of a channel routing problem consists of how to construct a *layout* for the nets (*routing*), and how to distribute the layout on the conductive

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Fig. 1. A multiterminal CRP instance.

layers that support the tracks (*wiring*). A net N = (P,Q) is represented by a pair of subsets P, Q of entry and exit terminals to be connected all together. Usually, terminals are represented by positive integers. The span of N = (X, Y) is defined as the pair [a,b] where  $a = \min(x: x \in X \cup Y)$  and  $b = max(x: x \in X \cup Y)$ . We represent a multiterminal net of span [a,b] with a horizontal segment from abscissa a to b, with downward and upward spokes corresponding to the entry and exit terminals, respectively. A multiterminal channel routing problem is shown in Fig. 1, where  $N_1 = (\{1, 10, 11\}, \{2, 7\}), N_2 = (\{\}, \{11, 14, 16\}), N_3 = (\{2, 6\}, \{3, 4\}), N_4 = (\{7, 12\}, \{10\}), N_5 = (\{14, 17\}, \{12, 17\}), N_6 = (\{3, 4\}, \{5, 8\})$  and  $N_7 = (\{9, 16\}, \{15\})$ . A net is a *two-terminal* net if  $|P \cup Q| = 2$ . A two-terminal net is a *unit* net if b - a = 1, and a *trivial* net if b - a = 0 (i.e.,  $P = Q = \{x\}$ ).

A fundamental parameter of the channel routing problem is the *channel density* d defined as follows. The density d is the maximum number of nets of spans  $(a_1, b_1), \ldots, (a_d, b_d)$  such that a non-integer value x with  $a_i < x < b_i$   $(1 \le i \le d)$  exists. That is, d is the maximum number of different nets crossing an arbitrary vertical line of abscissa x. In the example of Fig. 1, we have d = 3.

In this paper, we study the channel routing problem on a hexagonal grid. The paper is divided into sections as follows: In Section 2, we introduce the routing model and review the related results. In Section 3, we present an extended left-edge algorithm [10] for the multiterminal channel routing that obtains d + 3 as an upper bound to the channel width, where d is the problem density. Furthermore, we can wire the layout produced by the router using four layers, and there are no overlaps among different layers. In Section 4, we discuss our result in comparison with those for other models and pose some open problems for further research.

# 2. Motivations and routing model

An important issue for routing problems is the routing model. A routing model specifies the constraints and the rules of wire layout. A variety of routing models have been proposed for channel routing, with differences on underlying tessellations of the plane, the number of layers allowed and the ways in which wires are allowed to interact. Three main models have been investigated: the *Manhattan model* (MM) [1],



Fig. 2. A channel in TSM.

the *knock-knee model* (KK) [3, 9, 17] and the *overlap model* [8]. In the Manhattan model, two wires may share a grid point only by crossing at that point, but the wires are not allowed to overlap. In the knock-knee model, wires may share a grid point either by crossing or by bending at that point, but two wires are not allowed to overlap. In the overlap model, two wires are allowed to overlap. Besides the usual square grid, other tessellations of the plane, such as the diagonal grid [5, 13, 14, 16, 20], hexagonal grid [15, 19, 23], octagonal grid [18], and tri-hexagonal grid [21], have been proposed for solving channel routing problems. Some results on the wirability on uniform grids can be found in [12, 22].

The routing model we use is called *Times Square Model* (*TSM*) [15], where the grid is composed of *horizontal tracks*, *right tracks* (with slope  $+60^{\circ}$ ), and *left tracks* (with slope  $-60^{\circ}$ ). Clearly, TSM requires at least three layers if the wire crossing is allowed. A channel on the TSM grid is shown in Fig. 2. The entry and exit terminals are located at unit distance on the *entry* and *exit* lines. The *channel width* w is the number of horizontal tracks. To align the entry and exit terminals on vertical straight lines, the channel must be composed of odd width w = 2h + 1. We will present an efficient algorithm for routing multiterminal nets in TSM that obtains d + 3 as an upper bound to the channel width, where d is the problem density. Furthermore, we can wire the layout produced by the router using four layers. In our routing, knock-knee contacts are allowed, but no overlaps exist.

To evaluate the interest on TSM, let us compare it with the other routing models. For both Manhattan and knock-knee routing models [1, 17], density d is a lower bound on channel width. The Manhattan model also has flux f as a lower bound, where flux f can be as large as  $\Omega(\sqrt{n})$ . To eliminate this defect, a variation of the Manhattan model, called *diagonal model* (DM), was proposed in [13, 14, 16]. The grid is composed of right diagonal tracks with slope +45° and left diagonal tracks with slope -45°. For a multiterminal channel routing problem with density d, a 5d DM router was given in [16]. However, DM suffers from the fact that if the given channel routing problem has terminals placed one unit apart, then the distance between two parallel adjacent diagonal tracks, as well as the distance between any two adjacent grid points, is  $\sqrt{2}/2$ . In TSM the situation is much better. If terminals are placed one unit apart, the distance between two parallel adjacent tracks is  $\sqrt{3}/2$ , while the distance between two adjacent grid points remains one (see also Fig. 2). This appears to be acceptable in current technology, because wires are much narrower than contact cuts, and the separation distance between two connections is generally established by the closest vias [24].

Routing on hexagonal grid has been studied in recent years. The Steiner grid (based on a hexagonal grid) was first proposed for routing in [6]. A router, called Overture, was proposed in [23], which obtains  $2d/5 \le w \le d$  for two terminal channel routing problem in three layers. In [4], Brady et al. studied the channel routing problem on the hexagonal grid where the grid consists of vertical tracks, right and left tracks with slopes  $+30^{\circ}$  and  $-30^{\circ}$ , respectively. They gave an algorithm that solves the channel routing problem of two terminal nets of maximum horizontal span s in width  $2s/\sqrt{3} + O(1)$  in three layers. Times Square Model (TSM) was formulated in [15], where the hexagonal grid is composed of horizontal tracks, right tracks (with slope  $+60^{\circ}$ ), and *left tracks* (with slope  $-60^{\circ}$ ). In [19], Song and Tan proved a lower bound  $\lfloor 2d/3 \rfloor - 1$  to the width of channel in TSM, and for two-terminal problems they presented an optimal routing algorithm that obtains  $\lfloor 2d/3 \rfloor + 2$  as an upper bound to the channel width. However, the wiring problem remains unsolved. Recent advances in VLSI fabrication technology have increased the importance of multilayer channel routing [2, 7, 18]. In [15], Lodi et al. gave a routing algorithm that produces a layout for multiterminal nets in a channel of width 2d + 1, where four layers are generally required for wiring. Thus, the result obtained in this paper improves upon these previous results [15, 19].

#### 3. Channel routing in TSM

Let  $\Pi$  denote the given channel routing problem. To simplify the presentation, we assume first that there exists neither trivial net nor unit net in  $\Pi$ , that is, the span length of any net in  $\Pi$  is greater than or equal to 2. In order to route  $\Pi$ , we arrange the nets of  $\Pi$  in horizontal lines, called *chains*  $C_1, C_2, \ldots, C_d$  (*d* is the problem density). Two nets can be put in the same chain only if their spans do not overlap (although they may have one common extreme).  $C_1$  starts from left with the net having span [a, b], where *a* is the leftmost terminal; the successive nets in  $C_1$  are chosen as tightly packed as possible.  $C_2$  is constructed from the remaining nets using the same criterion, and so on. In Fig. 1, the nets are arranged in the chains  $C_1, C_2$  and  $C_3$ .

Our routing schema for  $\Pi$  is to place chain  $C_i$  in the *i*th horizontal track of the channel. The routing algorithm makes use of a representative property of TSM, that is, for a trivial net, two different connections can be used to realize it. Depending on the starting position to the entry terminal, one is called the *L*-connection and the other is called the *R*-connection (see Fig. 2). For a net N = (P,Q) with span [a,b] in chain  $C_i$ , our basic method is to use *L*-connections and *R*-connections to connect all entry



Fig. 3. An exchange operation for colliding terminals a' and b.



Fig. 4. The obtained solution for the instance of Fig. 1.

terminals in P and all exit terminals in Q to the *i*th horizontal track, respectively, and place the span [a,b] on the *i*th horizontal track from the position of a on the track to that of b. There may exist overlaps in this simple routing, because of a constant difference between grid points on even tracks and those on odd tracks in TSM. That is, a terminal x can be connected to the position of x + 0.5 or x - 0.5 on an odd track. Consider two nets N with span [a, b] and N' with span [a', b'] in a chain that share a common extreme (i.e., b = a') and are placed on an odd track. If b and a' are connected to the positions of b = 0.5 and a' + 0.5 on the odd track, respectively, then even a knock-knee cannot occur. But, if b and a' are, respectively, connected to the positions of b + 0.5 and a' - 0.5, an overlap occurs. We call such terminals b and a' *colliding terminals.* However, since b = a', the overlap can be avoided by exchanging the realization (L- or R-connection) of b with that of a' (see Fig. 3). In other words, the colliding terminals b and a' are connected to the odd horizontal track so that the positions of b and a' are, respectively, b = 0.5 and a' + 0.5. In conclusion, we can always route N and N' on the odd track so that neither overlap nor knock-knee occurs at the common extreme (terminals b and a'). Clearly, there is no conflict or overlap in the resulting layout. Fig. 4 shows such a routing for the example given in Fig. 1. In Fig. 4, an exchange operation is performed in routing  $N_1$  and  $N_2$ .

# **Routing Algorithm**

Input:  $\Pi = \{N_1, N_2, \dots, N_n\}.$ Output: The Routing R. {Chain construction}

d = 1;

WHILE  $\Pi$  is not empty **DO** 

CurrentPos = 1;

Take the net N of span [a,b] from  $\Pi$  so that a is the minimum among the extremes of the nets in  $\Pi$  with  $a \ge CurrentPos$ ;

Put N in  $C_d$  and let  $\Pi = \Pi - N$ ;

IF terminal b is greater than all leftmost terminals of the nets in  $\Pi$ 

**THEN** d = d + 1 and *CurrentPos* = 1

**ELSE** *CurrentPos* = b;

END; {WHILE}

{Routing phase}

FOR i = 1 TO d DO

Assign the *i*th horizontal track to chain  $C_i$ ;

**FOR** each net N of span  $[a,b] \in C_i$  **DO** 

Connect all entry terminal in P and exit terminals in Q to track i

using L-connections and R-connections, respectively;

IF either a or b is a colliding terminal

**THEN** Change the connections for the colliding terminals as shown in Fig. 3; Proceed on track i from the position of a to that of b;

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END {FOR}
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# END {FOR}

Consider now the wirability of the layout produced by the Routing Algorithm. Let four layers be numbered as 1,2,3 and 4. We call layers 1 and 2 *top layers*, layers 2 and 3 *middle layers*, and layers 3 and 4 *bottom layers*. L-connections and R-connections are wired in layer 1 and layer 4, respectively, whereas horizontal connections use middle layers. In order to wire the horizontal connection for a net N of span [a,b], we consider the following cases.

Case 1: The connections for both terminals a and b are L- (or R-) connections. In this case, the horizontal connection for span [a,b] is wired only in layer 2 (or layer 3).

Case 2: The connection for a is an L-connection and the connection for b is a R-connection. (The symmetric case can be analogously dealt with.) The basic method is to divide the span [a,b] into two subspans [a,b-1] and [b-1,b] and then place the subspan of [a,b-1] in layer 2 and the other [b-1,b] in layer 3.

Case 2.1: The span [a, b] is routed on an even horizontal track. We place a wire of length b - a - 1 from the position of a in layer 2 and a unit wire from b - 1 to b in layer 3. Clearly, a via at b - 1 is introduced to connect these two wires in layer 2 and layer 3. Since the space between the positions of a and b is greater than one in this case, no empty wire can be placed in either layer 2 or layer 3. In other words, there is at least a unit wire in both middle layers.

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Case 2.2: The span [a,b] is routed on an odd track. In this case, terminal a can be located at the position of a - 0.5 or a + 0.5 on the odd track, and terminal b at the position of b - 0.5 or b + 0.5. If the interval between the positions of a and b routed on the odd track is greater than one, then the wiring can be done as Case 2.1. That is, the first subspan is wired in layer 2 and the second unit wire in layer 3. If the interval is one (it may occur when a or b is a colliding terminal), then the length of first subspan becomes zero. In this case, the horizontal connection for span [a, b] is only wired in layer 3. (Under our assumption, the interval between the position of a and that of b cannot be zero.)

Vias are now introduced at the intersections of *L*- or *R*-connections with the horizontal connection. Clearly, no via is required from layer 1 to layer 4. We show below that the above layer assignment successfully wires the horizontal connections, i.e., no via conflict can occur at any point whether it is a crossing or a knock-knee point, and that there are no overlaps among different layers.

**Lemma 1.** The layout produced by the Routing Algorithm can be wired in four conducting layers, and there are no overlaps among different layers.

**Proof.** It is important to observe that the Routing Algorithm routes all spans of nets on a horizontal track with the length greater than or equal to 2 in the case where no collision occurs, and that in the colliding case, the exchange operation assures that no knock-knee occurs at the positions of colliding terminals.

Since L-connections, R-connections and horizontal connections are wired in layer 1, layer 4 and middle layers, respectively, there is no via conflict at a crossing point. Consider now knock-knee points. It is the trivial case that knock-knees occur between an L-connection and a R-connection, since L-connections and R-connections are wired in layer 1 and layer 4, respectively. A knock-knee can occur if two nets N with span [a,b] and N' with [a',b'] are routed on the same even horizontal track and b' = a(Fig. 5(a)). Suppose that the connection for terminal b is an L-connection and the connection for terminal a' is a R-connection. (The symmetric case can be analogously dealt with.) Then the whole span (Case 1) or the second subspan (Case 2) of N is wired in layer 3. Since both spans are routed on the even horizontal track, the wires for the above two subspans cannot be empty. Thus, the connections for N are wired in top layers at the position of b and the connections for N' are wired in bottom layers at the position of a'. It implies that no conflict can happen in this case.

A knock-knee can also occur in the case where the span [a, b] of net N and the span [a', b'] of net N' are routed on the same odd horizontal track and b + 1 = a'. That is, b and a' are respectively connected to the positions of b + 0.5 and a' - 0.5, see Fig. 5(b). (Recall that a knock-knee cannot occur in our routing when two nets N with span [a, b] and N' with span [a', b'] are routed on the same odd horizontal track and b = a'.) Without loss of generality, we assume that the connection for terminal b is an L-connection and the connection for terminal a' is a R-connection. Then, the second



Fig. 5. Two cases of knocl-knee contacts.

subspan of N (Case 2) is wired in layer 2 and it always has the length of one. The first subspan of N' (Case 2) is wired in layer 3. Since terminal a' is routed at the position of a' - 0.5 on the odd track and the length of span [a', b'] is greater than or equal to 2, the interval between the position of a' and that of b' routed on the odd track must be greater than or equal to 2. That is, the first subspan (Case 2) of N' cannot be empty. Hence, the connections for N (either Case 1 or Case 2) are wired in top layers at the position of b and the connections for N' (either Case 1 or Case 2) are wired in bottom layers at the position of a'. Since knock-knees can occur only in the above three cases, we obtain that there is no via conflict at a knock-knee point.

In our wiring, *L*-connections and *R*-connections are wired in layer 1 and layer 4, respectively. A horizontal span may make use of layer 2 and layer 3, but its two subspans are disjoint. Thus, there are no overlaps among different layers.  $\Box$ 

To complete our routing algorithm, we need to remove the assumption that there exists neither trivial net nor unit net in the given channel routing problem  $\Pi$ . First, all trivial nets can be put in a single chain. For a trivial net, we utilize the corresponding L- (or R-) connection to realize it. The chain of trivial nets does not occupy any horizontal track, and one layer (e.g., layer 1) is enough to wire the routing for trivial nets. Second, all unit nets can be simply arranged in two chains so that the spans of two nets in the same chain do not overlap. For simplicity, we arrange the unit nets that have either two entry terminals or one entry terminal with smaller integer in chain  $C_0$  and the rest nets in chain  $C_{d+1}$ , and route  $C_0$  and  $C_{d+1}$  in the first and last



Fig. 6. Illustraitons for unit triangles,  $L \circ R$  and  $R \circ L$  connections.

horizontal tracks of the channel, respectively. Since all spans have the length of one, a net can be simply routed either by a unit triangle (when two terminals are entry (or exit) terminals) or by an  $L \circ R$  (or  $R \circ L$ ) connection. See Fig 6. Clearly, one layer is enough to wire the routing for unit nets.

**Theorem 1.** Any multiterminal channel routing problem can be solved in a channel of width less than d+3 in TSM, and the layout produced by this router can be wired in four layers without overlaps. The routing algorithm takes  $O(n \log n)$  time.

**Proof.** All the nets with the span length greater than or equal to 2 are routed in *d* horizontal tracks by Routing Algorithm. The trivial nets and the unit nets are simply routed in additional two horizontal tracks. This implies the completeness of our routing algorithm. Since the width of a TSM channel is odd, we obtain that any multiterminal channel routing problem can be solved in a channel of width less than d + 3 in TSM. The four-layer wirability and non-overlaps are shown in Lemma 1.

For a k-terminal net, our algorithm introduces at most k + 1 vias. Note that k is the minimum number of vias required in the Manhattan model. We also note that our chain construction takes  $O(n \log n)$  and the routing algorithm runs in O(n) time. Thus, the time complexity of our algorithm is  $O(n \log n)$ .  $\Box$ 

# 4. Concluding remarks

We have presented a dense channel routing algorithm in TSM that solves any multiterminal channel routing problem in a channel of width of at most d + 3. The obtained layout can be easily wired in four layers.

To summarize, let us compare our result with those obtained for the other routing models, based on the channel width w, the number of layers, and the number of vias (Table 1). TSM compares favorably with MM and KK for the value of w, while, for the number of layers, MM and KK are instead superior. TSM compares favorably with DM too, except for the number of layers. However, with the advance in VLSI technology, utilization of more than two layers for routing has become feasible [7]. It makes TSM more interesting. For a k-terminal net, our routing algorithm introduce

Routing model	Layer	Channel width
TSM	4	d+3
MM	2	$3d/2 + O(\sqrt{d \log d} + f)$ [9]
DM	2	5d + 12 [16]
КК	3	$3d/2 + O(\sqrt{d\log d}) \ [9]$

Comparison of different models (f is the flux and in order of  $\sqrt{n}$  where n is the number of nets. [1])

k + 1 vias. This number is optimal (up to a constant factor 1) in the Manhattan Model. Note that the algorithms of [9, 16] provide their values of w at a cost of high number of vias, due to the insertion of "doglegs" in many connections. In addition, our routing algorithm for TSM is simpler than those for MM, DM and KK.

It is known that multiterminal channel routing is quite different from two-terminal one. While the later is quite understood, the former still poses the difficulty. In most routing models, the best upper bounds on channel width for multiterminal problems are twice worse than those for two-terminal ones. However, the situation in TSM is more favorable, as we have d + 3 for multiterminal case and  $\lfloor 2d/3 \rfloor + 2$  for two-terminal case [19].

On Manhattan grids, many multilayer routing methods are proposed [7]. In order to reduce channel width, several wires may be assigned with the same horizontal track but placed in different layers. This produces a lot of overlaps in layouts, which increases the track capacitance and cross-talk. Instead, there are no overlaps among different layers in the layouts produced by our algorithm, which is distinct and favorable.

Finally, we pose several questions on the wirability of general hexagonal routing. On the Manhattan grid, Lipski [11] have shown that it is NP-complete to decide whether an arbitrary layout is 3-layer wirable, and Brady and Brown [3] have shown that any layout in the knock-knee mode is 4-layer wirable. Can these methods be generalized to the layouts on hexagonal grids, or can we obtain the similar results on the wirability of general hexagonal routing? On the other hand, Tollis [21] has shown that any layout on a tri-hexagonal grid can be wired using five layers. Our further investigation is being directed to these problems.

# References

- B.S. Baker, S.N. Bhatt, F.T. Leighton, An approximation algorithm for Manhattan routing, Proc. 15th Ann. ACM Symp. on Theory of Computing, 1983, pp. 477–486.
- [2] B. Berger, M. Brady, D.J. Brown, F.T. Leighton, Nearly optimal algorithms and bounds for multilayer channel routing, J. ACM 42 (2) (1995) 500-542.
- [3] M. Brady, D.J. Brown, VLSI routing: four layers suffice, in: F.P. Preparata (Ed.), Advances in Computing Research, Vol. 2, JAI Press, Greenwich, CT, 1984, pp. 245–257.
- [4] M. Brady, D.J. Brown, K.D. Powers, Channel routing on a 60° grid, Proc. Conf. Information Science and Systems, 1990, pp. 926–931.
- [5] K. Chaudhary, Peter Robinson, Channel routing by Sorting, IEEE Trans. CAD 10 (6) (1991) 754-760.

Table 1

- [6] P. Chaudhuri, An ecological approach to wire routing. Proc. IEEE Internat. Symp. on Circuits and Systems, 1979, pp. 854-857.
- [7] J. Cong, C.L. Liu, A new approach to three- or four-layer channel routing, IEEE Trans. CAD 7 (1988) 1094–1104.
- [8] S. Gao, S. Hambrusch, Two-layer channel routing with vertical unit-length overlap, Algorithmica 1 (1986) 223–232.
- [9] S. Gao, M. Kaufmann, Channel routing of multiterminal nets, J. ACM 41 (4) (1994) 791-818.
- [10] A. Hashimoto, J. Stevens, Wire routing by optimization channel assignment within large apertures, in: Proc. 8th. Design Automation Workshop, 1971, pp. 155–163.
- [11] W. Lipski, On the structure of three-layer wirable layouts, in: F.P. Preparata (Ed.), Advances in Computing Research, Vol. 2, JAI Press, Greenwich, CT, 1984, pp. 231–244.
- [12] W. Lipski, F.P. Preparata, A uniform approach to layout wirability. Math. System Theory 19 (1987) 189–203.
- [13] E. Lodi, F. Luccio, L. Pagli, A preliminary study of a diagonal channel routing model, Algorithmica 4 (1989) 585–597.
- [14] E. Lodi, F. Luccio, L. Pagli, Channel routing for strictly multiterminal nets, Integration, VLSI J. 8 (2) (1989) 143–153.
- [15] E. Lodi, F. Luccio, L. Pagli, Routing in times square mode, Inform. Process. Lett. 35 (1990) 41-48.
- [16] E. Lodi, F. Luccio, X. Song, A 2d channel router for the diagonal model, Integration, VLSI J. 11 (2) (1991) 111–125.
- [17] K. Mehlhorn, F.P. Preparata, M. Sarrafzadeh, Channel routing in knock-knee mode: simplified algorithms and proofs, algorithmica 1 (1986) 213–221.
- [18] B. Rhee, Y. Sugai, H. Hirata, A new HVHD model four layer channel router using a channel-graph (in Japanese), Trans. IEICE Japan J77-A (1994) 671-679.
- [19] X. Song, X. Tan, An optimal channel routing algorithm in the times square model, IEEE Trans. CAD 13 (1994) 891–898.
- [20] X. Tan, X. Song, Improvement on the diagonal routing model, IEE Proc.-Circuits Dev. Systems 141 (1994) 535–536.
- [21] I.G. Tollis, Algorithms for VLSI layout, Tech. Rep. ACT-85, Coordinated Science Laboratory, University of Illinois at Urbana, 1987.
- [22] I.G. Tollis, Techniques for wiring in non-square grids, ISCAS'89, 1989, pp. 66-69.
- [23] D.C. Wang, Novel routing schemes for IC layout Part I: two-layer channel routing, Proc. 28th ACM/IEEE Design Automation Conf., 1991, pp. 49–53.
- [24] D.F. Wong, C.L. Liu, Compacted channel routing with via placement restrictions, Integration, VLSI J. 4 (1986) 287–307.