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Editorial

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This issue features approximate computing, analog circuit diagnosis, memory testing, system-on-chip (SoC) test scheduling, hardware security, and fault tolerance. It contains nine articles.

The first two papers address approximate computing. This is a topic of growing interest. Actually, electronic circuits and systems are machines built to fulfill the specified requirements exactly. This ensures correct operation from the deployed system. However, in many applications the final correctness depends on human judgement. For example, this is true in cases of speech and video where errors in the lower order bits of a computed magnitude may go unnoticed. Hence the question: Is machine-like accuracy an overkill? If we take advantage of relaxed requirements, we can design electronic circuits to reduce power and hardware or enhance performance. Note that in performing a manual task, we have a natural tendency of minimizing the effort, resources and time, as long as the results meet acceptable criteria. We could say that the idea of approximate computing is to have a machine imitate the human behavior.

Authors of the first article are Anghel, Benabdenbi and Vatajelu from University of Grenoble Alps, Grenoble, France and Bosio and Traiola from University of Montpellier, Montpellier, France. They discuss ways of using test and reliability methods for approximate computing. The paper provides a survey of the area with a large number of references.

The second article gives a design for a static memory for image processing applications. Reducing bits in the memory reduces area, power and delay at the cost of small increase in the peak signal to noise ratio (PSNR). Contributors of this research are Jothin from KGiSL Institute of Technology, Coimbatore, India and Vasanthanayaki from Government College of Technology, Coimbatore, India.

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The third article addresses test and diagnosis of a power regulator circuit. Power regulators, together with decoupling capacitors, control the sudden voltage drop (supply droop) caused by high switching activity on a VLSI chip. The authors, Dirican, Ozmen and Margala from University of Massachusetts Lowell, Massachusetts, USA, propose a built-in self-test circuit using an analog-to-digital converter to measure and store the droop information in digital format.

Then, we have two articles on memories. Focusing on the area, delay and power tradeoff, the first paper presents a column line code (CLC) for detection and correction of multiple cell upsets (MCU). This novel CLC uses an extended Hamming code and parity bits. Contributors are Silva, Silveira and Silveira from Federal University of Ceará, Marcon and Vargas from Pontifical Catholic University of Rio Grande do Sul (PUCRS), and Lima Jr. from Federal Institute of Ceará, Maracanaú, in Brazil.

The fourth article presents a technique to enhance the capability of a built-in self-repairing (BISR) scheme of a memory based on error correcting code (ECC). If locations of faulty cells on a chip render the implemented ECC ineffective, then this technique tries to remap addresses. This is accomplished by adding programmable row and column address remapping controllers (RARC and CARC). Because, some, though not all, fault maps allow feasible address remapping that is consistent with the ECC, in general, memory yield is enhanced. Authors of this interesting work are Lu, Jheng and Lin from National Taiwan University of Science and Technology, Taipei, Taiwan, and Hashizume from University of Tokushima, Tokushima, Japan.

Sixth article develops a mixed integer linear programming (MILP) model to minimize the test application time (TAT) for a system-on-chip (SoC). Core test scheduling uses frequency and voltage scaling so as not to exceed the power budget while maximizing concurrency. Besides, test partitioning further increases the number of concurrently tested cores. A key feature of the presented methodology is to ensure that the chip temperature does not exceed the specified limit. Contributors are Zhang, Ling and Jiang from Tongji University, Shanghai,

China, and Xiao from Zhejiang University of Technology, Hangzhou, China.

Seventh article uses a genetic algorithm to derive tests for detecting hardware Trojans. With the inclusion of controllability, observability and transition probability, the fitness function favors testing of rare nodes. Results show higher coverage of hard to trigger Trojans. The authors are Nourian and Fazeli from Iran University of Science and Technology, Tehran, Iran, and Hely from Grenoble Institute of Technology, France.

Next two articles are on fault tolerant designs. The paper by Islam from University of Michigan Dearborn, Michigan, USA gives a unique design for a flip-flop. This flip-flop operates with a sinusoidal clock signal that is distributed over the chip through a resonant RLC network without using any clock buffers. The benefit is a significant saving in clock power. In addition, the design uses dual interlocked cell (DICE) latch that prevents single event upsets (SEU).

The final paper in this issue proposes a fault tolerance scheme using the method of regular expression matching (REM). REM has been used in communications for detecting and correcting errors as well as for security of mission critical systems. The REM-based reliability requires less hardware than other alternatives like triple modular redundancy (TMR), but reduces performance. This paper uses various algorithms to design and implement efficient REM engines on FPGA and demonstrates improved performance. Authors Leipnitz and Nazar are from Universidade Federal do Rio Grande do Sul, Porto Alegre, Brazil.