A 56 Gbaud Reconfigurable FPGA Feed-Forward Equalizer for Optical Datacenter Networks with flexible Baudrate- and Modulation-Format

Christos Spatharakis, Giannis Kanakis, Nikolaos Iliadis, Paraskevas Bakopoulos, Hercules Avramopoulos
Photonics Communications Research Laboratory,
National Technical University of Athens,
Athens, Greece
cspatha@mail.ntua.gr

Konstantinos Maragos, George Lentaris, Dimitrios Soudris
Microprocessors and Digital Systems Laboratory,
National Technical University of Athens,
Athens, Greece
komaragos@microlab.ntua.gr

***Abstract*— The staggering growth of datacenter traffic has spurred the rapid uptake of advanced modulation-formats to increase throughput. Commodity optoelectronic components are used for cost-efficiency, assisted with digital equalizers to mitigate their bandwidth limitations. With optically-switched datacenter architectures gaining momentum, reconfigurable equalizers are sought allowing the receiver to adapt to different fiber lengths, bitrates and modulation-formats associated to different optical paths. An FPGA-based feed-forward equalizer (FFE) reconfigurable in baudrate and modulation-format is demonstrated. We verify its performance with NRZ and PAM-4 experimental data up to 56 GBaud, investigate its accuracy and extract the optimum FFE implementation for different transmission scenarios.**

Keywords—FPGAs, Optical Interconnects, Feedforward Equalization, Parallel Architectures, Datacenter Networks

I. INTRODUCTION

The proliferation of cloud services is bringing datacenter traffic to a steep growth curve, with sustained annual growth rates reaching 25% [1]. The largest portion of this traffic concerns communication between servers within the same datacenter, thus turning the spotlight on optical interconnects for distances spanning from 2 meters up to 2 kilometers [2]. Recognizing that optics dominate the cost of interconnects assemblies, equipment manufacturers are seeking simple, low-cost commodity optoelectronics to meet the stringent cost requirements of datacenters [3]. To compensate the bandwidth limitations of such cost-optimized components and reach the desired performance envelope, designers advocate the use of digital equalization, leveraging the strengths and flexibility of ubiquitous CMOS digital electronics [4]. Digital equalization is a key enabler not only for extending the signaling rate of optical interconnect links, but also to cope with the reduced noise margins of higher-order modulation formats like PAM-4, that are gaining traction in commercial systems [3],[4]. Compared to analogue equalizers, digital implementations offer a number of advantages such as higher performance, flexible architecture and smaller susceptibility to process, voltage and temperature (PVT) variations [5].

The flexibility of digital equalization paves the way for optical interconnect modules with broad applicability, by configuring the same hardware according to the particular operating conditions and impairments present in a given link (e.g. bandwidth limitations of optoelectronics and host PCB, chromatic dispersion of optical fiber). Thus, economies of scale can be achieved through the replacement of multiple specialized products targeting different deployment scenarios. In addition, the capability to dynamically reconfigure the equalizer is particularly attractive in the context of hybrid electronic-optical datacenter networks, which rely on the combined operation of optical circuit switches with conventional electronic packet switches. Long-lived, “elephant” flows are served by the optical circuit switches, whereas short-lived, “mice” flows are handled by the electronic packet switches [6]. Given that elephant flows remain in the optical domain throughout the circuit-switched network, the overall propagation distance of the optical signal varies for each source-destination pair, thus affecting the impairments it sustains, e.g. due to chromatic dispersion. In order to successfully receive all possible flows in the network, all links are configured according to the worst-case scenario, i.e. the combination of baudrate and modulation format that allows error-free transmission even for the longest link in the network, where dispersion effects are more acute. As a result, shorter links are underutilized, in the sense that they operate with a very high margin. An optical network with flexible baudrate and modulation format adapts the parameters of the transmitted signal according to the exact characteristics of each link, to maximize overall throughput. In this scenario, a dynamically reconfigurable equalizer is indispensable at the receiver side, to ensure optimum operation of the link under all possible configurations. A prominent computational platform for reconfigurable digital equalization is the Field Programmable Gate Array (FPGA). FPGAs offer programmability (reducing cost and time-to-market dramatically compared to application-specific integrated circuits - ASICs), tremendous throughput, dynamic reconfiguration and impressive performance-per-watt ratio, compared to conventional CPUs [7].

Recently we demonstrated a high-performance FPGA implementation of an FFE for optical interconnects and verified its performance with an externally modulated link operating up to 40 Gb/s [8]. In this paper we demonstrate dynamic reconfiguration of the FFE, and its successful operation with varying modulation format (NRZ, PAM-4), baudrate (ranging from 32-56 Gbaud) and transmission reach (0-2 km), achieving maximum throughput up to 80 Gb/s and sampling rate up to 56 GSa/s. The optical interconnect implementation is based on direct modulation of a single-mode long-wavelength VCSEL [9]. Direct modulation of VCSELs is more suited to the cost targets of intra-datacenter links, whereas single-mode operation can support long distances associated to mega-datacenters (typically 2 km). Reconfiguration time of the FPGA equalizer is estimated to be in the range of 74 to 104 ms according to the faster approaches of [10] and the size of the XC7VH580T device employed in this work, underpinning its compatibility with large-scale optical circuit switches, achieving typical reconfiguration times of 25-130 ms. Even though the cost of the FPGA board used in this work is not negligible, rapid progresses in CMOS electronics are expected to commoditize the technology, paving the way for widespread deployment in datacenter applications.

II. Equalizer Description

In this section we present the hardware (HW) implementation of the FFE and we describe the parallelization techniques we devised in order to exploit its inherent parallel nature and increase the maximum throughput rate.

The operation of the FFE relies on the transfer function:

$$y(n) = \sum_{i=0}^{N} c_i \cdot x(n-i), \qquad 0 \le i \le N \qquad (1)$$

where $x(n)$ is the input signal, $y(n)$ is the output signal, N is the filter's order and c_i is the i-th coefficient of the filter (the block diagram of a typical FFE implementation can be found in [5]). We developed a baseline FFE HW design, as illustrated in Fig. 1, which consists of the following components:

- A ROM where the coefficients values are stored.
- A FIFO for the temporary storage of the N oldest values of the input samples.
- A multiply-accumulate (MAC) processing unit where all the necessary operations of Eq. 1 are executed.
- A control module for the addressing of the ROM and FIFO, the initialization of the MAC unit, and the synchronization of the entire FFE operations.

To achieve maximum throughput rate we applied certain techniques to exploit the potential parallelization of Eq. 1. Firstly, we developed a fully parallel design for the FFE transfer function by dividing the ROM and FIFO components into $N+1$ sub-components and employing $N+1$ multipliers in parallel, which in turn feed an adder tree module to aggregate their products and produce the final output of the FFE. With this technique we increased the throughput rate to one output sample per cycle.

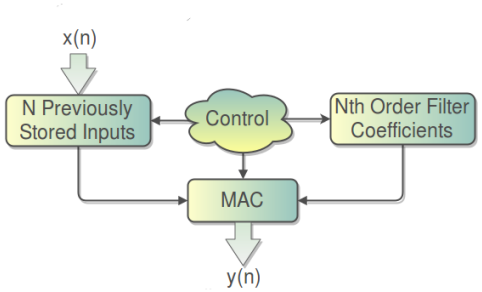

Fig. 1. Baseline HW architecture of FFE. It calculates one output sample $y(n)$ every $N+1$ cycles.

To further increase the throughput rate we enhanced our design to support the concurrent processing of multiple input samples. We organized multiple fully-parallel designs of the FFE engine described above, such that each FFE is dedicated to the calculation of an individual sample $y(n)$. We assume that $x(n)$ is transmitted at higher clock rate compared to that of the FPGA f_{FPGA} and, thus, we used a parallel-to-serial buffer between the FPGA transceivers and the FPGA logic which multiplexes D successive $x(n)$ samples received with rate $D \cdot f_{FPGA}$ into one D-tuple $[x(n), x(n-1), \ldots, x(n-D+1)]$ that is forwarded to the FFE at rate f_{FPGA}. The D parameter denotes the number of the employed FFE engines and is bounded only by the available FPGA resources. The final architecture of our implementation is depicted in Fig. 2.

III. Experimental Setup and DSP Processing

To investigate the performance of the implemented digital equalizer, a typical optical interconnect was implemented with the experimental setup of Fig.3. An 8-bit, 65 GSa/s arbitrary waveform generator (AWG) provided a single-ended output of different data rates and modulation formats: 32-and 40 GBaud PAM-4 and 35-45-56 Gb/s NRZ. The repeating pattern length was 2^{11} symbols. A Raised Cosine (RC) pulse-shaping filter was applied to the generated signal, with roll-off factor a=1 so as to constrain its spectrum to the main lobe. The AWG output signal had a voltage swing of 600 m V_{P-P} and was fed directly to the 20.5 GHz 3dB bandwidth VCSEL leading to the generation of an optical signal with output optical power of ~0 dBm. Spools of 500 m and 2 km standard SMF were employed in order to investigate the signal degradation in

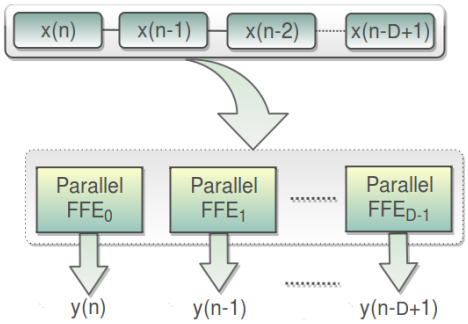

Fig. 2. Multiple fully parallel FFE engines. This architecture calculates D output samples per cycle

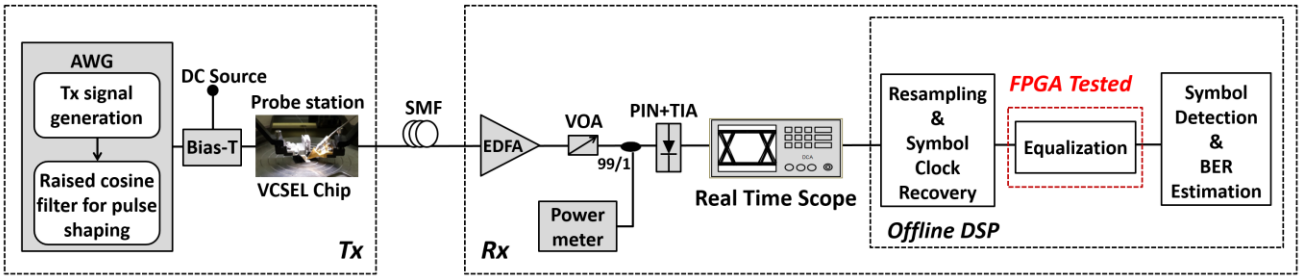

Fig. 3. Experimental setup of the studied optical interconnect link.

different transmission scenarios. An off-the-shelf 40 Gb/s photoreceiver was used for signal detection, consisting of a waveguide-integrated pin-photodiode (PD) and a trans-impedance amplifier (TIA) with limiting output buffer. The photoreceiver exhibited a 3 dB bandwidth of 35 GHz, 0.6 A/W responsivity, 500 V/W conversion gain and -12 dBm sensitivity (10^{-12} BER, 2^{31}-1 PRBS). Due to the limiting operation of the available photoreceiver, operation at low received power was necessary in order to avoid nonlinear distortion. A variable optical attenuator was placed at the input of the photoreceiver, to allow sweeping of the received optical power. The received signal was captured on a 33 GHz, 80 GSa/s real time oscilloscope for further offline DSP processing.

The captured data were initially processed in MATLAB using offline DSP algorithms in order to assess the link's performance. The discretized signals were resampled to 4 samples/symbol and the square timing algorithm was employed to recover the symbol clock. The resulting 1 sample/symbol at the best sampling point was then fed to a symbol-spaced Feed-Forward Equalizer (FFE) structure to estimate the channel response. The length of the FFE was varied to 16 and 32 taps depending on the signal's modulation format and baudrate. The equalizer taps were determined by employing an adaptive FFE with a known training pattern and the normalized least mean squares (LMS) algorithm, in order to estimate the channel (and therefore reverse its response). Once the estimation error was sufficiently minimized, the training process was concluded. The derived tap weights were then used to equalize the received data with a static FIR filter. Further processing and analysis could then be performed on the equalized data, including symbol detection and BER estimation with Gray encoding. In order to investigate the extent to which the performance of the implemented equalizer is affected due to the FPGA's limited resolution, a bit accurate model was developed in MATLAB and was compared with the full accuracy double precision (64-bit) implementation. The resolution of the input and output signals, as well as of the filter coefficients were determined by the baudrate of the signal and the number of the FFE taps. Before entering the static FIR equalizer, the signal and the filter coefficients were truncated so as to be representable by n binary bits. In order to consistently preserve the bit-accurate nature of the model, the values obtained through products and additions inside the filter, as well as at the filter output, were truncated in a similar manner to m binary bits; in the rest of the paper the selected accuracy is represented in the form of (n,m). Before applying the bit-accurate functions, the signal was normalized to get a value in the range (-3; +3) so that 3 binary bits are enough to represent the integer part, of which one is dedicated to the sign representation. As a result, n-3 bits of the input and coefficients and m-3 bits of the filter output are used to represent the fractional part of the values. The estimated equalizer configurations were implemented and tested in the FPGA. Equalization of the experimental data was simulated in the XILINX simulator tool and the simulation results were consistent with the bit-accurate model described earlier.

IV. Experimental Results and Discussion

In Fig.4, the BER performance of a 40 Gbaud PAM-4 and a 56 Gb/s NRZ signal are plotted as a function of the received optical power for the case where no equalization is employed and for the cases where the proposed equalizer and the reference MATLAB equalizer are used. Fig.4 is a typical bathtub curve where the saturation of the receiver results in performance degradation above a certain level of received optical power; the degradation in PAM-4 is shifted on the left compared to NRZ due to the higher OSNR requirement. The horizontal dotted lines represent the FEC thresholds of three common FEC codes used in datacenter applications: BCH(3456,3084), RS(528,514) and RS(280,260) [12]. The accuracy used in both cases was set to (10,8) while 16 taps were employed for the 56 Gb/s NRZ signal and 32 taps for the 40 GBaud PAM-4. The improvement

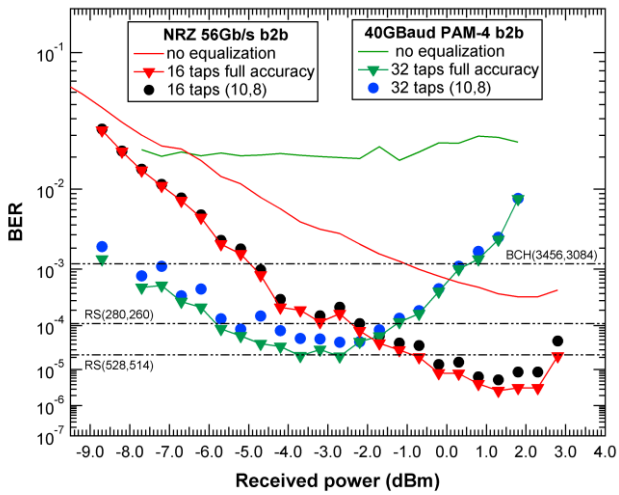

Fig. 4. BER results as a function of Rx optical power for two experimental data sets without equalization and with the proposed and reference (full accuracy) equalizers

TABLE I. THROUGHPUT RATE AND RESOURCES UTILIZATION OF VARIOUS FFE CONFIGURATIONS IMPLEMENTED IN THE XC7VH580T FPGA DEVICE

Testing Configuration			**Implementation Characteristics**		**XC7VH580T Resource Utilization**	
Signal	***Taps***	***Accuracy***	***Ext. Parallelism***	***Freq.***	***LUTs***	***DFFs***
NRZ 56 G	16	(10,8)	224	250 Mhz	161567 (44.53%)	442052 (60.92%)
NRZ 45 G	32	(10,8)	180	250 Mhz	101257 (27.91%)	273316 (37.67%)
PAM4 40 G	32	(10,8)	160	250 Mhz	152566 (42.05%)	388376 (53.52%)
NRZ 35 G	32	(10,9)	140	250 Mhz	93759 (25.84%)	169334 (23.34%)
PAM4 32 G	32	(10,9)	128	250 Mhz	197691 (54.49%)	417386 (57.52%)

of the BER performance is evident when equalization is employed, advocating the use of FFE for such optical interconnect links. Moreover, the implementation penalty due to the limited FPGA resolution for both NRZ and PAM-4 signals is limited to less than 1 dB, proving that the hardware implementation of the equalizer exhibits robust performance even with limited accuracy. The accuracy and the number of taps were determined by the FPGA utilization and the desirable throughput and are summarized in Table I. In this table we illustrate the implementation of various FFE configurations on the FPGA according to the target baudrate. *Ext. Parallelism* denotes the number of the employed FFE engines. Regarding the resource utilization, we do not use any BRAM memory resources since all storage components in our HW architecture are manipulated as single registers considering the fully parallel architecture of FFE (section 2). In order to assist the synthesis tool in optimizing all trivial calculations (e.g., multiplication with zero) we avoid the inference of the available embedded DSP blocks. Logic resources (LUTs, DFFs) are more susceptible to optimizations and thus, more resources can be saved. Table II summarizes the required power to achieve BER below the RS(280,260) FEC threshold with and without FPGA equalization and the minimum BER performance for all the tested signals.

CONCLUSIONS

We have implemented a reconfigurable FPGA-based FFE. The equalizer's performance was validated with experimental data of 35-45-56 Gb/s NRZ and 32-40 GBaud PAM-4 for transmission up to 2 km and low implementation penalty was verified compared to a full precision FFE. Operation for different baudrates and formats underpins the suitability of our FFE equalizer for hybrid flexible optical datacenter networks.

TABLE II. REQUIRED OPTICAL POWER TO ACHIEVE BER BELOW BCH(3456,3084) FEC THRESHOLD AND MINIMUM BER PERFORMANCE

Signal	**Required Optical Power**		**Minimum BER for the implemented FFE**
	No equalization	**Implemented FFE**	
PAM4 32Gbaud b2b	-5.8 dB	<-10 dB	$1.52 \cdot 10^{-6}$
PAM4 32Gbaud 500m	-2.5 dB	-10 dB	$3.72 \cdot 10^{-6}$
PAM4 32Gbaud 2km	-	-	$2.71 \cdot 10^{-3}$
PAM4 40Gbaud b2b	-	-7 dB	$4.44 \cdot 10^{-5}$
PAM4 40Gbaud 500m	-	-3.8 dB	$1.64 \cdot 10^{-4}$
PAM4 40Gbaud 2km	-	-	$3.61 \cdot 10^{-3}$
NRZ 35Gb/s b2b	<-10 dB	<-10 dB	$<8.67 \cdot 10^{-8}$
NRZ 45Gb/s b2b	-4.7 dB	-8 dB	$<8.67 \cdot 10^{-8}$
NRZ 56Gb/s b2b	-3.7 dB	-5 dB	$6.55 \cdot 10^{-6}$

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