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DESIGN OF A 10-BIT NON-LINEAR INTERPOLATION DAC

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ABSTRACT

This paper presents a novel design for a 10 bit DAC. The design is to be integrated in a direct digital frequency synthesizer (DDFS). The design consists of three main modules, a nonlinear course DAC, a linear fine DAC, and a nonlinear interpolation DAC. Each of these modules contributes in enhancing the DAC performance. The DAC is then integrated, and simulated using Mentor Graphics Tools. The simulation was done using a 3.3V, 0.35u CMOS technology. The design has an advantage over the published DACs in its simplicity and repeatability. The design operates at higher output frequency with considerable spectral purity.

KEYWORDS

CMOS, digital-to-analog converter, nonlinear digital-to-analog converter, Interpolation DAC, Direct Digital Frequency Synthesizer.

INTRODUCTION

The conventional DDFS consists of an phase accumulator, a lookup table which is a Read Only Memory (ROM) to converts phase to amplitude, and a DAC. The system is synchronized using a reference clock (figure 1).

$$\Delta f = \frac{f_{clk}}{2^M} \quad (1)$$

The DDFS has a minimum frequency resolution equals to the reference clock divided by the phase word (1).Where Δf is the frequency resolution, f_{clk} is the clock frequency and M is the Phase word.

The output amplitude is limited by ROM size. The larger the ROM size, the better the DDFS output resolution. Large ROMs consumes high power, so it is a trade off between resolution and power consumption. The urge to lower power consumption produced some reduction techniques. Examples of the used techniques are half and quarter wave symmetry, Hutchison's technique, Sunderland technique, Nicolas Technique and Taylor series approximation [1, 2].

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The compression ratio might reach 53:1 in some cases, which indicates that reducing power consumption is an important goal in DDFS design cycle. On the other hand, compression introduces some unwanted frequencies and the design might need a high performance reconstructive filter.

Another Approach is to design a ROM-less DDFS. The phase word is used to control the switching of a number of current sources constituting the DAC. This technique is known as current steering. Designing a DAC in a ROM-less DDFS is very critical. DAC is responsible for phase to amplitude conversion, high quality output and relaxing or even replacing the reconstructive filter.

The current steering DAC may be implemented in many topologies and architectures. There are three main architectures, the binary weighted, unary decoded, and Segmented Architectures [6]. The binary weighted architecture uses a binary coded phase to control the current sources switching. The advantage of this architecture is its compactness in size due to the use of few numbers of transistors. On the other hand, it has a disadvantage of having considerably high glitches due to binary switching scheme. The unary decoded architecture uses thermometer code to switch the current sources. The advantage of this architecture is its reduced magnitude of glitches because only one transistor is switched at a time. The main disadvantage of this architecture is the need for many transistors. The segmented architecture is a mixture of the former two architectures and has the best of both architectures that is why it is commonly used. In this architecture the most significant bits (MSB) are unary decoded to reduce glitches and the least significant bits (LSB) are binary coded to reduce the number of transistors. The LSB introduces glitches with small amplitude which is spread in the frequency domain as white noise.

The interpolation DAC is considered as an application of the current steering DAC. It consists of folded current sources switched using a reference clock and a number of delays to give an output similar to interpolation DAC [3, 4]. The disadvantage of this DAC is the large number of transistors that reached 192 transistor as in [5]. This leads to high power consumption and a reconstructive filter is needed.

PROPOSED DAC ARCHITECTURE

The proposed architecture is considered as a segmented current steering DAC. The DAC consists of both course and fine DACs. The course DAC is thermometry decoded and consists of nonlinear current sources. The fine DAC consists of a linear DAC and an interpolation DAC. The linear DAC is binary coded and consists of linear current sources. The linear DAC output is fed to the input of the nonlinear interpolation DAC. Then the course and fine outputs are added to form the output signal (figure 2).

The four MSB are used to switch 15 folded cascode current sources. The 6 LSB are xored with the MSB to reverse the shape of the linear DAC output for half of the cycle. The nonlinear interpolation DAC consists of 16 current sources similar to that of the course DAC. The 16 current sources are designed to be switched one at a time using 16 NMOS multiplexers. Each multiplexer chooses between linear DAC output and a reference voltage.

NON LINEAR INTERPOLATION DAC

The key feature of the design is the nonlinear interpolation DAC which is responsible for increasing the spectral purity. Each of its 16 cells consists of two switches and a current source (figure 3).
The switches control the amount of current in the cell. All transistors must be forced to operate in saturation mode. The output current of the cell depends on the differential input voltage and the switches transconductance according to equation 2 [7].

$$\Delta I_{out} = \frac{\beta}{2}\Delta V\sqrt{\frac{4I_{bias}}{\beta} - \Delta V^2} \qquad (2)$$

Where ΔI_{out} is the differential output current, ΔV is the differential input voltage, I_{bias} is the constant current and β is the Transconductance of the two switches.

The cell current is varied according to the course DAC step. Correspondingly the geometry of the switches is changed to keep a constant transfer function slope. This means that each cell has a different bias current and switches transconductance value. The cell transfer function is shown in (figure 4).

SIMULATION RESULTS

Each DAC described in the above sections is optimized to increase both spectral purity and operating frequency. The reduced layout area was also an issue. The final proposed DAC is then integrated and simulated using Mentor Graphics tools. The output of the linear DAC swings between V_{ref} and V_{ref} -50 mV in 64 steps as shown in (figure 5)

The linear DAC output is fed to the interpolation DAC. Each input of the interpolation DAC is one cycle of the linear phase signal. This is accomplished by the NMOS multiplexer which chooses between the desired cycle and a reference voltage value (figure 6). The first part of figure 6 is the required cycle while the second part of the figure represents the reference voltage. The reference voltage is responsible for turning off the current cell outside the desired cycle.

The 16 current source outputs of the nonlinear interpolation DAC are shown in (figure 7). The output depends on the switched-on current cell. The output from the course DAC is represents in (figure 8) . The output of the interpolation DAC is then added to the course DAC output to form the desired output wave (figure9). The shape of fine interpolated signal will change according to the rising edge or falling edge by xoring it with the most significant bit.

The synthesized frequency equals to $F_{clk}/1024$, with clock frequency of 1 GHz. The Spurious Free dynamic range (SFDR) was -49dBc, and the dominant spur is the 2nd harmonic as shown in (figure 10).

Using a simple low pass filter at the output, a smooth signal was obtained (figure 11). By applying higher clock frequencies the course output was reasonable but the fine output was poor due to limitation of the XOR gate.

CONCLUSION

A novel DAC was introduced based on nonlinear interpolation. The DAC desgin is of moderate complexity. The output frequency is $f_{clk}/1024$ for f_{clk}= 1GHz with SFDR > -49dB. The output frequency is about double the published designs having approximately the same SFDR.

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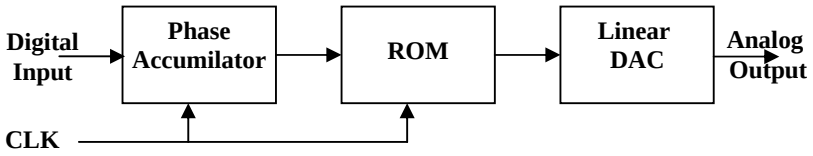

Fig.1. Conventional DDFS

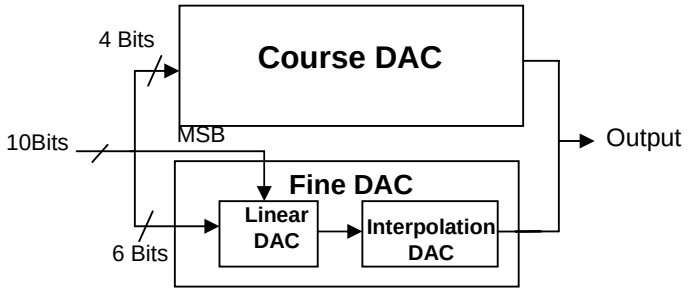

Fig.2. Proposed DAC Architecture

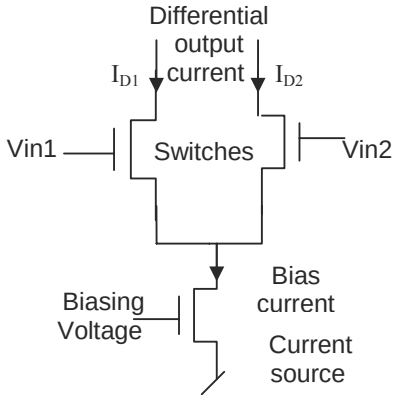

Fig. 3 Current Cell

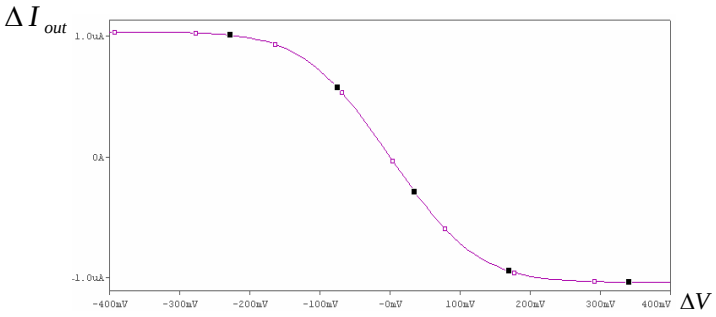

Fig. 4 Relation between differential input and differential output current

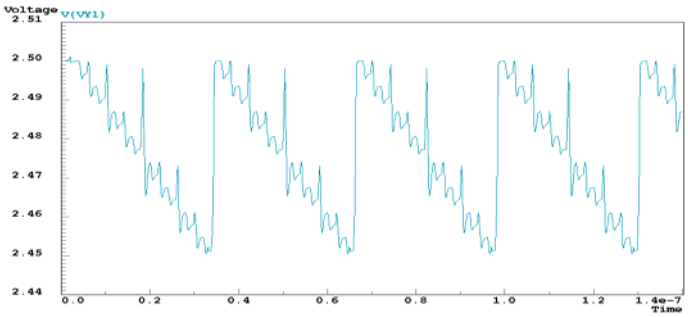

Fig. 5 output of the linear DAC

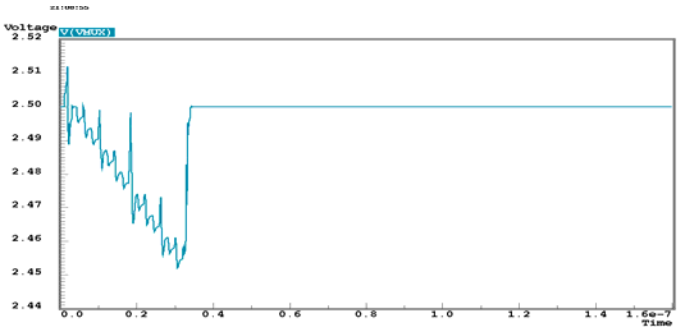

Fig. 6 Output of the multiplexer

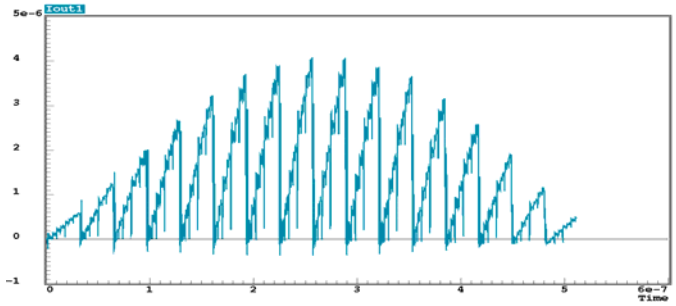

Fig. 7 Output of the interpolation DAC

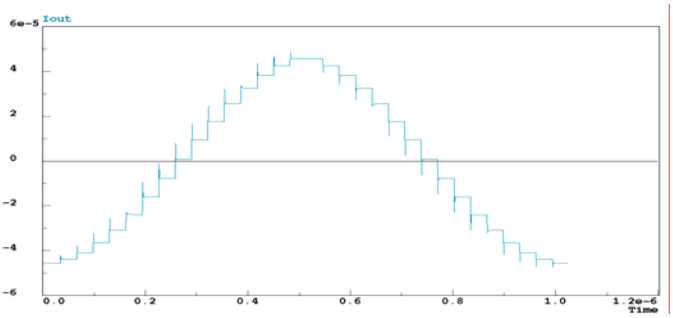

Fig. 8 The output of the course DAC

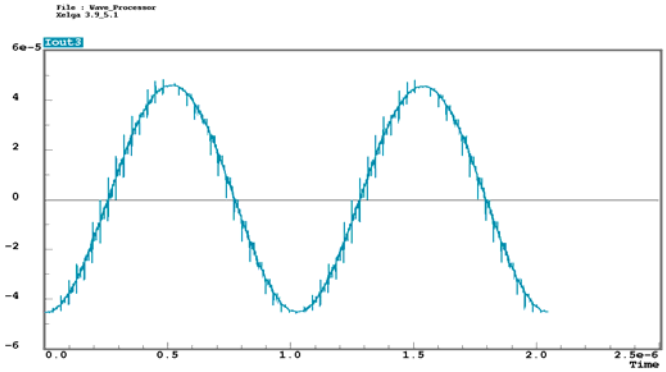

Fig.9 Combined Output

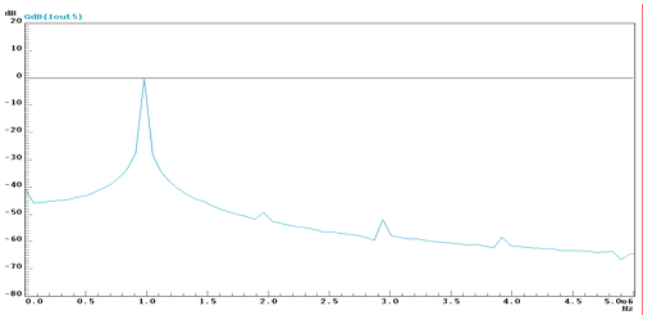

Fig.10 Spurious Free Dynamic Range

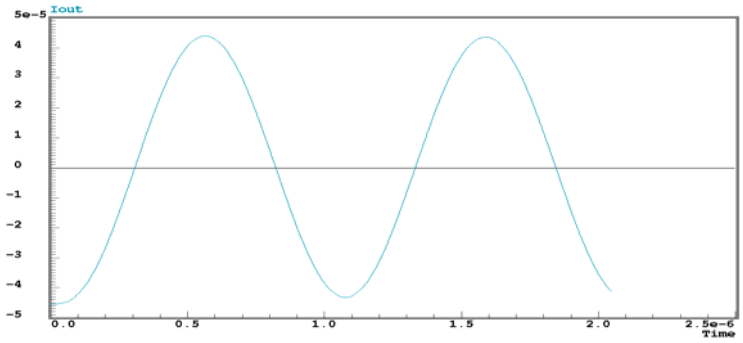

Fig. 11 Output signal after LPF