SOFT-SWITCHING SOLID STATE TRANSFORMER (S4T)

A Thesis
Presented to
The Academic Faculty

by

Hao Chen

In Partial Fulfillment
of the Requirements for the Degree
Doctor of Philosophy in the
School of Electrical and Computer Engineering

Georgia Institute of Technology
December, 2016

SOFT-SWITCHING SOLID STATE TRANSFORMER (S4T)

Approved by:

Dr. Deepak M. Divan, Advisor
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. Maryam Saeedifard
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. Thomas G. Habetler
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. Ronald G. Harley
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. J. Rhett Mayor
School of Mechanical Engineering
Georgia Institute of Technology

Date Approved: 10/03/2016

Dedicated to

my beloved parents

ACKNOWLEDGEMENTS

My journey of doctoral study at Georgia Tech has never been short of amazing experiences and great challenges. Without the inspiration, support, and advice from many people, these challenges could never have been conquered and no milestones of the journey could have been reached. This thesis is a result of the many experiences that I gained from these people, to whom I would like to express my acknowledgements.

First and foremost, I would like to extend my deepest gratitude to my advisor, Dr. Deepak Divan, for his encouragement, inspiration, and guidance throughout my doctoral study. Working on several projects under his support helped me to obtain valuable skills and confidence. He has been always instrumental in giving prompt suggestions whenever I sought guidance from him. The most valuable experience I learned from him is to know the importance of identifying problems, rather than just understanding how to solve them. It is my great honor to be one of his students and to be part of the newly-established Center for Distributed Energy at Georgia Tech that is directed by him. I sincerely believe that the fruitful experience I gained from him will continuously benefit me during my coming career as an engineer.

Further, I would like to extend my sincere thanks to my committee members Dr. Thomas Habetler, Dr. Maryam Saeedifard, Dr. Ronald Harley, and Dr. Rhett Mayor for squeezing the time out of their busy schedules to provide their valuable suggestions and feedback for my thesis.

Particularly, I would like to thank Dr. Ronald Harley for his support and guidance at the early stage of my PhD studies. His careful guidance and persistent attitude on advising students, doing research, and serving in academia have been highly beneficial to me. I am

also grateful to Frank Lambert for all his support and guidance while I was working on several projects at NEETRAC. Especially helpful to me during this time was Suresh Sharma, who has given me great encouragement and valuable advice at the end of my doctoral program and during my job hunting process.

I very much appreciate my colleagues Prasad Kandula, Anish Prasai, Amrit Iyer, Rohit Moghe, and Frank Kreikebaum, for their help in carrying out experiments, writing papers, and sharing knowledge.

Sincere thanks should also go to my friends Liang Du, Yi Du, Dawei He, Zhaoyu Wang, Nan Liu, Yi Deng, Heng Yang, Chen Jiang, Liyao Wu, Qichen Yang, Jinyuan Tian, Xiangyu Han, Hang Shao, Jingfan Sun, Chanyeop Park, Sathish Jayaraman, Shreyas Bhalchandra, Kavya Ashok, Nishant Bilakanti for their help, support, and inspiration.

Finally, I would like to express my special gratitude to my parents. They have given their sincere support and great encouragement for my PhD study.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

SUMMARY

Galvanic isolation is widely used in power supply networks to provide fault isolation and electric energy transfer between circuits at different potentials without a direct conduction path. Compared to the conventional 50 or 60 Hz low-frequency transformers, a power electronics converter with medium- to high-frequency isolation, which is commonly referred as a solid state transformer (SST), significantly reduces the weight and size by reducing the amount of high-volume magnetic core materials. In addition, the SST provides intelligence of: 1) bi-directional power flow control; 2) reactive power compensation; 3) harmonics isolation and elimination; 4) dc or multi-port interfacing; 5) voltage regulation and sag correction; and 6) fault isolations.

Most of the existing SST topologies are isolated voltage source converters, which have the issues of complex multi-stage structures, large component count, high system loss, and high failure rate of bulky energy storage elements. Advanced topologies for implementing the SST have simple circuit structures with lower component count. However, most of them involve either a complicated control strategy, or severe device loss and stress due to hard-switching conditions and inevitable circuit parasitic elements. Low efficiency and poor reliability are the main issues that hinder replacing the conventional utility transformers by the SSTs. Using emerging wide-band-gap devices such as Silicon Carbide (SiC) devices can lead to faster switching speed and higher efficiency. However, the spikes and resonances caused by parasitic elements are exacerbated due to the high *dv/dt* and *di/dt*.

This dissertation presents a novel soft-switching solid state transformer (S4T) topology, which has the features of:

1) minimal two-stage conversion with low device count;

2) soft-switching features for all devices at full range;

3) four-quadrant operation with voltage buck and boost capabilities;

4) arbitrary power factors and frequencies for the input and the output;

5) eliminating the dc energy storage capacitors to avoid inrush current and improve reliability;

6) fast dynamic response to transients;

7) ease of control to achieve soft-switching operation;

8) flexible configurations for two- or multi-terminal dc, single- and multi-phase ac systems such that acting as a universal converter;

9) modular design to scale to medium voltage and high power levels through series and/or parallel stacking the converter modules.

This dissertation presents the topology and the operating principle. Unique attributes, converter analysis, control, and design considerations of the S4T are also provided.

Various topologies can be derived from the proposed S4T, with the same major operating principles. In this dissertation, two soft-switching dynamic VAr compensators are also presented, one with a three-phase converter bridge structure and the other one with a modular structure. Both topologies achieve full-range soft-switching conditions for all main devices.

The high-frequency transformer is the key element of the SST, which acts as an energy transferring element with high-frequency galvanic isolation. Proper design of the high-frequency transformer is crucial to achieve compact size, low loss, low leakage, and high enough dielectric insulation. As part of the dissertation, the transformer design is presented in detail. For the proposed S4T, a constant dc current is maintained in the transformer

magnetizing inductance, resulting in a dc-biased magnetic flux in the high-frequency transformer. This dissertation also presents a hybrid transformer design technique of using high-frequency magnetic cores and permanent magnets to significantly reduce core volume.

The proposed S4T, which has a modular topology, can also be series and/or parallel stacked. This allows using fractionally-rated devices for high-voltage and high-power applications. Even though stacking of voltage source modular converters has been widely investigated in the past, the research of balance control for series stacking current source converters has not been initiated. The low inertial and strong coupling effect properties of the proposed converter impose more severe challenges for stable operation of the series-stacked converter. As part of the research, a robust multi-loop control strategy is developed to realize voltage and power balance for the series-stacked converter system.

A three-phase 208 V / 10 kVA three-phase S4T is designed and fabricated to experimentally verify the functionality of the proposed topology.

The S4T can find a wide range of applications such as dc energy storage interface, uninterruptible power supply (UPS) systems, electrified transportation, space and weight critical applications, smart distribution systems, flexible AC transmission systems (FACTs), and high voltage direct current systems (HVDC).

CHAPTER 1: INTRODUCTION AND RESEARCH OBJECTIVES

1.1. Galvanic Isolation in the Electric Grid

Galvanic isolation has been widely used in power supply networks to provide fault isolation as well as electric energy transfer between circuits at different potentials without a direct current flowing path. In the electric grid, power transformers of 50 or 60 Hz frequency are deployed to step up the voltage at generation for efficient, long distant electricity transmission and to step it down at the distribution system for customer use. In 2010, the U.S. demand for large power transformers, which are rated above 60 MVA, was 127,309 MVA, valued at more than $ 1 billion [1]. Fig. 1.1 represents the historical annual installment of large power transformers in the United States, not including replacement demand [1]. It can be seen from the figure that the need for large power transformers has been growing steadily since 1999, after a low investment period in 1990s.

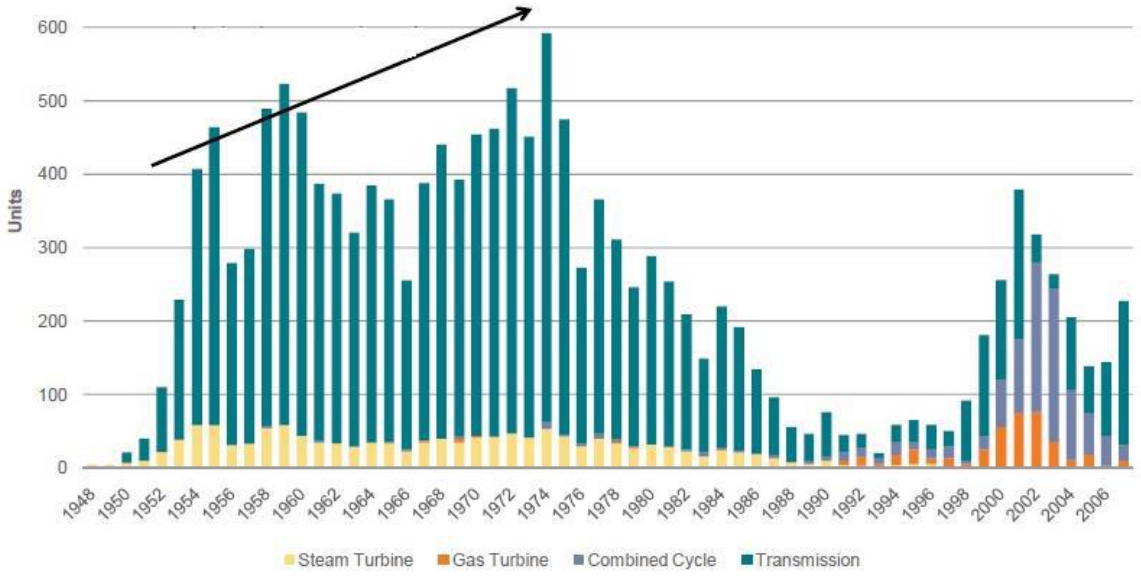


Fig. 1.1: Yearly installment of large power transformers in the United States from 1948 to 2006 [1].

The low-frequency transformer deployed in the grid, although proven reliable, efficient, and cost effective, has a high volume of steel that makes the transformer very bulky. The large dimensions and heavy weight pose unique requirements for safe transportation. In addition, the lack of intelligence makes dynamic control of the grid more challenging. The

distributed and renewable energy sources, which nowadays have a high penetration level, require additional power converters with proper galvanic isolation when connecting to the grid. Fig. 1.2 and Fig. 1.3 shows the U.S. total installed capacity and generation for wind and solar respectively [2].

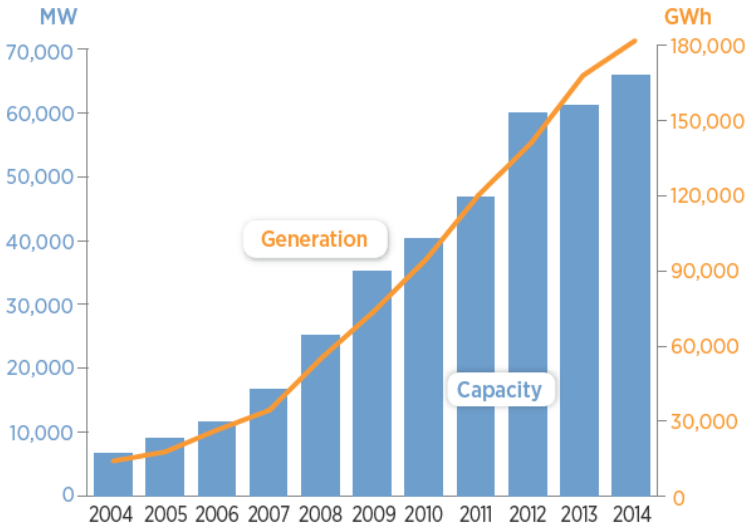


Fig. 1.2: U.S. total installed wind electricity capacity and generation [2].

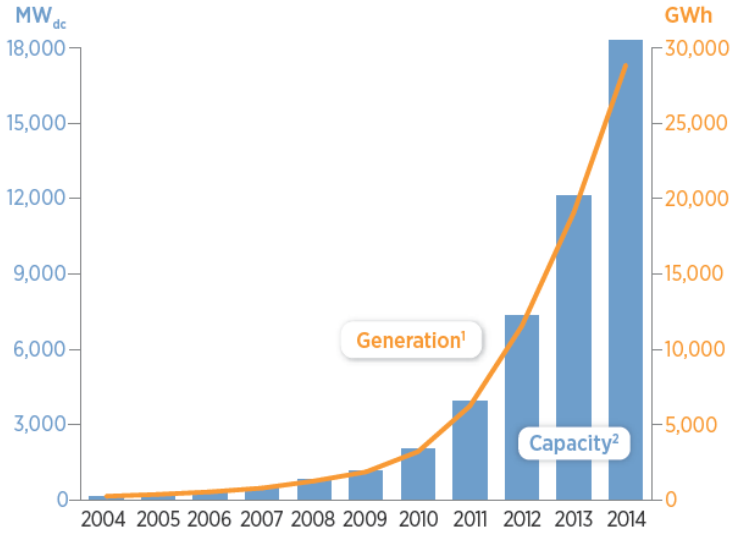


Fig. 1.3: U.S. PV electricity installed capacity and generation [2].

1.2. Solid State Transformer

The idea of a solid state transformer (SST) has attracted tremendous interest for almost five decades, ever since the principles of power conversion were first understood. The SST

is a combination of a high-frequency transformer link and solid state switching circuits. High-frequency isolation allows for the saving of significant volume and weight of magnetic materials. In addition, the SST introduces features that include, but are not limited to: 1) bi-directional power flow control, 2) reactive power compensation, 3) harmonic isolation and elimination, 4) dc or multi-terminal interfacing, 5) voltage regulation and sag correction, and 6) fault isolation. The promise of replacing numerous existing 60 hertz transformers, with a power-electronics-based device that is smaller, controllable, and more flexible, has an undeniable appeal. However, the reality has been much more challenging. It has proven difficult to match the low cost ($25/kVA), high efficiency (>97%), and long life (40 years) of the 60 hertz grid-connected transformer. Further, the practical challenges posed by fault current coordination (>10 kA) with downstream switchgear, and, for transformers connected directly to the 13 kV grid (or higher), the need for 120 kV (or higher) basic insulation level, seem well beyond the capability of cost-effective state of the art power conversion technology.

In more specific applications, the potential for SST's is real. Unidirectional ac/dc converters with high-frequency isolation are really switched mode power supplies, and should not be included in the family of solid state transformers. An SST should convert ac (or dc) voltage to another ac (or dc) voltage with galvanic isolation between the input and output, possibly at a different voltage level and/or frequency, and should inherently be able to provide bidirectional control of real and/or reactive power flows. Applications include locomotives, light rail, EV fast chargers, PV inverters, and battery energy storage systems – many of them emerging fields. It could also include specialized bidirectional drives where 60 hertz isolation transformers are often used to manage noise and transient injection into long cables or motors, along with converters to condition the voltage applied to the motor. With all the above potential applications, the global SST market is expected to be valued at more than $200 million by 2020 [3].

1.3. Problem Statement

Significant work has been done on implementing SSTs. These can typically be classified as single-stage with ac switches on the input and output, connected with a high-frequency transformer, two-stage with an ac/dc converter followed by an inverter, and three-stage based on ac/dc-dc/dc (including isolation)-dc/ac converters in cascade. It has been concluded that the three-stage converter, including a dual-active-bridge (DAB) soft-switched dc/dc converter, offers perhaps the best performance and controllability. Scaling the SST for higher power and higher voltages required for traction and direct grid connected applications, is also seen to be challenging, and has been addressed in many papers.

One of the major restrictions of direct ac/ac types of conversion comes from the leakage inductance of the transformer. At higher frequencies, this becomes the limiting element in the ability to transfer power across the isolation barrier. Factors such as diode reverse recovery can result in energy trapped in the leakage inductance, which in turn causes excessive stress on the components and limits operating range and efficiency. The DAB converter is considered attractive because it handles all real device and transformer parasitic elements, and still allows zero-voltage-switching (ZVS), albeit over a narrow range of voltage transfer ratios. Even for the three-stage SST, assuming that the DAB converter always operates under ZVS conditions, the rectifier and inverter have to operate in hard switching mode and incur high switching losses. Efforts have been spent to address these issues, for instance with resonant switching to reduce losses, or simpler minimal topologies to reduce complexity, but the efforts have always fallen short of addressing the myriad of issues that can limit solid state transformer performance.

1.4. Research Scope and Objectives

This paper presents a new topology for a soft-switching solid-state transformer (S4T), which has a simple and symmetrical architecture, minimal device and component count in the power flow path, with small-rated auxiliary components that enable the soft switching

property. Unlike the DAB converter, the S4T realizes soft switching for all its main devices over the entire load range, and features controlled *dv/dt* and *di/dt* rates. Further, it can realize dc, single- or multi-phase ac on the input/output at arbitrary frequencies and power factors with sinusoidal voltages and low electromagnetic interference (EMI). It shows simple control and benign shut down under fault and failure modes, and is relatively insensitive to key parameters such as transformer leakage inductance. By eliminating components such as electrolytic capacitors, it can also realize higher power density and longer life. Finally, it holds the promise of achieving high efficiency, particularly as it scales up in voltage and power. It provides the simplicity of single-stage SSTs, with the control attributes of the three-stage SSTs, with higher efficiency, lower *dv/dt* rate, and an ability to scale that seems unique.

Two soft-switching dynamic VAr compensators, which are derived from the proposed S4T using the same soft-switching operating principle, are also presented, one with a three-phase converter bridge structure and the other one with a modular structure. Both topologies achieve full-range soft-switching conditions for all the main devices.

The high-frequency transformer is the key element of the SST, which has to be properly designed to meet the objectives of achieving compact size, low loss, low leakage, and high enough dielectric insulation. As part of the dissertation, the transformer design is presented in detail. Apart from conventional transformer design methodology, this dissertation also presents a hybrid transformer design technique of using high-frequency magnetic cores and permanent magnets to significantly reduce the core volume.

The proposed S4T has a modular structure, allowing it to be scaled to high voltage through series stacking. However, the low-inertial and strong coupling properties of the proposed converter impose more severe challenges for stable operation of the series-stacked converters. As part of the research, a robust multi-loop control strategy is developed to realize voltage and power balance for the series-stacked converter system.

1.5. Outline of Chapters

Chapter 2 provides an overview of existing solutions for implementing the SST. It first summarizes the high-frequency isolation links for various topologies based on the functional difference. Then it gives a review of topologies for all types of conversion, including dc to single-phase ac, dc to three-phase ac, single-phase to single-phase ac, single-phase to three-phase ac, three-phase to three-phase ac, and multi-port power conversion. Comparisons for various topologies are also presented in this chapter.

Chapter 3 introduces the topology and operating principle of the Dyna-C, which is a minimal topology for implementing the three-phase SST. Various issues associated with hard-switching conditions are discussed.

Using wide-band-gap devices such as SiC is becoming prevalent in the design of efficient power converters. It seems to be able to address several issues of the hard-switching Dyna-C, and meanwhile makes it feasible to design the converter for medium voltage. However, many issues will arise due to the extreme high *di/dt* and *dv/dt* rates. Chapter 4 discusses and analyzes all these issues, and presents the necessity of designing the converter with soft-switching techniques.

Chapter 5 presents the proposed topology of the zero-current-switching solid state transformer. Principles of operation, simulation results, and some discussions are provided.

Chapter 6 proposes the topology of the zero-voltage-switching solid state transformer, named as S4T. A ZVS auxiliary resonant circuit is first proposed to achieve ZVS operation for current source converters, and then the ZVS SST topology is presented. Compared to the ZCS one, it shows more attactive benefits, and thus a prototype will be developed based on this topology. Various topology variations are also presented. Principle of operation and unique attributes are discussed.

Chapter 7 gives the analysis and control strategy for the S4T. Chapters 8 and 9 discuss the converter design and the high-frequency transformer design for the S4T, respectively. Chapter 10 presents the simulation and experimental validation from a 208 V/ 10 kVA S4T

unit. The unit design and the testing system are discussed, and experimental results are presented. As an extended application, the S4T is also operated as a low-voltage three-phase dynamic VAr compensator, whose operation is demonstrated with the fabricated S4T unit. Chapter 11 presents the converter operating principle under load transients, start-up, shut-down, and fault conditions.

Chapter 12 discusses the scaling to medium voltage through series stacking the converter modules, by using the example of the modular soft-switching dynamic VAr compensator. The converter shows low inertia and strong coupling properties, which impose challenges on stabilizing the series-stacked system. A robust multi-loop control strategy is presented in this chapter to address these issues.

Chapter 13 summarizes the research contribution, and presents recommendations for future work.

CHAPTER 2: REVIEW OF LITERATURE AND PREVIOUS WORK

2.1. Introduction

Since the first SST topology was introduced in 1968 as a single-phase ac/ac isolated matrix converter [4], various alternative topologies have been proposed to implement the SST. These include a multi-stage structure that uses an isolated dc/dc converter to provide high-frequency galvanic isolation, as well as an advanced integrated structure with reduced-stage that performs direct isolated ac/ac power conversion. The high-frequency transformer within these SST topologies works under distinct principles.

This chapter provides an overview of existing solutions for implementing an SST. It first summarizes the high-frequency isolation links for various SST topologies based on the functional difference. Then it gives a review of topologies for all types of conversion, including dc to single-phase ac, dc to three-phase ac, single-phase to single-phase ac, single-phase to three-phase ac, three-phase to three-phase ac, and multi-port power conversion. The topologies to accomplish each of the above conversion types can be classified as a multi-stage topology and a reduced-stage topology. For each type of conversion, multi-stage converters are first presented since it is the most straightforward way to implement the SST. Reduced-stage converters, which typically have more complicated operating principles compared to the multi-stage ones, are discussed afterwards. Scaling to high voltage using fractionally-rated converter cells is discussed. The impact from various parasitic elements such as transformer leakage inductance, parasitic inductance, and the diode reverse recovery issue is described. Comparisons for various topologies are also presented in this chapter.

2.2. High-Frequency Isolation Link

For all isolated circuit topologies, the high-frequency transformer is the energy transfer element that delivers energy from one side of the high-frequency link to another. Based on the operating principle during energy transfer, the high-frequency isolation links can be classified into three types, shown in Fig. 2.1: type I, II, and III. For the type I link (Fig.

2.1(a)), the transformer acts as a normal one that just delivers energy from the primary to the secondary side without temporarily storing any energy. Semiconductor switches, discrete inductors or capacitors, or a combination of them create high frequency ac voltage across the transformer such that the energy can pass through. This isolation link is used in most converters, such as the isolated matrix converter topology. For the type II link (Fig. 2.1(b)), the transformer leakage inductance acts as an energy transfer element. Topologies such as the dual active bridge (DAB) converter have this type link [5]. For the type III link (Fig. 2.1(c)), the transformer magnetizing inductance is used to temporarily store energy, and the transformer actually acts as a coupled inductor for this type. The Dynamic-current (Dyna-C) converter and the partial resonant ac link converter (discussed later in this dissertation) belong to this type.

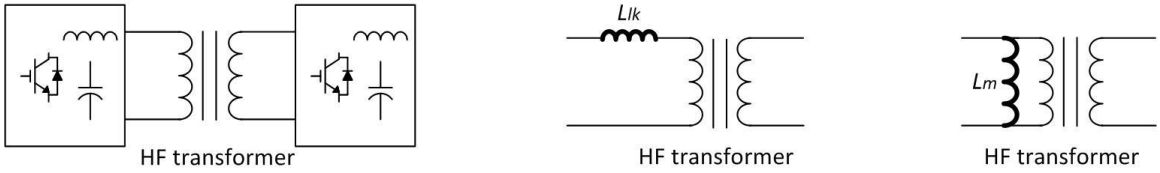


Fig. 2.1: High-frequency isolation links of (a) type I; (b) type II; (c) type III.

2.3. DC to Single-Phase AC Conversion

All topologies for dc to single-phase ac conversion can be classified into two groups. First group is the multi-stage converter consisting of an isolated dc/dc converter and a non-isolated ac/dc converter, in which the first stage provides high-frequency isolation. Second is the single-stage converter which directly accomplishes ac/dc power conversion without an intermediate rectification or inversion. The dc/ac type SSTs have a maximum of two conversion stages, since they do not need the rectification stage required by the ac/ac SSTs.

2.3.1. Multi-Stage Topology

The Multi-stage converter includes a bidirectional synchronous rectifier/inverter and an isolated bidirectional dc/dc converter. The rectifier/inverter interfaces to the ac system while providing adjustable power factor and reduced harmonics, and the high-frequency isolation

is provided by the dc/dc converter. Fig. 2.2 (a) shows the structure of these converters. Five types of isolated bidirectional dc/dc converters can be used here: 1) dual active bridge (DAB) converter; 2) series resonant converter; 3) parallel resonant converter; 4) hybrid series-parallel resonant converter; and 5) LLC resonant converter, with their high-frequency isolation links being shown in Fig. 2.2 (b) to (f).

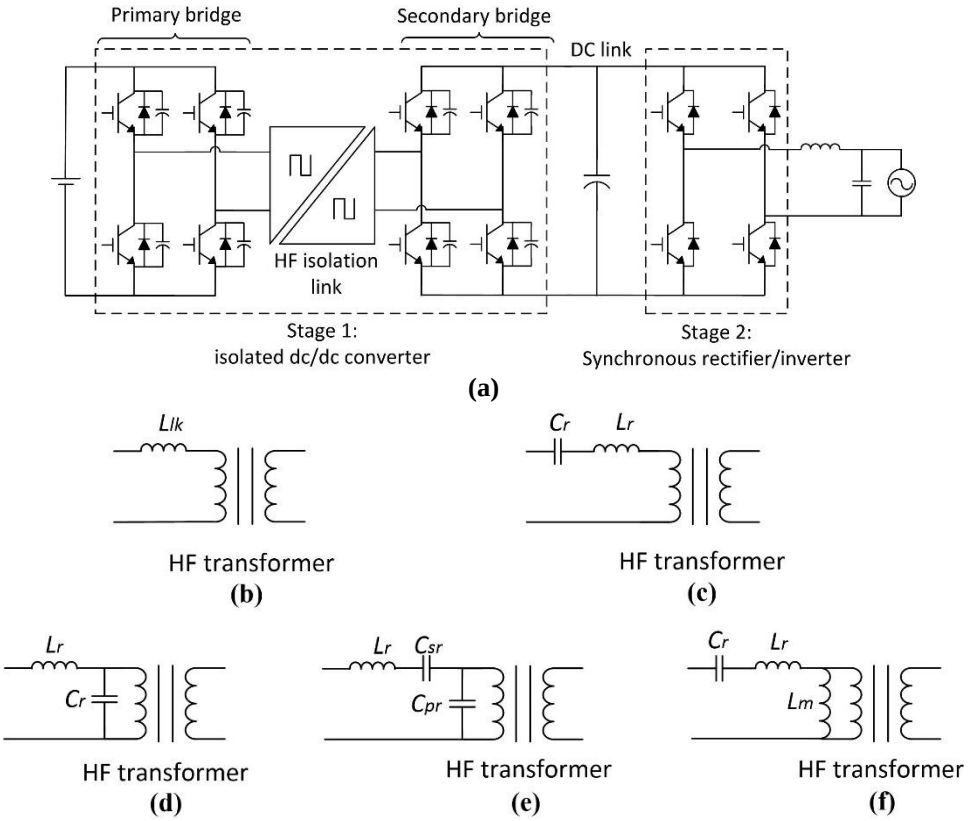


Fig. 2.2: Multi-stage isolated bidirectional dc to single-phase ac converter and the high-frequency isolation links: (a) converter structure; (b) DAB isolation link; (c) series resonant link; (d) parallel resonant link; (e) hybrid series-parallel resonant link; (f) LLC resonant link.

All the above dc/dc converter topologies are bidirectional with soft-switching feature. Among them, the DAB converter is mostly used for ac/dc power conversion [6]. The DAB converter is suitable for high-power applications since the devices do not suffer from high stress to achieve soft switching. Both primary and secondary bridges are switched at a 50% duty cycle with a phase difference between them. The transformer leakage inductance L_{lk} acts as a temporary energy storage element. Fig. 2.3 shows the conceptualized waveforms of the DAB converter. From top to bottom are the waveforms of the voltage applied to the

transformer primary side, the voltage applied to the secondary side, and the current through the transformer.

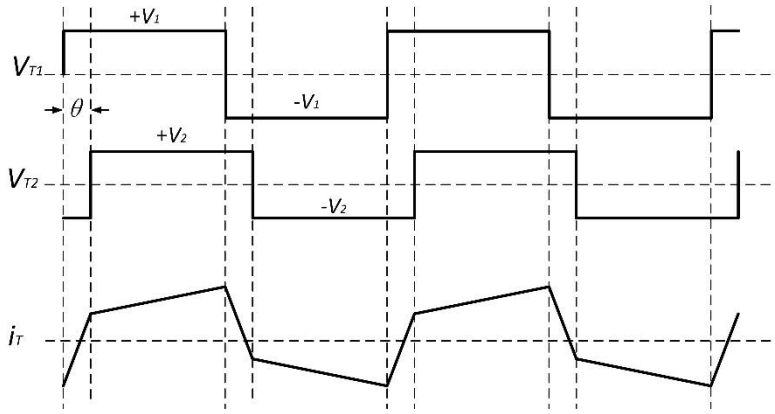


Fig. 2.3: Conceptualized waveforms for the DAB converter.

Unidirectional series, parallel, and hybrid series/parallel resonant converter [7]-[15], in which the secondary bridge is a diode rectifier, are well known topologies for high-frequency dc/dc conversion. When active devices are used for the secondary bridge, the circuit can transfer power in the reverse direction by controlling the firing angle of the devices [10]. The unidirectional LLC resonant converter proposed in [16] has an advantage of wider voltage regulation range over the other types of resonant converters. The bidirectional version of LLC resonant converter was first investigated in [17], and was built for high-power locomotive drive applications in [18]. However, all the four types of resonant converters have to adjust the switching frequency according to the loads, which is different from the DAB converter in which the devices are switched at a constant frequency.

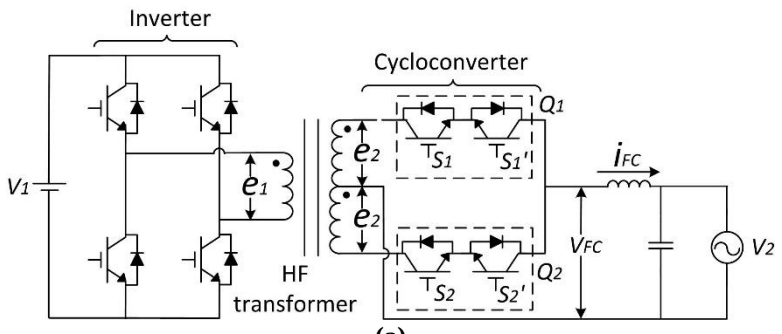
2.3.2. Single-Stage Topology

Being different from the multi-stage converters, single-stage converters directly perform ac/dc power conversion without an intermediate stage of power inversion or rectification. These topologies usually do not have a dc voltage link, and therefore the converter reliability is improved and lifetime is extended by eliminating dc energy storage capacitors. Five topologies were reported in literature: dc to single-phase ac cycloconverter [19], flyback converter [20]-[23], DAB converter [24], isolated partial resonant ac link

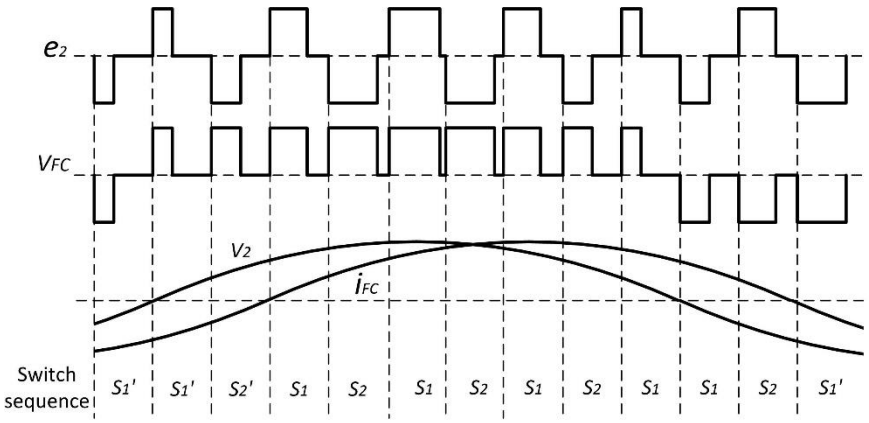
converter [25], [26], and isolated dynamic-current (Dyna-C) converter [27]-[30]. The final two topologies will be discussed later, with their three-phase variation. Their dc to single-phase ac converter topology can be easily configured by just employing two switch legs for both primary and secondary bridges. The operating principles are similar for dc, single-phase ac and three-phase ac sources. Therefore, their operations and controls will be explained in the three-phase ac/ac converter section and will not be repeated here.

DC to Single-Phase AC Cycloconverter

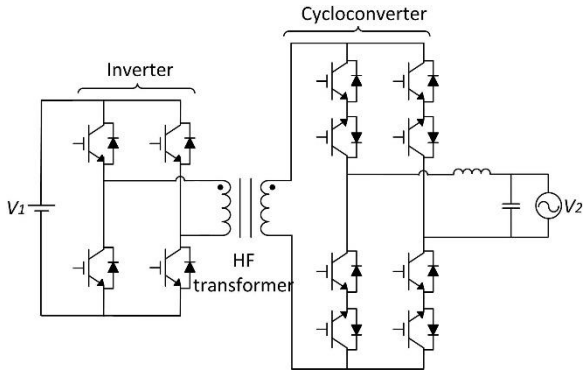
The cycloconverter proposed in [19] is a single-stage dc to single-phase ac topology, as shown in Fig. 2.4 (a). The inverter at the primary side of the high-frequency transformer outputs a pulse-width-modulated high-frequency ac voltage. The secondary-side converter, consisting of two bidirectional switches Q_1, Q_2 and a split secondary winding, converts the high-frequency ac voltage to line-frequency ac. Each of the bidirectional switches Q_1 and Q_2 are composed of back-to-back series-connected switches S_1, S_1' and S_2, S_2', respectively. Fig. 2.4 (b) shows the switching sequence of the cycloconverter. The conducting switch is determined according to the polarities of the transformer secondary voltage e_2, output voltage v_2, and current i_{FC}. Fig. 2.4 (c) shows the full-bridge version of this topology. The half-bridge one requires fewer devices, but with a 2 p.u. voltage rating. Based on the switching sequence shown in Fig. 2.4 (b), it can be seen that the ac side power factor can be adjusted. However, it should be noted that the peak value of the ac voltage cannot be higher than the dc voltage multiplied by the transformer turns ratio; thus it lacks buck-boost capability.



(a)



(b)



(c)

Fig. 2.4: DC to single-phase ac cycloconverter: (a) half-bridge version; (b) switching sequence; (c) full-bridge version.

DC to Single-Phase AC Flyback Converter

This converter, introduced in [20]-[23], is a variation of the flyback dc/dc converter. The circuit structure, shown in Fig. 2.5, consists of two separate flyback converters with four-quadrant switches. For each quadrant operation, the circuit operates under the same principle as the flyback dc/dc converter. Assuming that the power flows from dc to ac side, when the ac voltage is in a positive half cycle, S_4 is kept on while S_1 and S_3 are off. The components of S_2, L_1, L_3, and D_4 make up a flyback converter. S_5 switching is complementary to S_2, blocking D_4 when S_2 is conducting. When the ac voltage is negative, the circuit operates in symmetry of the previous condition. The components S_3, L_2, L_3 and D_5 make up another flyback converter. Similar operating principle can be derived for reverse power flow. The acting switch is controlled with a duty cycle which has a shape of rectified sinusoidal waveform to interface with the ac system. However, this converter has several issues. The

device voltage rating is high since it has to block the voltage of the input and output at off condition. Also, the energy trapped in the transformer leakage, which cannot be transferred from one side of the transformer to another during the bridge-to-bridge transition, has to be managed by a snubber to avoid catastrophic device damage [31], [32]. All the above stated issues prevent this converter from being used for high-power applications.

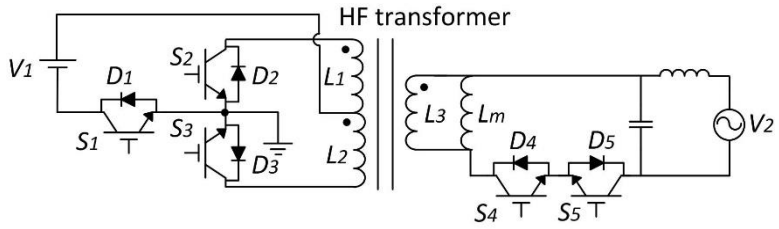


Fig. 2.5: DC to single-phase ac flyback converter.

DC to Single-Phase AC DAB Converter

The topology proposed in [24] is a variation of the dc/dc DAB converter. As shown in Fig. 2.6, it uses bidirectional switches on the ac side such that the voltage polarity can alternate. However, with the conventional phase shift modulation control proposed in [5], the converter has limited ZVS operation range with poor efficiency at no load condition, as discussed in [33]. In [34], by introducing a delayed firing angle between the two legs of the same bridge, the ZVS range is expanded. Other advanced control schemes are also introduced in [35]-[38] to enlarge the ZVS region. However, none of them can achieve the entire range of ZVS operation for both the input and output bridges. It indicates that the dc to single-phase ac DAB converter is only partially soft switching. Besides, the converter has a limited range on the power-input/output voltage ratio plane [37], indicating that the buck-boost capability is restricted.

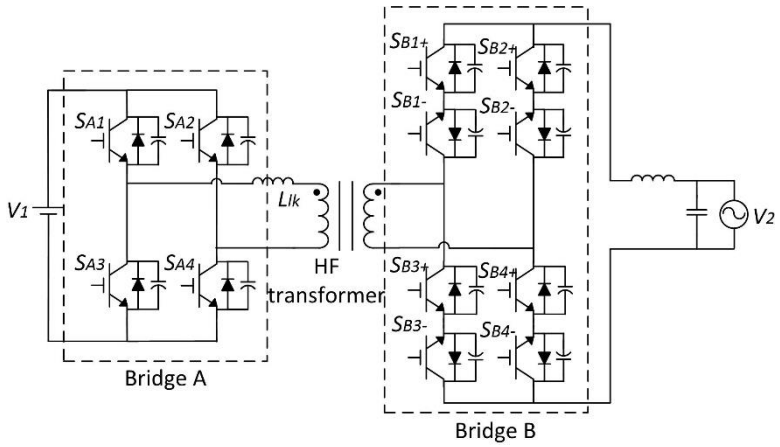


Fig. 2.6: DC to single-phase ac DAB converter.

2.4. DC to Three-Phase AC Conversion

Similar to the dc to single-phase ac SSTs, the topologies for dc to three-phase ac SSTs can be classified into two groups. First group is the multi-stage converter consisting of an isolated dc/dc converter and a non-isolated ac/dc converter. Second is the integrated single-stage converter to directly perform dc/ac conversion. The dc to three-phase ac SSTs have maximum two conversion stages, since they do not need the rectification stage as the ac/ac SSTs.

2.4.1. Multi-Stage Topology

The two-stage dc to three-phase ac converter consists of an isolated dc/dc converter, and a dc to three-phase ac inverter, as shown in Fig. 2.7. The isolated dc/dc converter can be DAB, series resonant, parallel resonant, hybrid series/parallel resonant, or LLC resonant converter.

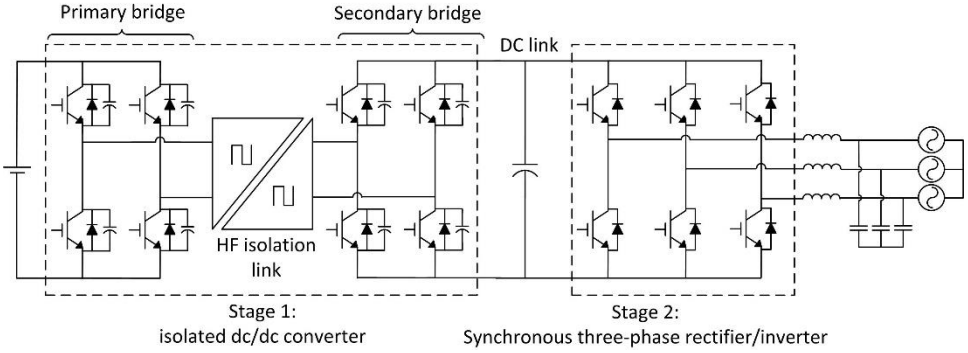


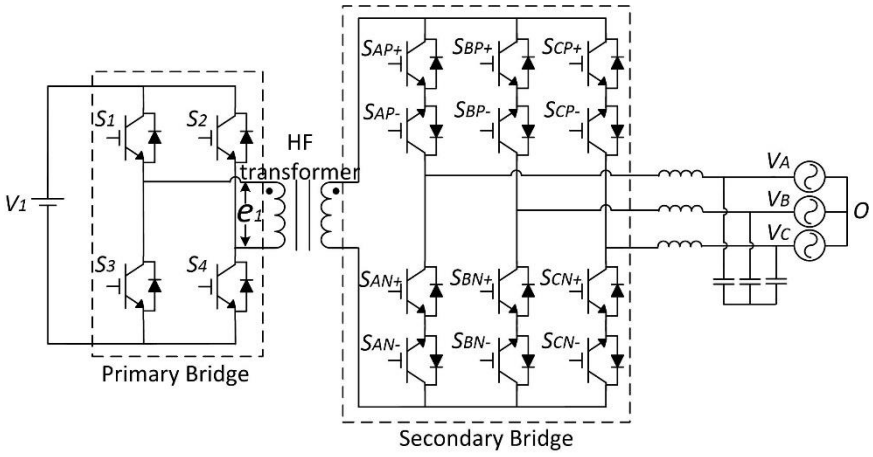
Fig. 2.7: Multi-stage isolated bidirectional dc to three-phase ac converter.

2.4.2. Single-Stage Topology

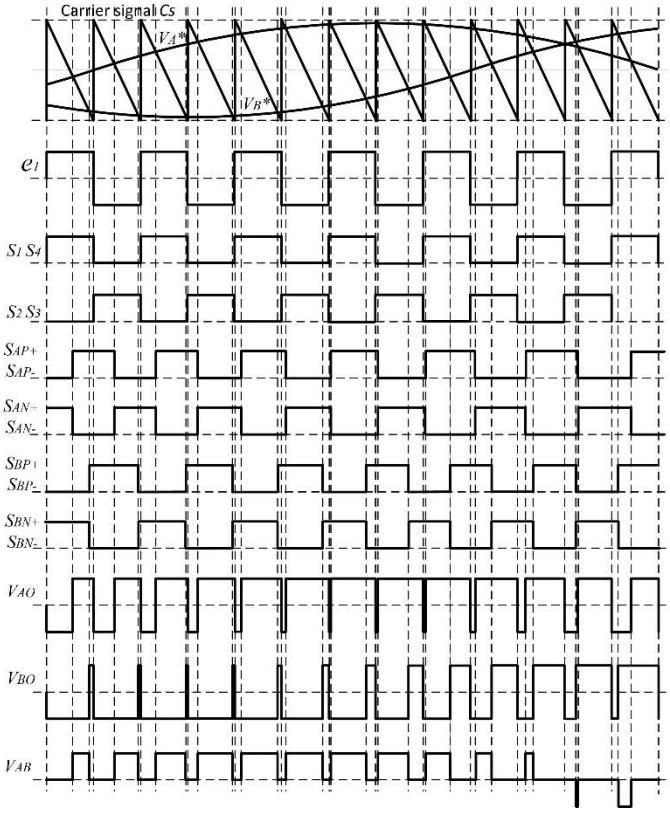
Five typical topologies are found in the literature to implement the single-stage dc to three-phase ac converter, i.e., dc to three-phase ac cycloconverter [39], DAB inverter [40], [41], ac-link converter [42], Dyna-C converter [27]-[30], and partial resonant ac link converter [43]-[45]. The final three topologies operate under a similar operating principle as for the three-phase ac/ac version and they will be discussed later.

DC to Three-Phase AC Cycloconverter

Fig. 2.8 (a) shows the dc to three-phase ac cycloconverter proposed in [39], and Fig. 2.8 (b) shows the switching sequence and relative waveforms for phases A and B. Different from the dc to single-phase ac converter shown in Fig. 2.4, the primary bridge of this converter is controlled with a 50% duty cycle, and the secondary bridge is modulated with a sinusoidal signal. The pulse width modulation (PWM) for the secondary bridge is modified from the conventional PWM modulation for the dc/ac voltage source inverter. The voltage source for the secondary bridge is a 50% duty square-wave ac rather than a constant dc. Therefore, the frequency of the carrier signal C_S is twice that of the switches. Devices S_{AP+}, S_{AP-} and S_{AN+}, S_{AN-} are switched at the intersection of the modulating signal V_A^* and carrier signal C_S, and the devices S_{BP+}, S_{BP-} and S_{BN+}, S_{BN-} are switched at the intersection of the modulating signal V_B^* and carrier signal C_S. The resulting phase voltages V_{AO}, V_{BO}, and V_{AB}, shown in Fig. 2.8 (b), have a sinusoidal fundamental component. A variation of this topology is to have an indirect matrix converter on the secondary side, which has been reported in [46] and will be shown later.



(a)



(b)

Fig. 2.8: DC to three-phase ac cycloconverter: (a) circuit topology; (b) switching sequence and waveforms.

DC to Three-Phase AC DAB Converter

The schematic of the dc to three-phase ac DAB converter, reported in literature [40], [41], is shown in Fig. 2.9. Even though this topology is similar to the cycloconverter shown in Fig. 2.8, the operation is entirely different. The converter operates in a similar way as the DAB dc/dc converter in that primary and secondary bridges have a phase shift with each

other and the transformer leakage inductance L_{lk} acts as an energy transfer element. On the secondary side of the transformer, within one switching cycle, the two phases which have the highest line-line voltage are connected to the transformer while the other phase is idle. The active phases of the secondary side will rotate among phases A, B and C within 360^o of one fundamental cycle. Therefore, the voltage applied to the transformer primary side has a square waveform with a constant amplitude, while on the secondary side the voltage is enveloped by the maximum sinusoidal voltages of the three phases. However, since there is always an idle phase within one switching cycle, strong harmonics filtering on the three-phase ac side is required. Besides, the voltage on the transformer secondary side varies along with the three-phase sinusoidal envelope, thus soft-switching condition cannot be always guaranteed.

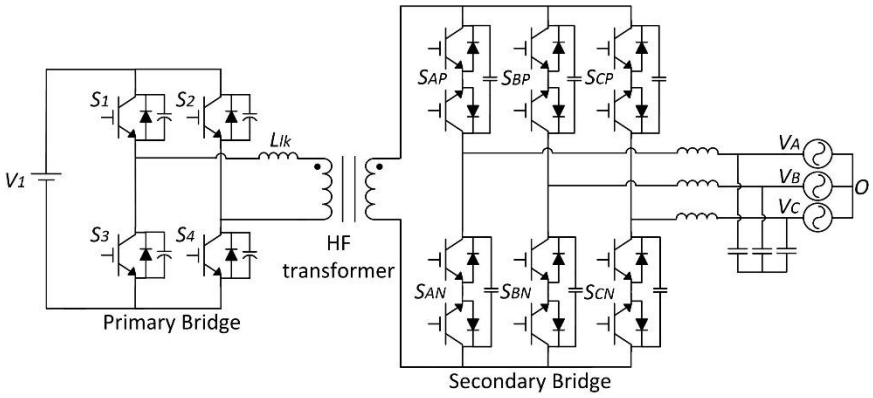


Fig. 2.9: DC to three-phase ac DAB converter.

2.5. Single-Phase AC to Three-Phase AC Conversion

The single-phase ac to three-phase ac converter with high-frequency isolation can be implemented by using an isolated dc/dc converter with three-phase rectifiers and/or inverters, i.e. a multi-stage topology, or an integrated isolated ac/dc converter with a rectifier/inverter, which is a two-stage topology. It should be noted that the single-stage topology of the single-phase ac to three-phase ac converter, without any energy storage components, cannot provide balanced distortion-free ac regulation and is not considered to be viable. This is due to the fact that the instantaneous power on the ac side fluctuates with

twice the line frequency while it is constant on the three-phase ac side. Topologies for single-phase ac to three-phase ac conversion are presented here prior to the single-phase ac/ac, since all these topologies can be used for the single-phase ac to single-phase ac conversion by replacing the three-phase rectifier/inverter with a single-phase version.

2.5.1. Multi-Stage Topology

The multi-stage topology is mostly used due to its power decoupling capability between the input and output, availability of voltage dc link, and control simplicity. The topology, shown in Fig. 2.10, has an ac/dc rectifier, an isolated dc/dc converter providing high-frequency isolation, and a dc/ac inverter. The topology requires two dc capacitors. The isolated dc/dc converter can be any of the types shown in Fig. 2.2.

Several papers have concluded that this three-stage topology offers perhaps the best performance and controllability [75], [76]. The three-stage topology exhibits easy control principle, full decoupling on the input/output, availability of dc link, and soft-switching feature for the middle converter stage. However, the multiple-stage conversion inevitably increases the system loss and complexity. The inverter and the rectifier are switched under hard-switching conditions, and the DAB converter, which is most commonly used for the middle stage, has limited soft-switching range. The reliability of dc link capacitors is also a primary concern.

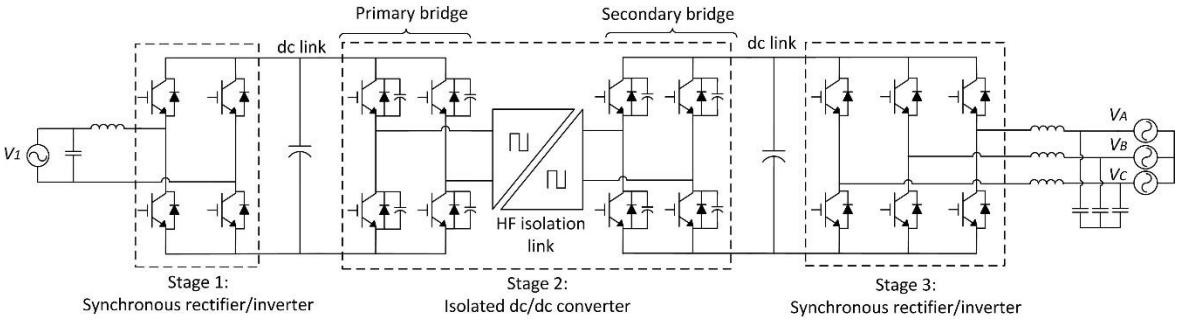


Fig. 2.10: Multi-stage isolated bidirectional single-phase ac to three-phase ac converter.

2.5.2. Reduced-Stage Topology

By integrating the ac/dc rectifier and the isolated dc/dc converter together by using bi-directional devices, the number of conversion stages for single-phase ac to three-phase ac can be reduced. Fig. 2.11 shows such a circuit diagram that was proposed in [47]. It consists of a single-phase ac to dc cycloconverter and a three-phase ac rectifier, as shown in Fig. 2.11. Obviously, in functionality, all other integrated ac to dc converters with high-frequency isolation presented in section 2.3.2 can be used for the ac/dc conversion stage as well.

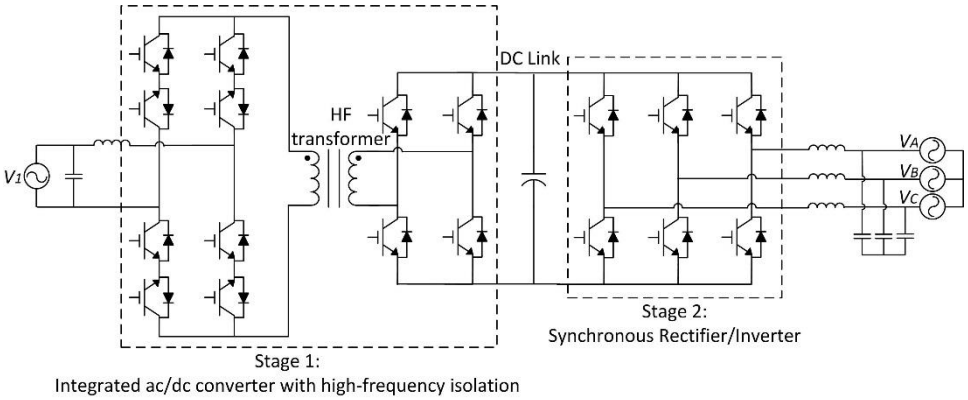


Fig. 2.11: Reduced-stage single-phase ac to three-phase ac converter.

2.6. Single-Phase AC to Single-Phase AC Conversion

2.6.1. Multi-Stage Topology

The multi-stage circuit for single-phase AC to single-phase AC conversion, discussed in [48], is similar to the single-phase ac to three-phase ac converter shown in Fig. 2.10 and Fig. 2.11, except that the three-phase ac rectifier/inverter is replaced by a single-phase version. The reduced-stage converter, discussed in [49], consists of a rectifier and an integrated isolated dc/ac inverter as shown in Fig. 2.6. Due to great similarities to the single-phase AC to three-phase AC conversion, detailed topologies for single-phase ac/ac are not repeated here.

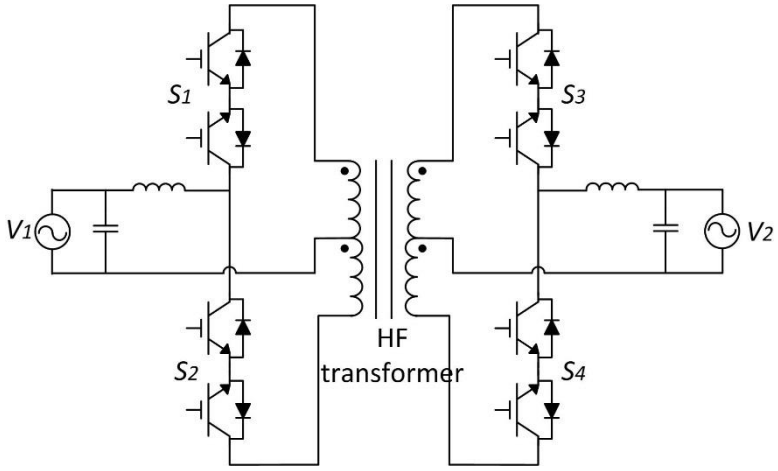
2.6.2. Single-Stage Topology

The following single-stage topologies for single-phase ac/ac conversion are discussed in this section: single-phase ac/ac cycloconverter, ac/ac flyback converter, and ac/ac DAB

converter. It should be noted that, due to the absence of the dc link, all these single-stage topologies can only provide voltage step-up and/or -down capability. It can neither realize frequency conversion nor achieve independent reactive power control. From this point of view, the single-stage topologies for single-phase ac/ac conversion cannot fulfill all the SST functionalities.

Single-Phase AC/AC Cycloconverter

The topology proposed in [4], [50], shown in Fig. 2.12 (a), is recognized as the first SST topology. Even though it is a cycloconverter, its operating principle is similar to that of the DAB converter. The bidirectional devices S_{11} and S_{12}, S_{21} and S_{22} on the primary and secondary sides are switched in a complementary mode with a 50% duty cycle, while the output voltage is regulated by a phase shift angle θ between the primary and secondary bridges devices. The related waveforms and switching sequences are shown in Fig. 2.12 (b). Fig. 2.12 (c) is the full bridge version proposed in [51], in which the number of devices is doubled with a single-winding for the primary and secondary sides of the transformer. However, the device voltage rating is only half that of the half bridge version.



(a)

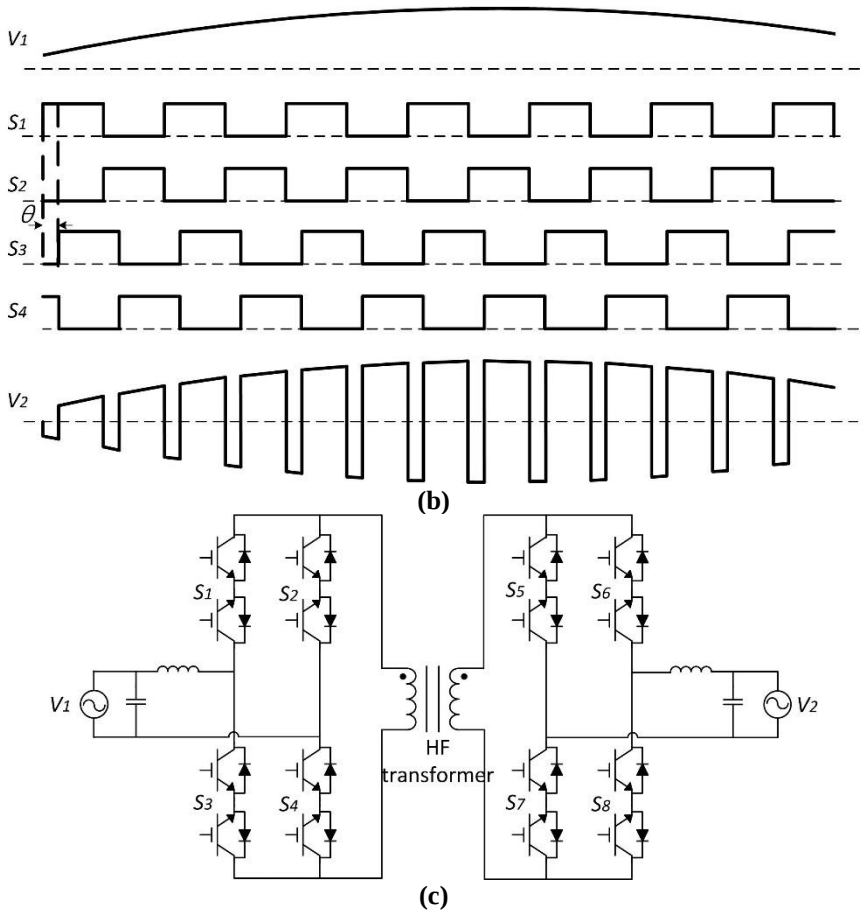


Fig. 2.12: Single-phase ac to ac cycloconverter: (a) half bridge topology; (b) switching sequence and waveforms; (c) full bridge topology.

Single-Phase AC/AC Flyback Converter

The topology of the flyback ac/ac converter, proposed in [52], [53], is similar to the flyback dc/ac converter shown in Fig. 2.5, except that the secondary side has a single winding with bidirectional switches. Fig. 2.13 shows the topology of this converter. The converter works as a conventional flyback dc/dc converter for each quadrant operation.

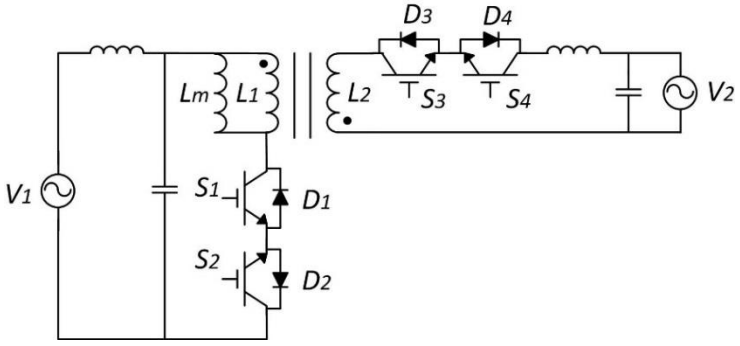


Fig. 2.13: Single-phase ac to ac flyback converter.

Single-Phase AC/AC DAB Converter

The single-phase ac/ac DAB converter was first proposed in [54], and the topology is shown in Fig. 2.14. Both of the primary and secondary sides are configured with bidirectional switches such that the four-quadrant operation is feasible. Its operation is similar to that of the DAB dc/dc converter except that accurate switching commutation for four quadrants devices needs to be accomplished. However, the switching of the devices in this converter goes to a hard-switching mode under some operating conditions. Therefore, as discussed in [55], a commutation scheme permitting seamless transition between soft-switching and hard-switching conditions is required.

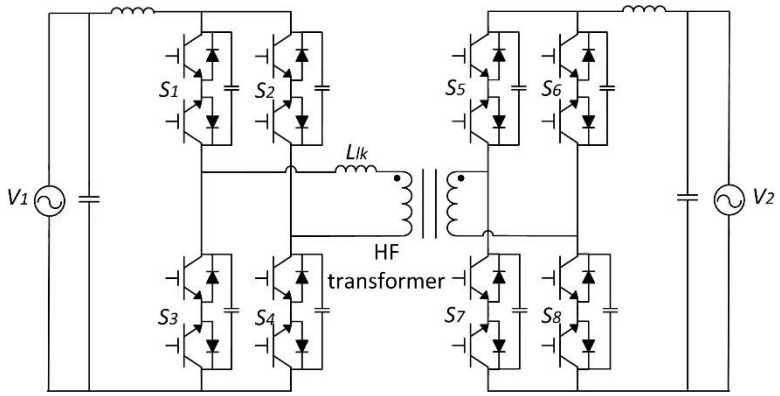


Fig. 2.14: Single-phase ac to ac DAB converter.

2.7. Three-Phase AC to Three-Phase AC Conversion

2.7.1. Multi-Stage Topology

The multi-stage topology consists of a three-phase ac/dc rectifier, an isolated dc/dc converter, and a dc/three-phase ac inverter, as shown in Fig. 2.15. The DAB dc/dc converter is widely used for high-frequency isolation since it is suitable for high-power applications. This topology is the most straightforward way to implement the SST with the features of easy control, decoupled input/output regulation, and availability of dc links. A 270 kVA converter design using this architecture is described in [56].

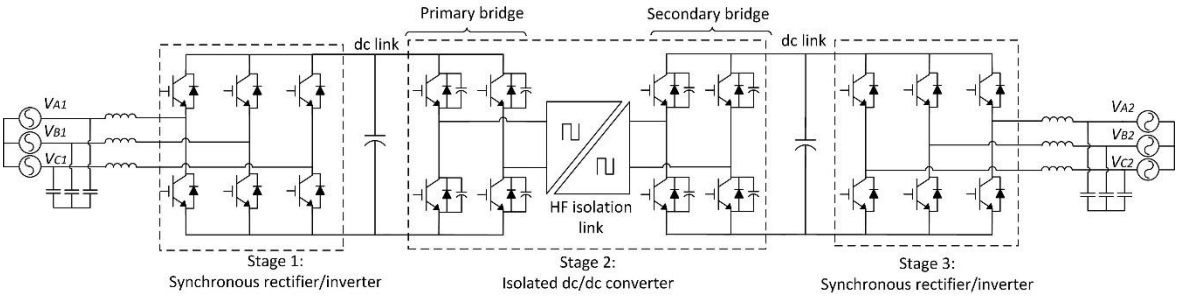


Fig. 2.15: Multi-stage isolated bidirectional three-phase ac to three-phase ac converter.

Another option is to use three of the three-stage single-phase ac/ac converters, one converter for each phase, as proposed in [57] and shown in Fig. 2.16. Compared to the topology of Fig. 2.15, this topology performs ac/ac conversion for each phase individually. The neutral connection on the input and output sides can easily accomplish the unbalanced three-phase power transfer. The isolated dc/dc converter stage again can be implemented by the DAB converter or any other isolated resonant dc/dc converter. The modularity of this option also allows scaling to high voltage. Apparently, this solution has a higher device and component count when compared to the topology of Fig. 2.15.

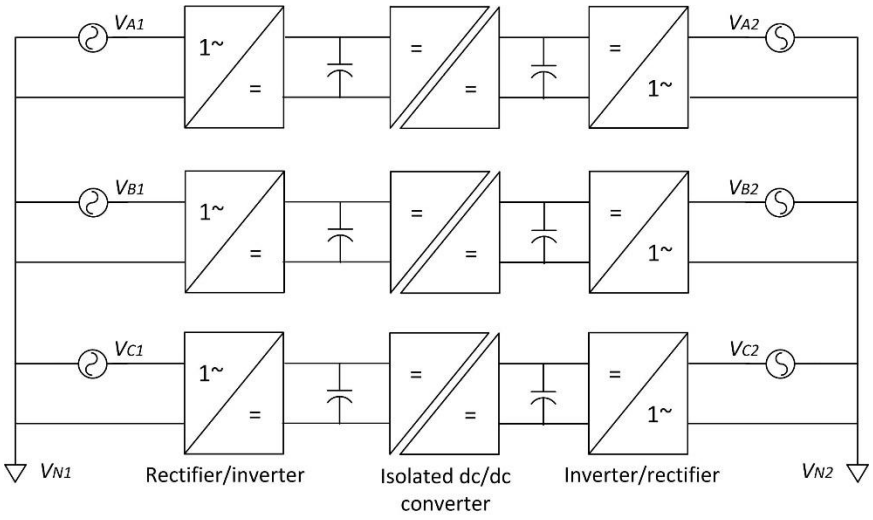


Fig. 2.16: Three-phase ac/ac topology using single-phase ac/ac converter modules.

The two-stage topology for three-phase ac to three-phase ac conversion utilizes the integrated ac/dc converters with high-frequency isolation, thus eliminating some of the dc voltage links. The two-stage topology for three-phase ac to three-phase ac conversion is

similar to the topology for single-phase ac to three-phase ac except that the single-phase rectifier/inverter is changed to a three-phase version.

2.7.2. Single-Stage Topology

Single-stage topologies for three-phase ac/ac conversion transfer power directly through the high-frequency transformer without any intermediate dc link. The topologies presented in this section include direct and indirect isolated matrix converters [60]-[62], three-phase ac/ac flyback converter [63], Dyna-C converter [27]-[30], AC-Link converter [42], [64], [65], and partial resonant ac link converter [25], [26].

Isolated Matrix Converter

The single-stage matrix converter with high-frequency isolation was first studied in [60], and the topology is shown in Fig. 2.17. The converter has three legs on both the primary and secondary bridges. Each converter leg consists of bidirectional devices. The circuit has a symmetrical configuration and requires a total of 24 semiconductor devices. It can perform direct three–phase ac/ac power conversion without intermediate dc energy storage.

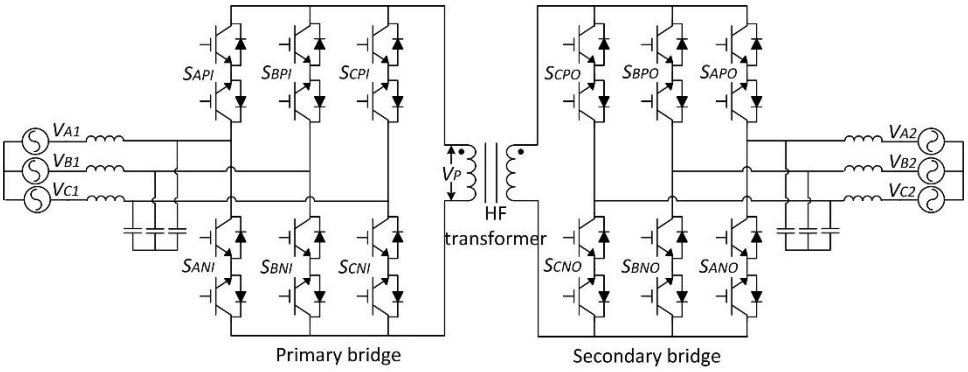


Fig. 2.17: Singe-stage three-phase ac/ac isolated direct matrix converter.

A variation of this converter is the indirect matrix converter, and the configuration of its one side bridge is shown in Fig. 2.18 (b). Compared to the direct matrix converter bridge of Fig. 2.18 (a), the indirect one reduces the semiconductor device count by two. In addition, the bridge can also be configured as the back-to-back converter with a dc link, shown in Fig. 2.18 (c). Even though the circuits of Fig. 2.18 (b) and (c) have great similarities, their operating principles are different due to the absence of dc link capacitors. By combining any

two of the three types of bridges shown in Fig. 2.18, the three-phase ac/ac converter can have nine circuit configurations in total [61]:

i) Primary: direct matrix converter; Secondary: direct matrix converter;

ii) Primary: direct matrix converter; Secondary: indirect matrix converter;

iii) Primary: direct matrix converter; Secondary: back-to-back dc link converter;

iv) Primary: indirect matrix converter; Secondary: direct matrix converter;

v) Primary: indirect matrix converter; Secondary: indirect matrix converter;

vi) Primary: indirect matrix converter; Secondary: back-to-back dc link converter;

vii) Primary: back-to-back dc link converter; Secondary: direct matrix converter;

viii) Primary: back-to-back dc link converter; Secondary: indirect matrix converter;

ix) Primary: back-to-back dc link converter; Secondary: back-to-back dc link converter.

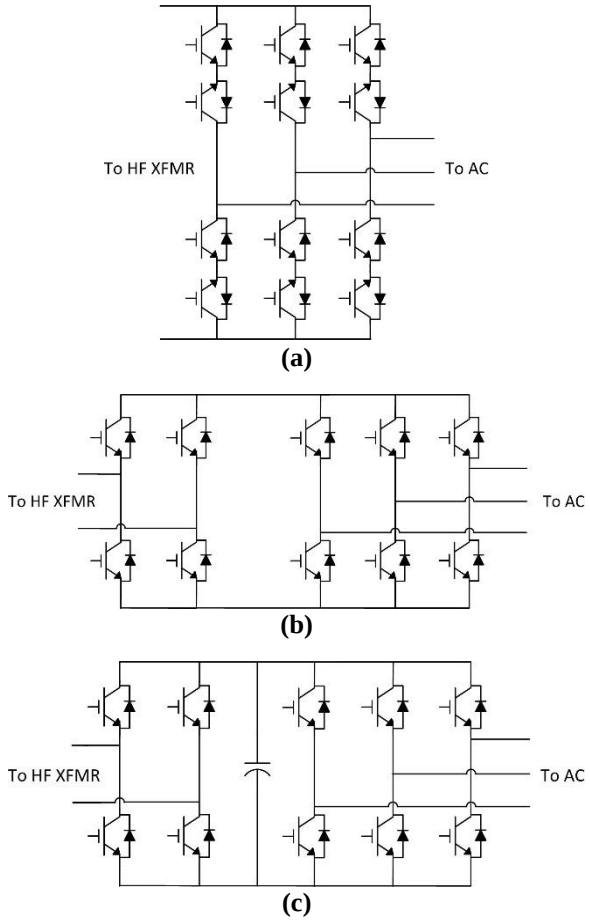


Fig. 2.18: Three types of bridge configuration: a) direct matrix converter; b) indirect matrix converter; c) back-to-back dc link converter.

As an example, Fig. 2.19 shows the configuration of type ii), consisting of a direct matrix converter on the primary side and an indirect matrix converter on the secondary side. For the back-to-back dc link converter, the three-phase sinusoidal voltage can be controlled in the same way as for the three-phase voltage source inverter. In the following, the control principle of the direct isolated matrix converter will be presented.

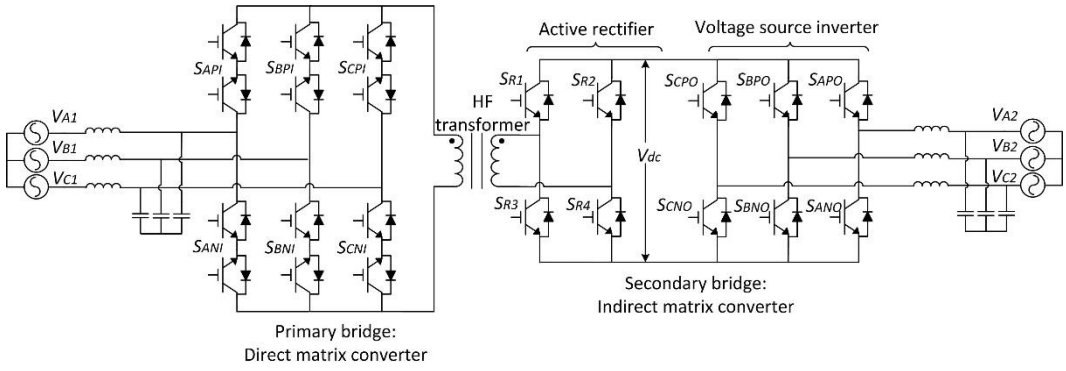


Fig. 2.19: Three-phase ac/ac converter: a direct matrix converter with an indirect matrix converter.

Referring to the topology of Fig. 2.17, the converter can be recognized as a three-phase rectifier on the primary side and an inverter on the secondary with a virtual dc link in between. Flux balance is required for the high-frequency transformer to avoid core saturation. This is achieved by alternatively applying a positive voltage and a negative voltage in two consecutive switching cycles T_S. Fig. 2.20 shows the operating mechanism of the input bridge for an instant when V_{AI} has the largest magnitude with a positive polarity while V_{BI} and V_{CI} have negative polarities, assuming a balanced three-phase input voltage.

For the first switching cycle *1-*T_S when a positive pulse is required, the positive voltage V_{ABI} is applied to the transformer primary winding by turning on S_{API} and S_{BNI} with a duty cycle d_{BI}. Then by turning on S_{CNI} and turning off S_{BNI}, another positive voltage V_{ACI} is applied to the transformer with a duty cycle d_{CI}. For the next switching cycle *2-*T_S, the negative voltages -V_{ABI} and -V_{ACI} are applied by turning on S_{ANI}, S_{BPI}, and S_{ANI}, S_{CPI} respectively. The resulting virtual dc link voltage V_{dc} is shown in Fig. 2.20.

The duty cycle of each device for the primary side is controlled such that sinusoidal currents are drawn from the three-phase voltage source with a desired power factor. The secondary side converter operates in a similar manner to generate three-phase sinusoidal

voltages. From this point of view, the converter can be treated as a current source rectifier cascaded with a voltage source inverter. Therefore, a modified space vector modulation scheme can be utilized to control the converter [62]. A current source space vector modulation is used for the primary side converter, and a voltage source space vector modulation is used for the secondary side converter. As shown in Fig. 2.21 (a), in the first switching cycle *1-T_S*, the reference current vector $\overrightarrow{I_{ref}}$, located in sector 1, is synthesized with the vectors $\overrightarrow{I_1}$ and $\overrightarrow{I_2}$. In the second switching cycle *2-T_S*, the vector $-\overrightarrow{I_{ref}}$, located in sector 4, should be generated using the vectors $\overrightarrow{I_4}$ and $\overrightarrow{I_5}$. The secondary side converter works similarly but with voltage source space vector modulation as shown in Fig. 2.21 (b).

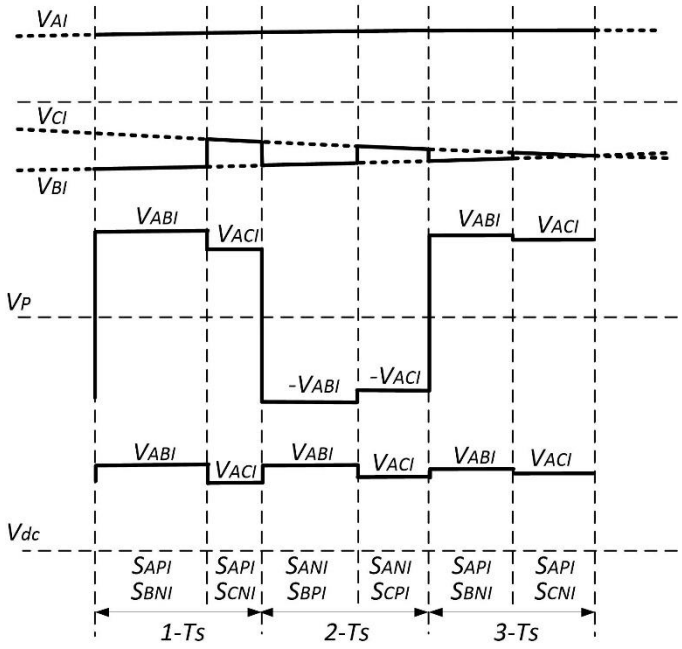
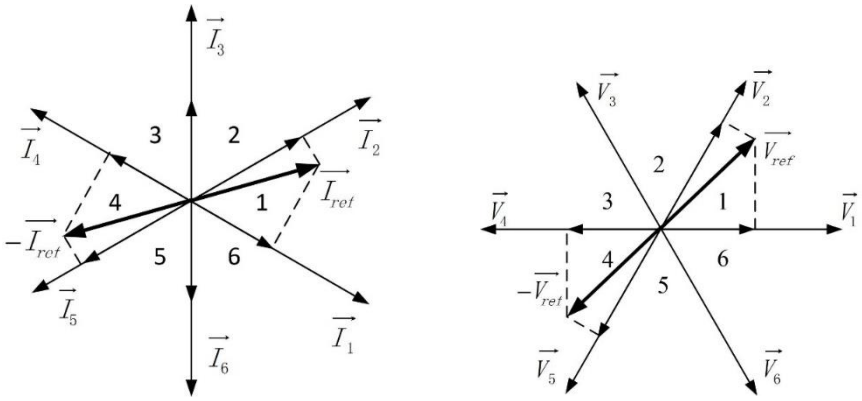


Fig. 2.20: Conceptualized waveforms for single-stage three-phase ac/ac isolated direct matrix converter.



(a) **(b)**

Fig. 2.21: Space vector modulation for single-stage three-phase ac/ac direct matrix converter: a) current space vector for primary bridge; b) voltage space vector for secondary bridge.

If an indirect matrix converter is used on the secondary side, as shown in Fig. 2.19, the device count can be reduced by two. The active rectifier is controlled with a 50% duty cycle signal to provide a dc voltage source for the inverter. In the switching cycle of *1-*T_S when a positive voltage pulse is applied by the primary bridge, S_{R1}, S_{R4} are turned on and S_{R2}, S_{R3} are off. While in the cycle of *2-*T_S, S_{R2}, S_{R3} are turned on and S_{R1}, S_{R4} are turned off. In this way, a dc voltage is maintained for V_{dc} even without dc link capacitors.

Three-Phase AC/AC Flyback Converter

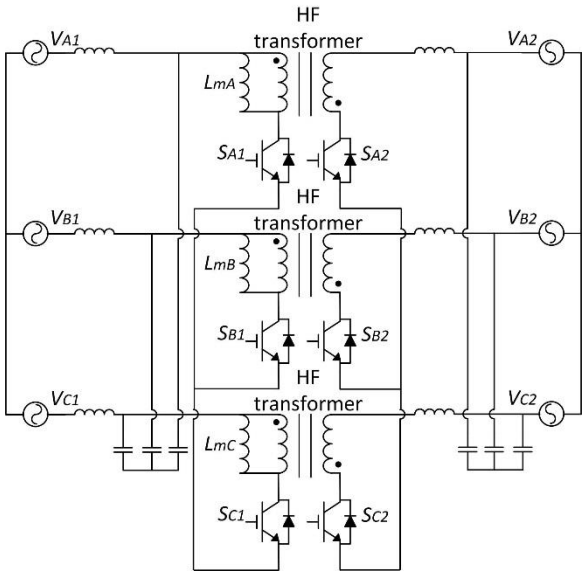


Fig. 2.22: Three-phase ac/ac flyback converter.

The converter topology, proposed in [63] and shown in Fig. 2.22, requires only six devices for bidirectional power transfer. It actually integrates three flyback dc/dc converters for three-phase ac power conversion, one for each phase. Each converter is controlled with a duty cycle *d*, same as for the dc/dc converter. Therefore, the voltage amplitude ratio between output and input is $\frac{d}{1-d}$. However, since the devices used in the topology are unidirectional, compared to the single-phase ac/ac flyback converter of Fig. 2.13, this converter can be only operated in two quadrants. It implies that the input and output voltages must be in phase with each other. Thus it can neither provide frequency conversion nor achieve independent reactive power control. This can be improved by using bidirectional devices of Fig. 2.13. Additionally, the energy trapped in the transformer leakage has to be managed properly with a snubber, which prevents its applications at high power levels.

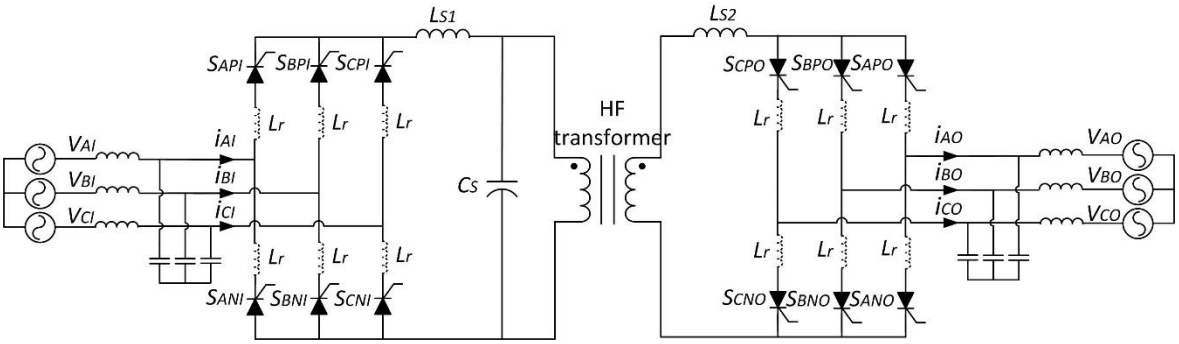
Dyna-C Converter

The Dyna-C converter, proposed in [27]-[30], is a current source converter alike a flyback converter. It realizes a minimal SST topology with 12 devices that can achieve three-phase ac (or dc) /three-phase ac (or dc) conversion, with trapped leakage energy being properly managed. The Dyna-C circuit does exhibit desirable properties in terms of scaling the voltage, and realizing multi-port structures for renewable energy applications. Detailed description of the Dyna-C converter will be covered in chapter 3.

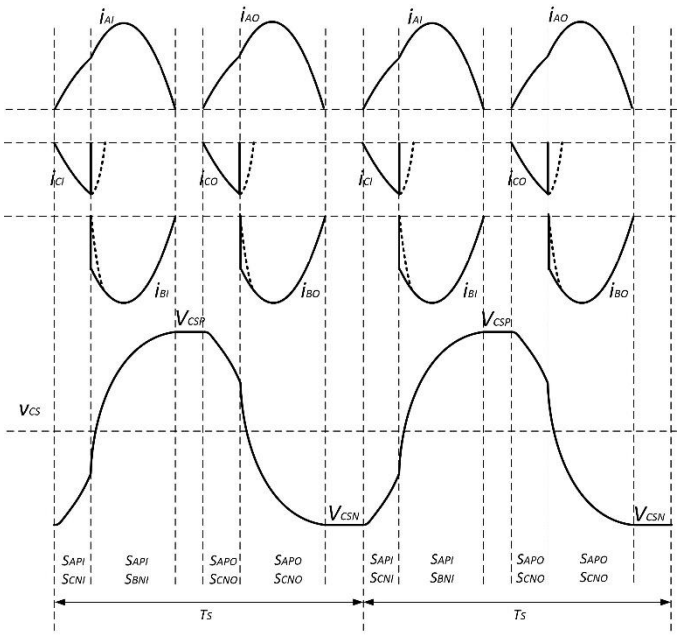
AC-Link Converter

The AC-Link converter, proposed in [42], [64], [65], is a ZCS resonant converter topology. The three-phase ac/ac topology is shown in Fig. 2.23 (a). It can also be configured as a three-phase ac to dc converter by employing two legs on one of the bridges. The input side bridge stores energy in C_S, and L_{S1} and C_S forms a series resonant path during that process. Then C_S releases energy to the output, and L_{S2} and C_S again forms another resonant path for output bridge operation. Since the current through all devices can be self-commuted to zero, indicating ZCS conditions, half-controlled devices such as thyristors can be used. The voltage of the central capacitor C_S has a high-frequency ac waveform due to the charge

and discharge operation. Therefore, a high-frequency transformer can be used for isolation. Fig. 2.23 (b) shows the corresponding waveforms and switching sequences. Assuming an instant when phase A input reference current has a largest value with a positive polarity, and the voltage V_{ABI} is larger than V_{ACI}, the converter operation within one switching cycle starts by turning on S_{API} and S_{CNI}. The capacitor C_S voltage is resonantly charged up with V_{ACI} and L_{S1}, from an assumed initial condition of a negative capacitor voltage V_{CSN}. After enough charge is delivered to phase C, S_{BNI} is turned on while S_{CNI} is self-commuted off since V_{ABI} is larger than V_{ACI}. Then the C_S is charged up again with the voltage of V_{ABI}. This state ends when the current through L_{S1} drops to zero and the voltage of C_S increases to V_{CSP}. As a result, the devices S_{API} and S_{BNI} are self-commuted off. The output bridge operates in a similar manner, and capacitor C_S is discharged to a voltage level V_{CSN} by the output side, concluding one switching cycle. For the operation transition from leg B to C, an inductor L_r can be connected in series with each device, shown as dashed lines in Fig. 2.23 (a), which creates ZCS turn-on conditions for intra-bridge transitions. As a result, the waveforms of the current flowing through each device leg are changed to the dashed lines, as shown in Fig. 2.23 (b).



(a)



(b)

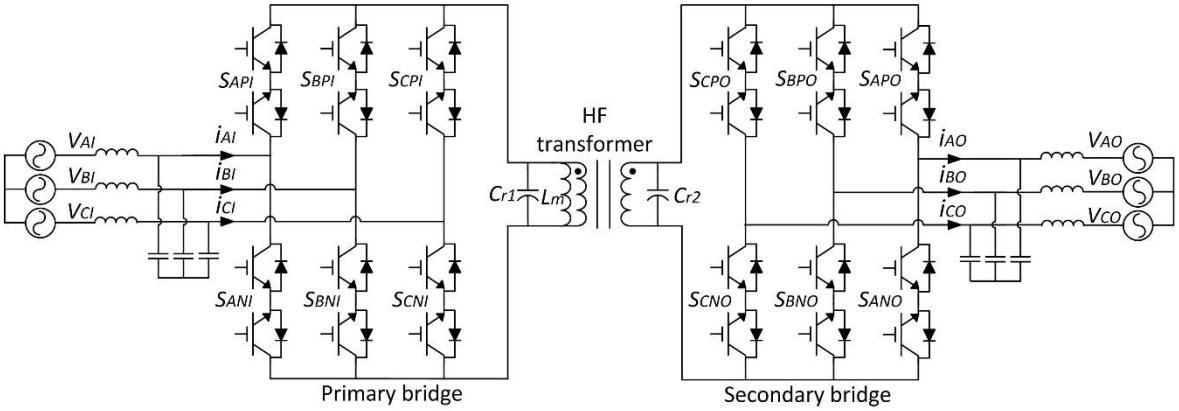
Fig. 2.23: AC-Link converter: a) converter topology; b) relative waveforms and switching sequences.

Even though all devices are switched at ZCS conditions, the resonant operation leads to high current and voltage stresses. The device reverse recovery develops trapped energy in the series connected inductors. Once the device is snapped off, this trapped energy will develop voltage spikes, whose amplitude is determined by the *di/dt* rate during the device recovery period. In addition, the devices triggering-on moments have to be accurately defined over one line-frequency cycle such that sinusoidal currents are generated, which is achieved by a look-up table based control [66]. The switching frequency needs to change according to the power levels. All these make the control strategy extremely complicated.

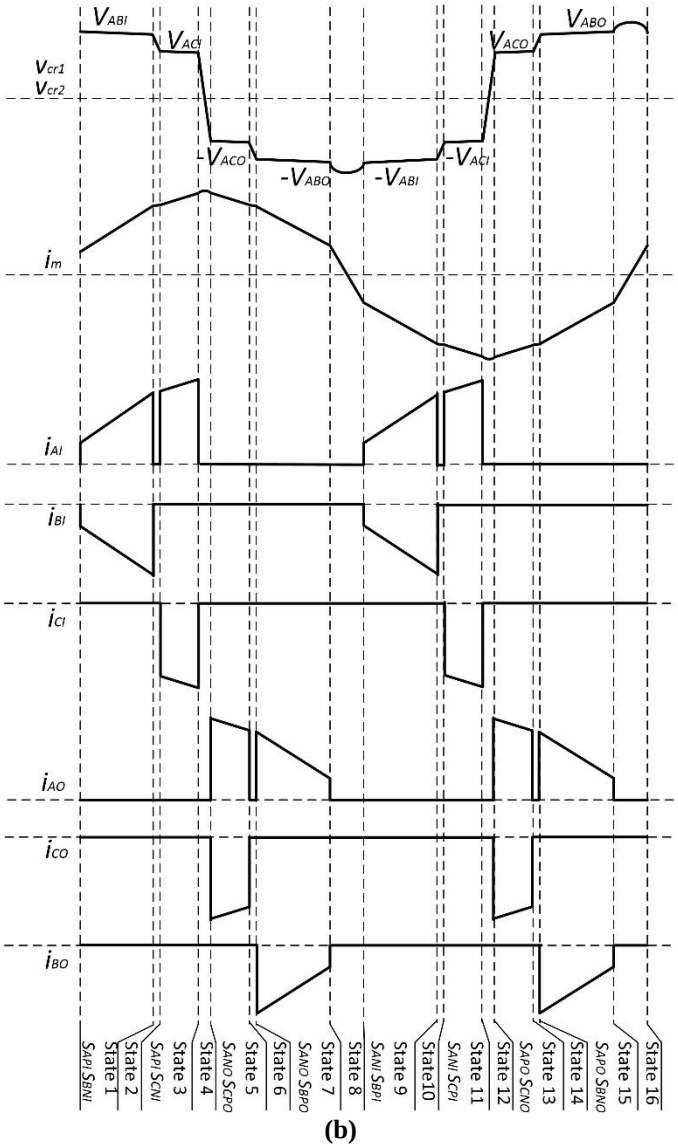
Partial Resonant AC Link Converter

The partial resonant ac link converter, proposed in [25], [26], is a ZVS based current source converter. The three-phase ac/ac topology, shown in Fig. 2.24 (a), requires a total of 24 semiconductor devices, and it can be reconfigured to interface with dc or single-phase ac sources by employing two legs in one bridge. The converter transfers energy from the input to the output through the transformer magnetizing inductance, and the capacitor in parallel with the high-frequency transformer creates ZVS conditions for all devices. Due to the transformer leakage effect, two individual capacitors C_{r1} and C_{r2} are required to ensure ZVS

for both the primary and secondary bridges. If isolation is not required, these two capacitors can be merged into one.



(a)



(b)

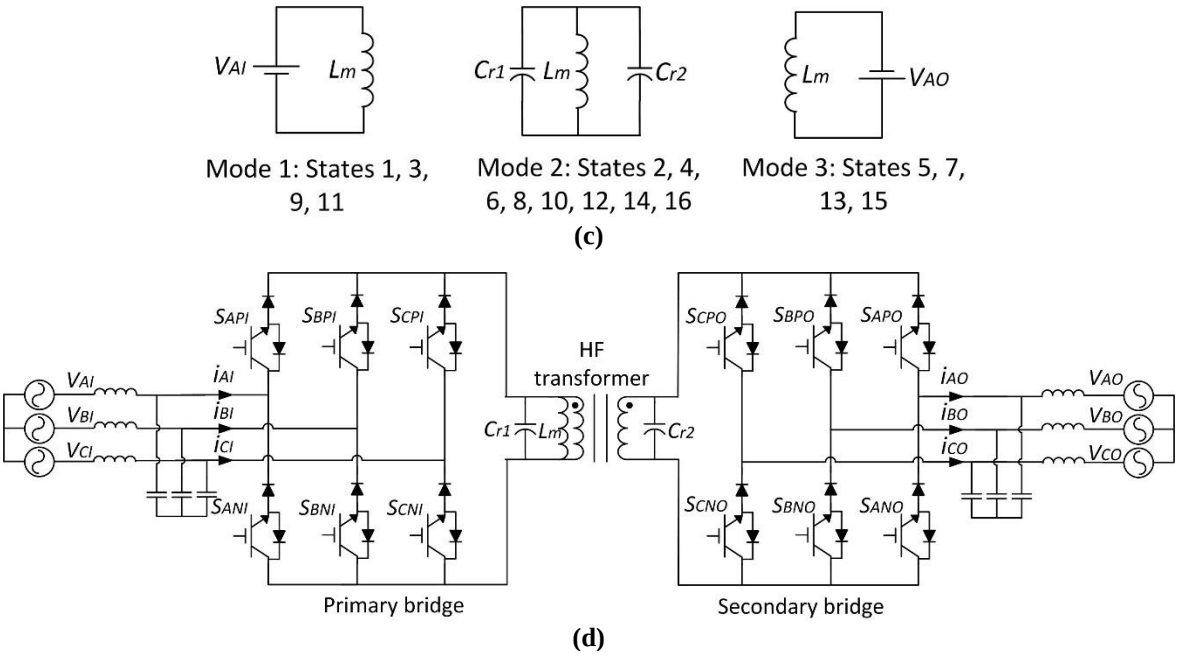


Fig. 2.24: Partial resonant ac-link converter: a) converter topology; b) relative waveforms and switching sequences; c) equivalent circuits of three basic modes; d) varied topology with reduced switch count.

The converter has a total of 16 operation states over one switching cycle. The relative waveforms and switching sequences are shown in Fig. 2.24 (b). Starting from state 1, by turning on S_{API} and S_{BNI}, the high-frequency transformer is connected to phase A and B which has the largest line-to-line voltage, and thus C_{r1} voltage is equal to V_{ABI}. The transformer magnetizing current I_m is built up with the voltage V_{ABI}. After the average current over one switching cycle equals to I_{B_ref}, S_{BNI} is turned off with reduced switching loss due to the presence of C_{r1}, and the transformer magnetizing inductance L_m resonates with C_{r1}. The resonant mode ends when the voltage of C_{r1} equals to the line-to-line voltage V_{ACI}. Then S_{CNI} can be turned on under ZVS condition. The output bridge works in a similar manner to deliver energy in the magnetizing inductance to the output side. After the end of the first half switching cycle at state 8, in the next half switching cycle, from state 9 to state 16, the converter operates with the complementary devices of each leg. All 16 states can be grouped into three basic modes: charging, resonating, and discharging mode, whose equivalent circuits are shown in Fig. 2.24 (c). A varied topology with reduced switch count is proposed in [67] and the circuit is shown in Fig. 2.24 (d), which requires 12 IGBTs and 12 diodes.

Even though diodes are connected in series with IGBTs, they do not suffer from the reverse recovery issue thanks to the ZVS operation of IGBTs. However, a long resonant duration is required to reset the capacitor voltage, which results in high current stress and circulating power loss.

The partial resonant ac link converter has the following features: arbitrary power factors and frequencies for the input and the output; voltage buck-boost capability; and ZVS conditions for all devices. However, accurate current and voltage sensing is required to achieve ZVS operation. The converter has to operate with different switching frequencies at different power levels. The current stress of all the devices is also high due to the resonant operation. In addition, resonance between the resonant capacitor and the transformer leakage inductance has to be managed properly. It was proposed in literature [67] and [68] that this resonance can be damped with increased transformer winding resistance, but it introduces additional conduction loss.

2.8. Multi-Port Topology

The multi-port converters have at least three terminals which can interface with multiple sources. It is obvious that any multi-stage converter that has a dc voltage link can be configured as a multi-port converter. Take the single-phase ac to three-phase ac converter in Fig. 2.10 for an example. The third terminal can be connected to either of the two dc voltage links through a single- or three-phase inverter or a dc/dc converter, depending on the type of sources it connected. This type of configuration has been discussed in [69].

The DAB converter, isolated matrix converter, Dyna-C converter, and partial resonant ac link converter can also be configured as multi-port topologies. The tri-port Dyna-C [28] and the partial resonant ac link converter [70] have the same operating principle as their three-phase ac/ac configurations, except that all three bridges in the tri-port configuration need to be sequentially operated within one switching cycle. Fig. 2.25 shows the topology of the tri-port partial resonant ac link converter.

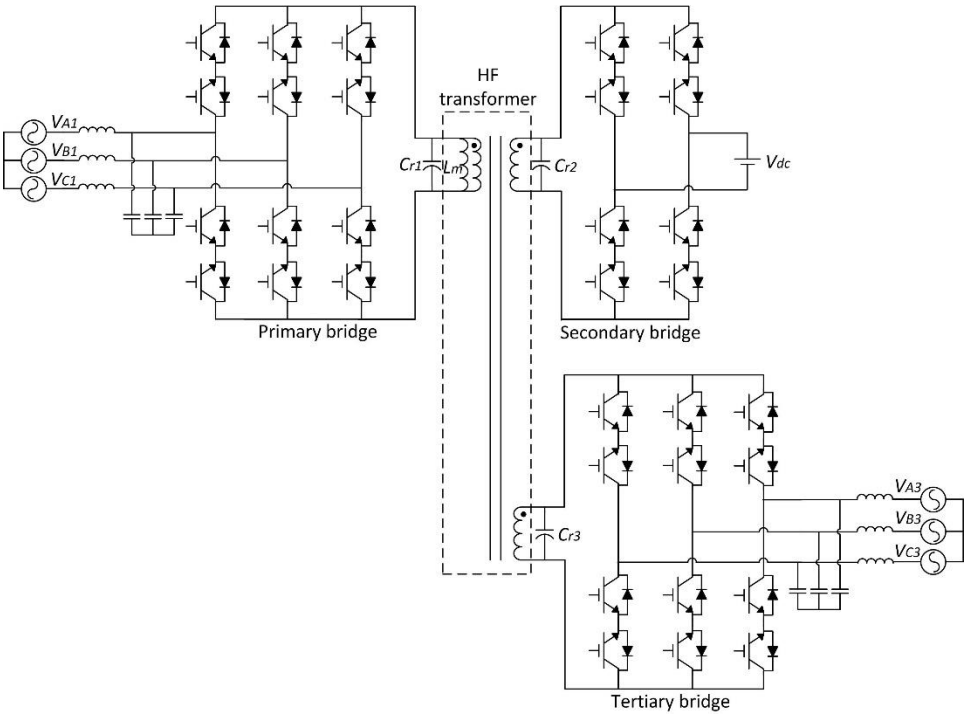


Fig. 2.25: Tri-port configuration of the partial resonant ac link converter.

The tri-port isolated matrix converter, proposed in [71], uses three individual single-phase ac/ac cycloconverters on the primary side to convert three-phase line-frequency ac to high-frequency ac, as shown in Fig. 2.26. This single-phase ac/ac conversion approach allows series stacking multiple fractionally-rated converter cells for a multi-level configuration. However, if the multi-level configuration is not required, any of the three-phase matrix converter bridges, shown in Fig. 2.18, can be used. The three-phase synchronous rectifiers on the secondary and tertiary sides convert the high-frequency ac to dc.

The tri-port DAB converter, proposed in [72], [73], shown in Fig. 2.27, is an extension of the conventional DAB converter. This converter can be modeled as an inductor network driven by multiple square-wave ac voltage sources, as shown in Fig. 2.28. Similar to the power flow in the networked grid, by adjusting the phase shift of the three voltage sources, power flow among the three converter bridges can be controlled.

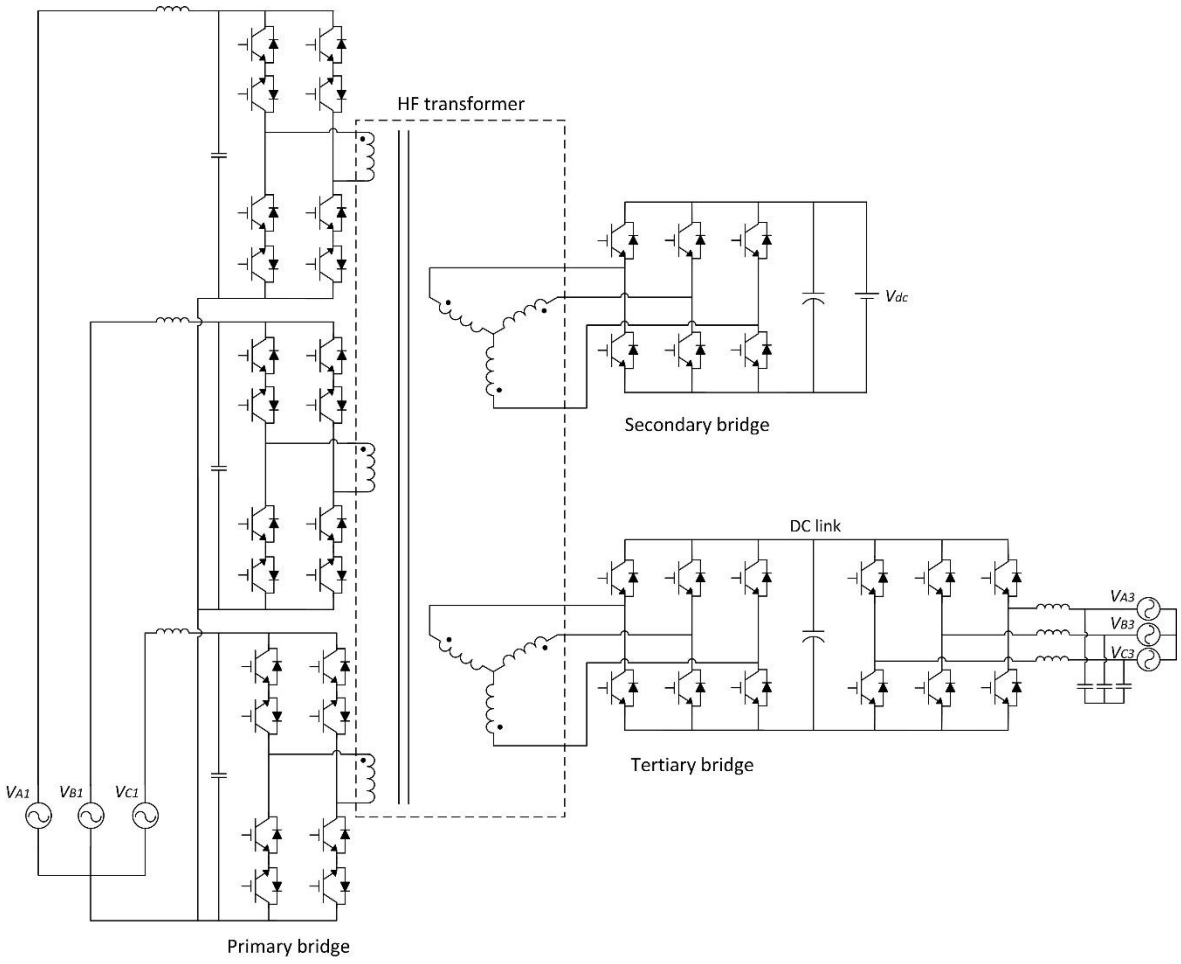


Fig. 2.26: Tri-port configuration of the isolated matrix converter.

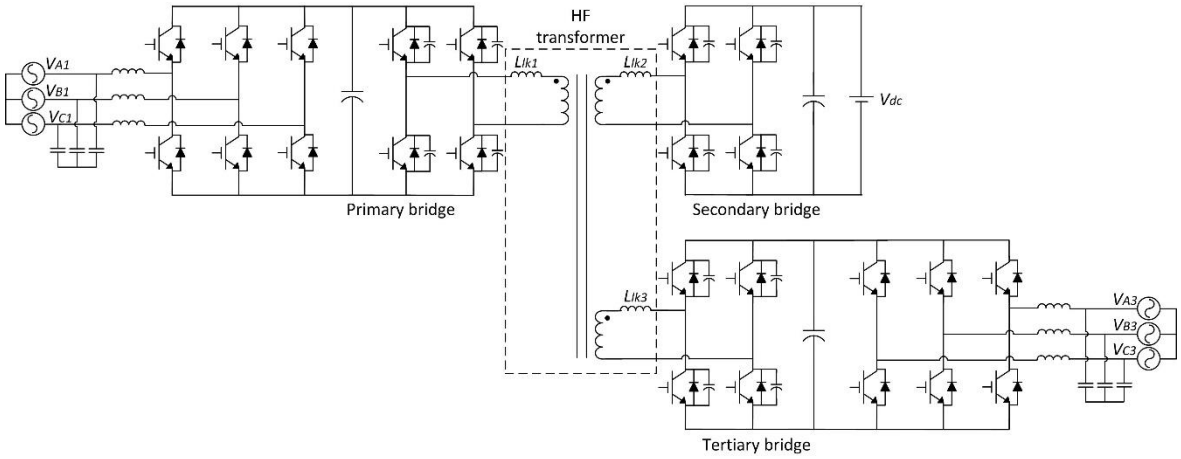


Fig. 2.27: Tri-port configuration of the DAB converter.

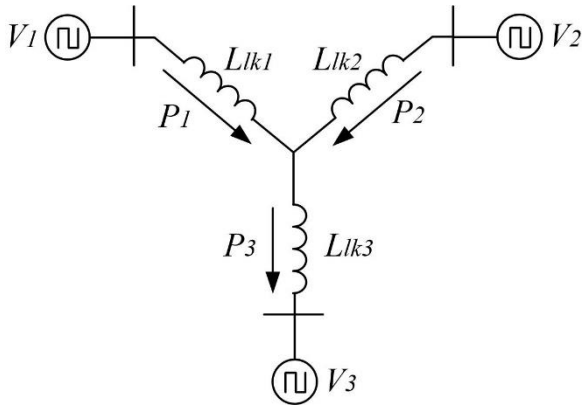


Fig. 2.28: Equivalent circuit of the tri-port DAB converter.

Because the input and output bridges of the Dyna-C converter and the partial resonant ac link converter are configured as current source inverters, they can be operated with independent control for all bridges. This allows using a simple control strategy for the multi-port configuration. However, the issue with these converters is that the peak of the magnetizing current increases in proportion to the number of bridges. For the multi-port isolated matrix converter and the DAB converter, all bridges are operated simultaneously; and thus they are coupled together, leading to a complicated control problem.

2.9. Scaling to High Voltage

For utility applications, where the SST has to interface multi-kV voltages, a multi-level approach has to be taken such that each device can be fractionally rated. The converter devices need to equally share the current on the low voltage / high current side and to share the voltage on the high voltage / low current side. There are two schemes to implement the high voltage-side converter. One is by using a modular converter configuration in which all modules are connected in series. The other one is by using a single module multi-level converter such as the diode-clamped converter. Fig. 2.29 shows the configuration for medium/high voltage to low voltage three-phase SSTs using modular multi-stage single-phase ac/ac converters, which was proposed in [58], [59], and [110]. Proper voltage and power balance control has to be designed to stabilize the system. Fig. 2.30 shows the

configuration with a diode-clamped multi-level converter for the high voltage primary side, which was proposed in [74].

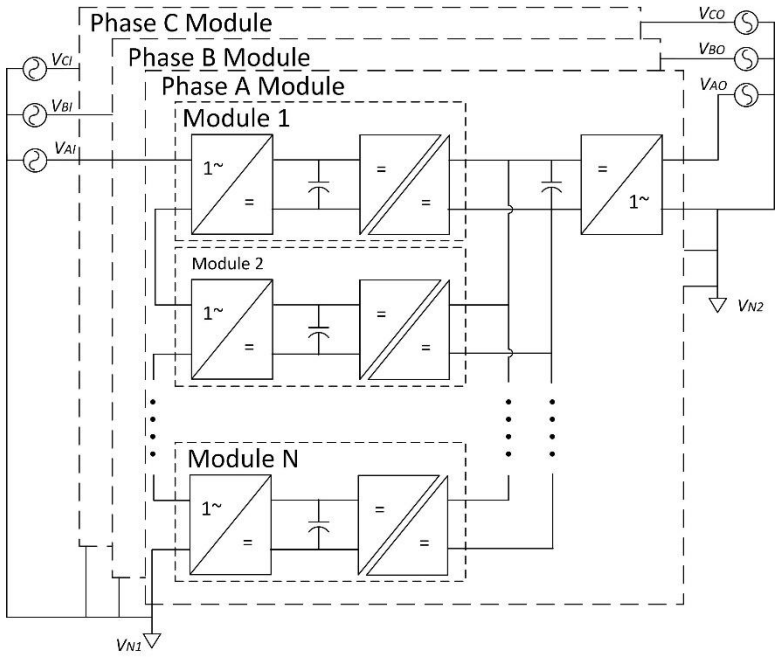


Fig. 2.29: Scaling to high voltage using modular converters.

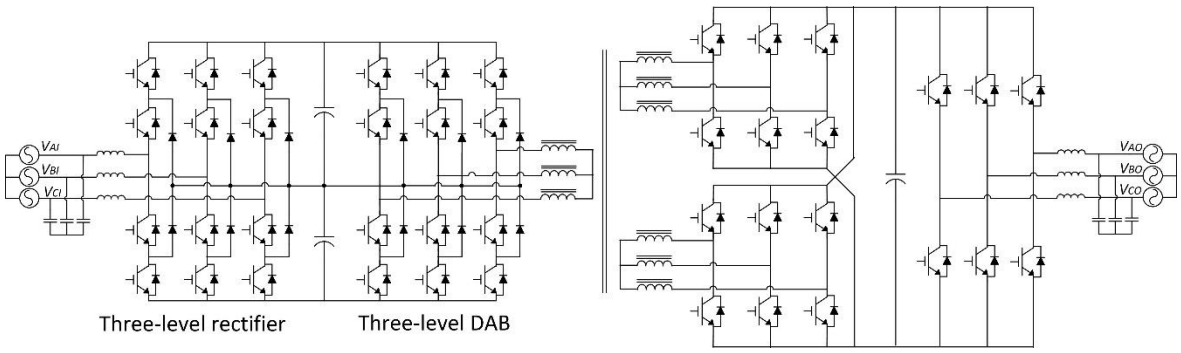


Fig. 2.30: Scaling to high voltage using a diode-clamped converter.

2.10. Impact of Parasitic Elements

Based on the above review, the basic circuit structures to implement various types of SSTs can be classified as the multi-stage cascaded voltage source inverter/rectifier with an isolated dc/dc converter, the cyclo/matrix converter, the flyback converter, the DAB converter, the Dyna-C converter, the ac-link converter, and the partial resonant ac link converter. In actual SST design, various converter non-idealities, such as parasitic inductance, diode reverse recovery, and transformer leakage inductance, will impact the

converter operating scheme. Obviously, impact to these converters will be different since their operating principles of transferring energy through the transformer are distinct.

For all the hard-switching topologies, including the inverter/rectifier stage of the multi-stage SST, the cyclo/matrix converter, the flyback converter, and the Dyna-C converter, parasitic inductance will develop voltage spikes across devices, which has to be considered as a derating factor for proper device selection. Obviously, hard-switching conditions also lead to other issues such as noise, resonance, switching loss, and EMI. All of these will be discussed in detail in chapter 4.

Diode reverse recovery leads to additional switching loss. In addition, in some circuit structures, the reverse recovery current tends to store energy in the inductive component, which, if not managed properly, will develop voltage spikes across the devices once the diode is snapped off. The flyback converter and the Dyna-C converter have energy trapped in the transformer leakage inductance due to the diode reverse recovery issue. The device reverse recovery of the ac-link converter develops trapped energy in the series inductor, even though all the main devices are switched under ZCS conditions. Using SiC devices can help mitigate this issue, but the junction capacitance still resonates with these inductive components to develop voltage spikes and subsequent resonance.

Energy trapped within the transformer leakage inductance is another important issue that has to be properly addressed when transferring energy from one side of the transformer to another. The flyback converter cannot manage the trapped leakage energy through switch commutation, thus snubbers are required to protect devices, which becomes an issue when the voltage and power levels scale up. The Dyna-C converter and the cyclo/matrix converter can actively manage the leakage energy, with additional two and four commutation states respectively within one switching cycle. These additional switching states reduce the active duty cycle for transferring power through the transformer. Besides, the diode reverse recovery also interacts with the leakage inductance to develop resonance and spikes.

2.11. Comparisons of Topologies

2.11.1. Topology Comparison for Various Circuit Configurations

Topologies of bidirectional power converters with high-frequency isolation interfacing with various power sources have been presented. It can be seen that the multi-stage converters using the isolated dc/dc converter or the integrated isolated ac/dc converter can be configured to interface with any type of power source. Besides, six topologies are presented as the single-stage converter: isolated cyclo/matrix converter, flyback converter, DAB converter, Dyna-C converter, AC-Link converter, and partial resonant ac link converter. Table 2.1 gives the summary of these topologies versus various circuit configurations. Among them, the dc to three-phase ac flyback converter and the three-phase ac/ac DAB converter are also feasible in terms of functionality, but have not been reported in literature. The table shows that none of these topologies can be configured as a single-stage single-phase ac to three-phase ac converter, without using an additional temporary energy storage component such as a capacitor or an inductor. This is due to the fact that the instantaneous power is fluctuating on the single-phase side while it is constant on the three-phase side.

Table 2.1: Topologies with various circuit configurations showing possible conversion functions.

Configuration	Multi-stage using dc/dc converter	Single-stage					
		Cyclo/matrix converter	Flyback	DAB	Dyna-C	AC-Link	Partial resonant ac link
dc – single phase ac	Yes	Yes	Yes	Yes	Yes	No	Yes
dc – three-phase ac	Yes	Yes	Feasible	Yes	Yes	Yes	Yes
Single-phase ac/ac	Yes	Yes	Yes	Yes	Yes	No	Yes
Single-phase ac – three-phase ac	Yes	No	No	No	No	No	No
Three-phase ac/ac	Yes	Yes	Yes	Feasible	Yes	Yes	Yes
Multi-port	Yes	Yes	No	Yes	Yes	No	Yes

2.11.2. Comparison of Topologies Based on Functional Capabilities and Device Rating

Power converters with a high-frequency transformer provide many functionalities that low-frequency transformers do not have. Table 2.2 lists the functional capabilities and the device rating of all topologies for the three-phase ac/ac configuration. The device count and the device rating in p.u. with respect to the transferred power are also presented. The total device rating is calculated as the device count multiplied by the per device rating. It can be seen from the comparison that the topologies with lower device count tend to have limited function capabilities. The topologies of the AC-Link converter and the partial resonant ac link converter have soft-switching features at the expense of high device stresses. By including an isolated dc/dc converter stage, the multi-stage converter provides an intermediate voltage source dc link that simplifies control. However, the large electrolytic capacitor for dc energy storage is usually the weakest component, which could shorten converter lifetime.

Table 2.2: Topologies functional capabilities and device rating for SSTs with three-phase ac/ac input/output.

Device rating and functional capability		Three-stage	Single-stage				
			Matrix converter	Flyback		AC-link	Partial resonant AC link
				Four quadrants	Two quadrants		
Device rating	Per switch rating (p.u.)	1	1	4	4	4.5	4
	Switch count	20	24 or 22	12	6	12	24
	Total switch rating (p.u.)	20	24 or 22	48	24	54	96
Function capability	Reactive power support	Yes	Yes	Yes	No	Yes	Yes
	Voltage buck-boost capability	Limited	No	Yes	Yes	Yes	Yes
	Independent line frequency	Yes	Yes	Yes	No	Yes	Yes
	Independent power factor	Yes	Yes	Yes	No	Yes	Yes
	Voltage source DC link access	Yes	No	No	No	No	No
	Soft-switching	Partial	No	No	No	Yes	Yes

2.12. Conclusions

Various topologies have been proposed to implement the SST since it was first proposed around fifty years ago. Among them, the most widely used one is the multi-stage topology

consisting of a rectifier, an isolated dc/dc converter and an inverter. This is because the multi-stage topology decouples the input and the output. Availability of dc voltage links and simplicity of control make it attractive. However, this converter has a high component count, a complex structure, and bulky dc link capacitors that can limit lifetime. Various topologies with a reduced number of stages have also been proposed to implement the SST, but they typically require complicated device configuration and control principles. High system loss is also an issue for the SST due to the complex circuit structure. As a result, resonant converter topologies with soft-switching features have been proposed to eliminate the switching loss. However, the associated high device stress is a concern for these topologies.

CHAPTER 3: ISOLATED DYNAMIC CURRENT (DYNA-C) SST

3.1. Introduction

Although several papers have concluded that the three-stage converter, based on a dual-active-bridge (DAB) soft-switched dc/dc converter, offers perhaps the best performance and controllability [75], [76], the Isolated Dynamic Current Converter (Dyna-C) proposed in [27]-[30], showed a minimal SST topology with 12 devices to fulfill all the SST functionalities. The Dyna-C has a current-source topology with two power conversion stages, in which each stage is comprised of a standard current-source inverter. The fundamental topology was first introduced in a thesis as a three-phase, four-quadrant flyback cycloconverter with isolation [77]. However, several key elements have been missing from discussions on the analysis, control, and operation of such a converter, the most important of which is the management of the trapped transformer leakage energy during bridge transitions. Furthermore, achieving input/output regulation on a switching cycle-by-cycle basis across all phases is critical for maintaining small transformer size. The Dyna-C was proposed to implement the SST, with the intention of addressing primary issues that were not discussed in [77]. However, as will be shown, the Dyna-C does not fully manage to address key limitations such as diode reverse recovery, voltage spikes and bumps, resonance, severe EMI, and low efficiency.

The S4T proposed in this thesis fully addresses all the primary requirements of single-stage SST's, and at the same time solves critical limitations faced by the Dyna-C SST. To understand the S4T fully, it is important to make sure that the Dyna-C operation and limitation are fully understood.

3.2. Dyna-C Topology

Fig. 3.1 shows the three-phase ac/ac topology of the Dyna-C, which consists of three elements: 1) a high-frequency, two- or multi-winding transformer to provide galvanic isolation and energy storage over short duration, 2) current-source inverter (CSI) bridges

with two, three, or four phase-legs for dc to three-phase ac interconnections, and 3) terminal LC filters for suppressing switching harmonics. With only 12 devices and a high-frequency transformer, a galvanic isolated bi-directional SST is realized with minimal component count.

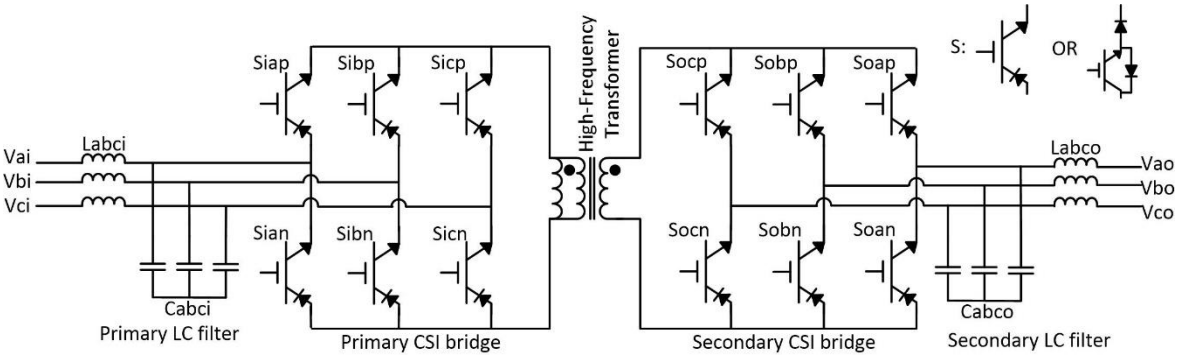


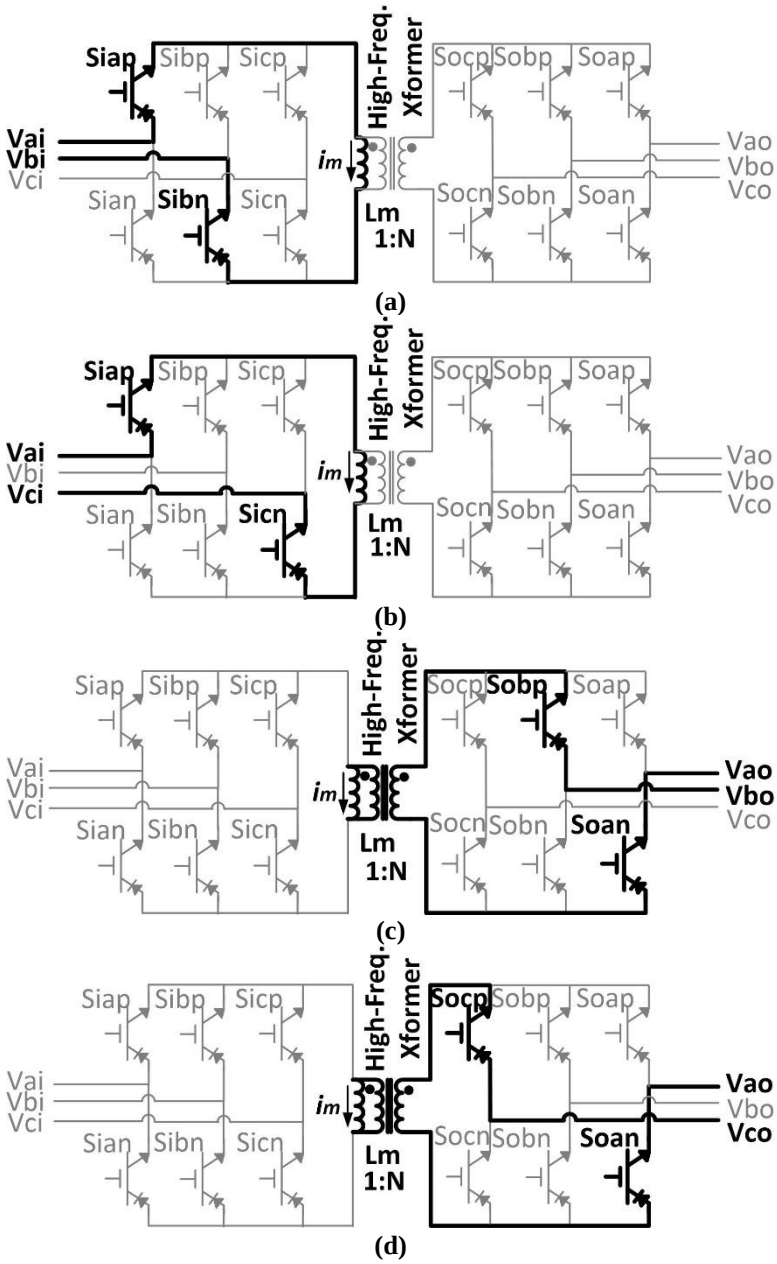
Fig. 3.1: Dyna-C three-phase ac/ac topology.

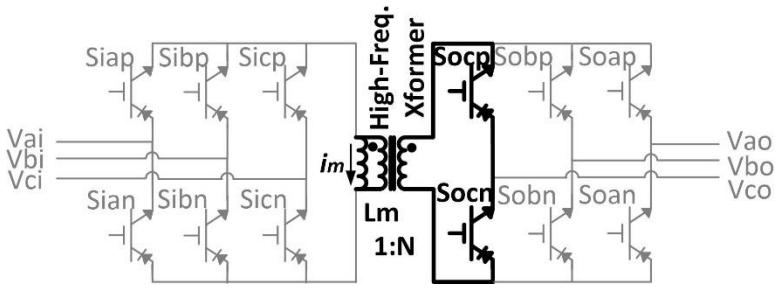
The individual bridges are configured like a CSI with switches that conduct current in one direction but block voltages in both directions. This can be implemented with either an IGBT in series with a diode, or a reverse blocking IGBT (RB-IGBT). The RB-IGBT, which is already available on the market from IXYS or Fuji Electric, has lower conduction loss than the normal IGBT/diode configuration and can achieve a more compact design without any module customization. The transformer's magnetizing inductance is used as means of transferring energy between bridges. Depending on the directionality of the power flow, the input bridge(s) charges the magnetizing inductance while the output bridge(s) discharges it to the load or another source. Volt-sec balance, and correspondingly the magnetizing current, is regulated on the transformer by controlling the charge or discharge times. Each bridge is sequenced consecutively such that a complete switching period consists of cycling through each phase of all the bridges. The topology provides voltage step-up/down capability with the input and output operating at arbitrary power factors and frequencies.

3.3. Principle of Operation

Without considering the transformer leakage effect, the Dyna-C three-phase ac/ac topology has five operation modes over one switching cycle, which are shown in Fig. 3.2.

The Dyna-C converter always performs inter-phase operation, which means that in any active mode, there are always two phases connecting to the transformer to perform charge/discharge control. The relative waveforms corresponding to each mode are shown in Fig. 3.3.





(e)

Fig. 3.2: Operation modes over one switching cycle for the Dyna-C three-phase ac/ac topology: a) mode 1: charging cycle with 1st input L-L voltage; b) mode 2: charging cycle with 2nd input L-L voltage; c) mode 3: discharging cycle with 1st output L-L voltage; d) mode 4: discharging cycle with 2nd output L-L voltage; and e) mode 5: free-wheeling.

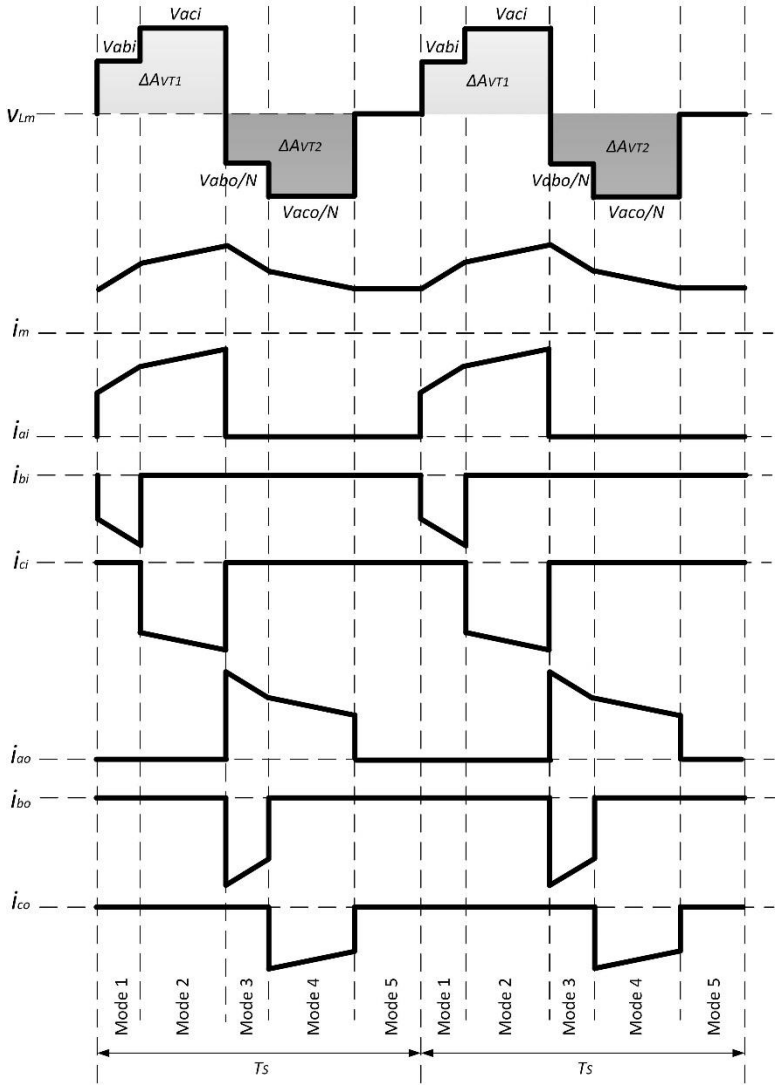


Fig. 3.3: Relative waveforms of the Dyna-C three-phase ac/ac topology.

Assuming an instant when phase A reference current at the input side has the largest amplitude with a positive polarity, then phase B and C reference currents should be negative

for a three-phase balanced system. The converter operation within one switching cycle starts from mode 1 by turning on *Siap* and *Sibn*, then transformer magnetizing current i_m flows through phase A, *Siap*, L_m, *Sibn* and phase B. This mode ends when the average current over one switching cycle delivered to phase B equals to its reference current I_{BI_ref}. After that, *Sibn* is turned off and *Sicn* is turned on in mode 2. Then current i_m flows through phase A and C, until reference current is delivered to phase C. For a three-phase balanced input, phase A reference current is obtained as long as phase B and phase C reference currents are delivered. Referencing to the transformer primary side, magnetizing inductance L_m is charged by the voltage of V_{abi} and V_{aci} respectively during these two modes, resulting an increase of i_m. Then the output bridge starts operation in a similar manner, with L_m being discharged by the voltages of V_{abo}/N and V_{aco}/N in mode 3 and mode 4, assuming a *1:N* transformer turns ratio. If the input and output bridges operation finishes in a time duration less than the switching cycle T_S, the devices within the same leg are turned on in mode 5. The current i_m freewheels through this leg, without delivering current to either the input or the output.

The transformer magnetizing current is regulated around a specific dc value, which is achieved by maintaining the volt-sec balance across L_m. Subsequently, ΔA_{VT1} and ΔA_{VT2}, as expressed in equations (3.1) and (3.2) and shown in the top waveform of Fig. 3.3, should be equal to each other.

$$\Delta A_{VT1} = V_{abi} * T_{m1} + V_{aci} * T_{m2} \tag{3.1}$$

$$\Delta A_{VT2} = \frac{V_{abo}}{N} * T_{m3} + \frac{V_{aco}}{N} * T_{m4} \tag{3.2}$$

T_{m1}, T_{m2}, T_{m3}, T_{m4} in these equations are the time duration for modes 1-4, respectively. Assuming a transformer with 1:1 turns ratio, equations (3.1) and (3.2) indicate that T_{m1} and T_{m2} will be equal to T_{m3} and T_{m4} respectively when the three-phase input and output voltages are the same. However, if the input and output have dissimilar voltage amplitudes, the time durations T_{m1}, T_{m2}, T_{m3}, and T_{m4} will also vary accordingly to ensure the volt-sec balance

across L_m. Therefore, the converter voltage step-up and -down capability is achieved by adjusting duty cycles of the input and output bridges.

Reverse power flow is achieved by exchanging the operation modes for the input and the output, in which the previous output phase charges L_m while the previous input phase discharges it. It should be noted that since the phase currents are directly controlled, the input and output sides can have arbitrary frequencies and power factors. Moreover, due to the current source characteristics, the converter itself has voltage step-up and -down capability in addition to the transformer turns ratio effect.

3.4. Leakage Management

One of the key innovations of Dyna-C is the approach to manage the energy trapped in the transformer leakage in a loss-less manner. As one bridge transitions to another, the winding current has to be driven to zero on the outgoing bridge, and simultaneously, the winding current on the incoming bridge has to be built up from zero to equal the magnetizing current. If a bridge transition were to occur without proper leakage management, the resulting voltage spike/ringing would cause high losses and a possible catastrophic destruction of semiconductor devices. While a snubber or clamp could be used for managing the leakage energy, converter losses and heat management will become an issue. Active snubbers that can recycle the energy provide one avenue, but come with added cost and complexity. An alternate loss-less approach was proposed in [27].

In addition to the five modes of operation shown in Fig. 3.2, the Dyna-C requires two additional modes for inter-bridge transitions, i.e., the transition from the input bridge to the output and vice versa. Fig. 3.4 shows one of the leakage management modes, which is required between mode 2 and mode 3 of Fig. 3.2. For driving the outgoing bridge winding current to zero, and simultaneously building the incoming bridge winding current to equal the magnetizing current, voltage has to be applied across the leakage in the direction the current needs to flow. This is accomplished by applying a negative voltage across the transformer by the outgoing bridge and simultaneously applying a positive voltage by the

incoming bridge. As shown in Fig. 3.4, the input line-line voltage V_{cai}, assuming a negative polarity at this instant, is applied to L_m by turning on *Sicp* and *Sian*. Meanwhile, the output line-line voltage V_{bco}/N, assuming a positive polarity at this instant, is applied to L_m by turning on *Sobp* and *Socn*. As soon as the current goes to zero on the outgoing bridge, that bridge can be turned off, and the incoming bridge can initiate its normal mode of operation. This approach enables safe and lossless management of the trapped leakage energy. A similar mode is also required for the transition from the output bridge to the input bridge.

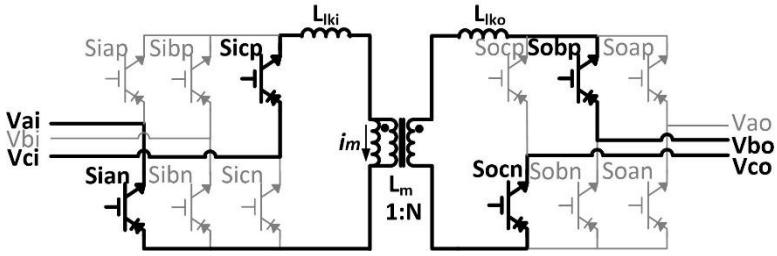


Fig. 3.4: Leakage management mode for the transition from the input bridge to the output bridge.

The simplified equivalent circuit of this mode is shown in Fig. 3.5, in which L_m is replaced with a constant current source I_m. The leakage management process is quite robust and requires that the applied voltages drive the outgoing bridge current to zero and incoming bridge current to I_m. The process can be achieved with equivalent line voltages as shown in Fig. 3.5, or a zero voltage on the input side by turning on *Sicp* and *Sicn*, while the output side remains the same as in Fig. 3.5.

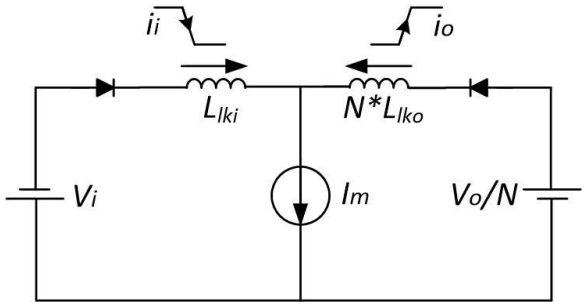


Fig. 3.5: Simplified equivalent circuit for the leakage management mode.

The energy stored in the leakage of the outgoing bridge, the input bridge, is given by equation (3.3), in which I_{ip} is equal to the peak magnetizing current reflected onto the input bridge when the bridge-to-bridge transition begins. Similarly, the energy that must be

injected into the leakage of the incoming bridge, the output bridge, is given by equation (3.4), in which I_{op} is equal to the peak magnetizing current reflected onto the output bridge when the bridge-to-bridge transition begins.

$$E_{lki} = \frac{1}{2} L_{lki} I_{ip}^2 \tag{3.3}$$

$$E_{lko} = \frac{1}{2} L_{lko} I_{op}^2 \tag{3.4}$$

Conceptualized waveforms showing the primary and secondary winding currents for the circuit of Fig. 3.4 are given in Fig. 3.6. The figure shows that during bridge transitions, the current is driven to zero on the outgoing bridge while simultaneously building up the current on the incoming bridge. The expression for the current slope is given as a function of applied voltages and various inductances. In Fig. 3.6, the magnetizing current is shown to be held constant during the leakage management periods, t_{lk1} and t_{lk2}. This is under the assumption that the leakage inductance is significantly small compared to the magnetizing inductance, and the times it takes to manage the trapped leakage energy occurs over relatively short durations. In actuality, the magnetizing current will be impacted slightly as well. The leakage management time durations, t_{lk1} and t_{lk2}, are calculated based on equations (3.5) and (3.6). If these times become relatively large compared to the switching period, T_s, compensation efforts to the control should be taken to avoid undesired distortion or harmonics at the input and output terminals.

$$t_{lk1} = \left(L_{lki} + N * L_{lko}\right) \frac{I_{ip}}{\left|V_i\right| + \frac{\left|V_o\right|}{N}} \tag{3.5}$$

$$t_{lk2} = \left(L_{lki} + N * L_{lko}\right) \frac{I_{op} * N}{\left|V_i\right| + \frac{\left|V_o\right|}{N}} \tag{3.6}$$

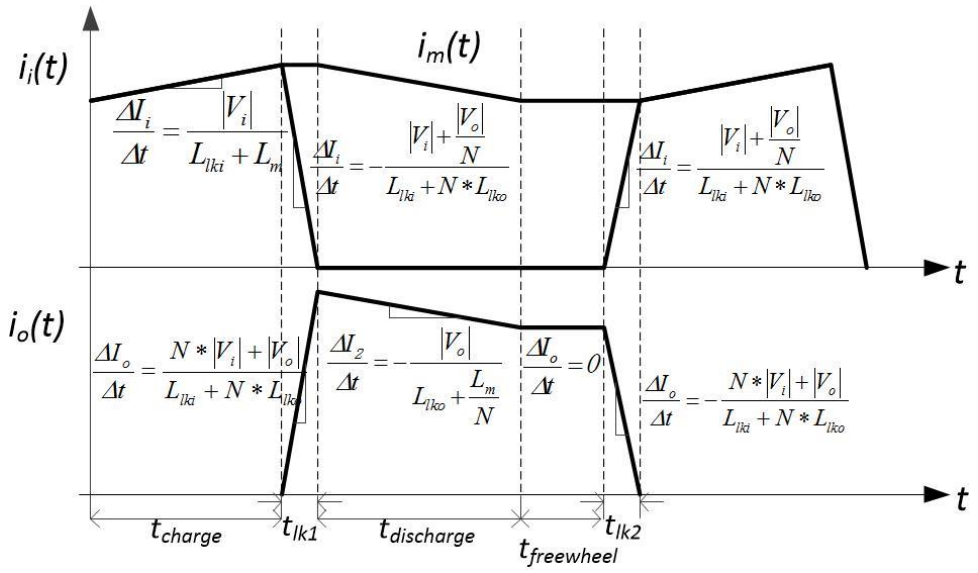


Fig. 3.6: Conceptualized waveforms of the primary and secondary winding currents during leakage management.

3.5. Issues with the Dyna-C Topology

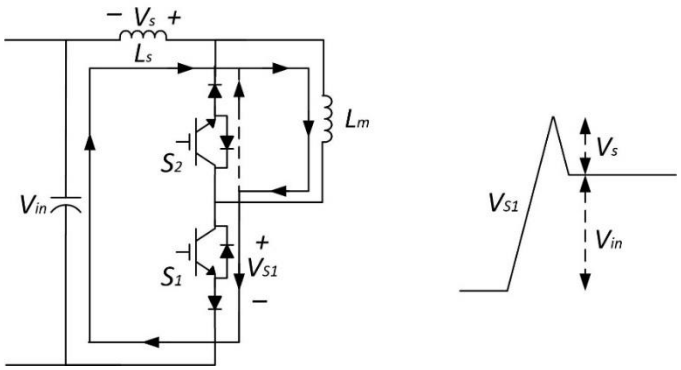
3.5.1. Converter Loss

The main converter loss includes devices conduction and switching losses. Compared with a simple non-isolated voltage source converter, the Dyna-C suffers from higher conduction loss due to the extra diode in series with each switch. The conduction loss, however, can be reduced by employing reverse blocking IGBTs (RB-IGBT), which can block both forward and reverse voltages in the off-state without an extra series diode [37]. Such RB-IGBT devices are already available on the market from IXYS or Fuji Electric. In addition, due to the fact that only one individual bridge is operating except for the leakage management transitions, the average transformer magnetizing current is N times the ac side peak current I_{gp}, where N is the number of the converter bridges. This indicates that all devices are switching at the current of $N*I_{gp}$, leading to a high switching loss. A 480 V / 50 kVA three-phase ac/ac Dyna-C converter was reported to have an efficiency of only 89% [29], albeit a potential improved efficiency of 93%~95% with RB-IGBTs or Silicon-Carbide (SiC) devices was considered possible. However, low efficiency is an issue for all the

existing SST topologies that have been presented in the literature survey, typically below 90% for 480 V class applications.

3.5.2. Device Stress at Phase-Leg Transitions

The devices suffer from high voltage spike/ringing during phase-leg transition, i.e., the transition between mode 1 and mode 2, mode 3 and mode 4, as well as mode 4 and mode 5 of Fig. 3.2. Fig. 3.7 (a) shows the equivalent circuit at the phase leg transition, in which L_m represents the transformer magnetizing inductance and L_s represents the lumped parasitic inductance of the filter capacitor, the device package, and the bus-planes that connect devices. At the turn-off transition of S_1, a voltage V_s is developed across L_s due to a finite *di/dt* rate. As a result, S_1 needs to block a voltage of $V_{in}+V_s$. The amplitude of V_s depends on the value of L_s and S_1 turn-off speed. Fig. 3.7 (b) shows the conceptualized voltage waveform across S_1 at this transition.



(a) **(b)**

Fig. 3.7: Device stress at phase-leg transition: a) equivalent circuit; and b) conceptualized voltage waveforms across S_1 at the transition.

3.5.3. Voltage Bump at Phase-Leg Transitions

Another unique operating characteristic typical to CSIs is the 'voltage bump' phenomenon associated with Silicon (Si) IGBTs [79], occurring at the phase-leg transition. When the current is forced to flow through the IGBT that is already gated on, the forward recovery of the IGBT causes a voltage bump, whose amplitude is associated with the *di/dt* rate. This phenomenon was explained as "conductivity modulation lag", in which the device on-state voltage drop is also a function of the *di/dt* [80], as shown in equation (3.7). In this

equation, L_{eq} represents the equivalent inductance for the conductivity modulation lag, and this value was observed to be much larger than the device internal parasitic inductance of the package. This voltage bump causes additional losses in the converter and impacts the overall efficiency.

$$V_{ce} = I_c R_{eq} + V_{offset} + L_{eq} \frac{di}{dt} \tag{3.7}$$

3.5.4. Device Stress at Leakage Management Transitions

At the leakage management transition (equivalent circuit has been shown in Fig. 3.5), the diodes suffer from excessive voltage stress. For a Si diode, the voltage peak depends on the slope of the diode recovery current. For a SiC diode, even though the reverse recovery current is negligible, the relatively high transformer leakage inductance resonates with the diode junction capacitance, developing a high voltage stress across the diode. Fig. 3.8 shows the simulated current and voltage waveforms at this transition for a Si diode of APTDF200H120G and a SiC diode of GDP60Z120E respectively. The transformer leakage inductance is 1 μH, and it carries an initial current of 100 A. The voltage to manage the leakage trapped energy is 300 V. It can be seen that the peak voltage stress of the diode is much higher than the input voltage of 300 V and has severe resonance. Results also show that the Si diode has a higher voltage spike than the SiC diode, primarily due to the excessive diode reverse recovery current.

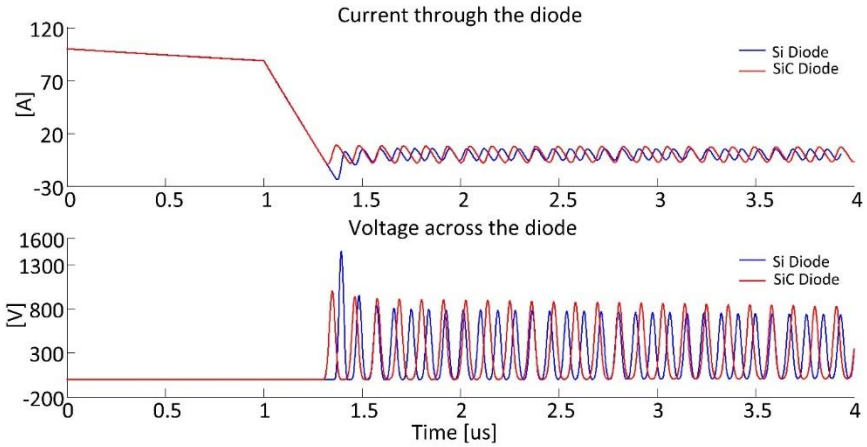


Fig. 3.8: Simulated current and voltage waveforms at the leakage management transition for a Si diode APTDF200H120G and a SiC diode GDP60Z120E.

3.6. Conclusions

The Dyna-C converter is a minimal topology to implement the three-phase bi-directional SST. The single-stage structure allows voltage step-up/down capability, along with arbitrary power factors and frequencies for the input and the output. The converter can also be easily reconfigured for single-/multi-terminal dc and single-/multi-phase ac systems. Leakage management is the key innovation for the Dyna-C, which successfully manages the energy trapped in the transformer leakage inductance during bridge-to-bridge transition such that the Dyna-C can be operated at a high power level.

However, the Dyna-C converter suffers from issues of high converter loss and device stress. Because of the hard-switching conditions, the Dyna-C suffers from severe voltage stress due to the circuit parasitic elements. In addition, conductivity modulation lag for the Si devices associated with CSIs introduces more device loss. Finally, even though the energy trapped within the leakage can be successfully managed by an additional switching state, the resonance caused by the leakage inductance and the parasitic capacitance of the series diodes tends to develop a high voltage spike across the devices, once the diodes are transitioning off.

Implementing the Dyna-C with SiC devices is expected to mitigate some of these issues. However, the high *di/dt* and *dv/dt* rates associated with the high switching speed of SiC devices lead to severe issues including voltage and current spikes and resonances, gate terminal resonance, phase-leg cross talk, gate-driver noise, and EMI. The next chapter will discuss all these hard-switching issues when designing with SiC devices.

CHAPTER 4: HARD-SWITCHING ISSUES FOR SILICON-CARBIDE DEVICES

4.1. Introduction

Although the Dyna-C exhibits attractive features of simple circuit structure, lower component count, elimination of inrush currents, and the flexibility to implement different circuit configurations, the hard-switching property brings several issues such as high device loss, voltage resonance and spike, and voltage bump at phase leg transitions. Using SiC devices for the Dyna-C converter can potentially address some of these issues. Also, SiC devices can significantly reduce the switching loss by speeding up the switching transition, removing the tail-current, and eliminating the voltage bump. In addition, SiC IGBTs, which can have a voltage blocking capability of more than 10 kV, make the Dyna-C potentially viable for medium voltage applications. Unfortunately, it is likely that the device stress and resonances caused by the circuit parasitic elements could be become more severe for SiC devices due to the high *di/dt* and *dv/dt* rates.

Nowadays, Si IGBTs at 1200 V and above are widely used for high-power converters. The common switching frequency for 1200V IGBTs is in the tens of kilo-hertz while for 6500 V IGBTs, this drops to several hundred hertz. The factor that mainly prevents IGBTs from operating at higher switching frequency is the loss caused by tail current [81]. MOSFET is a better device option with much lower switching loss and higher switching frequency capability, and it could be used at the frequencies of up to one mega-hertz. However, for the rating of above 1000 V, the MOSFETs show an unacceptable loss profile due to the high on-state voltage drop [82].

Fortunately, with the advent of wide-band-gap materials such as SiC, which shows a higher-energy electronic band gap, the MOSFETs could maintain low loss at a higher voltage level. Nowadays, 1200 V and 1700 V SiC MOSFETs with current rating up to 400 A are commercially available. With the parameters shown in the datasheets, these high-

power-rated SiC devices could be switched up to 1 MHz. However, the fast switching speed involves high *dv/dt* and *di/dt* rates. Meanwhile, at a high current level, the devices are mostly connected via copper bus-planes which inevitably introduce some parasitic inductance as well as parasitic capacitance between planes. This inductance becomes larger since the size of device package is bigger for higher-power-rated modules. With high *dv/dt* and *di/dt* rates, this parasitic inductance resonates with the parasitic capacitance of devices and other elements, which generates undesired side effects and prevents the device from fully utilizing its maximum switching speed and safe operation area (SOA). In this chapter, using a double-pulse test fixture built to test a 1200 V/100 A SiC MOSFET from Cree™, the switching waveforms are analyzed, and a detailed circuit model considering all parasitic elements is developed. The impact of fast switching, including device current and voltage resonances and spikes, gate terminal resonance, cross talk, gate driver noise, and EMI, are exploited and analyzed in this chapter.

4.2. Test Fixture and Detailed Circuit Model with Parasitic Elements

The device under test (DUT) is a 1200 V/ 100 A rated, half-bridge SiC MOSFET module from Cree™, with the part number of CAS100H12AM1. Fig. 4.1 shows the circuit function diagram of the test fixture. The output of a 0~140 V variable transformer is stepped-up through a transformer with a turns ratio of 1:5, which is then connected to a full bridge rectifier and electrolytic capacitors to provide 0~1000 V dc voltage for device switching operation. A 100 µH inductor is connected in parallel with the high-side switch Q_1, whose gate is shorted to the source terminal such that it is operated as a freewheeling diode. The low-side switch Q_2 is controlled by a double-pulse signal G_{Q2}, which is shown in Fig. 4.2 (a), and the theoretical voltage and current waveforms of Q_2, V_{Q2_DS} and I_{Q2_D} are shown in Fig. 4.2 (b). The time instants t_1 and t_2 are the moments to characterize the turning-on and turning-off conditions of the DUT. The voltage and current levels at switching instants of the DUT can be controlled by changing the variable transformer's output and the first charging duration t_1. Fig. 4.3 shows the test fixture built in the lab. The dc capacitors

comprise electrolytic capacitors and polypropylene capacitors, for which the former one has high capacitance to provide dc energy buffering in steady state, while the latter one has lower capacitance with lower parasitic inductance to provide energy support during switching transients. Copper bus-planes are used to connect the dc capacitors and the DUT. Magnetic field canceling techniques, in which the incoming and outgoing current flows in reverse directions through the bus-planes, are adopted such that the parasitic inductances are minimized. Closely putting the bus-planes together to decrease the parasitic inductance will in turn increase the parasitic capacitance between layers, which leads to higher common mode current. Detailed analysis on this will be shown later. A high bandwidth Pearson current sensor is used to capture the switching current waveforms of Q_2.

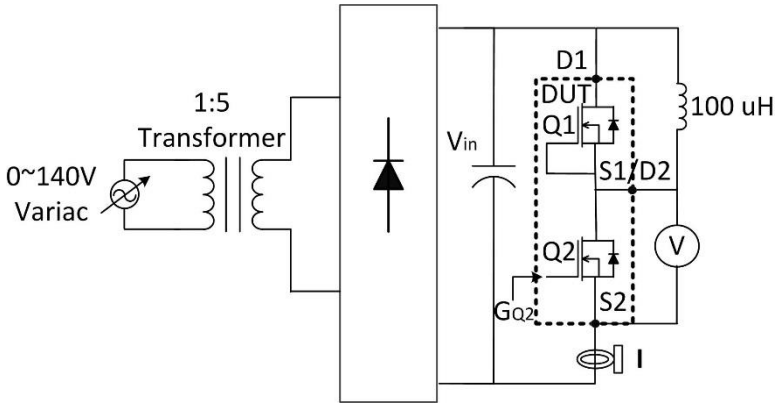
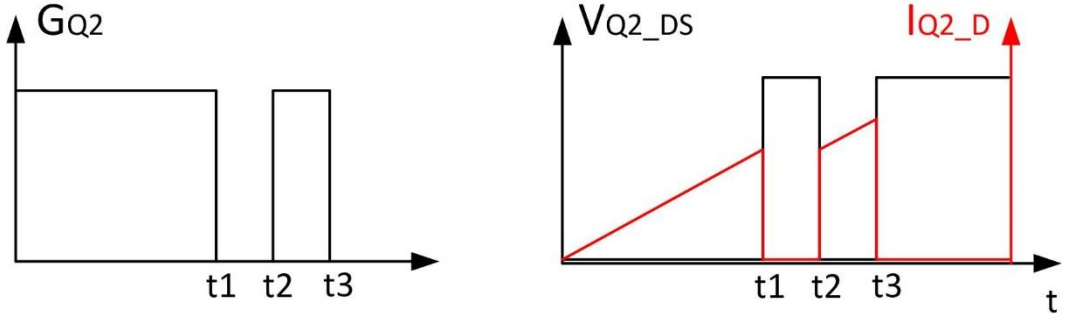
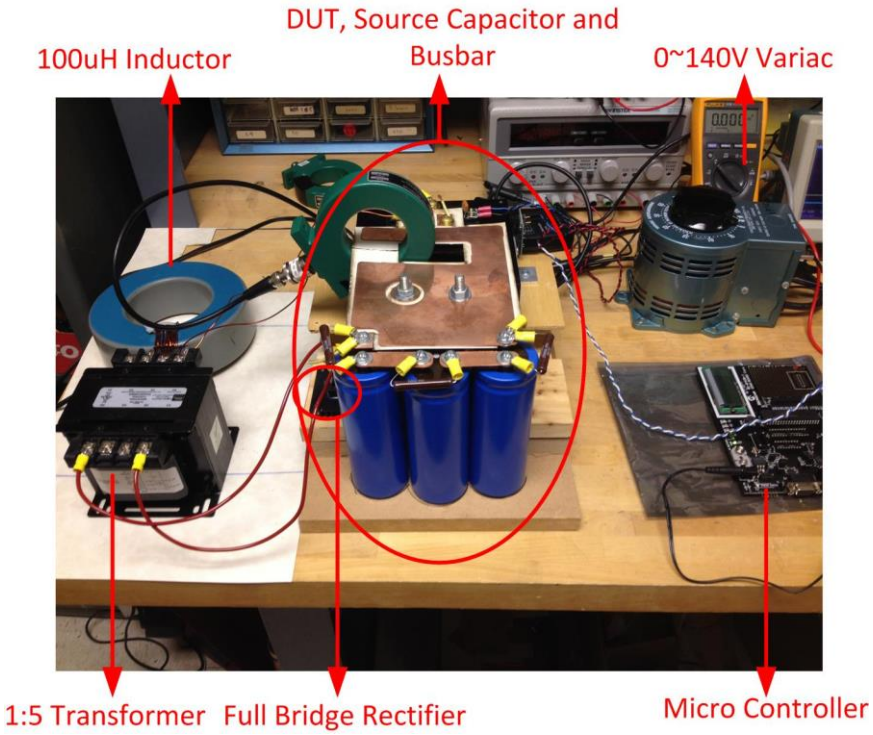


Fig. 4.1: Circuit diagram of the double-pulse test fixture.

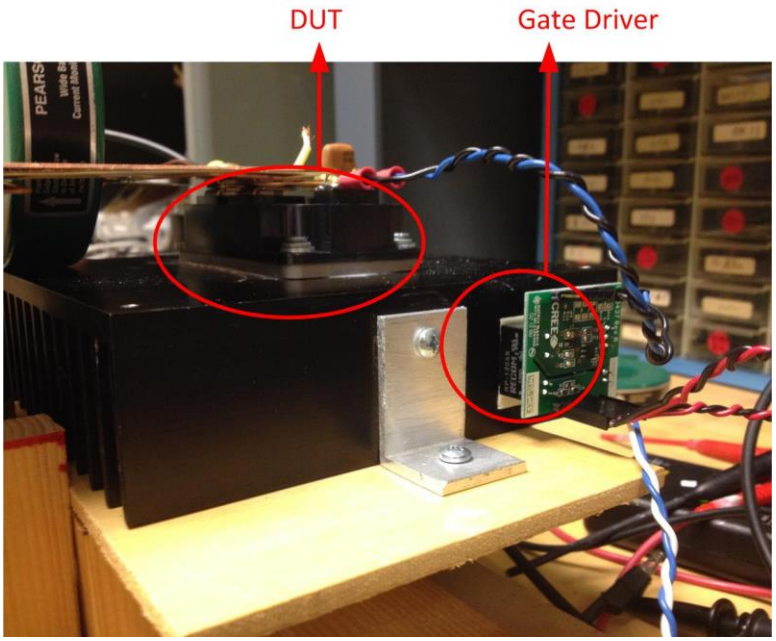


(a) **(b)**

Fig. 4.2: Theoretical waveforms: (a) *Q2* gate signal (b) *Q2* theoretical current, voltage waveforms.



(a)



(b)

Fig. 4.3: Photograph of the double-pulse test fixture: (a) test fixture; and (b) DUT and gate driver.

Given the extremely high *dv/dt* and *di/dt* for SiC devices, it is important that the impact of various parasitic elements is recognized. The parasitic elements that affect the switching operation include the stray inductances of source capacitors and copper bus-planes, the parasitic inductance and capacitance of the device package, the winding capacitance and

resistance of the main inductor, as well as the gate driver connector inductance and gate resistance. Fig. 4.4 shows the switching waveforms of Q_2 under 250 V, 20 A. It can be seen that due to the parasitic elements, substantial resonances and spikes are observed on Q_2 drain-source voltage V_{Q2_DS} and current I_{Q2_D}. With a gate resistance of 6.67 ohms, the DUT rising and falling time are 59.6 ns and 55 ns respectively, and I_{Q2_D} reaches the spike of 100 A. This shows that without reducing the switching speed, the device SOA is substantially reduced.

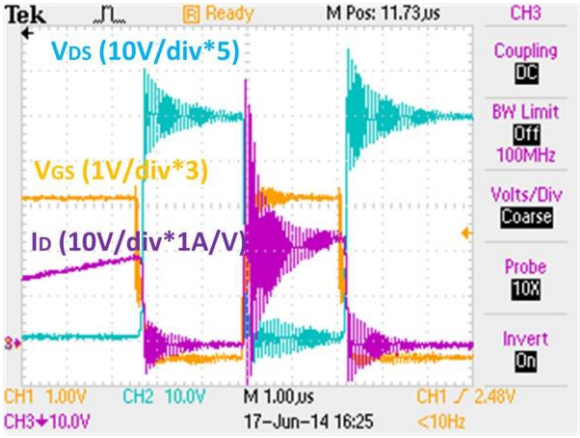


Fig. 4.4: Experimental switching waveforms from the double-pulse test fixture.

The detailed circuit model with all the parasitic elements is shown in Fig. 4.5. The ESL and ESR of the polypropylene capacitor C_S, which are 30 nH and 1 mΩ (sum resistance of leads terminals, leakage, and dielectric loss at 10 kHz) respectively, are obtained from the datasheet. The parasitic inductance L_S of copper bus-planes that connect C_S and DUT, is obtained through FEA simulation, and it has a value of 132.4 nH. The DUT package has internal inductances of L_{DD1}, L_{SS1}, L_{DD2}, L_{SS2} between the module terminals and the device die, which are obtained from the DUT datasheet. The device has an internal gate resistance of 1.25 Ω, represented as R_{GG1} and R_{GG2}. The parasitic inductances L_{GG1} and L_{GG2} between the device die and the gate terminal of the device module, as well as the inductance L_G of gate driver connector, are estimated based on the "rule of thumb" of 10 nH/cm [83]. The DUT has parasitic capacitances between the gate, drain, and source terminals, which are non-linear and can be obtained from the device datasheet.

There are also parasitic capacitances C_{H1} and C_{H2}, between the device module and the heatsink. The procedure to estimate these capacitances will be discussed later. The self-inductance, ESR, and parasitic capacitance of the main inductor are obtained from a resonant sweeping frequency test and triangle voltage excitation method [84].

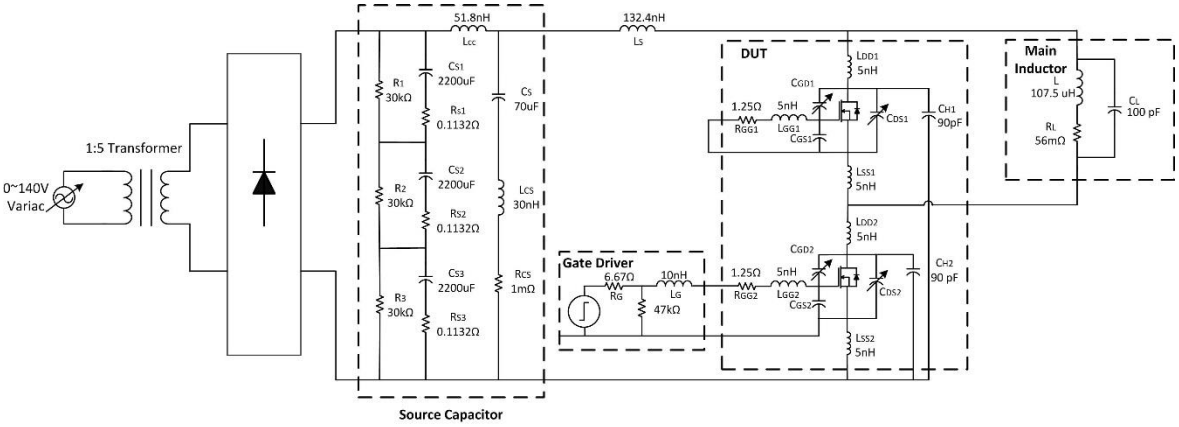


Fig. 4.5: Detailed circuit model with parasitic elements.

4.3. Hard-Switching Issues

4.3.1. Drain-Source Voltage and Current Spikes and Resonance

One of the well-known issues for half bridge switching is the voltage spike across the device due to the parasitic inductance *Ls* when it is turning off. This issue has been widely discussed in the literature [85]-[87] and will not be covered here. Additionally, at the instant of Q_2 turning-on, substantial current spike and resonance are observed in I_{Q2_D}. This current spike has two sources. First is the current flowing through Q_1 that charges its output capacitance C_{OSS1}, defined in equation (4.1), in which C_{GD1} and C_{GS1} are the miller capacitance and gate-source capacitance of Q_1. The second source is the current flowing through the parasitic capacitance C_L of the main inductor. In this test fixture, the first source is dominant since C_{OSS1} is 1.5 nF (obtained from the datasheet), which is much larger than the 100 pF C_L. Therefore, the resonance occurs mainly between the source stray inductance L_{STRAY} and C_{OSS1}, for which L_{STRAY} is the lumped parasitic inductance of copper bus-planes, source capacitors, and the device module, as shown in equation (4.2). The resonance period

is thus calculated as equation (4.3), which closely matches the zoomed in turn-on waveform of Fig. 4.6. Fig. 4.7 shows the resonant path as dashed lines during Q_2 turn-on.

$$C_{OSS1} = C_{GD1} + C_{GS1} \tag{4.1}$$

$$L_{STRAY} = L_S + L_{CS} + L_{DD1} + L_{SS1} + L_{DD2} + L_{SS2} = 182.4nH \tag{4.2}$$

$$T_R = 2\pi\sqrt{L_{STRAY}(C_{OSS1} + C_L)} = 107ns \tag{4.3}$$

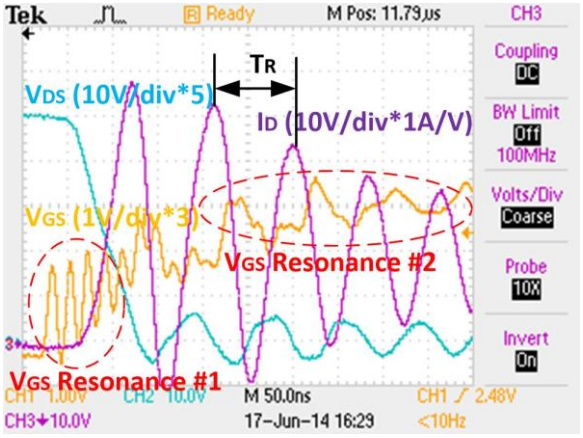


Fig. 4.6: Zoomed in Q_2 turn-on waveforms.

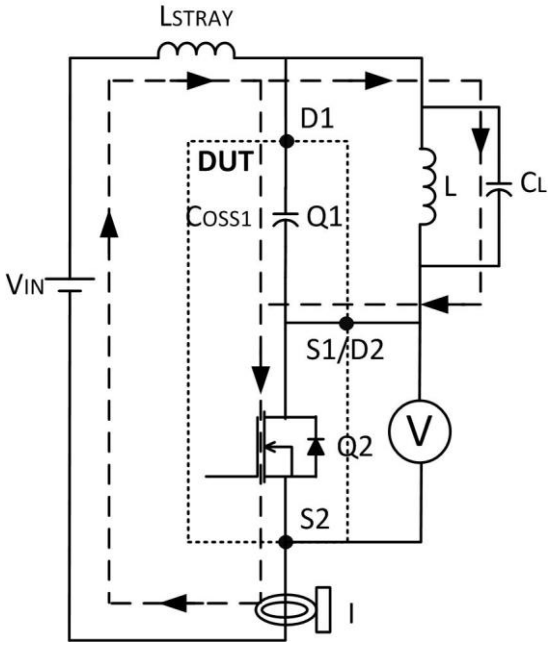


Fig. 4.7: Resonant path during Q_2 turn-on.

There are two methods that can effectively mitigate these resonances and spikes. One is to reduce the total source inductance by paralleling multiple capacitors for the dc voltage link, and by overlaying the copper bus-planes for the current incoming and outgoing path to

cancel the magnetic field. However, with an existing design in which L_{STRAY} cannot be further optimized, another method can be used as reducing the Q_2 switching speed. This can be achieved by either using a large gate resistor or by adding an external capacitor across the gate-source terminal of device Q_2. The latter one is preferred since a larger gate resistor may worsen the gate driver cross talk issue that will be discussed later. However, either approach will sacrifice device switch speed performance and increase switching losses. Fig. 4.8 shows the effect on the current spike, device rise time, and turn-on energy loss with different gate resistances and additional gate-source capacitance, when tested at 75 V, 6 A.

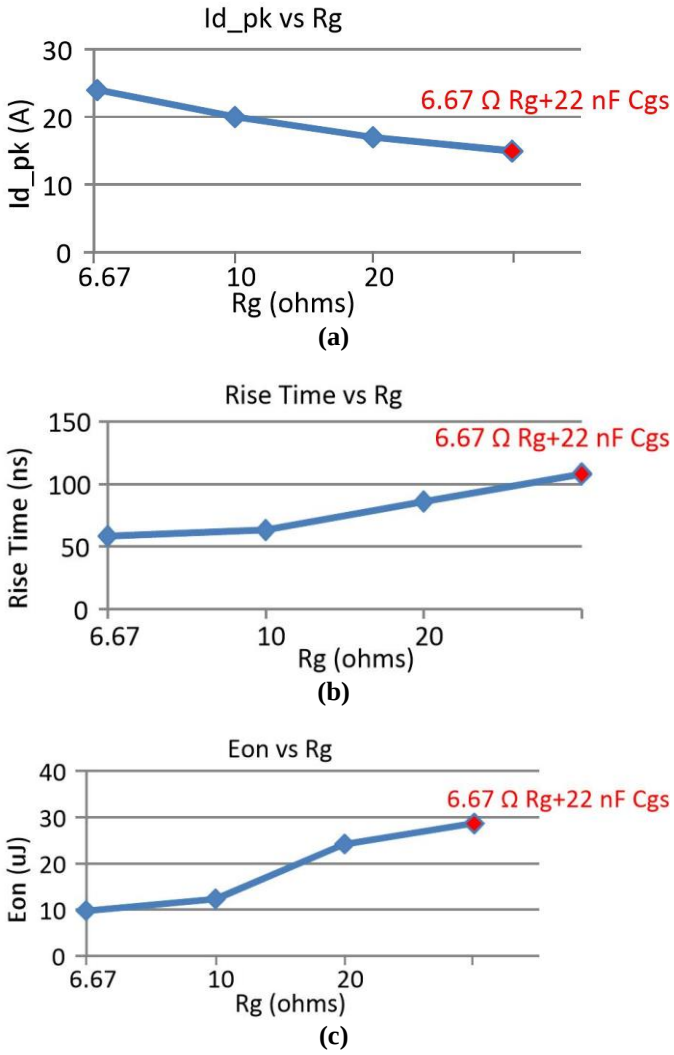


Fig. 4.8: Effects of different gate resistances and gate-source capacitance on: a) drain current spike I_{d_pk}; b) rise time; and c) turn-on loss E_{on}.

4.3.2. Gate-Source Voltage Resonance

It can be observed in Fig. 4.6 that two types of resonance exist on the Q_2 gate-source voltage V_{GS}. The first type resonance (resonance #1) has a much higher frequency (50 MHz) compared to resonance #2 (around 9 MHz). The experiments also show that the peak value of the resonance #1 does not increase as the switching current and voltage levels increase, but for resonance #2, it does. The V_{GS} resonance #1 could be again caused by several phenomena. First is the EMI pollution at the switching transient. Another is the resonance between the gate terminal inductance L_G+L_{GG} and the device input capacitance C_{ISS} which is the sum of C_{GS} and C_{GD}. The third is the resonance among the parallel-connected devices, since there are a total of five device dies connected in parallel inside the module. These resonant paths for parallel-connected dies are shown in Fig. 4.9 as dashed lines and have been discussed in [88]. Fortunately, the resonance #1 occurs during V_{GS} rising stage, and thus it will not exceed the V_{GS} maximum limit. However, the V_{GS} resonance #2 occurs after V_{GS} reaches the steady state value. The resonance peak may exceed the V_{GS} maximum rating and thus damage the device. In Fig. 4.6, it can be seen that this resonance has the same frequency as the I_D and V_{DS} resonances. This occurs when Q_2 is fully tuned on, and the I_D resonance ac component I_{D_R} develops a resonance ac voltage $V_{DS\_ON\_R}$ across the drain-source terminal, as shown in equation (4.4), in which R_{DS_ON} is the on-state resistance of the device. Then the device parasitic capacitances C_{DG} and C_{GS} act as a voltage divider for $V_{DS\_ON\_R}$, and thus the V_{GS} resonance ac component V_{GS_R} is developed. Equation (4.5) shows the relationship between the V_{GS_R} and $V_{DS\_ON\_R}$, and Fig. 4.10 shows the root cause of V_{GS} resonance #2. The V_{GS} voltage resonance at turning off is similar to the turning on and will not be repeated here.

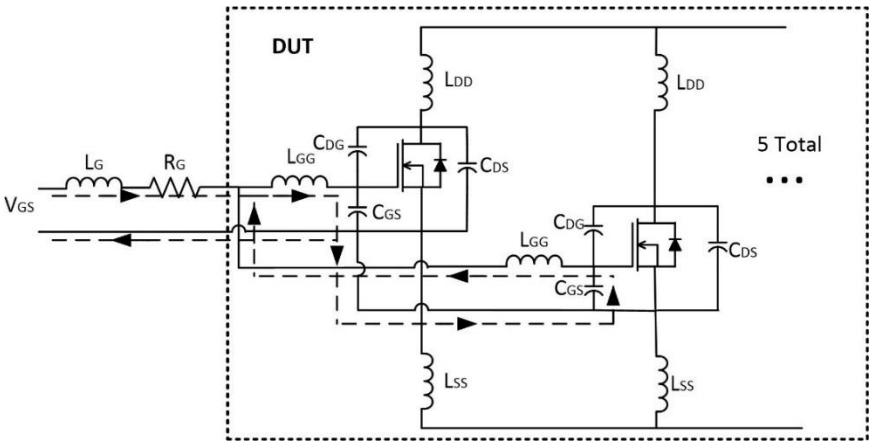


Fig. 4.9: Resonant path of V_{GS} resonance type #1.

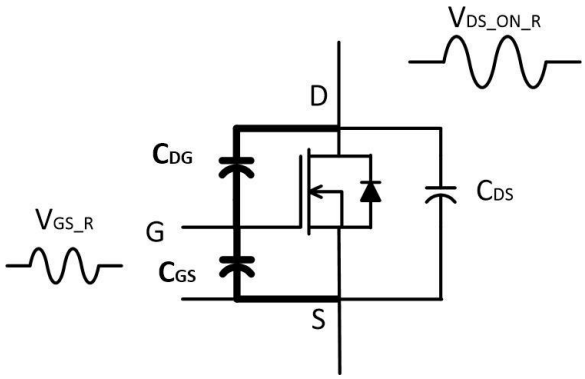


Fig. 4.10: Resonant path of V_{GS} resonance type #2.

$$V_{DS\_ON\_R} = I_{D\_R} * R_{DS\_ON} \tag{4.4}$$

$$\frac{V_{GS\_R}}{V_{DS\_ON\_R}} = \frac{1}{1+\frac{C_{GS}}{C_{DG}}} \tag{4.5}$$

By adding more gate-source capacitance, the V_{GS} resonance #2 can be significantly reduced. The first reason is that the $V_{DS\_ON\_R}$ is reduced because of slower device switching speed. Secondly, it can be observed from equation (4.5) that a larger C_{GS} leads to a smaller V_{GS_R}. In addition, a TVS diode is suggested to connect between the gate and source terminals such that the gate voltage is clamped at a safe level. However, increasing gate-source capacitance does increase the device switching loss.

4.3.3. Phase Leg Cross Talk

For devices with a half-bridge configuration, the high *dv/dt* during fast switching transient of one device affects the operating behavior of the complementary device [89].

Fig. 4.11 shows the mechanism causing the phase leg cross talk when Q_2 is switching and Q_1 is maintained off with a negative gate source voltage V_{GS1}. As shown in Fig. 4.11 (a), when Q_2 is turned on, V_{DS1} of Q_1 quickly increases with a high *dv/dt* rate, which causes a current flowing through C_{GS1} as well as the gate loop. The voltage V_{GZ1} across the gate impedance developed by the gate loop results in that the actual Q_1 gate-source voltage V_{GS1_S} is larger than the supplied gate voltage V_{GS1}. This spurious voltage may partially turn on Q_1 and lead to a current shooting through the phase leg. Similarly, when Q_2 is turned off, as shown in Fig. 4.11 (b), V_{GS1_S} will be lower than V_{GS1}. This case, however, does not cause current shoot through, but the V_{GS1_S} may overstress and damage the gate terminal since SiC devices usually have lower negative V_{GS} rating. To investigate the cross talk issue further, it is necessary to monitor the gate-source voltage of the chip and exclude the influence of the gate terminal inductance as well as the internal gate resistance inside the module, which makes the direct measurement impossible. Instead, the model of Fig. 4.5 is simulated in SABER for exploration. Fig. 4.12 shows the V_{GS1_S} waveform when Q_2 is turned on and off. It can be seen from the waveform that the gate-source voltage of Q_1 reaches as high as 3 V when Q_2 is turned on, which can partially turn on Q_1 and can cause a shoot through. While when Q_2 is turned off, a negative voltage spike is developed on the gate-source voltage of Q_1 and could potentially damage the gate terminal once it exceeds the maximum gate voltage rating.

The cross talk issue can be mitigated by reducing the device switching speed, which can be achieved by either increasing the gate resistance or adding additional gate-source capacitance. The latter is more effective since increasing gate resistance results in higher voltage difference between the gate driver side and the gate terminal of the device die.

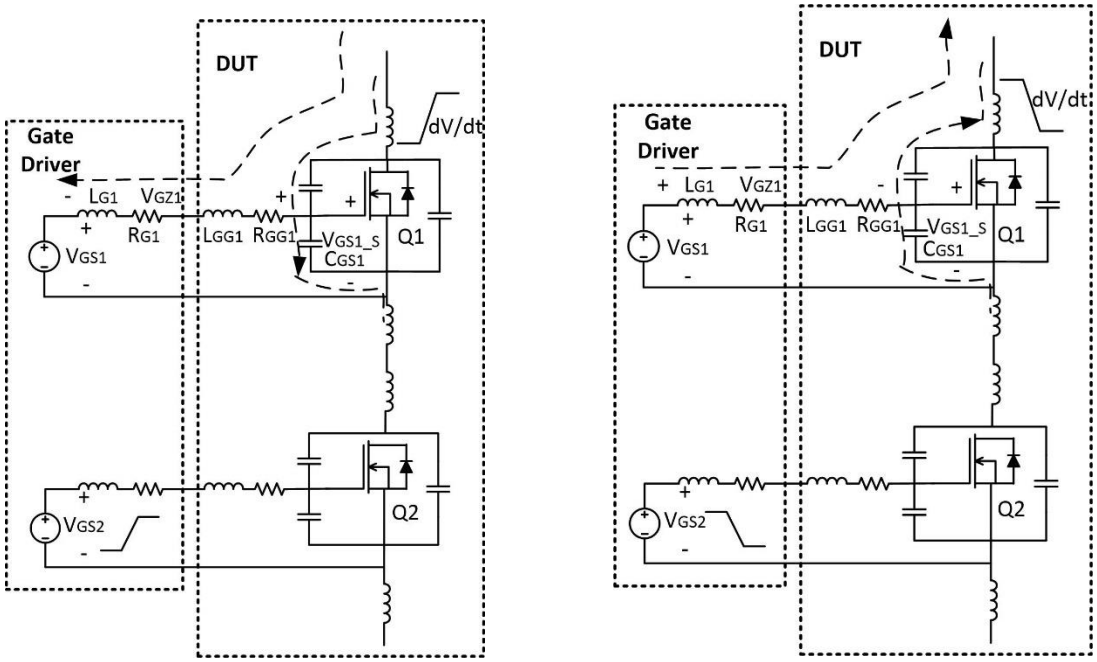


Fig. 4.11: Mechanism of causing cross talk during: a) Q_2 turn-on; b) Q_2 turn-off.

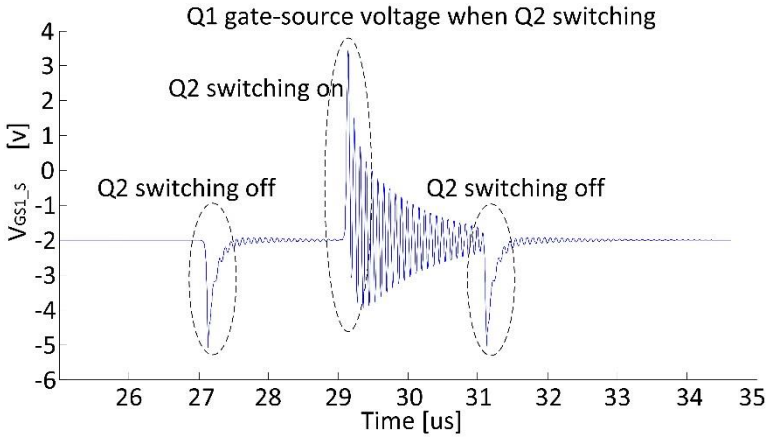


Fig. 4.12: Q_1 gate-source voltage during Q_2 switching.

4.3.4. Gate-Driver Noise

For the device gate driver, it is common to use fiber-optics or opto-couplers to provide isolation between the controller and the devices. However, both of these two components can be affected by the device switching noise and generate a faulty triggering signal for the gate driver IC, which in turn can switch the device by fault. Fig. 4.13 shows the circuit diagram of a gate driver with an opto-coupler and the conceptualized waveforms during the switching transition. The opto-coupler has a parasitic capacitance between its input and

output, denoted as C_{CM} in Fig. 4.13. When the low side switch Q_2 is turned off and blocks the voltage of V_C at t_1, the potential of the source terminal of Q_1 is raised to *Vc*, which results in a common mode noise of V_{CM} with a positive *dv/dt* rate between the input and output side of the opto-coupler. This noise generates a voltage drop on the output of the opto-coupler *G_o* when *G_o* is at the logic high state, even with no level change on the opto-coupler input *G_ctrl*. This voltage drop tends to turn on Q_1 if it exceeds the threshold voltage of the gate driver IC, assuming that the gate driver IC outputs an inverting signal of its input. Similarly, at t_2, when a negative *dv/dt* is developed on V_{CM}, *G_o* tends to turn off Q_1 when it is at the active low state. Opto-couplers usually have a limited maximum *dv/dt* tolerance, above which a fault switching action may occur. Fig. 4.14 shows the experimental waveforms, in which the opto-coupler turns off the device due to the common mode noise, even though the control signal is kept high.

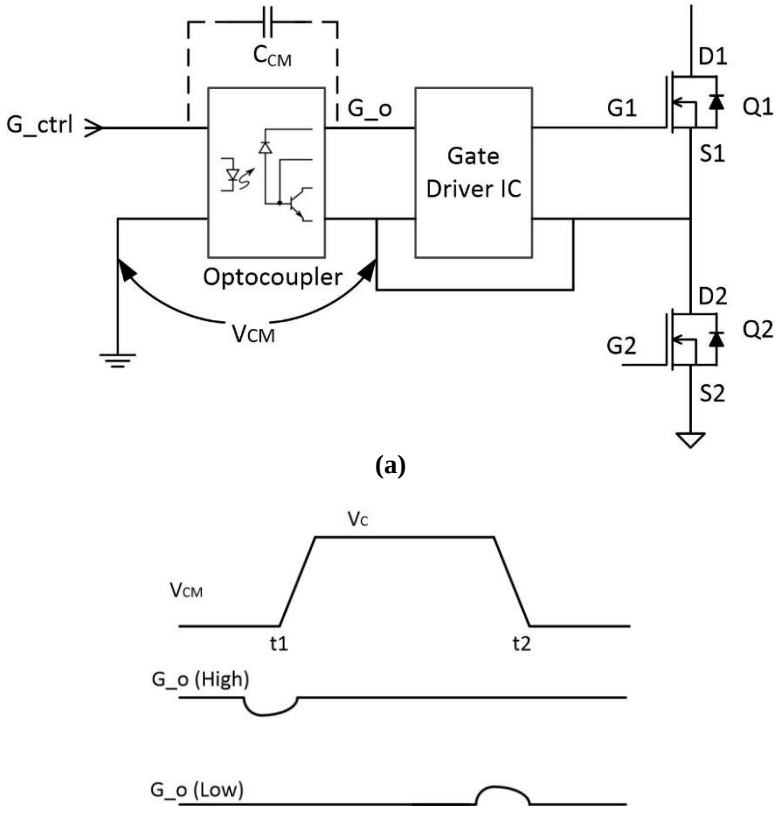


Fig. 4.13: Gate driver noise issue: a) circuit diagram of a gate driver with an opto-coupler; and b) conceptualized waveforms during the switching transition.

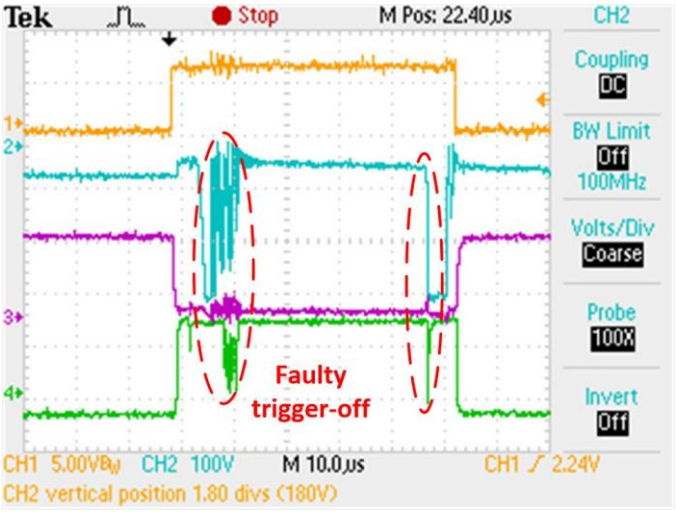


Fig. 4.14: Experimental waveforms of the gate driver noise issue: CH1 (2.5 V/div)-control signal *G_ctrl*; CH2 (50 V/div)-common mode noise V_{CM}; CH3 (10 V/div)-opto-coupler output *G_o*; CH4 (10 V/div)-gate signal V_{GS1}.

By reducing the device switching speed, the *dv/dt* rate of V_{CM} is reduced, and thus the fault triggering action can be avoided.

4.3.5. Electromagnetic Interference (EMI)

Inside the device package, there exists a small capacitance between the copper trace on the substrate and the mounting baseplate [83]. In addition, the module baseplate is mounted on a heatsink, which is usually grounded for safety. Therefore, there will be a parasitic capacitance C_H between the device module and the heatsink, which provides a common mode current flowing path when the device is switching and generates EMI. For a high-power-rated device, the package has a large area of copper trace on the substrate to carry high current, and thus C_H is larger, leading to a more severe EMI issue. Fig. 4.15 shows the common mode current flowing path.

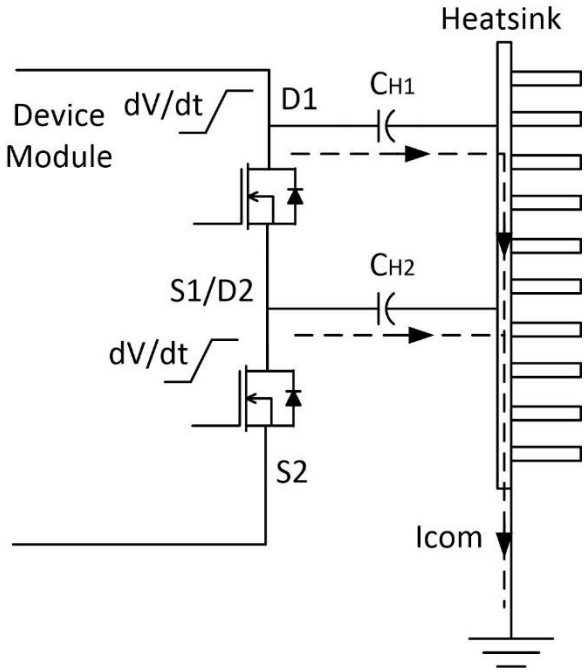


Fig. 4.15: Common mode current flowing path.

It is important to estimate the C_H value such that the EMI can be evaluated. The DUT of CAS100H12AM1 uses Si_3N_4 as the substrate material [90], which has the relative permittivity ε_r of 7.5. The substrate thickness d is around 0.38~0.63 mm for the isolation purpose [91]. Fig. 4.16 shows the internal layout of DUT package, from which the copper trace area A_C of drain terminal is estimated to be 5 cm^2 for both the high- and low-side switches. The parasitic capacitance C_H can be then estimated as equation (4.6), in which ε_0 is the permittivity of vacuum. The heatsink is directly attached to the ground potential, indicating a low ground loop inductance. Assume a 100 nH ground loop inductance here for preliminary analysis. Fig. 4.17 shows the spectrum of common mode current I_{com} during Q_2 switching for the two cases of with and without external C_{gs} connected to the device gate-source terminal. An additional 150 nF C_{gs} increases the rising and falling time of the device from 54 ns and 35 ns to 426 ns and 219 ns respectively. It can be seen that slower device switching speed leads to lower common mode current.

$$C_H = \varepsilon_r \varepsilon_0 \frac{A_C}{d} = 90\,pF \tag{4.6}$$

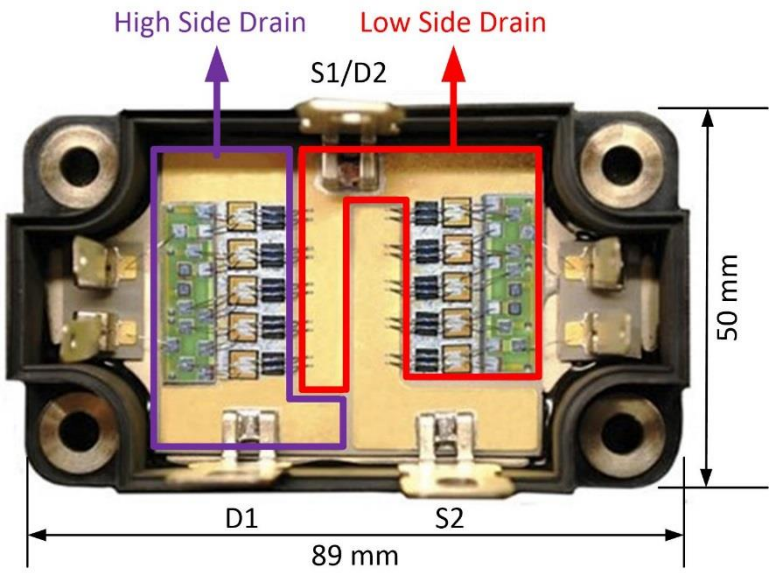


Fig. 4.16: Internal layout of CAS100H12AM1.

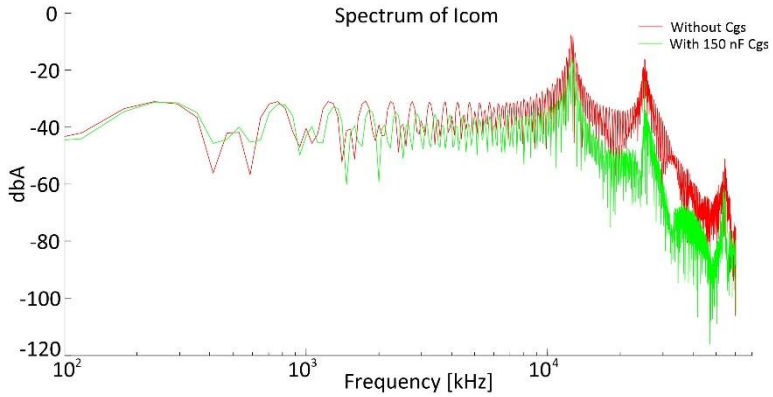


Fig. 4.17: Spectrum of common mode current I_{com}.

4.4. Conclusions

Due to the high *dv/dt* and *di/dt* rates as well as the circuit parasitic elements, SiC devices suffer from many issues, which prevent the device from fully utilizing either the SOA or the maximum switching speed. To explore these issues, a test fixture was built to characterize a 1200 V/100 A SiC MOSFET. The switching waveforms were analyzed, and the detailed circuit model that considers all the parasitic elements was developed. Based on these, all the fast switching issues, including device current and voltage resonances and spikes, gate terminal resonance, cross talk, gate driver noise, and EMI, were exploited and analyzed. The solutions include increasing the gate resistance or adding additional gate-source capacitance,

but both of these are followed by side effects of slower switching speed and higher switching loss.

For the Dyna-C SST, it has been found that using SiC devices can potentially help mitigate the diode reverse recovery issue and lower the device switching loss. However, due to its hard-switching feature, designing the Dyna-C SST with all SiC devices leads to side effects that have been covered in this chapter. To address these issues, the switching speed of SiC devices have to be slowed down for the Dyna-C, which may in turn increase the switching loss to a level comparable with the Si design. As a result, implementing the Dyna-C SST with SiC devices does not gain any benefits, while the unit cost will become much higher. It is desired to use soft-switching techniques, which significantly reduce the *dv/dt* and *di/dt* rates at the switching transition and thus eliminate the above state issues and improve the overall converter efficiency. Therefore, the soft-switching SST, which retains all the benefits of the single-stage Dyna-C SST but with all the devices operated under soft-switching conditions, seems to be a very attractive solution. Two approaches will be taken to implement the soft switching, a zero-current-switching (ZCS) type and a zero voltage-switching (ZVS) type, which will be presented in the following two chapters.

CHAPTER 5: ZERO-CURRENT-SWITCHING SOLID STATE TRANSFORMER

5.1. Introduction

As stated in the previous chapter, the Dyna-C converter suffers from various issues due to the hard-switching conditions. A design with SiC devices to address some of the issues, however, leads to severe side effects of various resonances, spikes, noises, and EMI, due to the extreme high *di/dt* and *dv/dt* rates associated with the fast switching speed. An effective way of successfully managing all these issues is expected to be through the use of soft-switching techniques. Therefore, two soft-switching solid state transformer topologies, that use zero-current-switching (ZCS) and zero-voltage switching (ZVS) principles respectively, are proposed in this research. This chapter will present the topology of the proposed zero-current-switching solid state transformer, while the ZVS one will be presented in the next chapter.

5.2. Topology

The topology of the zero-current-switching solid state transformer for three-phase ac/ac conversion is shown in Fig. 5.1. The topology consists of: 1) CSI bridges on the input and output side implemented with SCRs, or RB-IGBTs, or diodes in series with IGBTs; 2) a high-frequency transformer; 3) terminal LC filters; and 4) a ZCS auxiliary resonant circuit. The ZCS auxiliary resonant circuit consists of L_r, C_r, S_{r1}, and S_{r2}. The operating principle of transferring energy from the input side to the output through the high-frequency transformer is the same as that for the Dyna-C. Whenever a switching transition is required, the auxiliary resonant circuit starts operating to create a zero-current-switching condition for the main devices. Since the auxiliary circuit is outside the energy transfer path, the rating of the auxiliary circuit is minimal. In addition, the active switches S_{r1} and S_{r2} of the auxiliary circuit are also switched under ZCS condition. It should be noted that since all devices are turned

off at ZCS, half-controlled devices such as SCRs can be used, which have a higher power rating than the MOSFETs and IGBTs.

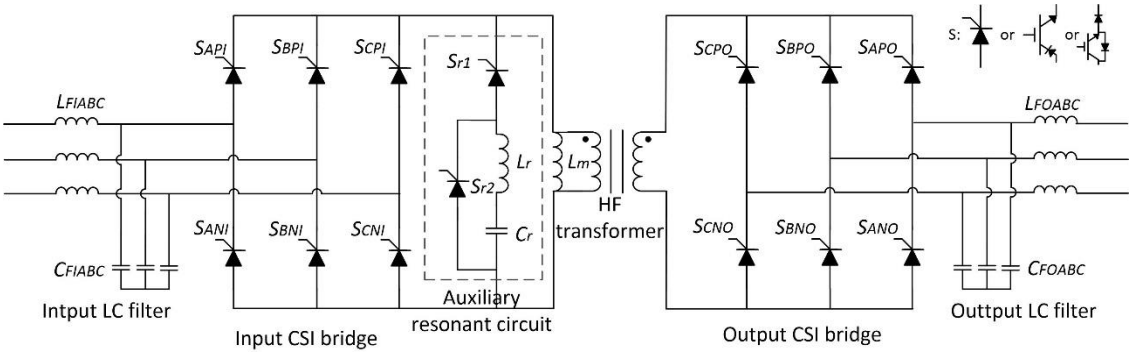


Fig. 5.1: Topology of the ZCS solid state transformer for three-phase ac/ac conversion.

5.3. Principle of Operation

The operating principle of transferring energy from the input to the output is the same as for the Dyna-C. The device duty cycles are controlled such that the required charge is delivered to specific input/output terminals to maintain sinusoidal voltages. The transformer magnetizing current is regulated at a constant value to act as a constant current source. The transformer works similarly to the flyback transformer in that the input side delivers energy to it and then it releases energy to the output side. The only difference of the ZCS topology from the hard-switching Dyna-C is the operation at the switching transitions. The Dyna-C devices are operated under hard-switching conditions such that the transformer magnetizing current transfers from one device pole to another. However, for the ZCS topology, the auxiliary resonant circuit acts as a temporary energy buffer during the switching transition, which brings the current of the main outgoing device to zero to achieve ZCS turning off for this device, and slowly increases the current of the main incoming device from zero to achieve ZCS turning on. This section will only cover the operation of ZCS transitions during device switching.

Assume a phase-leg transition in which S_{API} is about to turn off and S_{BPI} is to turn on, while S_{CNI} is kept on during the transition, i.e., the transformer magnetizing current I_m is diverged from the input phase pair A-C to B-C. Fig. 5.2 shows the operating modes for this

transition with a simplified circuit, in which the phase-to-phase input voltages are represented by dc sources and the transformer magnetizing current is represented by a current source I_m. Fig. 5.3 shows the relative waveforms during this transition.

In mode 0, S_{API} is conducting while S_{BPI}, S_{r1}, and S_{r2} are off. The input line-to-line voltage V_{ACI} is therefore directly connected to the current source I_m. Assume that the resonant capacitor has an initial voltage of V_{cr0}. The ZCS turn-off of S_{API} starts from mode 1 by turning on S_{r1} under ZCS condition. If V_{cr0} is larger than V_{AC}, the current through L_r will increase from zero, and thus I_A will decrease from I_m. The state equations at this mode are shown in equation (5.1). Solving equation (5.1) gives the expressions of i_A and i_r in equation (5.2). To ensure a ZCS turn-off condition for S_{API}, the current of i_A should be able to reach zero. Therefore, the initial capacitor voltage V_{cr0} should satisfy equation (5.3). Mode 1 ends when i_A drops to zero while i_r increases to I_m, then S_A can be turned off under ZCS condition. In mode 2, the constant current of I_m charges C_r, thus v_{cr} continuously decreases. Mode 2 ends when v_{cr} satisfies equation (5.4), which ensures a ZCS turn-off condition for the incoming conducting switch S_B. Mode 3 starts by turning on S_B. It should be noted that since i_r cannot drop sharply due to the presence of L_r, the current i_B will slowly increase from zero, indicating a ZCS turn-on. Mode 3 ends when i_B increases to I_m, and therefore i_r drops to zero. Then S_{r1} is turned off at ZCS. In mode 4, the current I_m flows through S_{BPI} and V_{BC}. S_{r2} is turned on under ZCS condition, formulating a L_r-C_r resonant circuit to reset the capacitor voltage. This mode ends when the current i_r reaches zero. As a result, S_{r2} can be turned off under ZCS condition, and the capacitor voltage polarity is flipped. Then the transformer magnetizing current successfully transferred from S_{API} to S_{BPI}, with ZCS conditions for both S_{API} turning off and S_{BPI} turning on. Next switching transition can be started in the same manner. The waveforms of i_A, i_B, i_r, and v_{cr} are shown in Fig. 5.2. It should be noted that the inter-bridge transition, i.e., transitions from the primary bridge to the secondary, has the same operating principle, except that the voltage polarities of the two sources are different from each other. Since the phase-leg current is driven up and down with a finite *di/dt* rate,

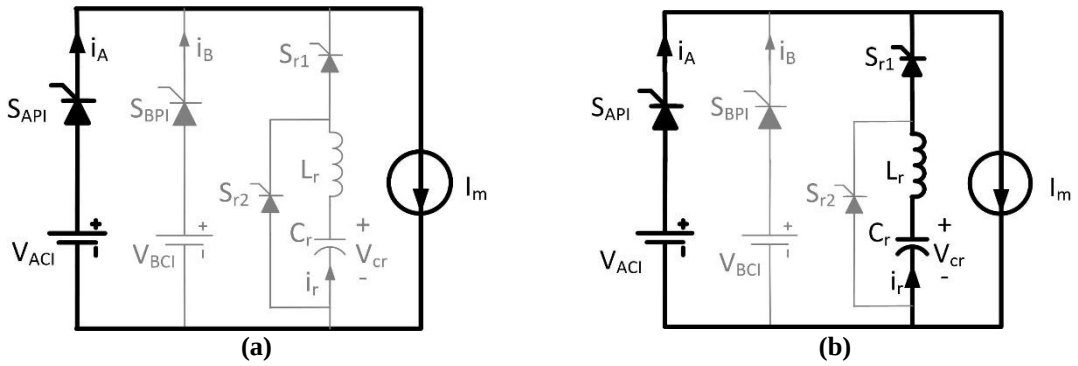
the leakage trapped energy is automatically managed in this proposed ZCS topology, which indicates that no extra leakage management transition mode is required. However, the transformer leakage will slow down the ZCS transitioning process.

$$\begin{cases} i_A + i_r = I_m \\ V_{AC} = v_{cr} - v_{Lr} \\ i_r = -C_r \dfrac{dv_{cr}}{dt} \\ v_{Lr} = L_r \dfrac{di_r}{dt} \end{cases} \text{ with the initial conditions of } \begin{cases} v_{cr}(t=0) = V_{cr0} \\ i_r(t=0) = 0 \end{cases} \tag{5.1}$$

$$\begin{cases} i_A = I_m - (V_{cr0} - V_{AC})\sqrt{\dfrac{C_r}{L_r}}\, sin\left(\sqrt{\dfrac{1}{L_r C_r}}t\right) \\ i_r = (V_{cr0} - V_{AC})\sqrt{\dfrac{C_r}{L_r}}\, sin\left(\sqrt{\dfrac{1}{L_r C_r}}t\right) \\ v_{cr} = V_{AC} + (V_{cr0} - V_{AC})cos\left(\sqrt{\dfrac{1}{L_r C_r}}t\right) \end{cases} \tag{5.2}$$

$$V_{cr0} > V_{AC} + I_m\sqrt{\frac{L_r}{C_r}} \tag{5.3}$$

$$v_{cr} > V_{BC} + I_m\sqrt{\frac{L_r}{C_r}} \tag{5.4}$$



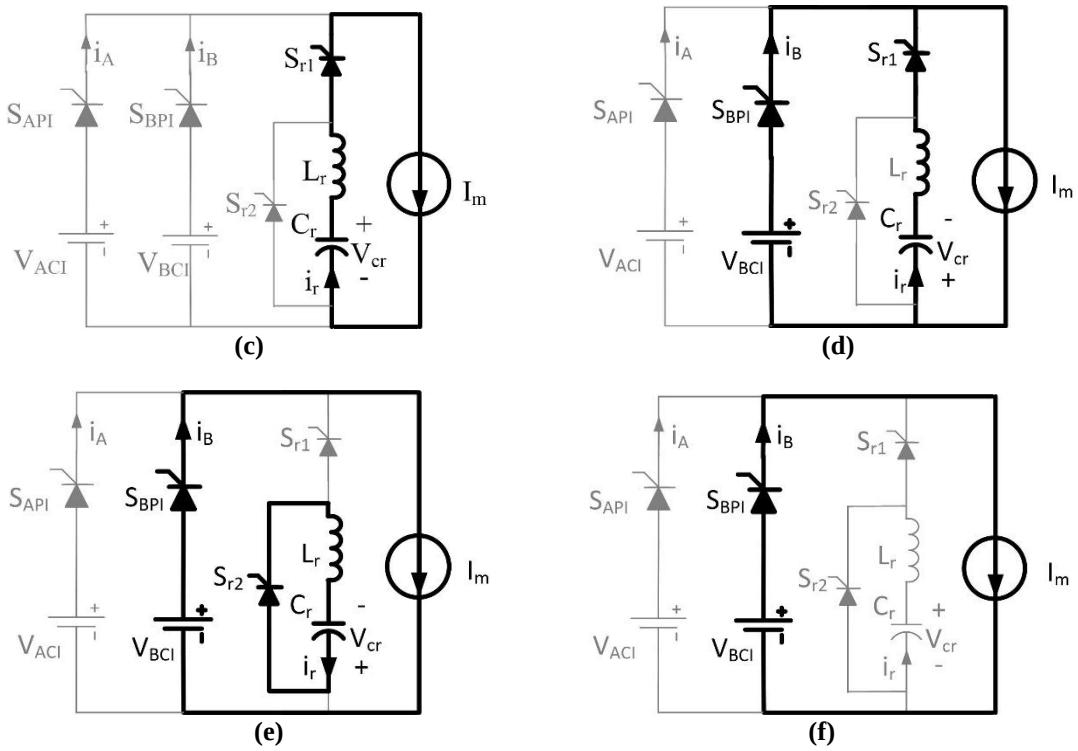


Fig. 5.2: Operating principle for phase-leg transitions: a) mode 0; b) mode 1; c) mode 2; d) mode 3; e) mode 4; and f) mode 5.

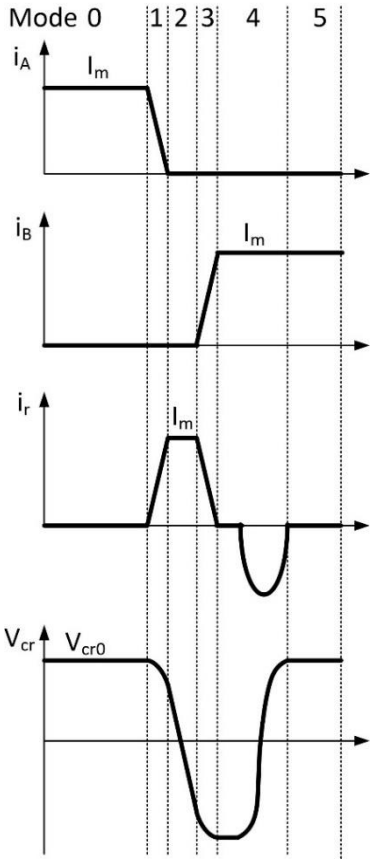


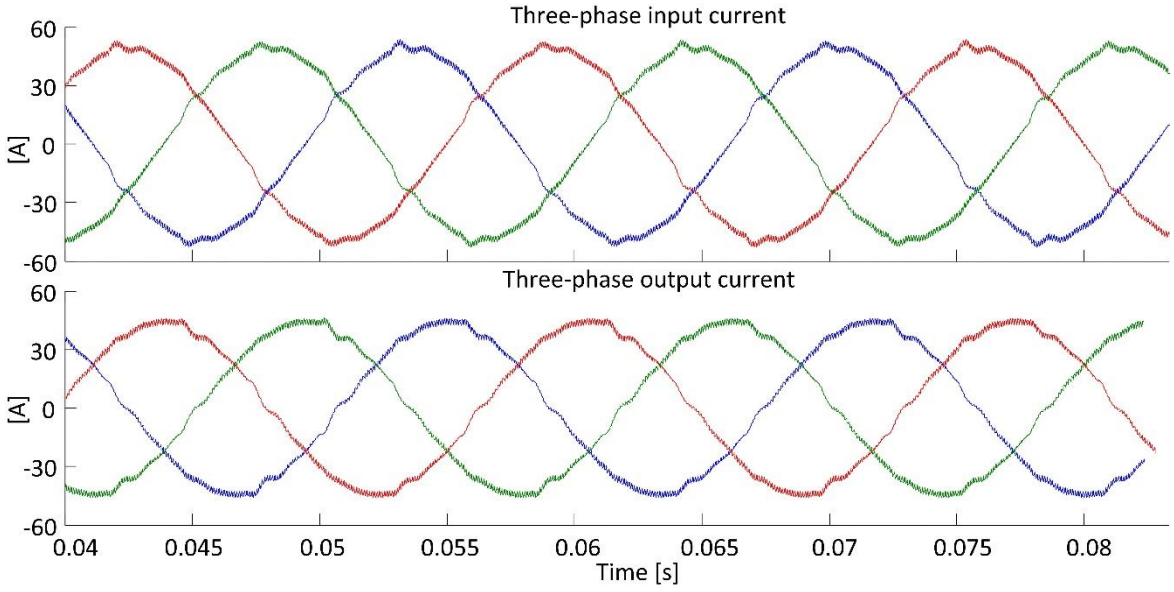
Fig. 5.3: Relative waveforms at the transition.

5.4. Simulation Results

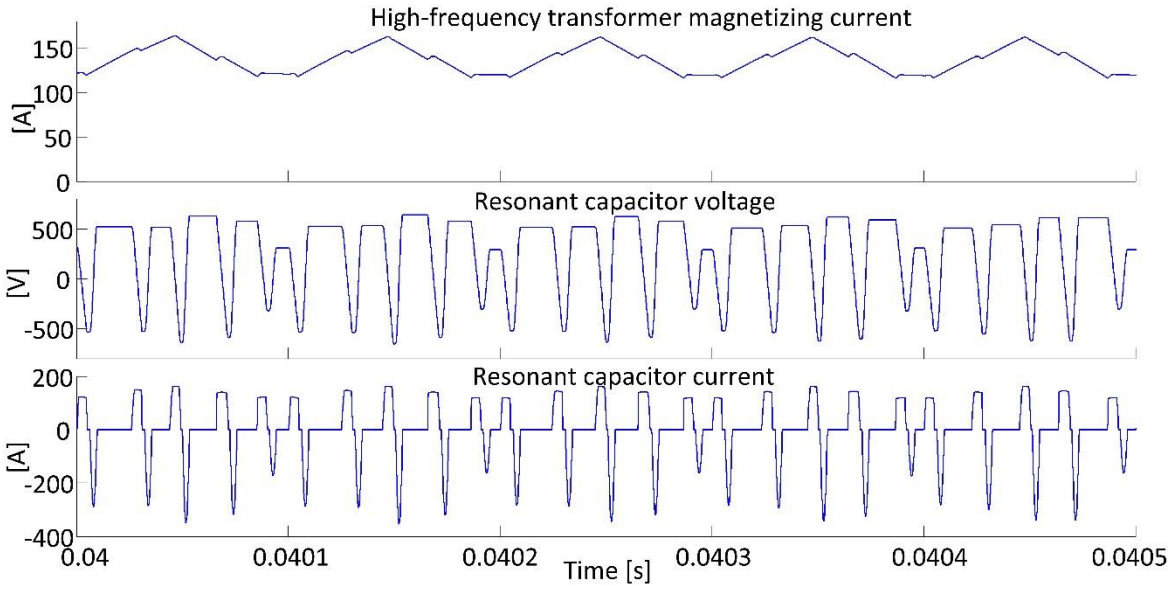
The operation of the three-phase ac/ac ZCS solid state transformer is validated through simulation, with the component parameters shown in Table 5.1. Fig. 5.4 shows the simulation waveforms of three-phase input and output currents, high-frequency transformer magnetizing current, as well as voltage and current of the resonant capacitor.

Table 5.1: Parameters of the simulated zero-current-switching solid state transformer.

Power rating	Input/output voltage	Switching Frequency	Magnetizing Inductance
10 kVA	208 V	10 kHz	200 µH
Filter Capacitor	Filter inductor	Resonant capacitor	Resonant inductor
60 µF	150 µH	0.6 µF	2 µH



(a)



(b)

Fig. 5.4: Simulation waveforms of the ZCS solid state transformer: a) three-phase input and output currents; and b) high-frequency transformer magnetizing current, voltage and current of the resonant capacitor.

5.5. Discussion

By introducing an auxiliary resonant circuit, the *di/dt* rate of all the main devices is controllable during switching transitions. Ideally, all the main devices can be operated under ZCS conditions with no switching loss. In addition, since the device current can be automatically driven to zero, half-controlled devices such as SCRs can be used to implement the converter, which is beneficial to design for high-power applications. Finally, since the auxiliary resonant circuit always drives the device current down to zero before it turns off, the energy trapped within the transformer leakage inductance is simultaneously managed during bridge-to-bridge transitions, which removes the additional converter state for the leakage management and eliminates the associated voltage stress issue of the hard-switching Dyna-C.

However, it should be noted that at each switching transient, the auxiliary resonant circuit needs to go through all the modes of operation shown in Fig. 5.2. This means that the auxiliary circuit needs to be activated five times within one converter switching cycle. Even though all devices (including the auxiliary devices) are operated under ZCS conditions, the converter has to spend considerable time on the auxiliary resonant circuit operation, which

actually reduces the duty cycles of the main devices for energy transferring from the input to the output. Another issue is that the reverse recovery of the devices contributes some switching loss and develops trapped energy within the transformer leakage, which subsequently creates voltage spikes across the devices once the diode is snapped off. Considering all these side effects, another soft-switching topology, which is a zero-voltage-switching solid state transformer, will be proposed. It demonstrates much more attractive benefits with all devices switched under ZVS conditions.

5.6. Conclusions

Considering all the hard-switching issues described in previous chapters, soft-switching circuit topologies are proposed to implement the solid state transformer. This chapter introduced the topology of the zero-current-switching solid state transformer, in which all the main devices are operated under ZCS conditions. The auxiliary resonant circuit provides ZCS transitions for turning off the outgoing devices and turning on the incoming devices, and it makes the *di/dt* rates of all devices controllable, with the auxiliary devices also being operated under ZCS conditions. Since the current through all the main devices can be automatically driven to zero, half-controlled devices such as SCRs can be used to implement the converter. The ZCS transition also successfully manages the energy trapped within the transformer leakage inductance, without using an additional leakage management state as the Dyna-C. However, the proposed circuit does have some significant drawbacks such as reducing the duty cycle of main devices over one switching cycle, as well as the losses and voltage spikes associated with the reverse recovery. Therefore, as an alternative, a ZVS solid state transformer topology will be proposed in the next chapter.

CHAPTER 6: ZERO-VOLTAGE-SWITCHING SOLID STATE TRANSFORMER

6.1. Introduction

Chapter 3 and chapter 4 show issues associated with hard-switching for the Dyna-C, and the challenges of designing with SiC devices due to high *di/dt* and *dv/dt* rates. It shows the necessity of operating the devices under soft-switching conditions to decrease the loss, mitigate the spikes and resonances, reduce the EMI, and improve the device reliability. Although a ZCS solid state transformer topology has been proposed in chapter 5 to show the success of controlling the device *di/dt* rates and achieving ZCS conditions for all the main devices, some side effects such as the reduction of main devices' duty cycle and reverse recovery effects impose challenges on implementing such a converter.

As an alternative, this chapter presents a zero-voltage-switching topology to implement the solid state transformer. The patent pending topology, named as S4T (i.e. soft-switching solid state transformer), has a simple and symmetrical architecture, minimal device and component count in the power flow path (similar to the Dyna-C in chapter 3), with small-rated auxiliary components that enable the soft switching property. Unlike the DAB converter, the S4T realizes ZVS for all its main devices over the entire load range, and features controlled *dv/dt* and *di/dt* rates. Further, it can realize dc, single- or multi-phase ac on the input/output at arbitrary frequencies and power factors with sinusoidal voltages and low EMI. It shows simple control and benign shut down under fault and failure modes, and is relatively insensitive to key parameters such as transformer leakage inductance. Similar to the Dyna-C, by eliminating components such as electrolytic capacitors, it can also realize higher power density and longer life. Finally, it holds the promise of achieving high efficiency, particularly as it scales up in voltage and power. It provides the simplicity of single-stage SSTs, with the control attributes of the three-stage SSTs, with higher efficiency, lower *dv/dt* rate, and an ability to scale that seems unique. In short, the proposed S4T

topology retains all the benefits of the Dyna-C to implement the solid state transformer, while eliminating all of its issues by operating the devices under ZVS conditions.

6.2. A ZVS Auxiliary Resonant Circuit for the Dyna-C

The ZVS resonant circuit for the voltage source converter (VSC) has been widely explored in the past [92]-[95]. The ZVS operation is realized by connecting an extra capacitor in parallel with each device. As shown in Fig. 6.1 (a), the extra parallel connected capacitor slows down the rising of the device terminal voltage when it is turned off, leading to a significant reduced turn-off loss. The current source I_L in the figure represents the load. Whenever the device needs to be turned on, the voltage of the capacitor is driven to zero by an inductor and a voltage source as shown in Fig. 6.1 (b). Consequently, the anti-parallel diode conducts and thus creates a ZVS turn-on condition for the main device.

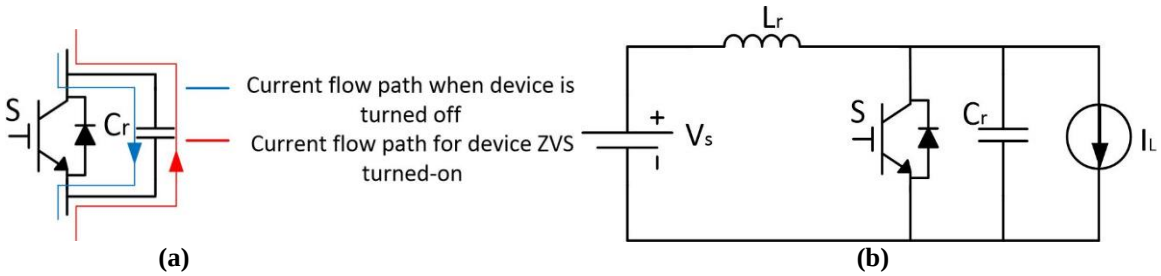
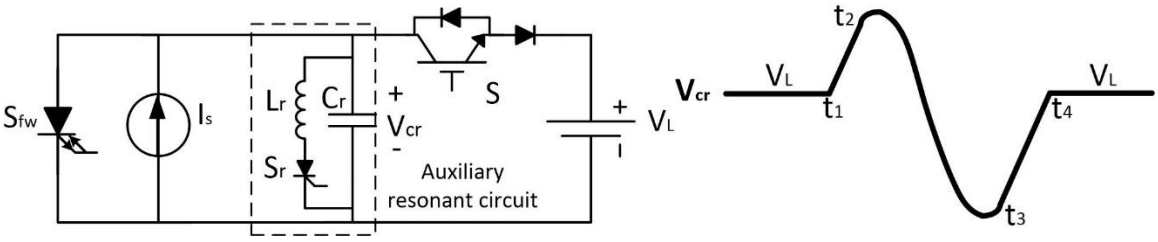


Fig. 6.1: ZVS switching for the voltage source converter: a) an extra capacitor connected in parallel with the device; and b) equivalent circuit during each switching transition [92].

Equivalently, for a current source converter, ZVS switching conditions can also be created for the main devices with a proposed auxiliary resonant circuit. To demonstrate the ZVS operating principle for CSI devices, Fig. 6.2 (a) shows the equivalent circuit for each switching transition, and Fig. 6.2 (b) shows the conceptualized waveform. The proposed auxiliary resonant circuit, consisted of L_r, C_r, and S_r, is circled by a dashed line in Fig. 6.2 (a). In the circuit, the main device is S and the load is modeled as a constant voltage source V_L for each switching transition. Device S_{fw} is used to freewheel the constant current I_s when not delivering energy to the load. When device S is conducting, the current source I_s directly feeds the load. Therefore, the capacitor voltage V_{cr} equals to V_L before t_1. Whenever S is turned off, V_{cr} slowly increases from t_1 due to the charging effect of I_s. As a result, the voltage

across the device *S*, which equals to the difference between V_{cr} and V_L, has a significantly reduced *dv/dt* rate, indicating a ZVS condition for turning off *S*. The charging of C_r by I_s continues until t_2, then a resonance occurs between L_r and C_r by turning on S_r. The resonant operation ends at t_3, and V_{cr} reaches to a value lower than V_L. The charging time between t_1 and t_2 should be long enough such that the energy loss during the resonant operation is compensated, and ensure that V_{cr} resonates back to be at a value lower than V_L. Thereafter, the series-connected diode blocks the voltage and the device *S* can be gated on. The current I_s does not flow through *S* until V_{cr} increases to a value equal to V_L at t_4, indicating a ZVS condition for turning on *S*. It should be noted that device S_r is switched on and off under ZCS condition due to the series connected L_r.



(a) **(b)**

Fig. 6.2: ZVS switching for the current source converter: a) equivalent circuit during each switching transition, and b) conceptualized waveform of V_{cr}.

From the above description, it can be seen that the proposed auxiliary resonant circuit, consisting of L_r, C_r, and S_r, provides ZVS conditions for the main device *S* of a current source inverter (CSI) during both turn-on and turn-off transitions. This auxiliary resonant circuit will be integrated to the isolated three-phase, four-quadrant flyback cycloconverter that was introduced in [77], resulting in a topology of the proposed S4T. It should be noted that the proposed auxiliary resonant circuit can also be integrated with any type of current source converter to achieve ZVS switching for their main devices.

6.3. Topology of the S4T

Fig. 6.3 shows the topology for the three-phase S4T, which comprises four elements: 1) an air-gapped high-frequency transformer to provide galvanic isolation and a limited amount of energy storage; 2) current-source inverter (CSI) bridges to interface sources and loads; 3)

terminal LC filters for suppressing harmonics; and 4) auxiliary resonant circuits to provide ZVS switching conditions for all the main devices. The CSI bridges are configured with switches that conduct current in one direction but block voltage in both directions, and can be implemented with either an IGBT in series with a diode, or a reverse blocking IGBT (RB-IGBT), with the latter providing lower losses and more compact converter design. The auxiliary resonant circuit comprises an active device, an inductor, and a capacitor. The auxiliary active device can be implemented with an IGBT in series with a diode, a RB-IGBT, or a thyristor (at least in principal), with the device operated under zero-current-switching (ZCS) condition. For real transformers, the finite transformer leakage inductance would interfere with the resonant transitions. As a result, the use of two auxiliary resonant circuits is proposed, one for each bridge.

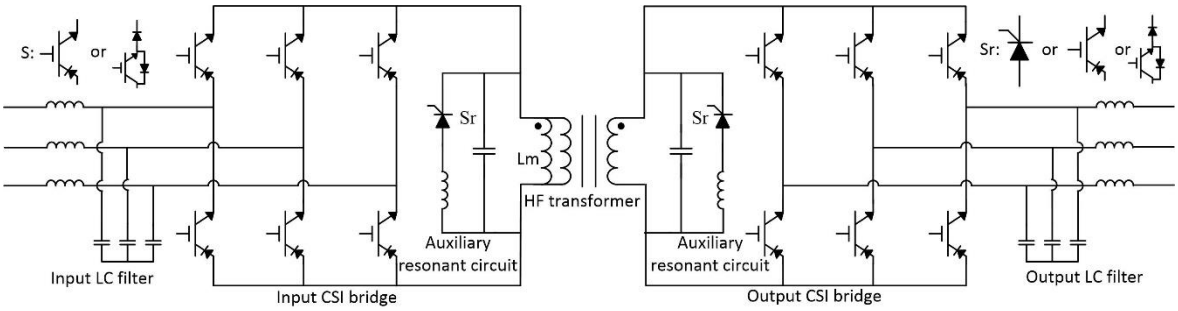


Fig. 6.3: Topology for the three-phase soft-switching solid state transformer (S4T).

Even though the circuit only requires 12 main active devices and two low-rated auxiliary devices, the S4T can provide all functionality of the more complex three-stage SST in a single-stage topology, including: 1) bi-directional power flow control; 2) independent input and output VAr injection; 3) voltage step-up and step-down; 4) arbitrary power factor and frequency (including dc) for the input and the output. The S4T topology possesses several key advantages that conventional SST solutions do not have: 1) no bulk dc energy storage capacitors; 2) no inrush current under start-up, shut-down, and fault conditions; 3) fast dynamic performance with direct current control; 4) modular structure to scale to high-voltage and high-power levels; 5) ZVS soft-switching conditions for all the main devices over the full load range.

6.4. Topology Variations

It should be noted that the S4T could be implemented for a variety of conversion functions. These include dc/dc, single-phase ac to dc, single-phase ac to three-phase ac, and multi-port structures. The device topology and configuration remains the same for both dc and ac sources/loads, and the power transfer with ZVS is purely achieved through control. As a result, the proposed S4T circuit acts as a universal ZVS power converter. Figs. 6.4-6.9 show some of the possible topology variations. The three-phase four-wire configurations shown in Figs. 6.6-6.8 can be used to connect three-phase unbalanced loads, in which a virtual neutral connection is provided. Two tri-port topologies are shown in Fig. 6.8 and Fig. 6.9. The three sources/loads are all isolated by the three-winding transformer in the topology of Fig. 6.8. Although the tri-port topology of Fig. 6.9 is exactly the same as that of Fig. 6.3, it can interface PV, battery, and the three-phase grid as shown in the figure. In this configuration, the PV panels and the battery can be directly grounded without any constraints, due to the isolation provided by the high-frequency transformer. Obviously, more and more sources/loads can be added to the topology by adding additional transformer windings and converter bridges, while the magnetizing current level will increase proportionally to the number of converter bridges.

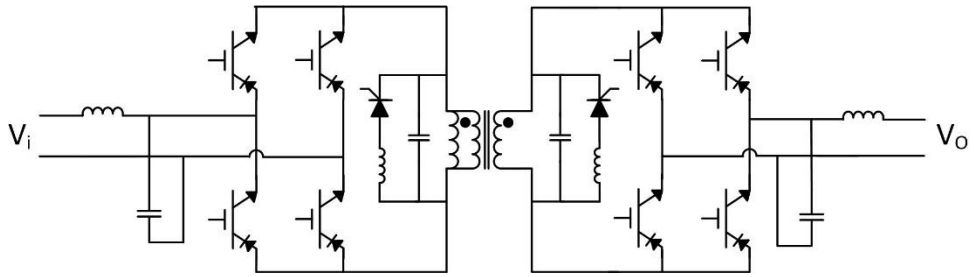


Fig. 6.4: Topology for dc or single-phase ac to dc or single-phase ac (excluding single-phase ac/ac conversion).

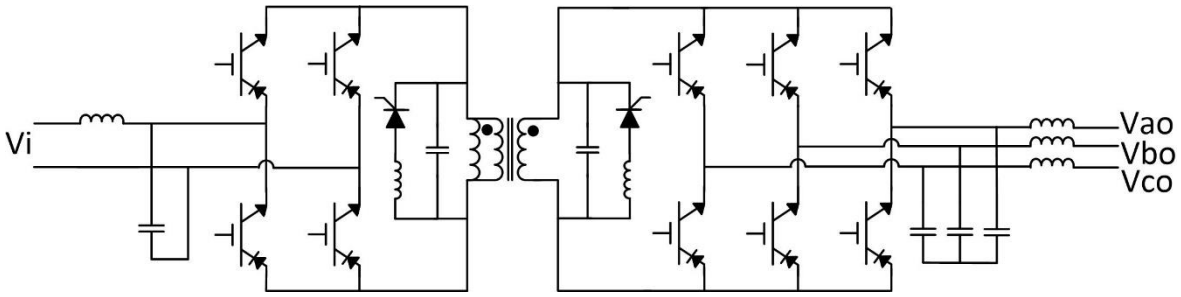


Fig. 6.5: Topology for dc or single-phase ac to three-phase ac.

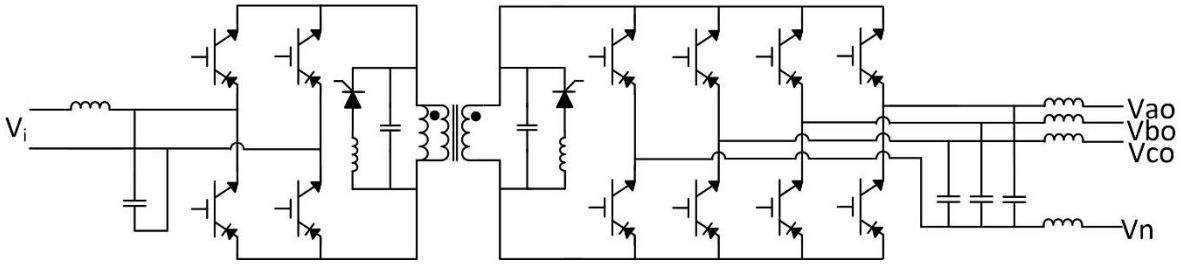


Fig. 6.6: Topology for dc or single-phase ac to three-phase four-wire ac.

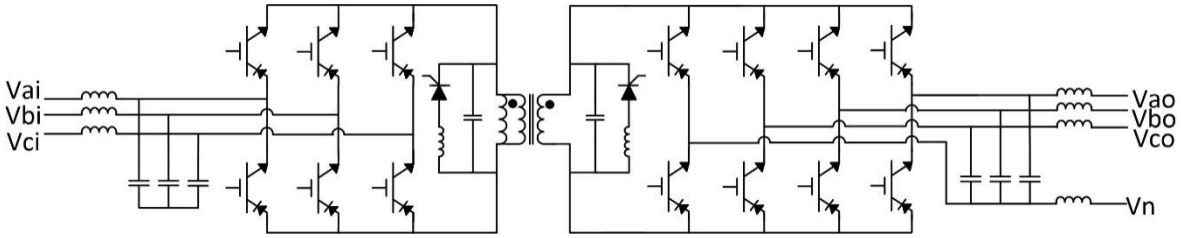


Fig. 6.7: Topology for three-phase three-wire ac to three-phase four-wire ac.

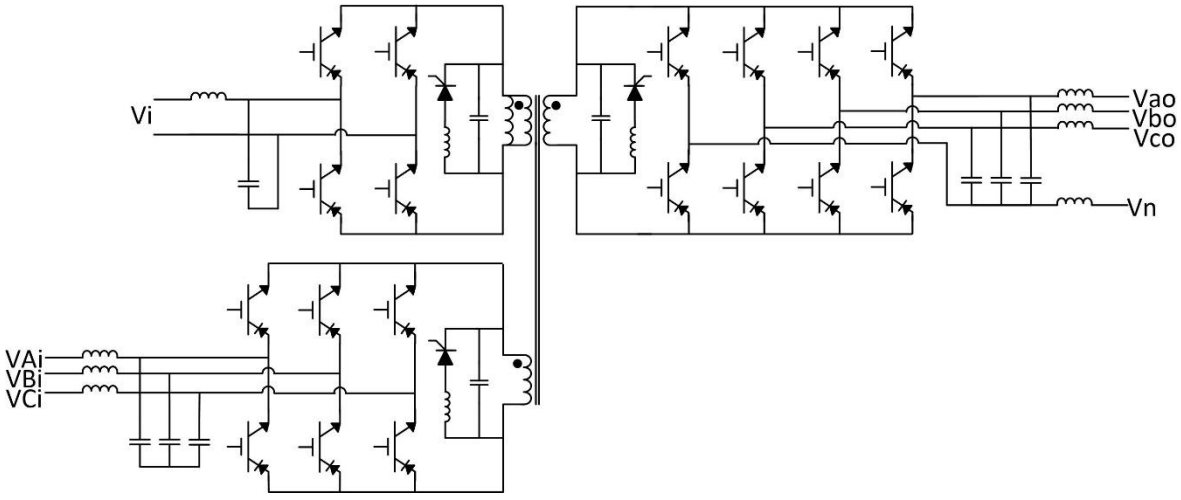


Fig. 6.8: Tri-port topology 1.

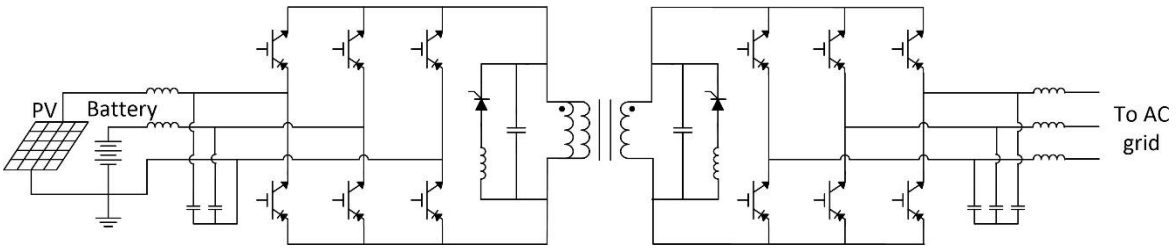


Fig. 6.9: Tri-port topology 2.

In the case of a non-isolated topology in which the transformer is replaced by an inductor, a single auxiliary resonant circuit could be used to provide ZVS conditions for both bridges. The non-isolated topology for three-phase ac/ac is shown in Fig. 6.10. Similar non-isolated topologies can be derived from all the topologies of Fig. 6.4 – Fig. 6.9 and will not be repeated here.

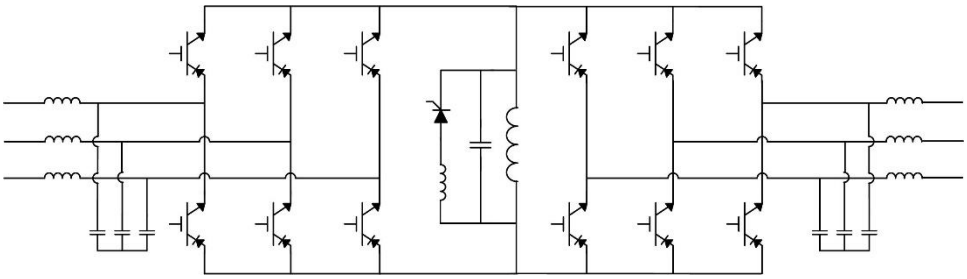


Fig. 6.10: Non-isolated topology for three-phase ac/ac.

In addition, if power only flows in one direction, the device configuration can be even simpler. Fig. 6.11 shows the converter to connect the PV panel and the grid, in which only one active device is used on the PV side.

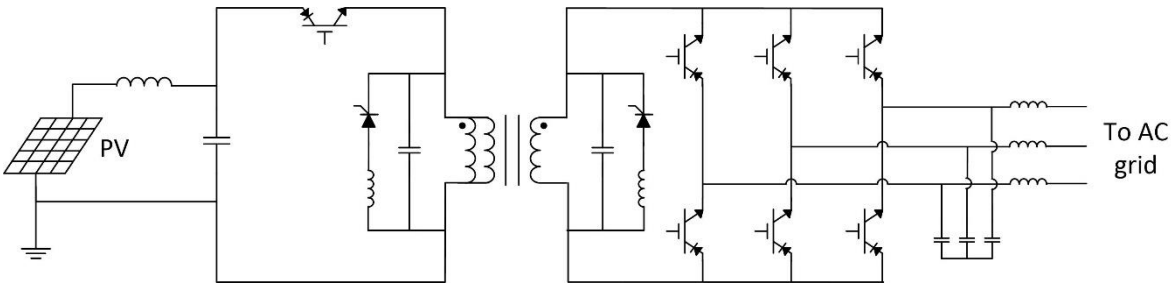


Fig. 6.11: Simplified circuit configuration for unidirectional power flow.

6.5. Principle of Operation

In the steady state, the S4T maintains a constant dc current through the transformer magnetizing inductance. Its operation is similar to the dc/dc flyback converter in that the

input bridge charges the transformer magnetizing inductance and the output bridge discharges it (although the concept of input and output in bidirectional converters in purely notional). Over one switching cycle, the isolated converter has the following types of states: 1) five active states in which the transformer magnetizing current flows in a loop between the input or output bridge and the transformer magnetizing inductance, 2) one ZVS transition state between any two adjacent active states in which the magnetizing current flows through the resonant capacitors to provide ZVS conditions for turning off and turning on the main devices, and 3) one resonant state in which the resonant capacitor voltage is reset so as to be ready for the next switching cycle operation.

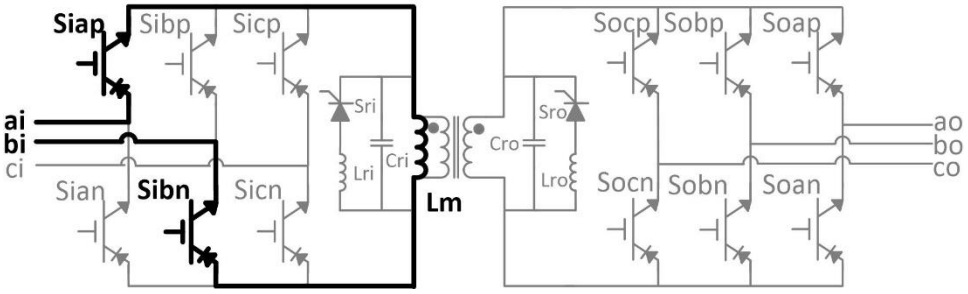
For the five active states, the duty cycle of each state is determined by the actual charge delivered to the specific terminal over each switching cycle. The device duty cycle dT_S is governed by equations (6.1) and (6.2), in which I_m is the dc current flowing through the transformer magnetizing inductance L_m, I_g^* is the referenced line current, and T_S is the switching period.

$$\int_0^{dT_S} I_m dt = Q^* \tag{6.1}$$

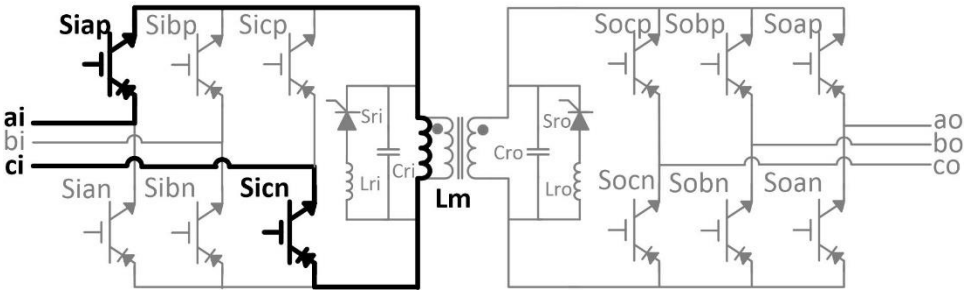
$$I_g^* = Q^*/T_S \tag{6.2}$$

The operating states over one switching cycle are shown below. The corresponding circuit states and conceptualized waveforms are shown in Fig. 6.12 and Fig. 6.13. An overall cycle can be summarized as follows. The "charging" cycle in which the current in the transformer magnetizing inductance is built up consists of two active states. The incoming line-line voltage with the highest voltage level (a_i and b_i in this example) is connected to the transformer (Fig. 6.12 (a)). After a time determined by equations (6.1) and (6.2), S_{ibn} is turned off and S_{icn} is turned on. The magnetizing current flowing through the resonant capacitors C_{ri} and C_{ro} causes the voltage across the transformer to vary with a controlled *dv/dt* rate until switch S_{icn} begins to conduct (ZVS transition state in Fig. 6.12 (f)). This allows zero turn-off loss for S_{ibn} and zero turn-on loss for S_{icn}. When the controller determines that S_{icn} should be turned off, the same process is repeated, with the converter entering a free-wheeling state

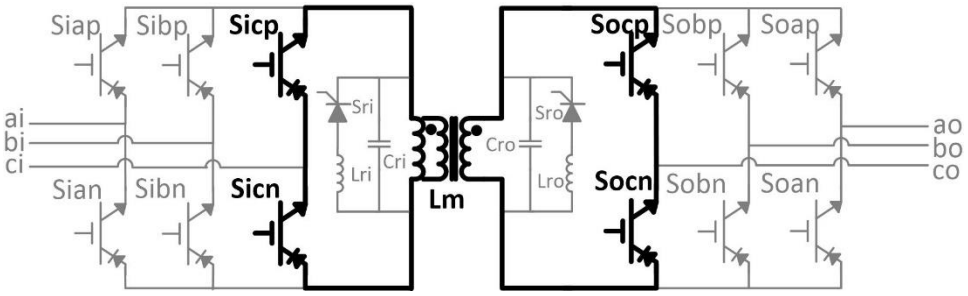
(Fig. 6.12 (c)). The output bridge now continues the process, discharging the transformer magnetizing inductance, while continuing the process of moving from state to state, using ZVS transitions to achieve the desired soft switching. The discharge cycle ends when the line-line voltage with the highest magnitude on the output side is connected across the transformer. At this point a resonant transition is enabled by the auxiliary resonant circuit, which resets the voltage across the resonant capacitors, and sets up the conditions for the next switching cycle. The process is described below in greater detail.



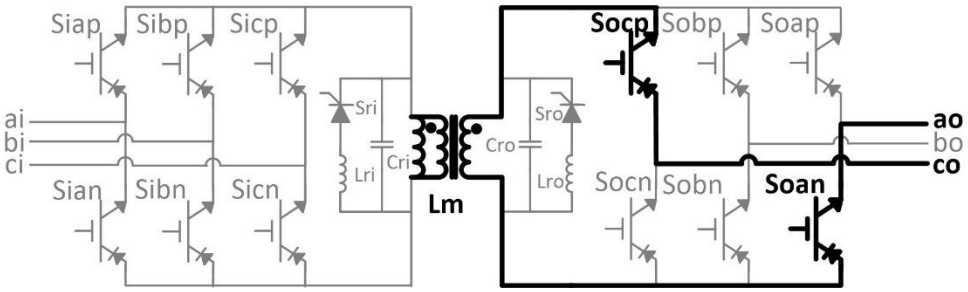
(a) State 1



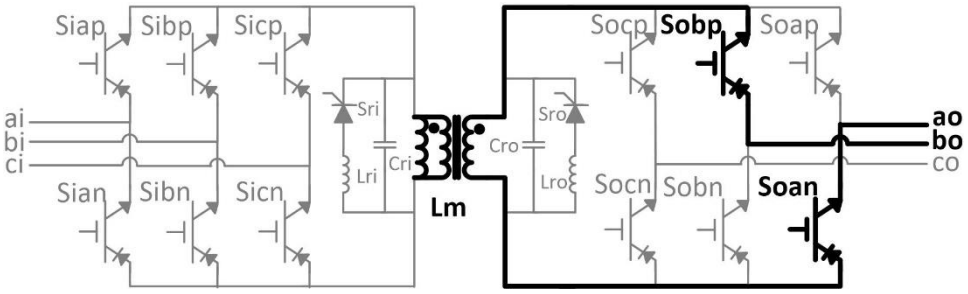
(b) State 2



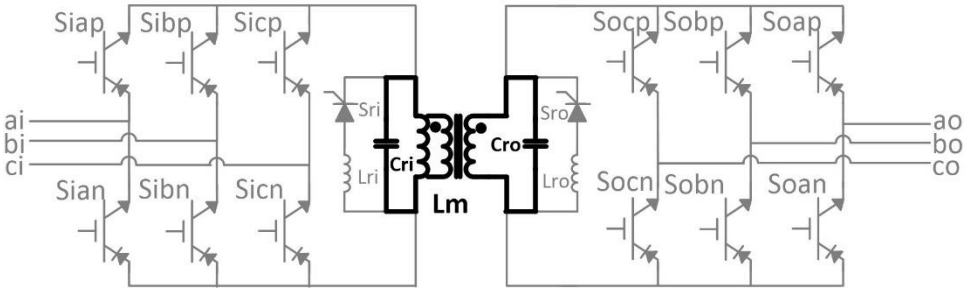
(c) State 3



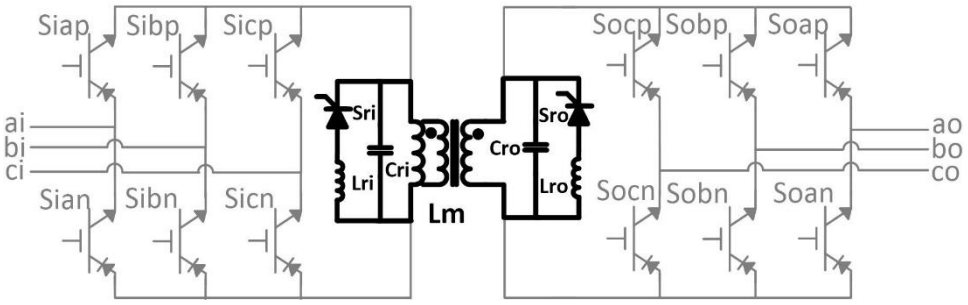
(d) State 4



(e) State 5



(f) State 0



(g) State 6

Fig. 6.12: Operating states over one switching cycle: (a) state 1 – charging the magnetizing inductance with the 1st line-to-line input voltage; (b) state 2 – charging the magnetizing inductance with the 2nd line-to-line input voltage; (c) state 3 – freewheeling; (d) state 4 – discharging the magnetizing inductance with the 1st line-to-line output voltage; (e) state 5 – discharging the magnetizing inductance with the 2nd line-to-line output voltage ((a) – (e) are the five active states); (f) state 0 – ZVS transition state; and (g) state 6 – resonant state.

A. State 1: Charging the magnetizing inductance with the 1st line-to-line input voltage (Fig. 6.12 (a))

The transformer is connected to phases a_i and b_i by turning on S_{iap} and S_{ibn}. The voltage across the resonant capacitors, which is V_{Cr}, equals to the 1st line-to-line input voltage V_{abi}. The transformer magnetizing inductance L_m is being charged by V_{abi}, and thus the current i_m increases linearly. This state ends when the average current delivered to phase b_i over one switching cycle equals to its reference current, as governed by equation (6.2).

B. State 0: ZVS transition state (Fig. 6.12 (f))

S_{ibn} is turned off, causing the magnetizing current to flow through the resonant capacitor, providing significantly reduced *dv/dt* rate. S_{ibn} can be turned off with zero switching loss. Capacitors are charged by i_m, and its voltage starts dropping from V_{abi}. Within this state, the incoming device S_{icn} can be gated-on. However, there is no current flowing through the devices since V_{Cr} is larger than V_{aci} and the devices are reverse blocked. This state ends when V_{Cr} drops to a value equal to V_{aci}, then S_{iap} and S_{icn} conduct. S_{icn} is actually turned on with zero switching loss.

C. State 2: Charging the magnetizing inductance with the 2nd line-to-line input voltage (Fig. 6.12 (b))

S_{iap} and S_{icn} conduct, and L_m is charged by V_{aci}. i_m linearly increases again, and V_{Cr} equals to V_{aci}. This state again continues until the average current delivered to phase c_i over one switching cycle equals its reference.

D. State 0: ZVS transition state (Fig. 6.12 (f))

S_{iap} and S_{icn} are turned off under ZVS conditions. The resonant capacitors are charged by i_m again until its voltage drops to zero.

E. State 3: Freewheeling (Fig. 6.12 (c))

The converter enters the freewheeling state by turning on S_{icp} and S_{icn} of the input bridge as well as S_{ocp} and S_{ocn} of the output bridge under ZVS conditions. i_m flows through these two legs rather than flowing to the input/output terminals. V_{cr} equals to zero at this state.

F. State 0: ZVS transition state (Fig. 6.12 (f))

S_{icp}, S_{icn}, and S_{ocn} are turned off under ZVS conditions. Resonant capacitors are charged by i_m again, and its voltage starts to drop towards a negative value.

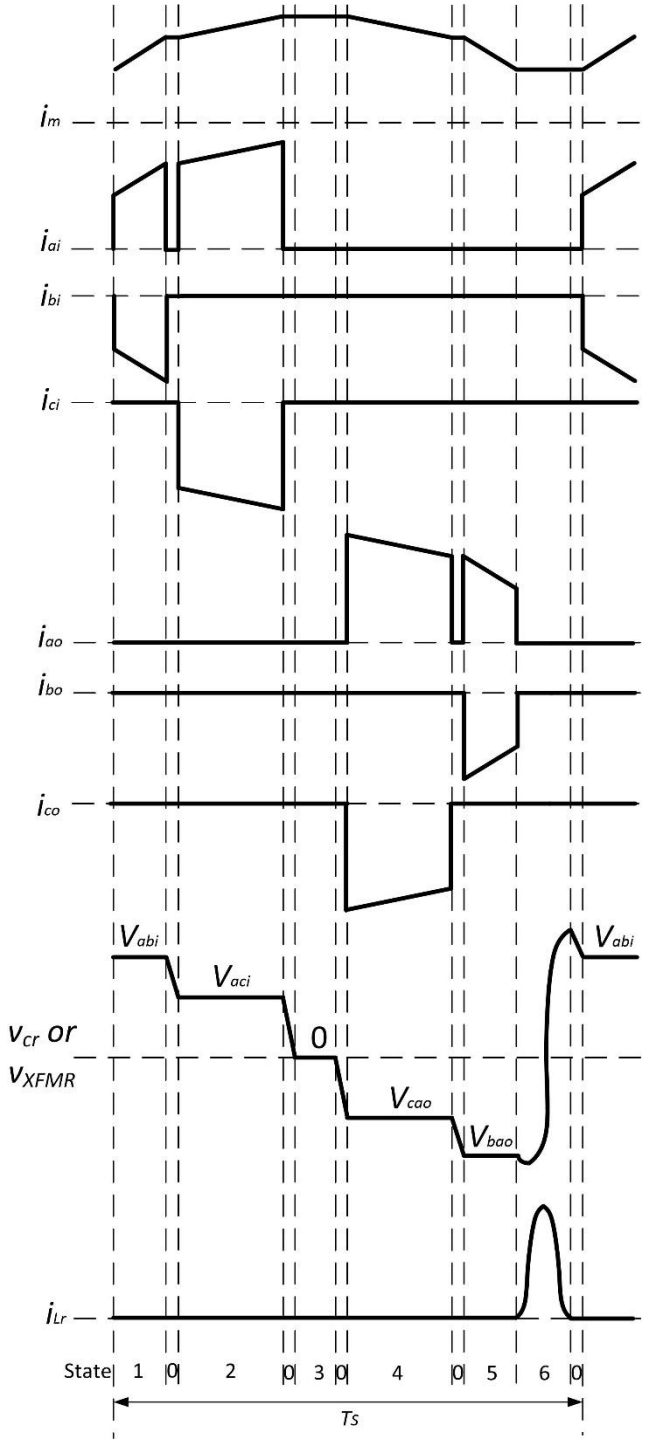


Fig. 6.13: Conceptualized waveforms (states 1 – 5 correspond to Fig. 6.12 (a) – (e); state 0 corresponds to Fig. 6.12 (f); and state 6 corresponds to Fig. 6.12 (g)).

G. State 4: Discharging the magnetizing inductance with the 1st line-to-line output voltage (Fig. 6.12 (d))

S_{ocp} and S_{oan} conduct under ZVS conditions, and L_m is discharged by V_{cao}. V_{cr} equals to V_{cao}. This state ends when the average current delivered to phase c_o over one switching cycle equals to its reference.

H. State 0: ZVS transition state (Fig. 6.12 (f))

S_{ocn} is turned off under ZVS condition. Resonant capacitors are charged by i_m again until its voltage equals to V_{bao}.

I. State 5: Discharging the magnetizing inductance with the 2nd line-to-line output voltage (Fig. 6.12 (e))

S_{obp} and S_{oan} conduct under ZVS conditions, and L_m is discharged by V_{bao}. V_{cr} equals to V_{bao}. This state ends when the average current delivered to phase b_o over one switching cycle equals to its reference.

J. State 6: Resonant (Fig. 6.12 (g))

S_{obp} and S_{oan} are turned off under ZVS conditions. Auxiliary switch S_r is turned on under a ZCS condition to initiate the resonant operation between L_r and C_r. This state ends when the current through L_r drops to zero, and S_r is turned off under ZCS condition. As a result, the voltage polarity of C_r is reversed. Since the current through the auxiliary switch self-commutates to zero, devices such as SCRs can in principle be used for S_r. The two auxiliary resonant circuits can be simultaneously activated to start the resonant operation rather than being controlled individually.

K. State 0: ZVS transition state (Fig. 6.12 (f))

With the completion of the resonant state, the capacitor voltage reaches a value larger than the highest line-to-line voltage V_{abi} again. To ensure this, a state 0 can be flexibly inserted between state 5 and state 6 to deliver more energy to the capacitor if needed such that the capacitor voltage can always resonate to a voltage level higher than V_{abi}. Then the incoming devices S_{iap} and S_{ibn} can be turned-on under ZVS condition. Resonant capacitors

are charged by i_m till its voltage drops to a value equals to V_{abi}, which starts the operation of next switching cycle.

The transition from one bridge to another (e.g. transition from state 2 to 3) involves management of the leakage energy. For the S4T, the energy trapped in the transformer leakage inductance is automatically managed through the resonance between the leakage inductance and the two resonant capacitors. The voltage difference between these two resonant capacitors tends to drive the outgoing bridge current down to zero and simultaneously build up the incoming bridge current, achieving a leakage management for bridge-to-bridge transitions. This procedure occurs automatically and it does not need an additional switching state as for the Dyna-C. The time spent on leakage energy transfer is as small as a few micro-seconds, which slightly reduces the duty cycle for active power transfer through the transformer. Therefore, to avoid impacting normal performance, the transformer leakage inductance should be kept low. The transformer leakage effect will be analysis in details in chapter 7.

During the entire switching cycle, the resonant capacitors provide ZVS transitions for turning off the outgoing devices and turning on the incoming devices. ZVS transitions occur in a passive manner in which the transformer magnetizing current automatically transfers between the active devices and the resonant capacitors. As a result, the converter does not require any intentionally added dead-time or overlap-time for device transitions. The auxiliary device is only operated once at the end of each switching cycle to reset the resonant capacitor voltage. Unlike other resonant converters which involve great complexity, the passive ZVS transitions simplify the S4T control.

6.6. Full Range of Soft Switching

Unlike the DAB converter which has a limited soft-switching range, the S4T realizes ZVS over the full load range. From the above stated operating principles, it can be seen that device turn-off always occurs under ZVS conditions. To ensure ZVS turn-on, the resonant capacitor voltage should be higher than the incoming line-line voltage when the device is

turned on, which means that the incoming device should be always reverse biased when its gate is turned on.

Over one switching cycle, before the end of state 5, ZVS turn-on can be always guaranteed as long as the device gate is turned on before the end of state 0. However, the ZVS turn-on region is not restricted within state 0. Instead, the incoming device allows to be turned on even before state 0 starts. For example, the gate of S_{icn} can be turned on within state 1. In this case, since V_{abi} is larger than V_{aci}, S_{icn} is reverse blocked, and it does not conduct. The ZVS transition from S_{ibn} to S_{icn} automatically occurs within state 0, and it does not need any intentional control. Fig. 6.14 shows the allowed ZVS turn-on region of each device that corresponds to the example switching cycle of Fig. 6.13. The devices can be turned on at any time within their specific regions, and the ZVS turn-on transitions are always guaranteed. This figure shows that the devices of the S4T realize ZVS switching over a wide four-quadrant range, including for voltage buck and boost modes of operation. This is a great advantage compared with other soft-switching converters, for which the devices have a very short time period over which they must be turned on. Additionally, for the proposed converter, even if the device misses the allowed time region and it is turned on after the end of state 0 because of faulty operation, the only issue is that the device is turned on with losses, while the converter is still able to operate normally after the transition.

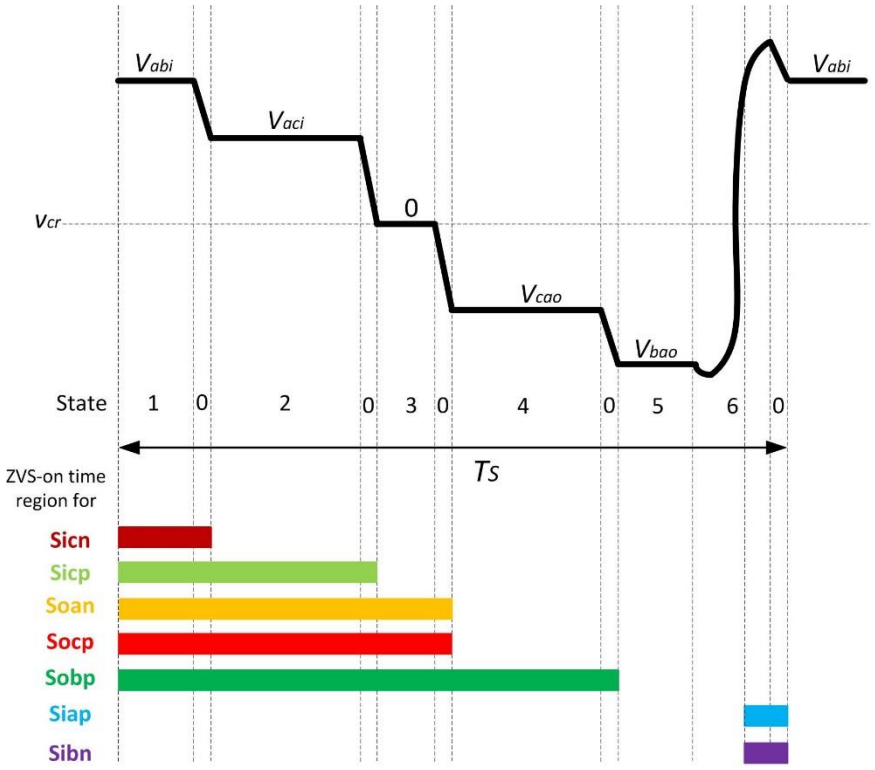
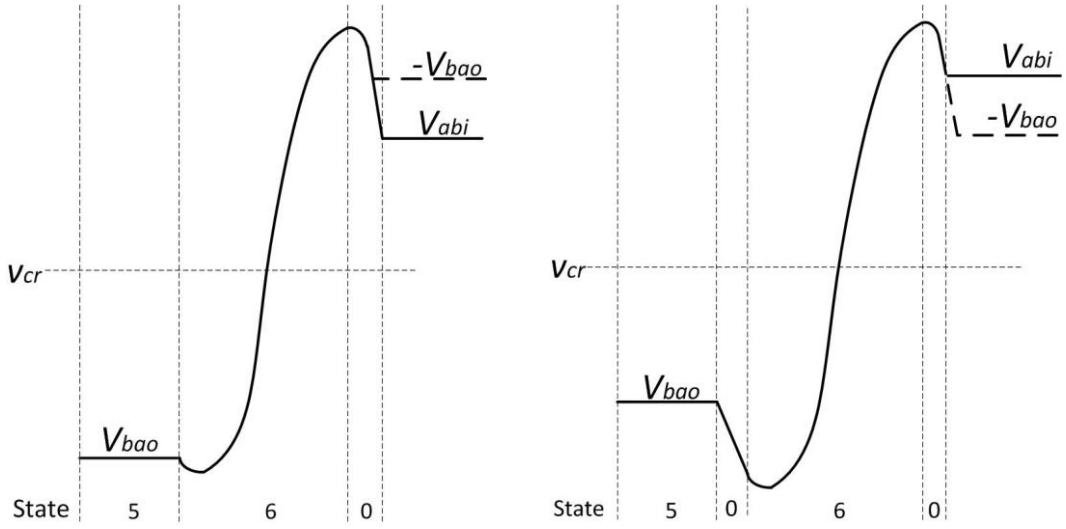


Fig. 6.14: Allowed ZVS turning-on time region for each device corresponding to the example switching cycle of Fig. 6.13.

After state 5, the resonant capacitor voltage V_{cr} reaches the most negative value. To ensure ZVS operation of the subsequent switching cycle, after the resonant operation of state 6, V_{cr} should reach a value higher than that of the incoming highest positive voltage, V_{abi} in this example. This is achieved by flexibly adding state 0 between state 5 and state 6.

Under voltage-boost operation in which the amplitude of the output is higher than the input, state 6 can occur immediately after state 5, since V_{cr} can always reach a value higher than the highest input voltage after the resonant operation of state 6. The conceptualized waveform of V_{cr} for this case is shown in Fig. 6.15 (a). The amplitude of the output voltage V_{bao} is higher than that of the input voltage V_{abi}, indicating a voltage-boost operation. Under voltage-buck operation, however, the amplitude of V_{bao} is lower than V_{abi}. Therefore, state 0 is needed after state 5. V_{cr} will be then charged to a greater negative value to ensure that it can be resonated to a value higher than V_{abi} after state 6. The conceptualized waveform of V_{cr} under voltage-buck operation is shown in Fig. 6.15 (b).



(a) **(b)**

Fig. 6.15: Conceptualized V_{cr} waveforms with optional state "0" after state "5" under: a) voltage-boost operation; and b) voltage-buck operation.

6.7. Unique Attributes of the S4T

6.7.1. Ease of Control

The ZVS soft-switching range of the S4T is independent of load levels, a significant advantage when comparing with DAB-based three-stage SSTs. Further, a wide range of turn-on and turn-off times provides ease of control at the individual device level. ZVS operation is not sensitive to resonant circuit parameters, and the fixed-frequency PWM capability is retained. The fundamental frequency control for the S4T is also simple, and uses the instantaneous actual magnetizing current to estimate the duty cycle of each switch. This results in very clean harmonic-free voltage waveforms at the input and output, even though the magnetizing current amplitude varies significantly, an issue that will be discussed in detail later.

6.7.2. Robustness

For the DAB based three-stage SST, bulky dc capacitors are needed to support the dc buses on both sides. This impacts the robustness and reliability of such SSTs. Inrush currents have to be managed at start-up, shutdown, and under fault conditions. Under short circuit faults, de-saturation protection and soft turn-off are required to avoid inductive voltage

spikes. This can be particularly challenging for SiC devices, which may be needed to get to higher voltage levels. By way of contrast, the S4T has inherent current limiting, and eliminates inrush current under both start-up and fault conditions. De-saturation protection is not required for the devices, making the gate driver design simpler.

The S4T is also highly differentiated from conventional CSIs. Interrupting current flow in a CSI, for instance due to a loss of the control power, can quickly result in a voltage spike across the devices. The high *dv/dt* under open-circuit failure for CSIs requires a very fast acting overvoltage protection scheme. However, for the S4T, since the resonant capacitors significantly reduce the *dv/dt* rate, the devices can be easily protected by only connecting MOVs in parallel with the resonant capacitors, and by independent turn-on of the resonant circuit devices if needed.

In addition, the S4T offers several very important features that conventional VSIs and CSIs do not offer: 1) the converter does not require any intentional added dead time or overlap time for device transitions; 2) there is no severe inrush current when devices on the same leg are turned on simultaneously under fault; 3) devices do not suffer from catastrophic voltage stress when interrupting the inductive current flowing path; 4) reduced *dv/dt* rate significantly mitigates all the hard-switching issues such as resonance, spikes, noise, and EMI.

6.7.3. Fast Dynamic Response

The S4T is operated under the charge modulation control, which delivers the required charge to input and output terminals on a cycle-by-cycle basis. This indicates that the source and load current can be controlled with very fast dynamic response. It does not need an external current control loop to regulate the line current as in the conventional VSI, and a fast step response of several switching cycles is easily achieved.

To optimize S4T efficiency, the transformer magnetizing current level can be varied according to the load levels. This will decrease the time period of the freewheeling state and will reduce conduction losses. However, for conventional CSIs, dynamically changing the

dc current according to load levels can slow down the response because of the large inductor. For the S4T, the transformer magnetizing inductance can be made relatively small, which reduces the system inertia. As a result, the transformer magnetizing current can be built up and driven down to a new reference value within several switching cycles. The detailed discussion of the converter operation under load transients will be presented in chapter 8. In addition, the transformer can have a compact design and lower conduction losses due to the smaller magnetizing inductance that is acceptable.

6.7.4. Modular Design

The minimal topology lends itself to very efficient packaging. If RB-IGBTs are used, the packaging becomes even simpler. The absence of bulky dc capacitors and the ability to achieve higher switching frequencies reduce the transformer size, while ZVS allows smaller heatsinks.

The S4T also allows scaling to higher voltage and power levels. Using available Si devices above 1700 volts entails severe compromises in switching speed and losses. Even with emerging high-voltage Silicon-Carbide devices, the ability to realize grid-connected converters will require series connection of devices or modules. The S4T offers unique advantages in scaling for higher voltage/power. For instance, a traction drive could be realized with an S4T module that has single phase on the high-voltage side, and a three-phase converter on the low-voltage side. The single-phase converters could be stacked in series, while the three-phase converters could be paralleled to drive the traction motor. This topology could realize fully bidirectional power flow, simple converter design, and high efficiency. Issues of dynamic balancing are important and will be discussed in chapter 12.

6.8. Conclusions

This chapter introduced the topology of the ZVS solid state transformer. The S4T offers several important features including: 1) full four-quadrant SST functionality; 2) minimal two power-conversion stages with lower device count; 3) elimination of the bulk dc energy

storage capacitors; 4) elimination of inrush current; 5) fast dynamic response; and 6) modular structure to scale to high-voltage and high-power levels which will be discussed in chapter 12. More importantly, all devices are switched under soft-switching conditions over the full four-quadrant load range, which eliminates the switching loss to improve the converter efficiency, and reduces *dv/dt* rate at switching transitions to mitigate EMI. The converter topology can also be extended to other types of power conversion such as dc, single-phase ac, multi-phase ac, and multi-terminal, acting as a universal power converter. Operating principle on a cycle-to-cycle basis was presented, and the feature of full range soft-switching was discussed. The converter exhibits several unique attributes including ease of control, robustness, fast dynamic response, and modular design. In the following chapters, detailed analysis, control, preliminary simulation results, and design of the converter will be presented.

CHAPTER 7: ANALYSIS AND CONTROL OF THE S4T

7.1. Introduction

The previous chapter has discussed the topology and operating principle for the S4T, and presented several unique attributes. This chapter will give a detailed analysis of the S4T converter in steady state operation. The effect of the transformer leakage inductance on converter operation will also be analyzed. Finally, a control strategy for the S4T will be presented.

7.2. Analysis of the Converter

The control of the magnetizing current in the high-frequency transformer is crucial in S4T operation. A stable and robust magnetizing current regulation must be guaranteed to maintain the converter's normal operation. On a cycle to cycle basis, the input side charges the magnetizing inductance and the output side discharges it. Duty cycle of the converter bridges is controlled such that the magnetizing inductance delivers desired charge to each phase and thus sinusoidal voltages/currents can be maintained on the input and output sides. The magnetizing current regulation has the following attributes:

- Loss in the converter and the high-frequency transformer should be compensated such that the magnetizing current is regulated at a specific dc level;
- The magnetizing inductance should have a relatively small value to achieve a compact transformer design. This will lead to large current ripples on the magnetizing current due to the charge and discharge operation;
- Since the magnetizing inductance and its energy storage capability are relative low, single-phase ac to single-phase ac conversion with different power factors on the input and output sides may not be viable. Magnetizing current regulation from single-phase ac source is not feasible since the instantaneous power on that side is fluctuating;

- If one side of the S4T is connected to dc or three-phase ac sources, loss compensation can be fulfilled on that side since it can always provide energy to regulate the magnetizing current;
- Small magnetizing inductance also allows rapid change of the magnetizing current according to the load levels within a few switching cycles, which achieves very fast dynamic response for the converter.

7.2.1. Optimal Transformer Magnetizing Current Level

The S4T enters the freewheeling state (state 3 of Fig. 6.12) after delivering the referenced charge from the input to the output terminals, in which the current flows through a closed phase leg, representing conduction loss. Thus, it is essential to shrink the freewheeling state duration. A higher magnetizing current leads to shorter time duration for the active states (states 1, 2, 4 and 5 of Fig. 6.12), and a longer time for the freewheeling state. Therefore, the magnetizing current should be dynamically regulated at a level such that reference charges are just able to be delivered from the input to the output terminals within one switching cycle T_s, without much time remaining for freewheeling. The following analysis excludes the effect of the ZVS transition period (state 0 of Fig. 6.12) and the resonant period (state 6 of Fig. 6.12), which are small compared to the entire switching cycle. Assuming that the high-frequency transformer has a 1:1 turns ratio and that the input and output voltages are in phase and both have unity power factor, the average magnetizing current should satisfy equations (7.1) and (7.2), in which I_{ip}, I_{op} are the peak current of the input and the output, and t_i, t_o are the operation time durations of the input and output bridges, respectively. Neglecting the time spent on the ZVS transition and resonant operation, equation (7.3) should be satisfied to minimize or eliminate the free-wheeling duration when the input and output instantaneous currents are at their peaks, which in turn leads to the minimal average magnetizing current in equation (7.4).

$$I_{m.ave} * t_i = I_{ip} * T_S \tag{7.1}$$

$$I_{m.ave} * t_o = I_{op} * T_S \tag{7.2}$$

$$t_i + t_o = T_S \tag{7.3}$$

$$I_{m.ave} = I_{ip} + I_{op} \tag{7.4}$$

7.2.2. Switching Ripple of the Magnetizing Current

The voltages applied across the transformer during states 1 and 2 are governed by equations (7.5) and (7.6), in which V_{ip} is the peak line-to-line voltage of the input. These voltages rotate among three phases every $\pi/6$ radians based on three-phase voltage amplitudes. The average voltages in modes 1 and 2 over $\pi/6$ cycle are calculated as equations (7.7) and (7.8). For unity power factor, equation (7.9) is valid, in which $t_{1.ave}$ and $t_{2.ave}$ are the operation times for modes 1 and 2, and $I_{i1.ave}$ and $I_{i2.ave}$ are the average line currents that are delivered to the line in modes 1 and 2. The average voltage applied across the transformer for the input bridge is then given by equation (7.10). Equation (7.11) shows the average magnetizing current ripple over $\pi/6$ cycle, in which f_s is the converter switching frequency and V_{op} is the peak line-to-line voltage of the output.

$$V_{i1} = V_{ip}\left|\cos \omega t\right| \tag{7.5}$$

$$V_{i2} = V_{ip}\left|\cos\left(\omega t + \frac{2\pi}{3}\right)\right| \tag{7.6}$$

$$V_{i1.ave} = \frac{6}{\pi}\int_0^{\pi/6} V_{ip}\left|\cos \omega t\right| d(\omega t) = \frac{3}{\pi} V_{ip} \tag{7.7}$$

$$V_{i2.ave} = \frac{6}{\pi}\int_0^{\pi/6} V_{ip}\left|\cos\left(\omega t + \frac{2\pi}{3}\right)\right| d(\omega t) = \frac{3}{\pi}\left(\sqrt{3} - 1\right) V_{ip} \tag{7.8}$$

$$\frac{V_{i1.ave}}{V_{i2.ave}} = \frac{I_{i1.ave}}{I_{i2.ave}} = \frac{t_{1.ave}}{t_{2.ave}} \tag{7.9}$$

$$V_{i.ave} = \frac{V_{i1.ave} t_{i1.ave} + V_{i2.ave} t_{i2.ave}}{t_{i1.ave} + t_{i2.ave}} = \frac{V_{i1.ave} t_i \dfrac{V_{i1.ave}}{V_{i1.vae} + V_{i2.ave}} + V_{i2.ave} t_i \dfrac{V_{i2.ave}}{V_{i1.vae} + V_{i2.ave}}}{t_i} = \frac{45 - 18\sqrt{3}}{3\sqrt{3}\pi} V_{ip} \tag{7.10}$$

$$\Delta I_{m.ave} = \frac{V_{i.ave} t_i}{L_m} = \frac{\left(45 - 18\sqrt{3}\right) V_{ip} V_{op}}{3\sqrt{3}\pi f_S L_m \left(V_{ip} + V_{op}\right)} \tag{7.11}$$

It can be seen from equation (7.11) that a larger L_m leads to a smaller current ripple, thus smaller transformer core loss, but it will result in a large core volume and thus higher copper loss. Therefore, the transformer design should make a compromise between the current ripple, the core loss, and the core volume.

7.2.3. Boundary Conditions for Continuous Conduction Mode Operation

The discontinuous conduction mode (DCM) operation should be avoided for the S4T, i.e., the magnetizing current should never drop to zero for any duration. The maximum magnetizing current ripple over $\pi/6$ radians occurs at $\omega t = \pi/6$, during which time both of the voltages across the transformer in states 1 and 2 are equal to $2/\sqrt{3}V_{ip}$, thus the maximum magnetizing current ripple is as shown in equation (7.12). To ensure continuous conduction mode (CCM) operation, the average magnetizing current should be larger than half of its ripple, thus equation (7.13) should be satisfied.

$$\Delta I_{m.max} = \frac{2 V_{ip} V_{op}}{\sqrt{3} f_S L_m \left(V_{ip} + V_{op}\right)} \tag{7.12}$$

$$f_S L_m > \frac{V_{ip} V_{op}}{\sqrt{3}\left(V_{ip} + V_{op}\right)\left(I_{ip} + I_{op}\right)} \tag{7.13}$$

7.3. Analysis of the Transformer Leakage Effect

The hard-switching Dyna-C requires a leakage management state when transitioning from one bridge to another. Ideally, this active leakage management methodology can manage the trapped leakage energy in a loss-less manner. However, at the end of this state, the diode junction capacitance tends to resonate with the leakage inductance and thus develop a high voltage stress across the diode. Silicon diodes have a more severe issue than SiC diodes due to their excessive reverse recovery current. In addition, transitioning from

the normal operating state to the leakage management state leads to additional switching loss.

For the proposed S4T topology, however, the auxiliary resonant capacitor can inherently sink the transformer leakage energy in a passive manner. This avoids using an additional leakage management strategy and thus eliminates all the associated issues. During the transition from one bridge to another as shown in Fig. 6.12 (f), the two resonant capacitors located on both the primary and secondary sides of the transformer will be simultaneously charged by the magnetizing current. However, it should be noted that during the transition, the leakage inductance will tend to resonate with these two capacitors. When transitioning from one side of the bridge to the other, the energy trapped within the leakage is actually automatically transferred through this resonance, without the need of additional switching state as the Dyna-C. In the following, the leakage energy transfer from one side to the other is analyzed.

Take the transitioning instant from state 1 to state 0 as shown in Fig. 6.12 for an example. Fig. 7.1 shows the equivalent circuit once the S4T enters state 0, in which the high-frequency transformer is replaced by a constant current I_m, and L_{lk} represents the transformer leakage inductance on the primary and secondary sides. The currents flowing through the primary and the secondary windings are i_1 and i_2. Before this transition, the two resonant capacitors have the same initial voltage of V_0, and all the magnetizing current flows through the primary side winding, i.e. i_1 equals I_m, and i_2 equals 0.

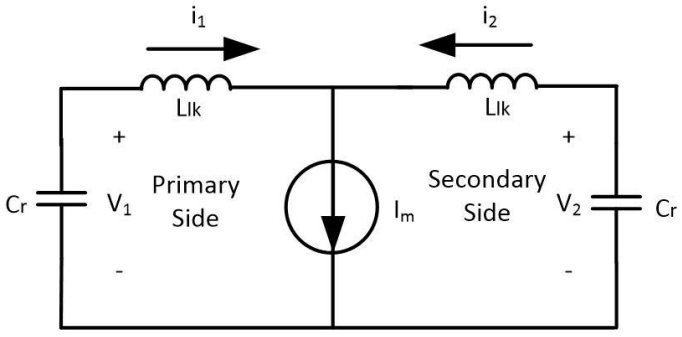


Fig. 7.1: Equivalent circuit at the ZVS transition.

Equation (7.14) describes the converter state once entering state 0. The solution to this equation is given in equation (7.15). Equation (7.16) is the required time to have the transformer magnetizing current equally distributed to the primary and secondary windings. It shows that the time spent on the leakage energy transfer from one winding to another depends on the leakage inductance and the resonant capacitance.

$$\begin{cases} i_1 + i_2 = I_m \\ L_{lk}\dfrac{di_1}{dt} - L_{lk}\dfrac{di_2}{dt} = v_1 - v_2 \\ C_r\dfrac{dv_1}{dt} = -i_1 \\ C_r\dfrac{dv_2}{dt} = -i_1 \end{cases} \text{ with the initial conditions of } \begin{cases} i_1(t=0) = I_m \\ i_2(t=0) = I_m \\ v_1(t=0) = V_0 \\ v_2(t=0) = V_0 \end{cases} \tag{7.14}$$

$$\begin{cases} i_1 = \dfrac{I_m}{2}\left(1 + \cos\left(\sqrt{\dfrac{1}{L_{lk}C_r}}t\right)\right) \\ i_2 = \dfrac{I_m}{2}\left(1 - \cos\left(\sqrt{\dfrac{1}{L_{lk}C_r}}t\right)\right) \\ v_1 = -\dfrac{I_m}{2}\sqrt{\dfrac{L_{lk}}{C_r}}\sin\left(\sqrt{\dfrac{1}{L_{lk}C_r}}t\right) - \dfrac{I_m}{2C}t + V_0 \\ v_2 = \dfrac{I_m}{2}\sqrt{\dfrac{L_{lk}}{C_r}}\sin\left(\sqrt{\dfrac{1}{L_{lk}C_r}}t\right) - \dfrac{I_m}{2C}t + V_0 \end{cases} \tag{7.15}$$

$$t_{lk} = \frac{\pi}{2}\sqrt{L_{lk}C_r} \tag{7.16}$$

The leakage energy transfer can also be explained in a more intuitive manner. Once the converter enters state 0, equation (7.15) shows that the voltages of the two resonant capacitors will be different, due to the resonance between the leakage inductance and the two resonant capacitors. This voltage difference tends to drive the outgoing bridge current down and simultaneously build up the incoming bridge current, achieving a leakage management for bridge-to-bridge transitions.

However, equation (7.15) shows that the resonance will continue even after the transformer magnetizing current is equally distributed to the primary and secondary

windings at the time specified in equation (7.16). The winding resistance of the transformer can help damp the resonance and stabilize the two winding currents. However, if the leakage inductance is too large, a huge resonance that lasts for a very long time may result in operational failure of the converter. In this case, to overcome this issue, two additional diodes D_{ri} and D_{ro} can be connected in series with the transformer to prevent the resonance, which is shown in Fig. 7.2. The drawback of this solution is that it introduces additional conduction loss for the converter since they are always in the magnetizing current path. It is thus desired to select diodes that have a low voltage drop. SiC diodes are also preferred here for low reverse recovery purpose.

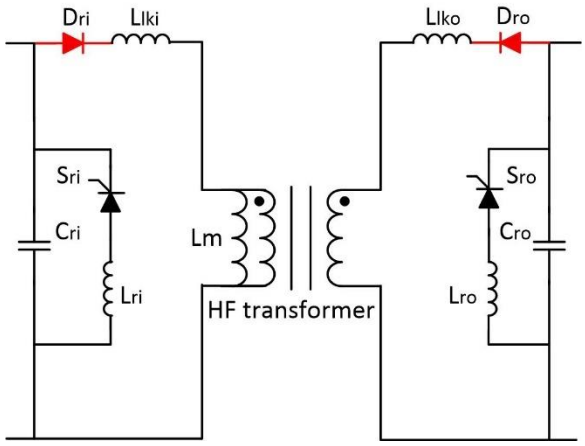


Fig. 7.2: Two diodes to manage the resonance if leakage inductance is large.

7.4. Control of the Converter

A charge-control based modulator, which was initially proposed to control a rectifier [96], is selected for controlling the S4T, in which the duty cycle of each state is determined by the actual charge delivered to the specific terminal over each switching cycle. The entire controller of the S4T consists of two loops, which are outer loops for input and output bridges to determine the reference phase current and required charge for each switching cycle, and an inner loop to regulate the converter running from one switching state to another. The outer loop control architecture of the input bridge is shown in Fig. 7.3. When synchronized with the input line voltage, the D component of the input current is used to regulate the dc magnetizing current. For maintaining a unity power factor, the Q current reference is

typically set to 0. Load feed-forward is provided on the branch generating I_{D0i}^* to ramp up/down the input current in response to changes in the load, in which P_o is the three-phase output instantaneous active power, calculated as equations (7.17) to (7.19), in which v_{ao}, v_{bo}, v_{co}, i_{ao}, i_{bo}, i_{co} are output three-phase voltages and currents, and θ is the phase angle referencing to the input side voltage. The feedback loop generates ΔI_{Di}^* from magnetizing current error Δi_m and compensator G_{Mi} is used to compensate the converter loss such that i_m is regulated at its reference I_m^*, in which G_{Mi} can be a simple PI regulator as shown in equation (7.20). The *DQ* current references are used as inputs to the "sector detection and charge reference calculation" block. This block outputs a signal "*sector_i*", which contains the information of the operating sequence for the device poles corresponding to each phase, based on the three-phase voltage and current amplitudes of the input, and it calculates the required charges Q_{1i}^* and Q_{2i}^* that need to be delivered in states 1 and 2 of Fig. 6.12.

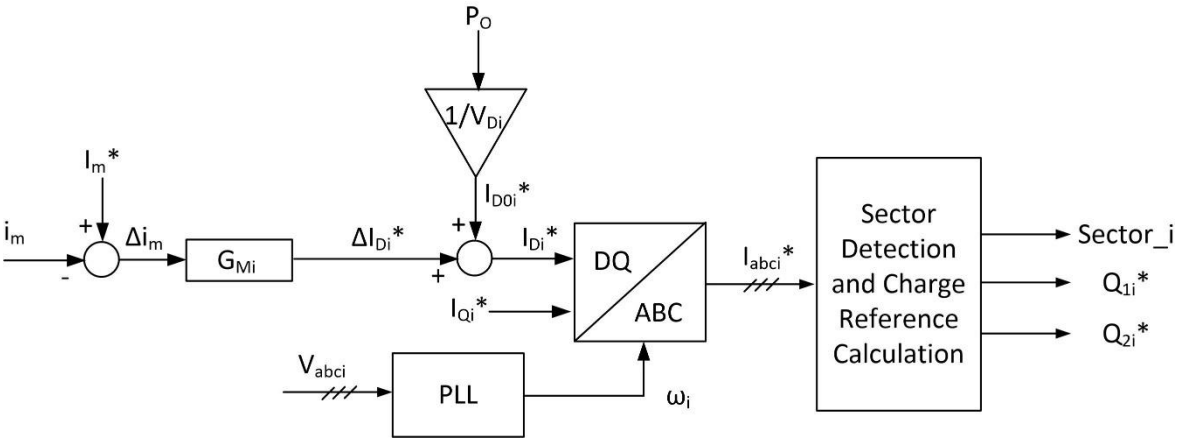


Fig. 7.3: Outer loop control architecture for the input bridge.

$$P_o = V_{do} I_{do} + V_{qo} I_{qo} \tag{7.17}$$

$$\begin{bmatrix} V_{do} \\ V_{qo} \end{bmatrix} = \begin{bmatrix} \cos\theta & \cos\left(\theta - \frac{2\pi}{3}\right) & \cos\left(\theta + \frac{2\pi}{3}\right) \\ -\sin\theta & -\sin\left(\theta - \frac{2\pi}{3}\right) & -\sin\left(\theta + \frac{2\pi}{3}\right) \end{bmatrix} \begin{bmatrix} v_{ao} \\ v_{bo} \\ v_{co} \end{bmatrix} \tag{7.18}$$

$$\begin{bmatrix} I_{do} \\ I_{qo} \end{bmatrix} = \begin{bmatrix} \cos\theta & \cos\left(\theta - \frac{2\pi}{3}\right) & \cos\left(\theta + \frac{2\pi}{3}\right) \\ -\sin\theta & -\sin\left(\theta - \frac{2\pi}{3}\right) & -\sin\left(\theta + \frac{2\pi}{3}\right) \end{bmatrix} \begin{bmatrix} i_{ao} \\ i_{bo} \\ i_{co} \end{bmatrix} \tag{7.19}$$

$$G_{Mi} = K_p * \Delta i_m + K_i \int \Delta i_m dt \tag{7.20}$$

The outer loop control block diagram of the output bridge is shown in Fig. 7.4. The load voltage regulator forms the outer loop. The compensators, G_{MDo} and G_{MQo}, can be PI regulators. If the converter output is connected to active power sources and it is operated in the current control mode, the voltage control loop is not required and current references I_{Do}^*, I_{Qo}^* are directly specified. In this case, the outer control loops for the input and output bridges are fully symmetrical. The *DQ* output current references serve as inputs to the "sector detection and charge reference calculation", which outputs a signal "*sector_o*" and the required charges Q_{1o}^* and Q_{2o}^* to determine the operating sequence for the output bridge.

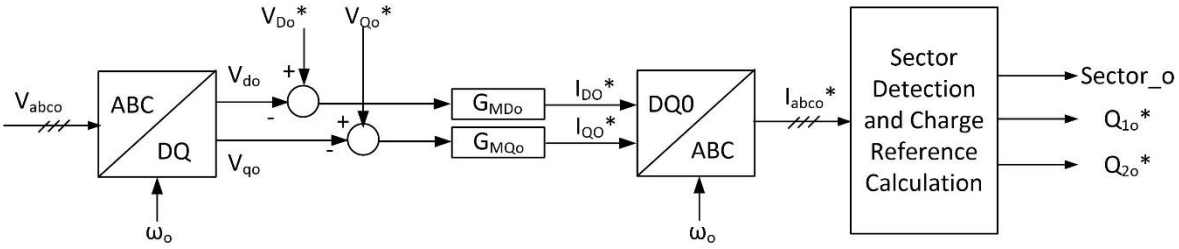


Fig. 7.4: Outer loop control architecture for the output bridge.

Using the sector information and charge references of the input and output generated from the "sector detection and charge reference calculation" block as well as the filter capacitor voltages of the input and the output, the inner control loop shown in Fig. 7.5 is constructed as a state machine, which runs the converter from one state to another, following the sequence described in Fig. 6.12. To determine the duty cycle of each state, the actual charge, which is calculated as the integration of the transformer magnetizing current as shown in equation (7.21), is continuously compared with the reference charge. Once the actual charge is equal to the reference, the current state operation is concluded and next state operation starts.

$$Q_m = \int_{\tau=t} i_m(\tau) d\tau \tag{7.21}$$

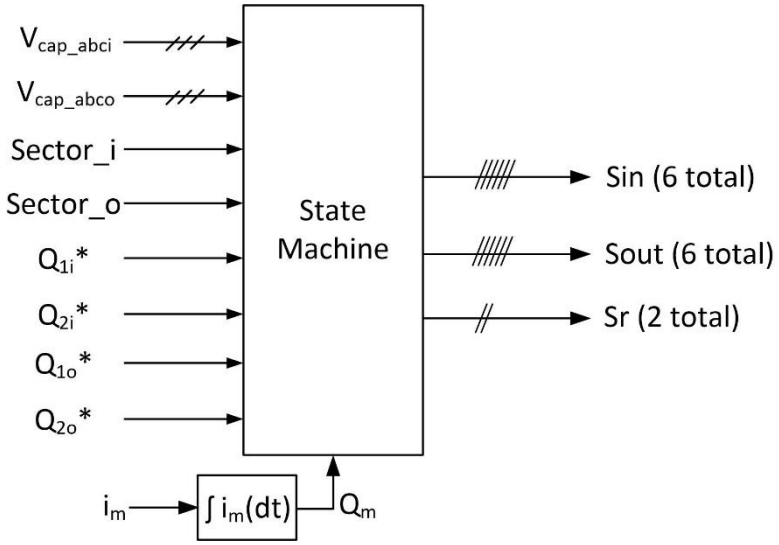


Fig. 7.5: Inner control loop.

7.5. Conclusions

This chapter covers the analysis of the converter during steady state operation. The optimal transformer magnetizing current level, switching ripple of the magnetizing current, and boundary conditions to ensure CCM operation are derived. Transformer leakage inductance plays a key role in the converter operation. This chapter also analyzes the impact of the leakage inductance and shows that the leakage energy is automatically managed through the resonance between the leakage inductance and the resonant capacitors during bridge-to-bridge transitions. Finally, the control architecture for the S4T is presented.

CHAPTER 8: CONVERTER DESIGN FOR THE S4T

8.1. Introduction

To experimentally verify the proposed S4T, a 208 V / 10 kVA prototype for three-phase ac/ac applications was designed and built. This chapter presents the detailed design of the S4T converter, which includes design, selection, and sizing of semiconductor devices, gate drivers, filters, snubbers, and sensors. Detailed optimization and design of the auxiliary resonant circuit are shown. The S4T is controlled by a customized DSP/FPGA control board. The design of the embedded controller is also described. Finally, the converter protection scheme for various faults is also discussed.

8.2. Design of Power Stage

8.2.1. Semiconductor Devices

The main devices of S4T are stressed at 2 p.u. current, the optimum value to maintain the transformer magnetizing current. However, since the duty cycle of each device is less than 0.5, the devices do not suffer from a heavy thermal burden. The semiconductors usually can be stressed at a high current level when the duty cycle is small. In addition, ZVS operation eliminates all switching losses, which further reduces the thermal stress on the S4T devices. Since the converter only has conduction loss, devices with low voltage drop are preferred such that overall efficiency is high.

The S4T unit to be designed is rated at 208 V / 10 kVA with a switching frequency of 15 kHz. The corresponding RMS value and peak value of the line current are 28 A and 40 A, respectively. The converter is tested by connecting the input and the output terminals to the same voltage source and circulating the power in the loop. Since the input and the output terminals are at the same voltage level, the input and the output bridge has the same duty cycle. Considering the time period of the ZVS transition and the resonant transition, the actual duty cycles of the input and the output bridges are slightly less than 0.5. Therefore, to ensure that 40 A peak current can be delivered to both the input and the output terminals, the

dc value of transformer magnetizing current is set at 100 A, which is slightly higher than twice the peak line current. The transformer magnetizing inductance is selected to be 200 μH, which leads to a compact transformer design with an acceptable current ripple of 50 A. As a result, the peak current handled by the device is approximately 125 A. A detailed transformer design is presented in chapter 9.

The devices for the S4T should be able to conduct current in one direction but block voltage in both directions. This can be implemented using a reverse blocking IGBT (RB-IGBT) or an IGBT/MOSEFT in series with a diode. Due to the limited availability of the RB-IGBTs in the market, S4T is implemented with series diode/IGBT devices. SiC diodes are used for the design since they do not have a reverse recovery current. Both Si IGBTs and SiC MOSFET can be used for the active devices. SiC MOSFET, which is almost 10 times more expensive than the Si IGBT for the same rating, is optimized for minimizing the switching loss. For the S4T, the efficiency is dominated by the conduction loss, while the switching loss is almost negligible. The SiC MOSFET C2M0025120D from Cree™ and the Si IGBT NGTB50N120FL2WG from ON-Semiconductor ™ are compared. Both are rated at 1200 V and have a TO-247 package. Their conducting voltage drops are compared in table 8.1. As can be seen, the SiC MOSFET and Si IGBT have a drain-source or collector-emitter voltage drop of 2.8 V (SiC) and 2.6 V (Si) at 100 A when operated at 25 °C. In addition, when the junction temperature increases from 25 °C to 150 °C, the voltage drop of SiC MOSFET reaches 5.6 V, while the Si IGBT voltage drop is only 3.3V. The positive temperature coefficient for SiC devices is a valuable feature for paralleling devices to equally share the current, but will cause much more conduction loss when operating at high current. Based on the above comparison, it is predicted that the Si IGBTs can provide higher efficiency with 10 times less cost. The final selected diode for the converter is SiC diode GDP60Z120E from Global Power Technology™, rated at 1200 V / 161 A. The selected IGBT is NGTB50N120FL2WG from ON-Semiconductor™, rated at 1200 V / 100 A. The IGBT also has an anti-parallel diode within the package, which provides a reverse current

flowing path when the SiC diode parasitic capacitance is charged during its switching-off transition. Both the SiC diode and the Si IGBT have a TO-247 package.

Table 8.1: Device comparison on the conducting voltage drop for SiC MOSFET C2M0025120D and Si IGBT NGTB50N120FL2WG.

Junction Temperature	SiC MOSFET (C2M0025120D)			Si IGBT (NGTB50N120FL2WG)		
	30 A	60 A	100 A	30 A	60 A	100 A
25 °C	0.7 V	1.5 V	2.8 V	1.8 V	2.2 V	2.6 V
125 °C	1.3 V	2.9 V	5.6 V	2 V	2.7 V	3.3 V

8.2.2. Converter Switching Frequency

Even though the converter does not have significant switching loss, the switching frequency cannot be set arbitrarily high. This is because the converter needs to spend time on state 0 (ZVS transition state) and state 6 (resonant state). If the switching frequency is too high, the duty cycle of these two types of states will be large, which would then require a high magnetizing current, leading to higher losses. This shows the tradeoffs that inevitably need to be made in the converter design. It should be noted that a relatively small value of magnetizing inductance gives flexibility in dynamically controlling the dc magnetizing current so as to achieve low loss and a wide control range. Considering all these factors, the final S4T is designed to have a switching frequency of 15 kHz.

8.2.3. Gate Driver

The gate driver from Cree™ CRD001 is selected to drive the active devices. It has isolated dc/dc converters to provide adjustable positive and negative gate pulse voltages, with an isolation rating of 5.2 kV. The opto-isolator has a high common mode transient immunity of 30 kV / μs. In the converter design, the gate driver boards are placed close to the devices such that the parasitic inductance of the gate driver loop is minimized.

8.2.4. Filters

Filters are needed at the input and output terminals to suppress the switching harmonics. Filter capacitors provide energy filtering on a switching cycle-to-cycle basis and ensure sinusoidal output voltages on the input and the output. Filter capacitors should be large enough such that the voltage ripple is maintained within an acceptable range. A 5~10% voltage ripple is considered reasonable for selecting the filter capacitance. Also, the reactive power effect of the capacitors should be considered when selecting the capacitance values. Different from the voltage source converter, the capacitive filters of S4T offer very low *dv/dt*, low EMI, and low harmonic distortion across the unit terminals.

It is important to achieve low parasitic inductance for the filter capacitors. Large parasitic inductance of the filter capacitors will result in a voltage spike when the devices are switching off, which leads to switching loss for the S4T. Film capacitors are used for the design, which typically have low ESL. Capacitor banks consisting of multiple parallel-connected large and small capacitors are used for the design to achieve even smaller equivalent ESL. Large capacitors provide energy buffering for the entire switching cycle. Small capacitors are placed close to the devices, providing snubbering and low ESL path for the device switching transients.

Filter inductors ensure sinusoidal current injection into the input and the output. With filter capacitors being selected, the filter inductors should be sized such that the switching harmonics components are attenuated enough to meet the harmonics standard. The S4T has a capacitive filter structure, for which the filter inductor is connected with a shunt filter capacitor such that it does not see the switching voltage ripples as the conventional voltage source converter. This leads to lower filter inductor losses. It should also be noted that for some types of load such as motors, filter inductors are not needed due to the inductive property of these loads.

The second-order LC filter has a resonant frequency at $1/2\pi\sqrt{L_f C_f}$. Since the source voltage contains some harmonics at various frequencies, the harmonic component around

this resonant frequency causes resonance, and thus the corresponding current harmonics will be amplified. To damp this resonance, a passive damping method is used, in which a resistor is connected in series with the filter inductor. The filter with a damping resistor for each phase is shown in Fig. 8.1. The optimal damping resistor value is calculated as equation (8.1) [97]. However, this damping resistor will degrade the harmonics attenuation of the filter since it provides an alternative path for the harmonics current. Therefore, the resistor needs to be slightly tuned around its optimal value to achieve the highest quality current injection.

$$R_{damp} = \sqrt{\frac{L_f}{C_f}} \tag{8.1}$$

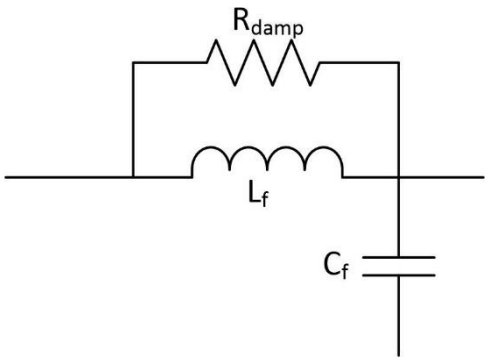


Fig. 8.1: LC filter with a damping resistor.

8.2.5. Snubbers

Unlike hard-switching converters, the main devices of the S4T do not need extra snubbers due to the soft-switching feature. The resonant capacitors provide active voltage clamping for all the devices with a reduced *dv/dt*. However, the S4T still needs several small-rated snubbers for the auxiliary devices as well as the diodes in series with the transformer.

For the diodes connected in series with the transformer, when the current is transferring from one bridge to another, the transformer leakage inductance and the diode parasitic capacitance C_{d_series} start to resonate, which will develop a voltage spike across the series diode. A proper RC snubber is needed for protecting the series diode, as shown in Fig. 8.2. The resonance frequency of L_{lk} and C_{d_series} without a snubber is determined by equation (8.2). By adding C_{ds}, the resonant frequency is changed to the one shown in equation (8.3).

It is common to select C_{ds} such that the resonant frequency is reduced by half. R_{ds} is selected using equation (8.4) such that it can provide critical damping for the oscillation.

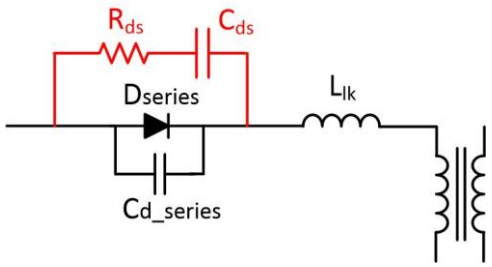


Fig. 8.2: Diode in series with the transformer and its snubber.

$$f_{d\_resonant} = \frac{1}{2\pi\sqrt{L_{lk}C_{d\_series}}} \tag{8.2}$$

$$f_{d\_resonant\_new} = \frac{1}{2\pi\sqrt{L_{lk}\left(C_{d\_series} + C_{ds}\right)}} \tag{8.3}$$

$$R_{ds} = \sqrt{\frac{L_{lk}}{C_{ds} + C_{series}}} \tag{8.4}$$

8.2.6. Sensors

Parameters need to be sensed include the transformer magnetizing current, filter capacitor voltages of the three-phase input and output, three-phase grid voltage, and three-phase line current. LEM^{TM} sensors are used to sense all the voltages and currents, which give high-frequency resolution and dc signal sensing capability. To sense the magnetizing current, the positive terminals of both the primary winding and the secondary winding pass through a LEM^{TM} current sensor. The sum of the primary and secondary winding current always equals to the magnetizing current. The magnetizing current measurement scheme is shown in Fig. 8.3.

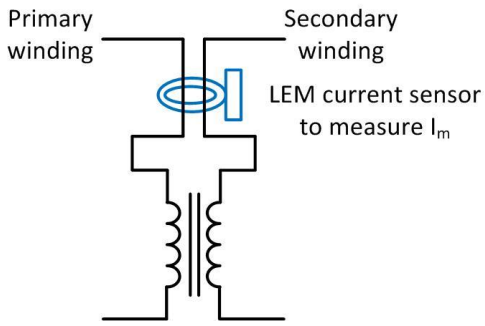


Fig. 8.3: LEM current sensor to measure the transformer magnetizing current.

8.3. Design of the Auxiliary Resonant Circuit

8.3.1. Design of the Resonant Inductor L_r and the Resonant Capacitor C_r

The auxiliary resonant circuit, consisting of C_r, L_r, and S_r, is key to successful operation of the S4T over its designed load range. It provides ZVS conditions for all the main devices. It is reset at each switching cycle by starting a resonant operation of L_r and C_r. C_r determines the *dv/dt* rate when the main devices are turned off, and thus it governs the turn-off loss of devices. L_r and C_r determine the length of the resonant period and the current stress of S_r. Therefore, the design of the auxiliary resonant circuit is guided by the following objectives.

1) C_r should be selected such that device turn-off loss is minimized to almost zero;

2) The peak value of i_{Lr} should be within the safe operation area of the auxiliary device;

3) The RMS value of i_{Lr} should be minimized to reduce the circulating power loss;

4) The resonating time period of L_r and C_r should be minimized such that most of the switching time period is used for transferring energy from the input to the output;

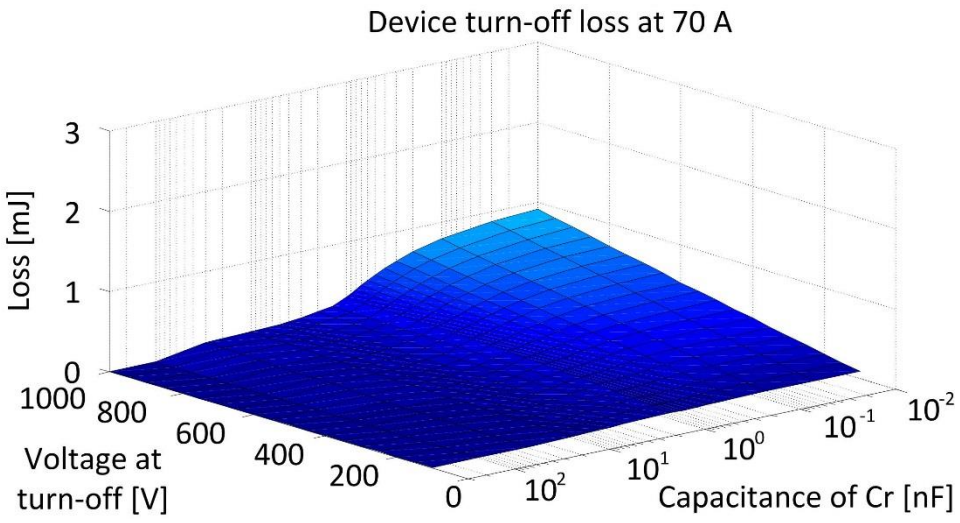
5) The peak voltage of v_{cr} should be close to 1 p.u;

6) Time duration of the ZVS transition should be long enough to ensure that the incoming turn-on device is gated-on within this transition state.

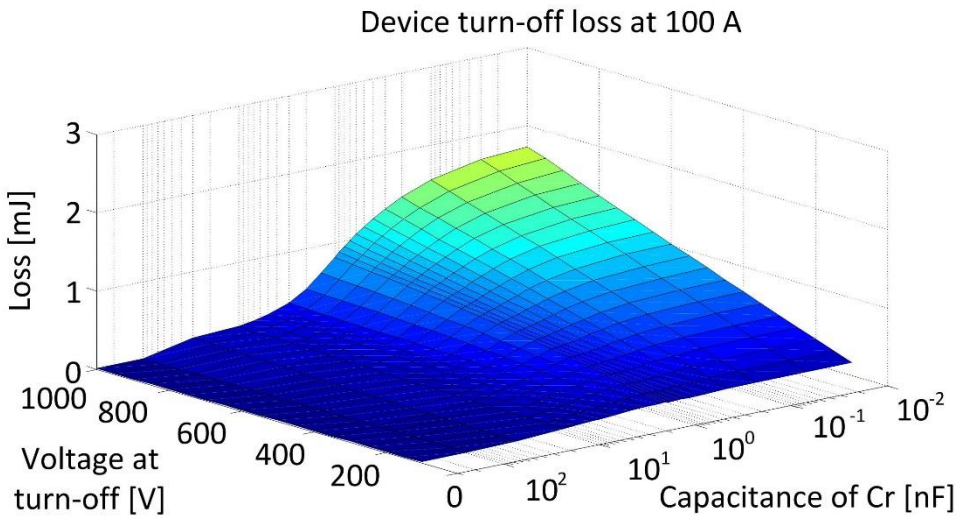
For objective 1), the *dv/dt* rate at the device turn-off transition is controlled by C_r, which in turn determines the device turn-off loss. There are two turn-off scenarios for the S4T, one for phase-leg transition and one for bridge-to-bridge transition. One device is turned off for the phase-leg transition, while two are simultaneously turned off for the bridge-to-bridge

transition. The *dv/dt* for the latter one is only half of the former. Therefore, C_r should be large enough such that the turn-off loss at the phase-leg transition is reduced to almost zero. Consider a converter rated at 208 V / 10 kVA, with a switching frequency of 15 kHz and L_m of 200 µH. Simulation results show that in the steady state operation at the full load level of 10 kVA, the devices are always switched around the three current levels of 70 A, 100 A, and 130 A. Fig. 8.4 shows the device turn-off loss versus different C_r values for the device of C2M0025120D at these three current levels. It can be seen from the figure that the turn-off loss is close to zero when C_r is larger than 0.1 µF. At the highest switching current level of 130 A, the *dv/dt* at the device turn-off transition is governed by equation (8.5). With 0.1 µF C_r, the corresponding *dv/dt* at 130 A is 1300 V/µs. As a comparison, the *dv/dt* for the Si IGBT NGTB50N120FL2WG is 6000 V/µs and for the SiC MOSFET C2M0025120D is 28500 V/µs, as given by the datasheet. However, even though 0.1 µF C_r is enough to reduce the turn-off loss to zero, the C_r value also determines the maximum voltage stress of all the main devices due to the magnetizing current charging effect after the resonant operation.

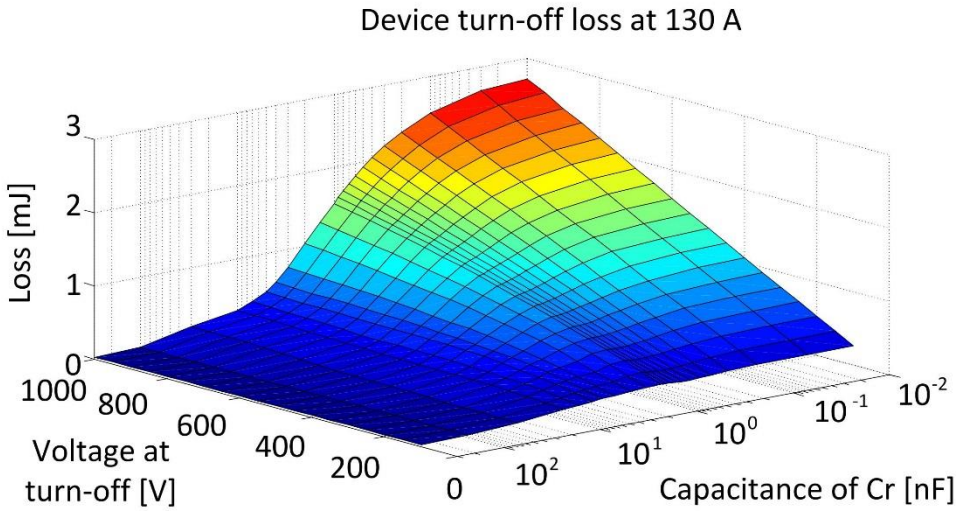
$$\frac{dv_{cr}}{dt} = \frac{130}{C_r} \tag{8.5}$$



(a)



(b)



(c)

Fig. 8.4: Device turn-off loss versus C_r capacitance at three turn-off current levels during the phase-leg transition.

The peak value, RMS value of the resonant current i_{Lr}, resonant time period T_r, and the peak value of v_{cr} are all governed by the resonant state, whose corresponding state is governed by equation (8.6). The expressions of v_{cr} and i_{Lr} are then given in equation (8.7). The peak current of i_{Lr} is obtained by having di_{Lr}/dt equal to zero, as given by equation (8.8). The resonant time period T_r shown in equation (8.9) is derived by having i_{Lr} equal to zero. The RMS value of i_{Lr} is calculated using equation (8.10). Finally, the peak value of v_{cr}, given by equation (8.11), is obtained by having dv_{cr}/dt equal to zero. Fig. 8.5 shows the peak value,

RMS value of i_{Lr}, resonant period T_r, and the peak value of v_{cr} versus different L_r and C_r values.

$$\begin{cases} i_{Lr} + i_{Cr} = I_m \\ v_{Cr} = L_r \dfrac{di_{Lr}}{dt} \\ i_{Cr} = C_r \dfrac{dv_{Cr}}{dt} \end{cases} \text{ with the initial conditions of } \begin{cases} v_{Cr}(t=0) = V_{Cr0} \\ i_{Lr}(t=0) = 0 \end{cases} \tag{8.6}$$

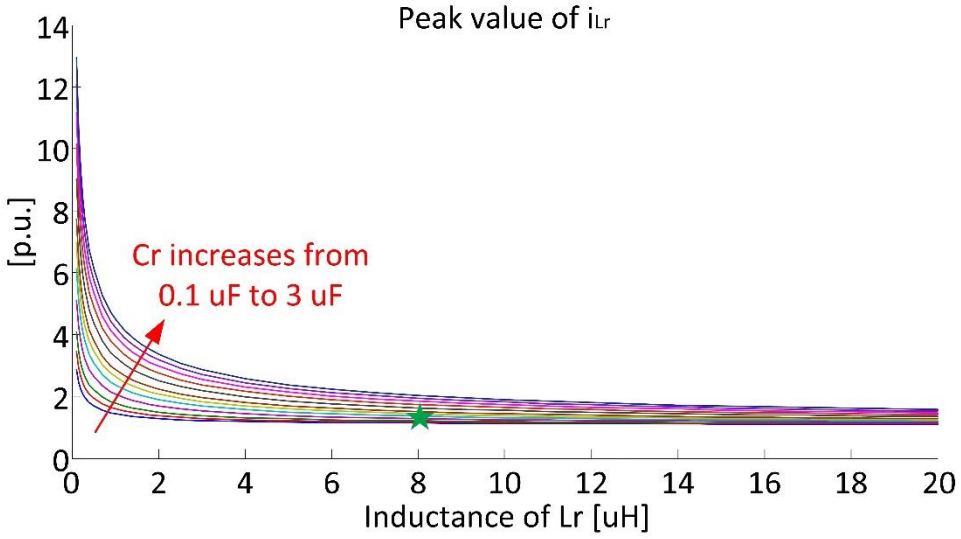
$$\begin{cases} v_{Cr} = I_m \sqrt{\dfrac{L_r}{C_r}} \sin\left(\sqrt{\dfrac{1}{L_r C_r}} t\right) + V_{Cr0} \cos\left(\sqrt{\dfrac{1}{L_r C_r}} t\right) \\ i_{Lr} = I_m \left(1 - \cos\left(\sqrt{\dfrac{1}{L_r C_r}} t\right)\right) + V_{Cr0} \sqrt{\dfrac{C_r}{L_r}} \sin\left(\sqrt{\dfrac{1}{L_r C_r}} t\right) \end{cases} \tag{8.7}$$

$$I_{Lr,pk} = I_m \left(1 + \sqrt{\frac{L_r I_m^2}{C_r V_{Cr0}^2 + L_r I_m^2}}\right) + C_r V_{Cr0}^2 \sqrt{\frac{1}{L_r C_r V_{Cr0}^2 + L_r^2 I_m^2}} \tag{8.8}$$

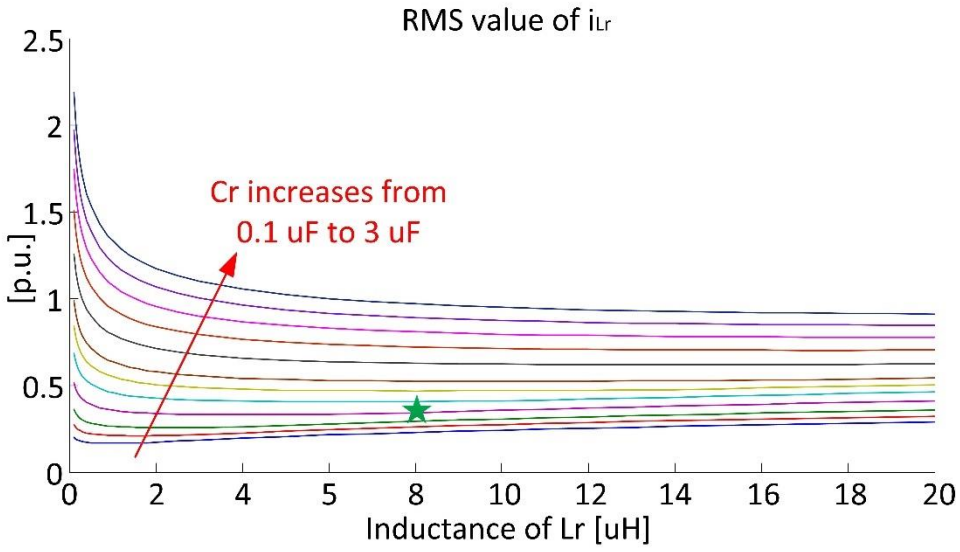
$$T_r = \sqrt{L_r C_r} \left(2\pi - \sin^{-1} \frac{2 V_{Cr0} I_m \sqrt{L_r C_r}}{L_r I_m^2 + C_r V_{Cr0}^2}\right) \tag{8.9}$$

$$I_{Lr,rms} = I_{Lr,pk} \sqrt{\frac{T_r}{2T_{SW}}} \tag{8.10}$$

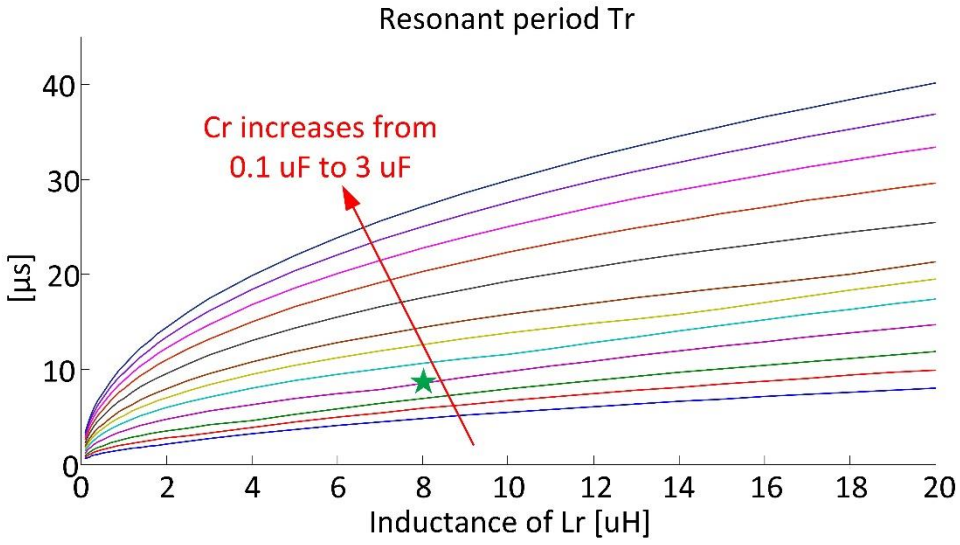
$$V_{Cr,pk} = I_m^2 L_r \sqrt{\frac{1}{L_r C_r I_m^2 + C_r^2 V_{Cr0}^2}} + V_{Cr0}^2 \sqrt{\frac{C_r}{L_r I_m^2 + C_r V_{Cr0}^2}} \tag{8.11}$$



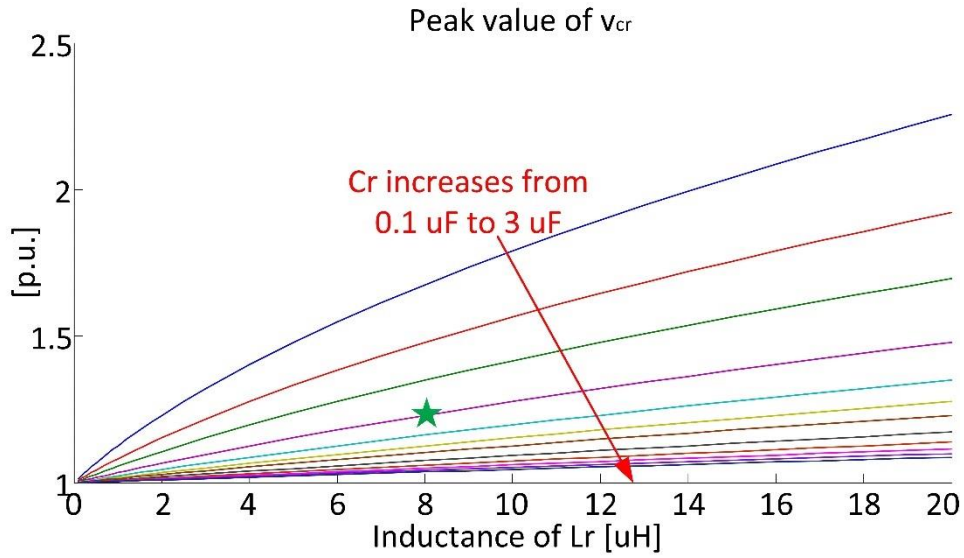
(a)


RMS value of iLr
2.5
2
1.5
1
0.5
0
[p.u.]
Cr increases from
0.1 uF to 3 uF
0
2
4
5
8
10
12
14
16
18
20
Inductance of Lr [uH]

(b)


Resonant period Tr
40
30
20
10
0
[µs]
Cr increases from
0.1 uF to 3 uF
0
2
4
6
8
10
12
14
16
18
20
Inductance of Lr [uH]

(c)



(d)

Fig. 8.5: Peak value, RMS value of i_{Lr}, resonant period T_r, and peak value of v_{cr} versus different L_r and C_r values.

It can be seen from the figure that a larger L_r leads to a higher peak and RMS value of i_{Lr}, a longer resonant period T_r, and a higher peak value of V_{cr}. Although a larger C_r also leads to a higher peak and RMS value of i_{Lr}, as well as a longer resonant period T_r, the peak value of V_{cr} will become smaller. In addition, the *dv/dt* rate, controlled by C_r, should be low enough such that the devices can finish their switching action on time at the desired transition, considering the latency of the controller, the gate driver, and the device switching time. As a result, the parameters of L_r=8 µH and C_r=0.4 µF, corresponding to the green star indicator shown in Fig. 8.5, are selected for the 208 V / 10 kVA converter.

8.3.2. Design of the Snubber for the Auxiliary Device S_r

The device S_r of the auxiliary circuit is implemented by an active device in series with a diode, and it is connected in series with the resonant inductor L_r. There are two scenarios for which an over-voltage stress will be developed across S_r. First, the reverse recovery current of the series diode of S_r causes resonance between the diode parasitic capacitance C_{dr} and L_r. At end of the resonant operation between L_r and C_r, the current through S_r and L_r resonates to zero with a reduced *di/dt* rate. If a Si diode is used for S_r, reverse recovery current is developed, and the associated energy stored in L_r is given by equation (8.12), in

which I_{rr} is the peak diode reverse recovery current. Once the diode snaps off, this amount of energy starts a resonance between L_r and the parasitic capacitance of the diode C_{dr}, which will cause a voltage spike across S_r. Even if a SiC diode is used for S_r, for which the reverse recovery is negligible, the resonance between L_r and C_{dr} still develops a voltage spike, but with a reduced amplitude. Therefore, a RCD snubber is required to protect the auxiliary device S_r. The secondary scenario is that the active device S_r is turned off before the current through it resonates to zero, due to any faulty operation. In this case, turning off S_r interrupts the L_r current flowing path, and thus a voltage spike will be developed across S_r. Considering this issue, another RCD snubber is also needed. One integrated snubber shown in Fig. 8.6 can provide voltage clamping for S_r in both the scenarios. The snubber, which is highlighted in red, consists of two diodes D_{s1} and D_{s2}, a capacitor C_s, and a resistor R_s. For the first scenario, D_{s1} conducts when the voltage developed by the resonance exceeds a certain level, and C_s provides voltage clamping to protect S_r from over-voltage stress. For the second scenario, D_{s2} provides an alternative current flowing path if the current through L_r is interrupted by S_r. For both cases, the energy trapped in L_r should be dumped to C_s without a large voltage spike developed across C_s. Since a SiC diode is connected in series with a Si IGBT to implement S_r and the SiC diode has a very small reverse recovery current, sizing of the snubber should be dominated by the second scenario, and the corresponding snubber design will be as follows.

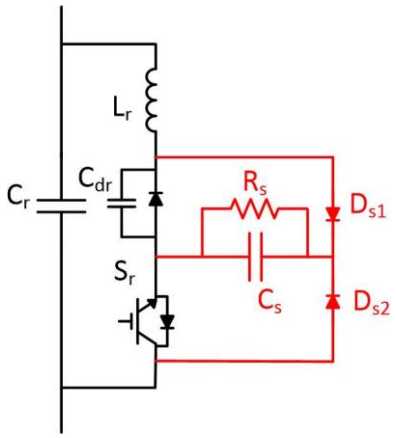


Fig. 8.6: Resonant circuit and snubber for the auxiliary device.

$$E_{Lr} = \frac{1}{2} L_r I_{rr}^2 \tag{8.12}$$

Assuming S_r is turned-off by fault when the current through S_r is I_{sr_fault}, and assuming this occurs in every switching cycle for the worst case, then the minimum capacitance value of C_s is governed by equation (8.13), in which V_{cs} is the steady state voltage of C_s and ΔV_{cs} is the allowed voltage ripple when the energy trapped in L_r is fully transferred to C_s. V_{cs} determines the voltage clamping level for the device. The power that needs to be dissipated by the resistor R_s is governed by equation (8.14), in which f_{sw} is the converter switching frequency. Then the resistance value is calculated using equation (8.15).

$$\frac{1}{2} C_s \left(\left(V_{cs} + \Delta V_{cs} \right)^2 \right) - \frac{1}{2} C_s V_{cs}^2 = \frac{1}{2} L_r I_{sr\_fault}^2 \tag{8.13}$$

$$P_s = \frac{1}{2} L_r I_{sr\_fault}^2 f_{sw} \tag{8.14}$$

$$R_s = \frac{V_{cs}^2}{P_s} \tag{8.15}$$

8.4. Design of Controller

8.4.1. Control Board

The embedded controller for the S4T collects several sensed signals, performs signal processing such as noise filtering, runs the embedded control algorithm, and generates gate commands for the device gate drivers. The controller used for the S4T is a customized FPGA-DSP based control board, shown in Fig. 8.7. It has a 50 MHz Altera™ EP4CE series FPGA and a 225 MHz TI™ floating point DSP TMS320C6713. The board has three 16-bit ADCs and two 12-bit DACs. It has 18 signal processing channels, and each of them has a signal amplification stage and a filtering stage. It also has fiber optic I/Os, digital I/Os, relays, and communication ports.

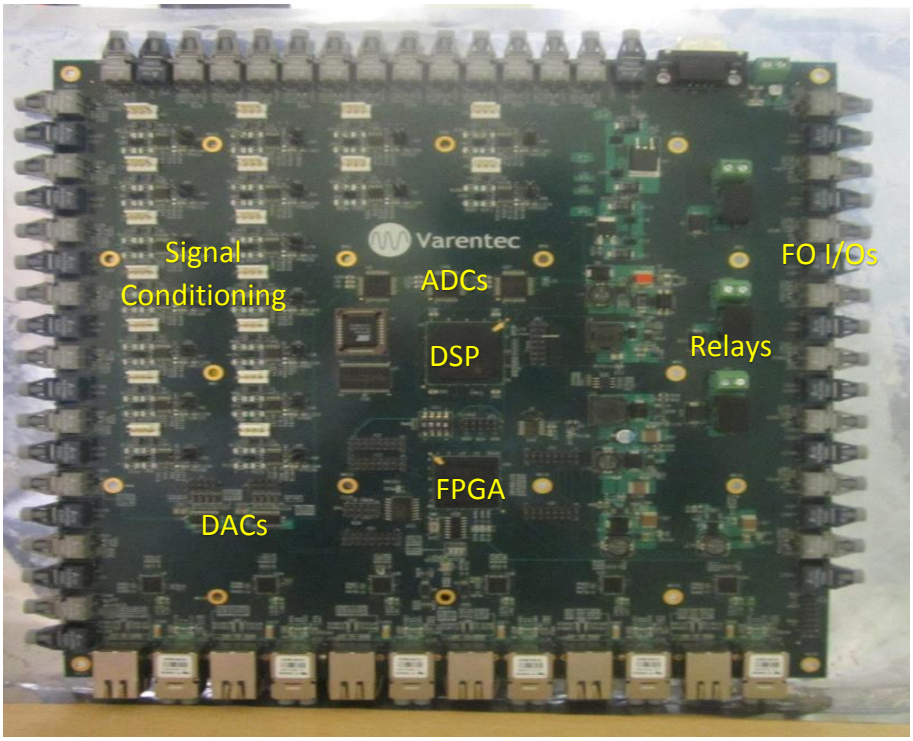


Fig. 8.7: FPGA-DSP based customized control board for controlling the S4T.

Each of the three ADCs can simultaneously sample six-channel signals at the same sampling frequency. Control principle for the S4T requires that the magnetizing current and filter capacitors voltage need to be sampled at a much higher frequency, while the grid voltage and line current can be sensed at the switching frequency. Therefore, the ADCs are assigned to sense signals in the following way: one ADC for sensing the magnetizing current at 400 kHz using one channel, one for sensing the input and output filter capacitor voltage at 400 kHz with all six channels, and one for sensing three-phase line voltage and current at 15 kHz with all six channels. For the signal conditioning circuit, each channel should have the cutting-off frequency of the filtering stage select properly such that the corresponding sensed signal is not attenuated.

8.4.2. Data Processing

After analog signals are processed through signal conditioning circuits and converted to digital signals through ADCs, the embedded firmware will run the control algorithm to generate commands for gate drivers. The embedded code is programmed in both the DSP

and the FPGA, with the FPGA continuously running at 50 MHz and the DSP interrupt routine being triggered once every switching cycle. The data processing flow is as follows. At the beginning of each switching cycle, the FPGA generates a signal to trigger the ADC to start signal processing (for signals that need to be sensed at a higher frequency, the FPGA has an independent state machine to generate a triggering signal). Once the ADC conversion is done, the FPGA processes the series data received from ADCs and converts it into a parallel format such that it can be stored in registers of the FPGA. After data processing is finished, the FPGA generates an interrupt signal to the DSP. The DSP then goes into the interrupt routine, in which the DSP reads data from the FPGA, runs the control algorithm, and writes calculation results to the FPGA. The FPGA then receives data from the DSP and updates the state machine, which is programmed to control the converter from one switching state to another. When the DSP interrupt routine is not triggered, the FPGA continuously monitors all the sensed signals. Once any fault is detected, it will drive the converter to the fault state to softly shut down the converter such that the converter is protected. The data flow exchanged among ADCs, the DSP, and the FPGA is shown in Fig. 8.8. The data reading and writing between the DSP and the FPGA is through the EMIF (external memory interface) to expedite the data exchange.

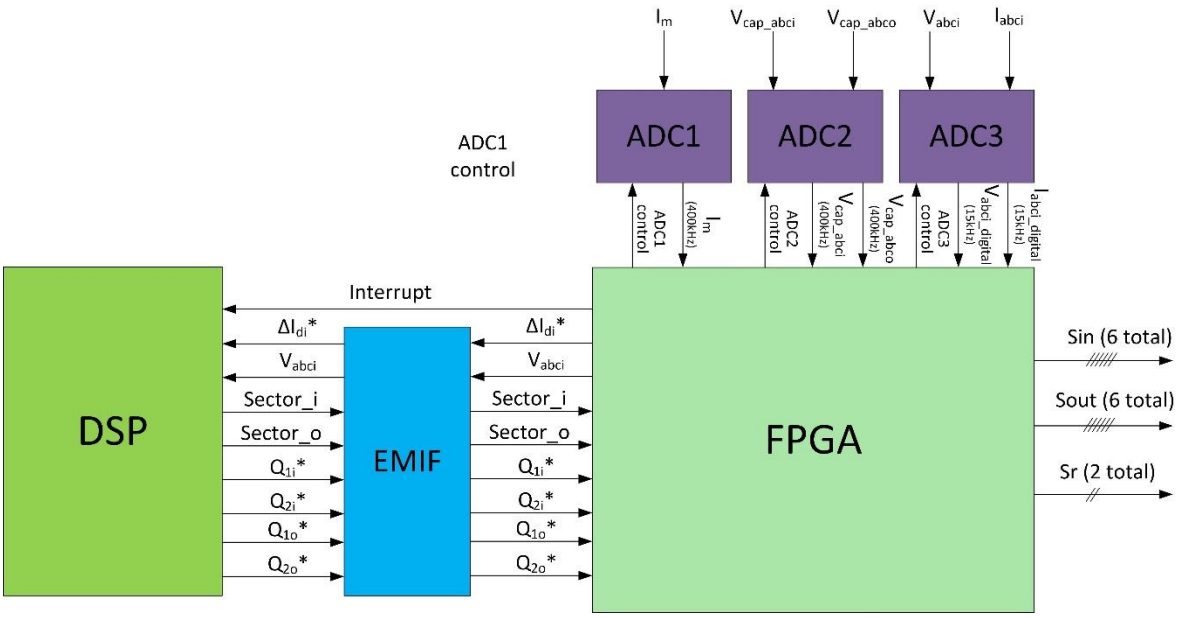


Fig. 8.8: Data exchange among ADCs, the DSP, and the FPGA.

8.4.3. Algorithms

From the above stated data processing flow, it can be seen that the algorithm in the DSP is triggered once at each switching cycle, while the FPGA is running at a much faster frequency. However, the DSP is good at performing math-intensive calculations while the FPGA is not. Therefore, the entire control algorithm should be properly divided, for which the math-intensive part is programmed in the DSP and the time-sensitive part is programmed in the FPGA. Within the entire control architecture, the phase-lock-loop (PLL) for tracking the grid voltage, the abc-to-dq and dq-to-abc transformations, and the line voltage sector detection require complicated mathematical calculations, and they can be processed only once every switching cycle. Therefore, the algorithm corresponding to these parts is programmed in the DSP. The state-machine to control the S4T and the fault protection need a much shorter latency, and are thus programmed in the FPGA. In addition, the control loop to regulate the magnetizing current as well as the charge calculation and modulation need much faster processing, which are also programmed in the FPGA. Finally, since the magnetizing current and filter capacitor voltages are sensed at a much higher frequency of 400 kHz, these data are only processed in the FPGA, and they are not passed to the DSP. The algorithm to be programmed in the DSP and the FPGA is highlighted in Fig. 8.9.

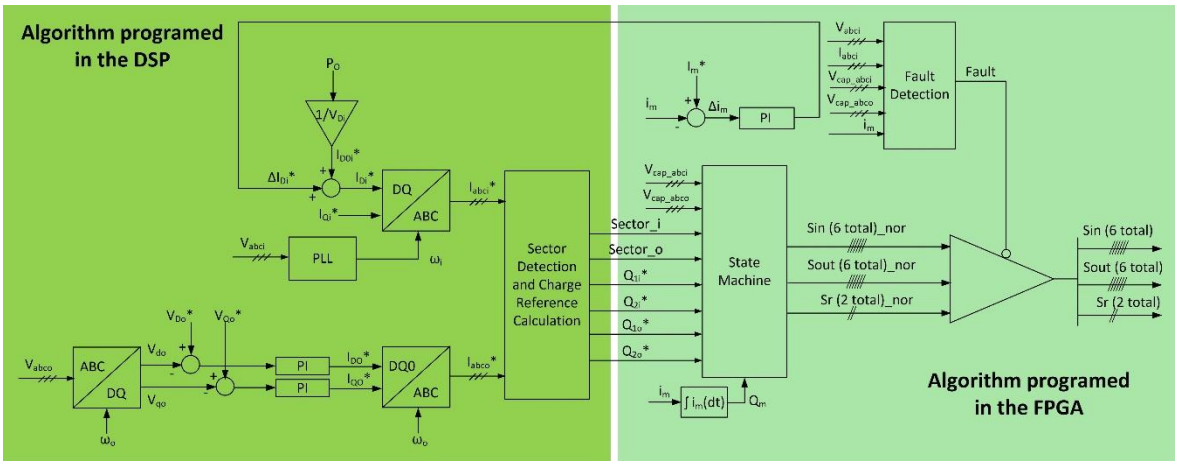


Fig. 8.9: Control algorithm to be programmed in the DSP and the FPGA.

8.4.4. State Machine

The state machine commands the converter switching from one state to another. In the steady state, the converter has two active charging states, two active discharging states, one freewheeling state, and six ZVS transitioning states over one switching cycle. Fig. 8.10 shows the state machine programmed in the FPGA for the S4T. For each switching cycle, the implemented state machine actually starts from the discharging state (i.e., the output bridge operation). The reason for this is to make sure that the freewheeling state, that is following the two active charging states, occurs last within a switching cycle. In this way, the time duration of the freewheeling state does not need to be pre-calculated. It starts after the two charging states, and ends when a new switching cycle is initiated.

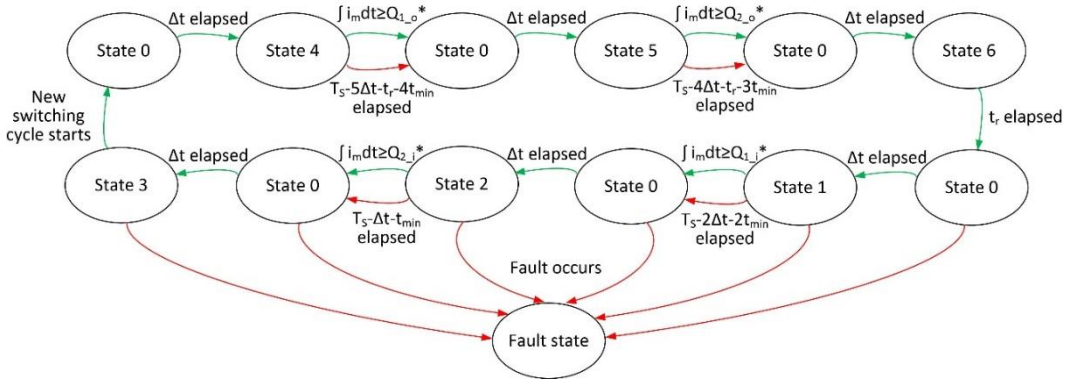


Fig. 8.10: State machine programmed in the FPGA to control the converter.

Conditions for normally transitioning from one state to another are described as below, which are also denoted as green arrows in Fig. 8.10. For the transitions from active states (state 4, 5, 1, 2,) to the ZVS transition state (state 0), the condition is that a required charge is delivered to specific terminals of the input or the output (i.e. charge control modulation). For transitions from state 0 to other states, the condition is that state 0 lasts for a duration of Δt. Δt should be selected such that after this amount of time duration, the resonant capacitor voltage is still higher than the incoming line-to-line voltage, ensuring ZVS turning-on of the incoming devices. Δt is set to be 100 ns for the designed S4T converter, considering the *dv/dt* rate corresponding to 100 A dc current and 0.4 µF resonant capacitors. For transitioning from the resonant state (state 6) to the ZVS transition state (state 0), the condition is that

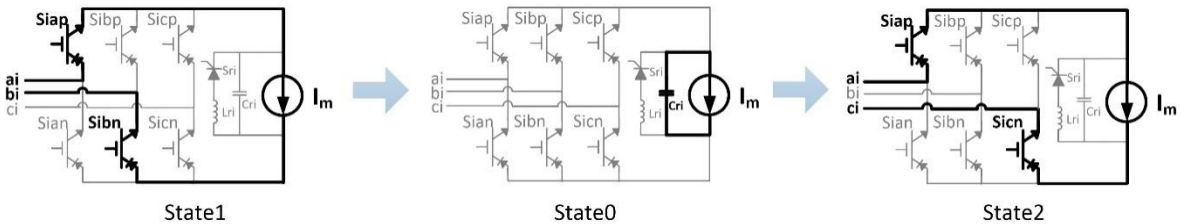
state 6 lasts for a duration of t_r. t_r should be selected large enough such that the resonant operation between L_r and C_r concludes and that the current through L_r reaches zero. t_r is selected to be 7.5 μs for the designed S4T converter, considering the resonant period corresponding to 0.4 μF C_r and 8 μH L_r. The condition for transitioning from the freewheeling state (state 3 which is the last state for the entire switching cycle) to state 0 is the start of a new switching cycle.

All the above conditions are for the normal transitions from one state to another. However, for some cases, these transitioning conditions may not be satisfied. For example, the transformer magnetizing current may be too low such that it takes a very long time duration to deliver the required charge. Then the converter will be staying at an active state for a very long time just because the transition condition is not met. As a result, the converter will not be able to cycle through all these states before the ending of the entire switching cycle. When a new cycle starts, the converter directly switches from the current state to state 0 and then to state 4. Taking a specific example, the converter stays at state 5 until the end of the switching cycle, because it cannot deliver the required charge to the second output phase pair. When a new switching cycle starts, the converter is forced to enter state 0 and then state 4. In this case, the resonant capacitor voltage directly jumps from a lower voltage level to a higher one, causing inrush current. To avoid this, alternative transitioning conditions are programmed, shown as red arrows in Fig. 8.10. In these alternative conditions, a "watch dog" timer initiates alternative action. The timer starts counting at the beginning of each switching cycle, and it is reset at the end of each cycle. If the "watch dog" finds that the converter stays within one state for a too long time, it will force the converter to enter the next state, regardless whether the normal transitioning conditions have been satisfied or not. The "watch dog" is programmed to make sure that the converter cycles through all the states, under both normal and abnormal conditions. The minimum time duration for each active state is t_{min}, which is set to be 1 μs in the program.

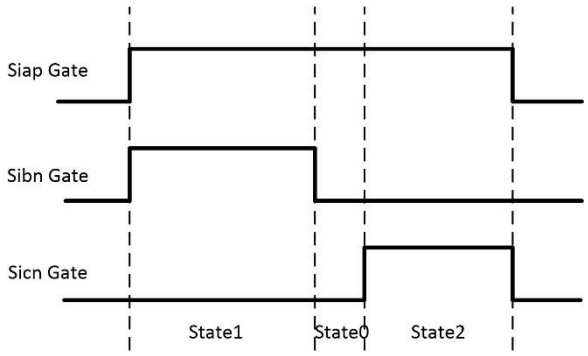
In addition, the state machine also has a fault state. If any fault is detected, the state machine will stop cycling through all the states, and it will enter the fault state, which is a freewheeling state to bring the transformer magnetizing current to zero. However, the converter is only allowed to directly switch to the fault state from specific states (states 1, 2, 3 and the corresponding state 0 in between), as shown in Fig. 8.10. If the converter is in other states, the state machine has to continuously run until the converter enters these allowed states, before switching to the fault state. This is to avoid inrush current caused by the charging the resonant capacitor, which will be discussed in chapter 11.

8.4.5. State Transition Considering the Common Emitter Inductance Effect

Ideally, when the converter transitions from one active state to the ZVS state and then to another active state, only one device needs to be switched. Taking a transition from state 1 to state 0 and then to state 2 as a specific example, Fig. 8.11 (a) shows the circuit states during this transition, in which only the primary side bridge is shown and the transformer magnetizing current is represented as a constant dc current source I_m. In state 1, S_{iap} and S_{ibn} are on, which have the dc current flowing through these two devices. After that, device S_{ibn} is turned off, then converter enters state 0 and it causes I_m flowing through the resonant capacitor. Device S_{icn} can be turned on within state 0, and it will automatically conduct once the voltage across it drops to zero. The current I_m is thus transferred from S_{ibn} to S_{icn} with all devices being switched under ZVS conditions. Through the entire transition, the gate signal of S_{ian} can be kept high. Fig. 8.11 (b) shows the gate signals of these three devices through this transition.



(a)



(b)

Fig. 8.11: Transition from state 1 to state 0 and then to state 2: a) circuit states during the transition; and b) relative device gate signals.

However, for the devices that have a common emitter parasitic inductance, turning off S_{ibn} can develop a voltage spike on the gate terminal of S_{iap}. Fig. 8.12 shows the device S_{iap} with a common emitter inductance L_{ee}. When S_{ibn} is turned off, the current flowing through both S_{iap} and S_{ibn} is interrupted, and then I_m flows to the resonant capacitor. The *di/dt* at the turning-off transition will develop a voltage spike across parasitic inductance L_{ee} of S_{iap}, as shown in Fig. 8.12, which will cause the actual gate terminal voltage of S_{iap} to be higher than the gate driver's output voltage, as shown in equation (8.16). This gate voltage spike can destroy the device if it exceeds the maximum rating of the gate terminal. For SiC devices, it becomes more severe since the SiC devices have a much higher *di/dt* rate but a lower maximum gate voltage rating. Taking the SiC device C2M0025120D as an example, this 1200 V/ 90 A rated device can have a *di/dt* rate of 1800 A/μs at turning off. It is suggested to be driven at a voltage level of 20 V to achieve low conduction loss, while the maximum gate voltage rating is only 25 V. This means that with 1800 A/μs *di/dt*, the voltage spike developed across the common emitter parasitic inductance has to be controlled within 5 V, which is very challenging. Fig. 8.13 shows the experimental waveform of the gate voltage spike of a high-side device when a corresponding low-side device is turned off.

$$V_g^{'} = V_g + L_{ee}\frac{di}{dt} \tag{8.16}$$

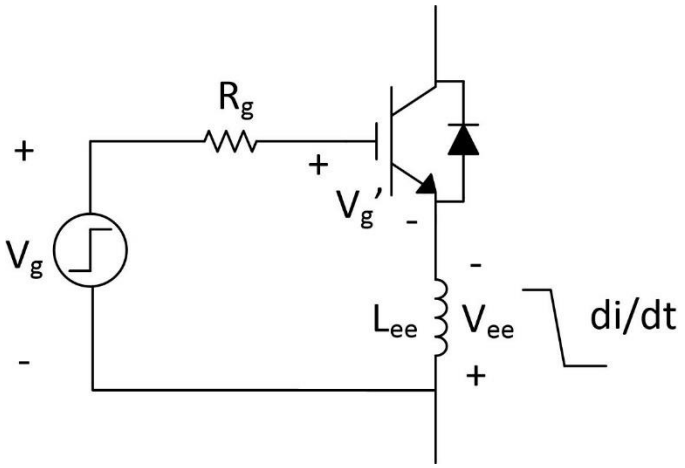


Fig. 8.12: A device with a common emitter parasitic inductance.

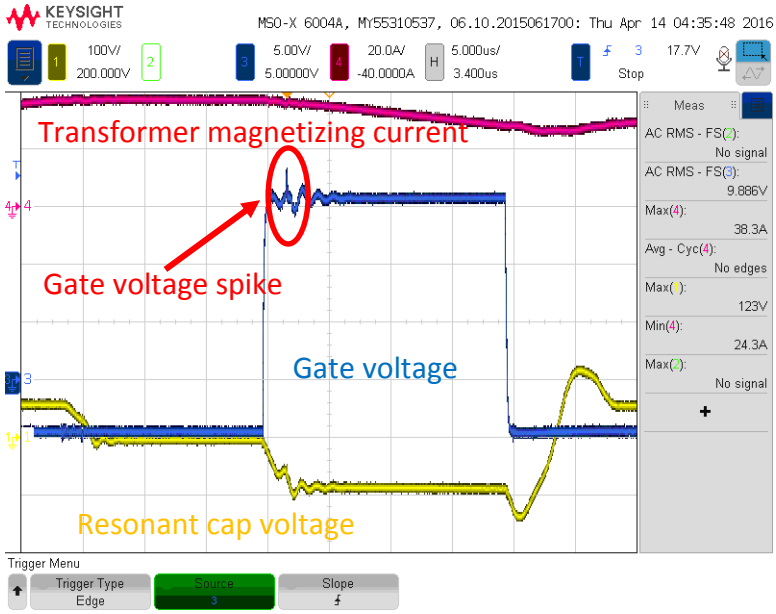


Fig. 8.13: Experimental waveform of the gate voltage spike.

This is a unique issue for the S4T in that turning off one device will develop a gate voltage spike on the complementary device. One way to solve this problem is to simultaneously turn off S_{iap} when S_{ibn} is turned off. In this way, the gate voltage of S_{iap} is pulled low, having the total voltage amplitude seen by the device gate terminal to be smaller, even though a voltage spike is developed across the common emitter parasitic inductance. Fig. 8.14 shows the modified device gate signals of S_{iap}, S_{ibn}, and S_{icn}, considering the common emitter inductance issue, in which the S_{iap} gate signal is pulled low at state 0.

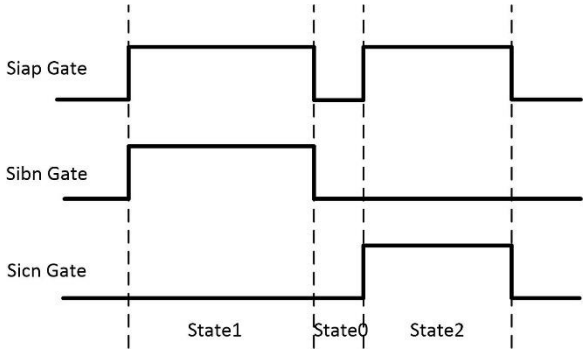


Fig. 8.14: Modified device gate signals when considering the common emitter inductance issue.

Another effective method to solve this issue is by using a device that has a Kelvin Emitter connection, whose circuit diagram is shown in Fig. 8.15. For this type of device, the gate loop and the power loop do not share the same emitter parasitic inductance. The gate loop has its own emitter terminal, and thus the main current of the device will not flow through the emitter parasitic inductance in the gate loop. This will avoid the gate voltage spike when turning off the complementary device. In this case, the gate drive signals do not need to be modified during the transition.

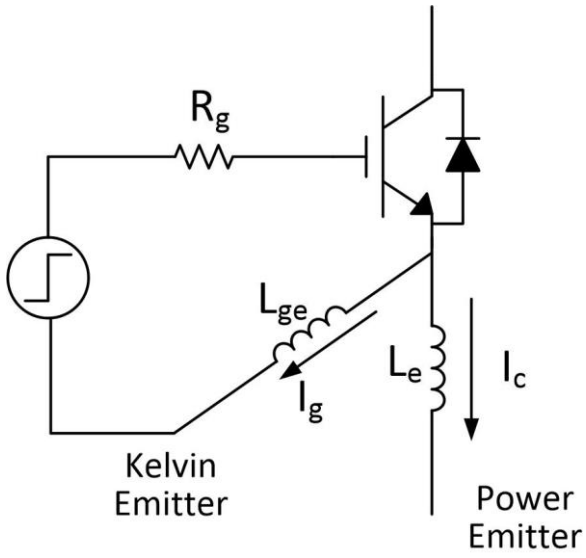


Fig. 8.15: Device with a Kelvin Emitter connection.

8.5. Fault Protection

Various faults, such as line over-voltage fault, line over-current fault, over-voltage across the resonant capacitors, and over-current through the transformer magnetizing

inductance due to faulty operation, may occur in the S4T unit. The converter has protection implemented in both hardware and software to protect the unit from all the above faults.

8.5.1. Hardware Protection

In the S4T, the inherent current limiting capability avoids inrush current. However, as a backup protection, fuses are connected in both the input and output terminals of the S4T.

The resonant capacitor determines the voltage stress of the device. Once faulty operation occurs, the resonant capacitor voltage may reach a very high level. Interrupting current flow in a conventional CSI, for instance due to a loss of the control power, can quickly develop a voltage spike across the devices. The high *dv/dt* under an open-circuit failure for CSIs requires a very fast acting overvoltage protection scheme. However, for the S4T, since the resonant capacitors significantly reduce the *dv/dt* rate, the devices can be easily protected by only connecting metal-oxide varistors (MOVs) in parallel with the resonant capacitors. The MOVs should be selected such that they start conducting all the transformer magnetizing current before the resonant capacitor voltage reaches the maximum voltage level that devices can withstand.

8.5.2. Software Protection

During the S4T operation, the FPGA continuously runs the state machine to monitor signals of the input and output capacitor voltage, line current, and transformer magnetizing current. Once any of these signals exceed certain levels, the converter will immediately go to the soft shut-down mode. To shut down the converter, one device leg of the input or output bridge is turned on, or one device leg of both the input and output bridge are simultaneously turned on, which freewheels the magnetizing current and the voltage drop across the conducting devices brings the current to zero. However, the shut-down process can be only initiated when the resonant capacitor has a positive voltage, which avoids the inrush current when turning on the devices. The soft shut-down process was discussed in detail in chapter 8.

8.6. Conclusions

This chapter presents the detailed designs for the S4T, including the design, selection, and sizing of semiconductor devices, gate drivers, filters, snubbers, and sensors. The only snubber needed is to protect the diodes that are connected in series with the transformer, while the main devices do not need any snubber thanks to the soft-switching feature. The detailed design guidelines for the auxiliary resonant circuit and the associate snubber are also presented. The S4T is controlled by a customized DSP/FPGA control board. The data flow process for the controller and the embedded firmware architecture are described. Algorithm and the state machine to control the S4T under normal and fault conditions are developed. Finally, protection for the unit from various fault conditions through both hardware and software is presented. Compared to conventional current source inverters, the S4T exhibits higher reliability to various faults and can protect the devices much more easily.

This chapter covers the design of the power converter and the controller of the S4T. Next chapter will discuss the high-frequency transformer design, which is the most critical element of the S4T.

CHAPTER 9: HIGH-FREQUENCY TRANSFORMER DESIGN

9.1. Introduction

The high-frequency transformer is a key element of the S4T. It provides energy transfer between the input and the output with galvanic isolation. Due to high-frequency operation, the transformer design should be driven by objectives of maintaining low core loss and low copper loss, with relative low cost and small size. This requires a proper selection of core materials and an appropriate design of the windings. In addition, the need for high insulation levels could conflict with the requirement that transformer leakage should be kept low enough such that it does not affect the converter's normal operation. This chapter will present the detailed design of the high-frequency transformer. Transformer characterization is also performed to obtain various parasitic elements. Finally, since dc flux is stored in the transformer core for the S4T, a hybrid transformer design which integrates electromagnetic cores and permanent magnets is also explored. The hybrid design can significantly save magnetic core materials to store the same amount of energy.

9.2. Transformer Design with Magnetics

9.2.1. Magnetic Core

The core design is driven by two factors, core loss and core volume. As the transformer operates at a medium to high frequency, typically 10 – 20 kHz, the core loss should be kept low. The core loss consists of hysteresis loss and eddy current loss, which increases proportionally with the operating frequency and the flux swing. Loss data for a specific core material is typically given as watts/volume or watts/lbs. Core materials should be properly selected such that the core loss is kept small. Another important parameter for the transformer design is the peak flux density of the core material, which indicates the maximum flux that the core can carry before it saturates. The peak flux density determines the core volume for storing a desired amount of energy.

Table 9.1 lists several magnetic core materials for high-frequency applications, including ferrite (manganese zinc), amorphous-iron (Fe-based), and nano-crystalline (Fe-Si-B-Nb-Cu) [111]-[114]. Compared to amorphous-iron, nano-crystalline materials exhibit lower core loss by a factor of seven for a frequency of 25 kHz. Its peak flux density is around three times higher than that of the ferrite. Finally, the nano-crystalline material also has a higher curie temperature of 570 ^{o}C, which preserves the magnetic properties over a large range of temperature. Based on these comparisons, nano-crystalline is selected for the design.

Table 9.1: Characteristics of high-frequency magnetic materials [111]-[114].

Parameters		Ferrite	Nano-crystalline	Amorphous-iron
Saturation flux density B_{MAX} (T)		0.47	1.25	1.56
Core loss (mW/cm^3) at ±0.3 T	25 kHz	200	70	600
	50 kHz	500	200	2100
Curie Temperature (^{o}C)		200	570	399

For the S4T, the transformer needs to store a significant amount of dc energy in the core, thus it requires an air gap. The length of the air gap determines the inductance and the amount of energy that can be stored in the transformer. Most of the nano-crystalline cores have a U shape. For the transformer design, two U cores can be clamped together with air gaps between them. The core should have a large enough window area such that it can fill all the windings. One issue associated with the air gap is the stray flux that passes through the fringing field outside the air gap, which, if not designed properly, can lead to a significant amount of copper loss and noise and EMI that propagate to external circuits. Distributed air gaps and proper winding design can help mitigate this issue.

9.2.2. Winding Design

For high-frequency transformers, the winding should be designed properly to maintain a low winding loss. The winding loss consists of dc winding loss and ac winding loss. The dc winding loss only depends on the resistivity of the conductor and typically has a low value. The ac winding loss, resulting from the skin effect and the proximity effect, may become significant as the frequency goes higher. One effective way of minimizing the

winding loss is to use litz wires for the winding, which consist of many thin insulated wire strands. However, the litz-wire-based approach adds a significant cost to the design. It also leads to poor filling factor for the cores, and it may have higher resistance for dc current. A cost-effective method is to use the copper foil conductor with large conductor width, which is used in this design. Finally, proper insulation should be provided between windings to avoid voltage break-through. The insulation layer should be as thin as possible such that the transformer is designed to have a low leakage inductance, which is also a major driver for transformer design.

9.2.3. Leakage Inductance

The leakage inductance of the S4T transformer needs to be designed at an acceptable level. Even though the S4T does not need an additional leakage management state to deal with the energy trapped within the leakage inductance as the Dyna-C converter, a too large leakage inductance may still impact the converter's steady state operation. Several design methodologies can achieve a low leakage inductance. The co-axial transformer, proposed in [98], [99], has an outer conducting tube as the one-turn primary winding, and litz wires inside the tube as the secondary winding. The leakage flux is well contained within the tube, and the leakage inductance can be controlled at a very low value. However, this design imposes a manufacturing challenge when multiple turns of windings are required for the conducting tube. An alternative method is to layer the primary and secondary windings on top of each other such that the leakage flux is only constrained within the gap between them. Thin insulation materials should be used to keep this gap as small as possible to ensure that the leakage inductance is low, while still meeting insulation requirements.

9.2.4. Design Procedure

The transformer magnetizing inductance should be kept relatively low to achieve a compact transformer design. Even though this approach leads to a large dc current ripple, the converter control can maintain a high quality injection at the input and the output terminals through cycle-by-cycle charge regulation. However, a too low inductance

associated with a very large dc current ripple will cause large core loss, higher copper loss, and high device current stress. Equation (7.11) has shown the dc current ripple in relation to the switching frequency, magnetizing inductance, and line voltage amplitude. Equation (7.13) has given the boundary condition for maintaining CCM operation. Considering all these factors, the S4T transformer is designed to have a magnetizing inductance of 200 μH with a current carrying capability of 160 A (with some margin considered). Under full load conditions, the peak-to-peak current ripple is 50 A for a 15 kHz switching frequency. The turns ratio between primary and secondary sides is 1:1. Based on these specifications, the detailed design procedure is as follows.

Tentatively select the core by assuming that the design is driven by peak flux density, then the required core area product is given as equation (9.1).

$$AP = A_W A_E = \left(\frac{LI_{SCpk}}{B_{MAX}} * \frac{I_{FL}}{K_1} \right)^{4/3} \tag{9.1}$$

In this equation, L is the required magnetizing inductance, which is 200 μH when operated at the peak current. I_{SCpk} is the maximum short-circuit current, which is equal to the peak magnetizing current of 160 A based on the design specification. I_{FL} is the full-load current, which is calculated as the average primary/secondary side current and is equal to 52.5 A. B_{MAX} is the saturation limited flux density of the selected core material, which is set to be 1.0 T for nano-crystalline (with some margin considered). K_1 is the window utilizing factor, which is equal to 0.0085 for the transformer of an isolated flyback converter [115]. Equation (9.1) gives a required core area product of 1151 cm^2. Nano-crystalline core of SC2068M1 from the MK Magnetics™ can meet the design, which has a total area product of 1178 cm^4, a volume of 1184 cm^3, and a cross section area A_E of 28 cm^2.

The core loss should be evaluated to see whether it exceeds 100 mW/cm^3 – a typical maximum core loss limit for natural convection cooling. To obtain the core loss, the maximum flux swing should be calculated as shown in equation (9.2).

$$\Delta B_{MAX} = B_{MAX} \frac{\Delta I_{PP}}{I_{SCpk}} = 0.4T \tag{9.2}$$

In this equation, ΔI_{PP} is peak-to-peak current ripple. Referring to the nano-crystalline datasheet with this maximum flux swing, the corresponding loss data is seen to be 17 mW/cm^3, which is much smaller than the limit of 100 mW/cm^3. The total core loss is then calculated as equation (9.3), which shows that the core loss is almost negligible. This is because the flux swing of the transformer is kept small, as a large number of turns is needed to set the desired magnetizing inductance.

$$P_{core} = 17mW / cm^3 * 1184cm^3 = 20W \tag{9.3}$$

Then the number of turns to provide the desired inductance when operating around B_{MAX} is calculated using equation (9.4), resulting in 12 turns for this design.

$$N = \frac{L * \Delta I_{PP}}{\Delta B_{MAX} A_E} = 11.4 \tag{9.4}$$

The air gap length is then calculated using equation (9.5) to achieve the desired inductance with the above calculated turns. μ_0 is the permeability of free space in this equation.

$$l_g = \mu_0 N^2 \frac{A_E}{L} * 10^4 = 2.54mm \tag{9.5}$$

The windings are then designed as follows. Copper foil with a large conductor width is selected for the winding design to achieve low loss. The width of the copper foil is selected to be 7.62 cm, which is the size of an available copper foil roll on the market and can fit into the window of the selected core. The thickness of the copper foil should be selected such that it can carry high enough current with relative low loss. The RMS current $I_{m.RMS}$ that the primary/secondary winding should carry is calculated using equation (9.6), considering a square shape current waveform. In the equation, I_{MAX} and I_{MIN} are the maximum and minimum values of the magnetizing current. The dc component of the winding current $I_{m.DC}$

is calculated as equation (9.7), considering a 50% duty cycle for the input and output bridges, and the ac component $I_{m.AC}$ is calculated as shown in equation (9.8).

$$I_{m.RMS} = \sqrt{2}\left(I_{MAX} + I_{MIN}\right)/2 = 81A \tag{9.6}$$

$$I_{m.DC} = \left(I_{MAX} + I_{MIN}\right)/2 * 0.5 = 57.5A \tag{9.7}$$

$$I_{m.AC} = \sqrt{2}\left(I_{MAX} + I_{MIN}\right)/2 = 57.5A \tag{9.8}$$

For copper conductors, a current density of 450 A/cm^2 is usually selected for the conductor design under passive cooling conditions [131], which leads to a required copper thickness of 0.237 mm. A 22 mils (0.5588 mm) copper foil is selected to further reduce the dc resistance. Given the core dimension of the selected core, 12 turns results in the winding length of 303 cm. The winding dc resistance is then calculated using equation (9.9), in which ρ is the resistivity of copper, l is the winding length, and A is the conductor cross-section area. The resulted dc winding loss is calculated using equation (9.10).

$$R_{DC} = \rho\frac{l}{A} = 2.3 * 10^{-6} * \frac{303}{0.05588 * 7.6} = 1.64m\Omega \tag{9.9}$$

$$P_{DC} = I_{m.DC}^2 * R_{DC} = 57.5\hat{}2 * 0.00164 = 5W \tag{9.10}$$

The ac winding loss is then calculated as follows. The skin depth for copper is calculated as equation (9.11), in which f is the transformer frequency. For the selected conductor thickness of 0.5588 mm, the Q factor for calculating the ac loss is given by equation (9.12). By entering D_{PEN} and Q factor to Dowell's curve, along with 12 turns, the ac resistance is then calculated as shown in equation (9.13), and the resulted ac winding loss is calculated using equation (9.14). The total winding loss for both the primary and the secondary sides is then given by equation (9.15).

$$D_{PEN} = 7.6/\sqrt{f} = 0.062cm \tag{9.11}$$

$$Q = 0.05588 / D_{PEN} = 0.9 \tag{9.12}$$

$$R_{AC} = 9 * R_{DC} = 14.8m\Omega \tag{9.13}$$

$$P_{AC} = I_{m.AC}^{2} * R_{AC} = 57.5\hat{}2 * 0.0148 = 49W \tag{9.14}$$

$$P_{winding} = \left(P_{AC} + P_{DC}\right) * 2 = 108W \tag{9.15}$$

For the final transformer design, two air gaps are created between the two U cores. In this way, the length of each air gap is only half of the total gap length, which helps mitigate the stray flux issue. Two sets of parallel windings are made such that each set of windings carries half of the total current, which reduces the winding loss by half, as shown in equations (9.16) – (9.18). The resulting total transformer loss is then calculated per equation (9.19). The calculated overall efficiency for the 10 kVA transformer is 99.3%, as shown in equation (9.20).

$$P_{DC.parallel} = \left(\frac{I_{m.DC}}{2}\right)^{2} * R_{DC} * 2 = 2.5W \tag{9.16}$$

$$P_{AC.parallel} = \left(\frac{I_{m.AC}}{2}\right)^{2} * R_{AC} * 2 = 24.5W \tag{9.17}$$

$$P_{winding\,parallel} = \left(P_{AC.parallel} + P_{DC.parallel}\right) * 2 = 54W \tag{9.18}$$

$$P_{XFMR.loss} = P_{core} + P_{winding\,parallel} = 54 + 20 = 74W \tag{9.19}$$

$$\eta_{XFMR} = \left(1 - P_{XFMR.loss}/10000\right) * 100\% = 99.3\% \tag{9.20}$$

For the winding design, each set of windings is placed around each air gap such that flux is constrained within the air gap, with very little stray flux propagating to the external area. Primary and secondary windings are layered on top of each other to achieve low leakage inductance. Kapton™ tape is used to provide multi-kV insulation between layers, while its very small thickness keeps the leakage inductance low. The winding mechanism for the designed transformer is shown in Fig. 9.1. A photograph of the fabricated transformer for the S4T is shown in Fig. 9.2.

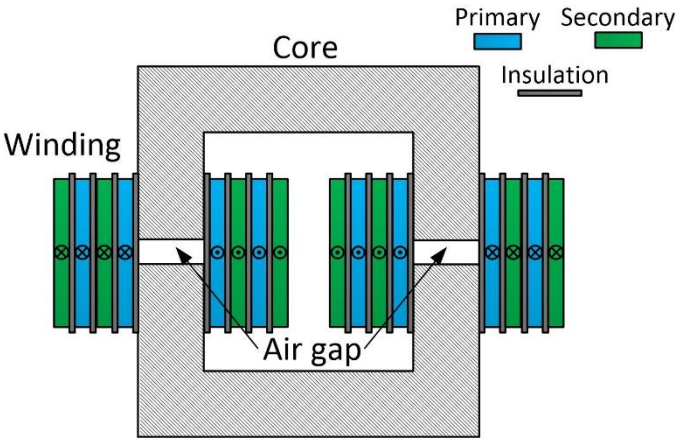


Fig. 9.1: Transformer winding mechanism.

Fig. 9.2: Photograph of the fabricated high-frequency transformer for the S4T.

9.3. Transformer Characterization

Parasitic elements of the transformer, including the leakage inductance, self-winding parasitic capacitance, and winding-to-winding parasitic capacitance, are important parameters of the high-frequency transformer. A characterization of the transformer should be performed to obtain these parasitic elements.

The equivalent circuit for the transformer considering various parasitic elements is shown in Fig. 9.3, in which C_p, C_s, C_{ps}, L_m, L_{lkp}, and L_{lks} represent the self-winding parasitic capacitance of the primary and the secondary sides, winding-to-winding parasitic capacitance, magnetizing inductance, and leakage inductance of the primary and secondary,

respectively. These parameters can be extracted by performing various open-circuit and short-circuit analysis using the impedance analyzer.

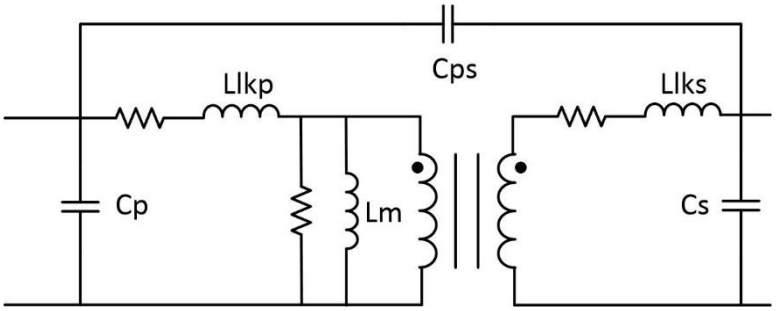


Fig. 9.3: Equivalent circuit of the transformer considering various parasitic elements.

By keeping the secondary side open, L_m and C_p can be obtained from the measured impedance curve of the primary side, as shown in Fig. 9.4. The measured impedance is expressed as equation (9.21), from which L_m and C_p are calculated as 175 μH and 136 pF.

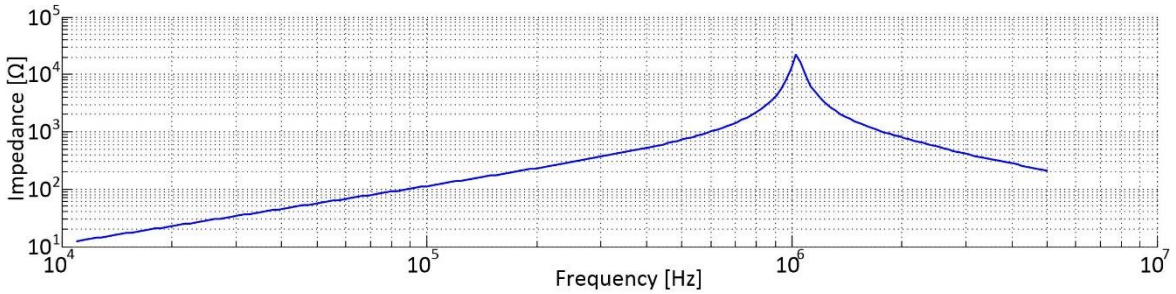


Fig. 9.4: Measured impedance curve of the primary side when keeping the secondary side open.

$$Z_{sec.open} = j\omega L_m \left\| \frac{1}{j\omega C_p} \right. \tag{9.21}$$

By keeping the secondary side short, the measured impedance curve for the primary side is shown as shown in Fig. 9.5. Excluding the external connector's parasitic inductance, the leakage inductance of the transformer is 740 nH.

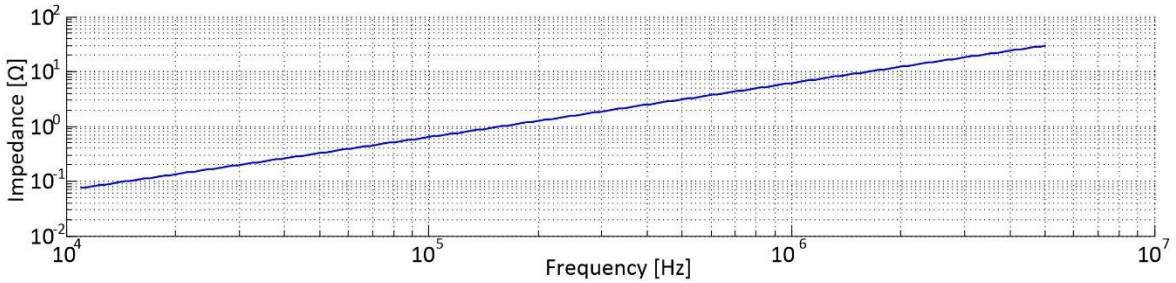


Fig. 9.5: Measured impedance curve of the primary side when keeping the secondary side short.

The winding-to-winding capacitance C_{ps} can be obtained by measuring the impedance between the primary side positive rail and the secondary side positive rail with both primary and secondary windings shorted. The measured impedance curve is shown as Fig. 9.6, which indicates C_{ps} to be 32 nF. The resonant point shown in the figure is caused by the parasitic inductance of the external connectors of the transformer.

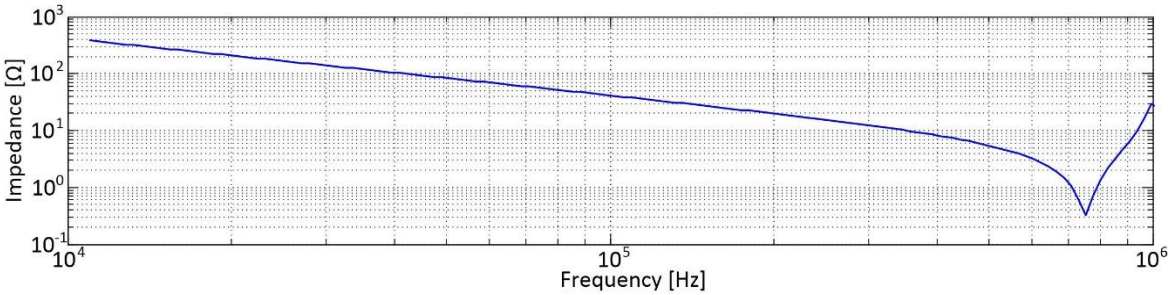


Fig. 9.6: Measured impedance curve between the primary side positive rail and the secondary side positive rail with both primary and secondary windings shorted.

The transformer energy storage capability is then evaluated by injecting a current into it. A pulsed voltage with a controllable duration is applied across one side of the transformer, while keeping the other side open. The current will increase linearly before the core is saturated. The experimental waveform for testing the transformer is shown in Fig. 9.7. With the knowledge of the *di/dt* of the transformer magnetizing current and the applied voltage, the magnetizing inductance versus current curve is plotted in Fig. 9.8. The curve shows that as the current increases, the inductance value slightly decreases due to the saturation. The curve indicates that at 160 A, the transformer still keeps a high inductance value, which proves the design efficacy.

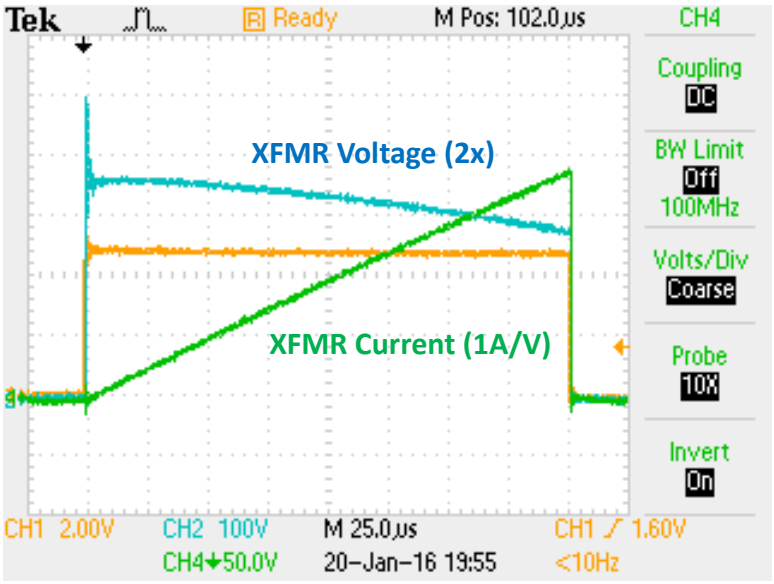


Fig. 9.7: Experimental waveforms of evaluating transformer's energy storage capability (Blue curve: voltage applied to the transformer with a scaling factor of two; Green curve: current through the transformer with a ratio of 1 volt/ampere).

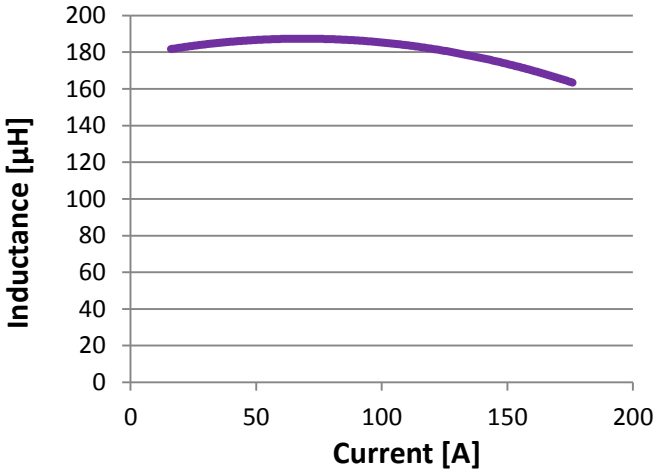


Fig. 9.8: Calculated magnetizing inductance versus current curve based on the result of Fig. 9.7.

9.4. Hybrid Transformer Design with Pre-Biased Flux

9.4.1. Theory Background

When designing the transformer, the peak flux density through the core should be kept below the saturation point of the B-H curve, as shown in equation (9.22), in which B_w is the flux density due to the winding excitation, and B_{sat} is the saturation flux density of the core. Therefore, the transformer size is determined by the maximum flux density of the magnetic

core when the design is driven by saturation flux density. The S4T has a unique feature of dc-biased flux in the transformer magnetizing inductance, which means that the working point is restricted within the first quadrant of the B-H curve while the region of the third-quadrant is not utilized, as shown in Fig. 9.9.

$$B_w \leq B_{sat} \tag{9.22}$$

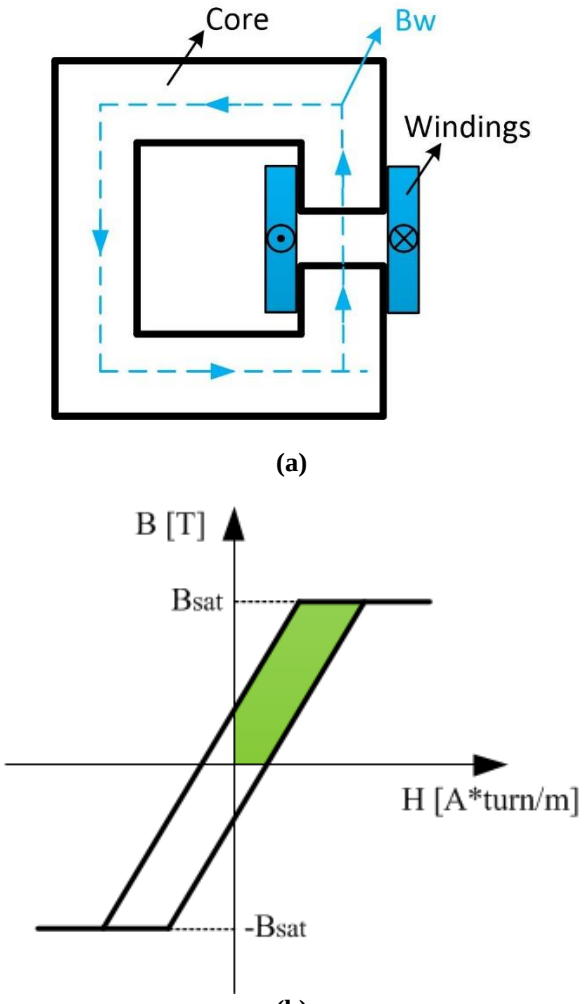


Fig. 9.9: Transformer design with magnetic core only: a) windings with dc current excites core to cause flux to flow in one direction only; and b) corresponding B-H curve shows that only the 1st quadrant is utilized.

Considering this dc-biased flux feature, permanent magnets can be integrated with the magnetic materials to provide a pre-biased flux for the core, leading to a hybrid design. The flux generated by the permanent magnets should be in a reverse direction to the flux excited by the windings. As shown in equation (9.23), the resultant equivalent flux density (B_{eq})

within the core will be the flux density of the excitation from the winding (B_w) minus the flux density caused by permanent magnets (B_{pm}). If the core flux density is kept below the saturation level, more energy can be stored in the transformer, as shown in equation (9.24). In this way, the usable B-H curve can be extended to the 3rd quadrant, which helps reduce the amount of magnetic materials needed. A simple design to achieve this is by putting the permanent magnet inside the airgap. The permanent magnet is placed in a direction such that it tries to cancel the flux generated by the windings. Fig. 9.10 (a) shows this design, and Fig. 9.10 (b) shows the resultant usable B-H curve range.

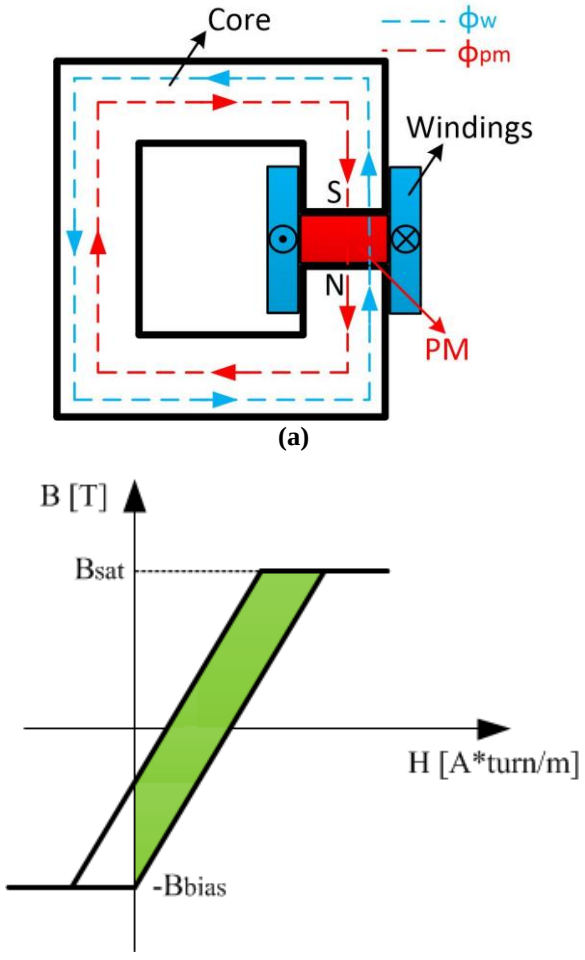


Fig. 9.10: Hybrid transformer design with permanent magnets inside the magnetic core's air gap: a) flux generated by windings and permanent magnets; and b) usable B-H curve extended to the 3st quadrant.

$$B_{eq} = B_w - B_{pm} \leq B_{sat} \tag{9.23}$$

$$B_w \leq B_{pm} + B_{sat} \tag{9.24}$$

The *B-H* characteristic of permanent magnet materials is shown in Fig. 9.11 [100], in which two curves are shown as the normal curve and the intrinsic curve. The normal curve depicts the flux of the permanent magnet generated by both the electromagnet and the permanent magnet, while the intrinsic curve depicts the flux generated by the permanent magnet only. Two important points are shown in the curve as the coercive force H_c and the intrinsic coercive force H_{ci}, which correspond to the zero crossing points of the normal curve and the intrinsic curve. For proper operation, the magnetic field strength excited by the windings and seen by the permanent magnet should be kept on the right hand side of H_c point, or at least the H_{ci} point. Violating this constraint will cause the demagnetization of the permanent magnets. For the hybrid transformer design, the consequence is that the permanent magnet flux will change its direction. In this case, rather than cancelling the flux excited by the winding, the permanent magnet flux will be added onto it and will further saturate the core. Coercive force H_c, intrinsic coercive force H_{ci}, residual flux density B_r, and maximum operating temperature T_{max} of various permanent magnets are given in Table 9.2 [101]. The material NdFeB is selected for the hybrid design since it has the largest H_c and H_{ci} values. Meanwhile, its residual flux density is close to the saturation flux density of the nano-crystalline material, indicating that it can fully bias the core.

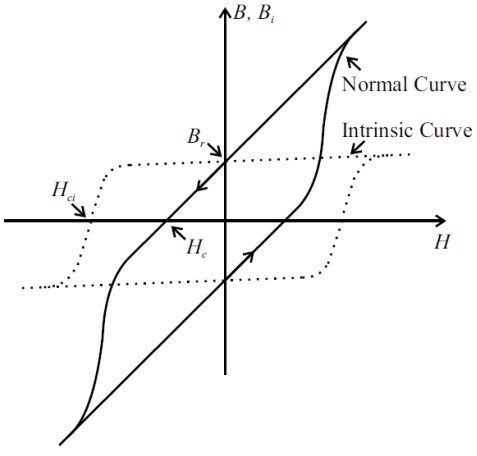


Fig. 9.11: *B-H* characteristic of permanent magnet materials [100].

Table 9.2: Characteristics of various permanent magnets.

Materials	H_c (kA/m)	H_{ci} (kA/m)	B_r (T)	T_{max} (°C)
NdFeB (39H)	979	1671	1.28	150
SmCo	732	796	1.05	300
Alnico	51	51	1.25	540
Ceramic	255	259	0.39	300
Flexible	109	110	0.16	100

A tentative design is performed by directly inserting the permanent magnet into the air gap, with the design procedure similar to the conventional transformer design depicted in section 9.2.4, but with an equivalent saturation flux density of $B_{sat} + B_r$ for nano-crystalline cores. The selected core based on this design is SC2063M1 from MK Magnetics™, which has an area product of 425.4 cm^4, a core volume of 469 cm^3, and a cross section area of 14.3 cm^2. The corresponding number of turns for the winding is 11 and the air gap length is 1.09 mm.

It needs to be analyzed whether the permanent magnet has a potential to be demagnetized when inserted into the air gap. The equivalent magnetic circuit for this hybrid transformer design is shown in Fig. 9.12, in which the permanent magnet acts as a constant flux source.

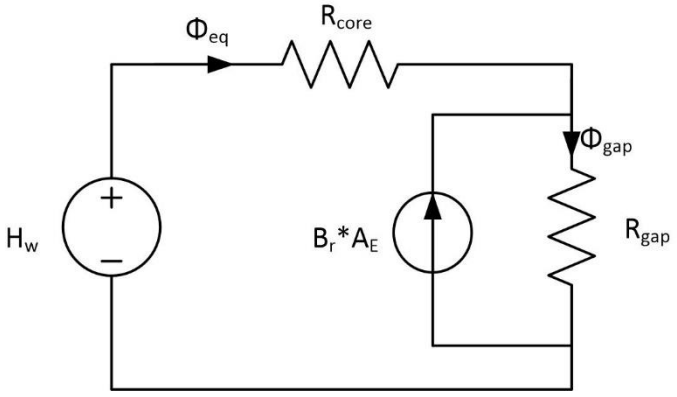


Fig. 9.12: Equivalent magnetic circuit for the hybrid transformer design when inserting the permanent magnet into the air gap.

The magnetic field strength generated by the winding is calculated as equation (9.25). The mean magnetic length l_{core} of SC2063M1 core is 32.8 cm, and the air gap length l_{gap} is 1.09 mm. The relative permeability for nano-crystalline material and NdFeb is 6000 and

1.0335 respectively. The reluctance of the core and the permanent magnet or the air gap is then calculated as equations (9.26) and (9.27). Based on the equivalent circuit, the magnetic equation can be written as equation (9.28). The flux and flux density of the core is then calculated as equations (9.29) and (9.30). The magnetic field strength seen by the permanent magnet H_{pm} is then calculated as equation (9.31), in which the flux density of the core is taking a negative value since the flux direction is reverse to the permanent magnet's flux. The absolute value of H_{pm} from (9.31) is shown to be larger than H_{ci} of NdFeb, which indicates that demagnetization will occur if the permanent magnet is directly inserted into the air gap. Therefore, an alternative design has to be explored for the hybrid transformer design.

$$H_w = N_w * I_w = 11 * 160 = 1760 A/m \tag{9.25}$$

$$\Re_{core} = {l_{core}}/{\mu_0 \mu_r A_E} = 30437 H^{-1} \tag{9.26}$$

$$\Re_{gap} = {l_{gap}}/{\mu_0 A_E} = 500000 H^{-1} \tag{9.27}$$

$$\begin{cases} H_w = \Phi_{eq} * \Re_{core} + \Phi_{gap} * \Re_{gap} \\ \Phi_{gap} = \Phi_{eq} + B_r A_E \end{cases} \tag{9.28}$$

$$\Phi_{eq} = \frac{H_w - B_r A_E \Re_{gap}}{\Re_{core} + \Re_{gap}} = 0.0012 Wb \tag{9.29}$$

$$B_{eq} = \frac{\Phi_{eq}}{A_E} = 0.842 T \tag{9.30}$$

$$H_{pm} = \frac{(-B_{eq}) - B_r}{\mu_0 \mu_{pm}} = \frac{(-0.842) - 1.28}{4\pi * 10^{-7} * 1.0335} = -1634 kA/m \tag{9.31}$$

9.4.2. Proposed Hybrid Transformer Design

Previous analysis shows that directly inserting the permanent magnet into the air gap will demagnetize the core. Therefore, to avoid the demagnetization issue, the permanent magnet should be placed out of the main flux path while providing dc flux bias to the core.

Some design methodologies have been proposed in [102]-[104], but most of them involve a complicated design of the core. The design proposed in this dissertation is shown in Fig. 9.13. Two pieces of permanent magnets are placed on the side of the core around the air gap. With the winding current direction shown in the figure, the direction of the flux generated by the winding Φ_w is counter-clockwise. The flux generated by the permanent magnet should have a reverse direction to cancel it. The permanent magnet on the top of the air gap should be placed such that its south pole is facing towards the magnetic core, while the one below the air gap should have its north pole facing towards the core. In this way, the two permanent magnets create a flux flowing path as shown in the figure, which tends to cancel the flux generated by the winding. The cross section area of the two permanent magnet should be the same as the core's such that enough biased flux is generated.

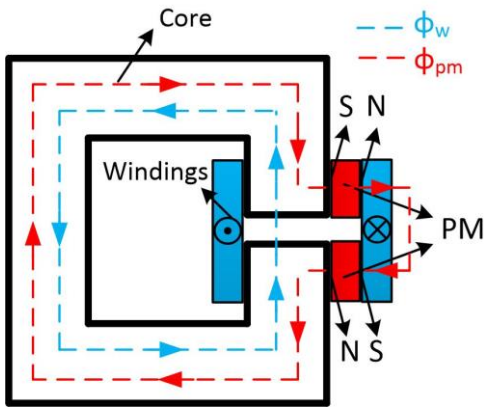
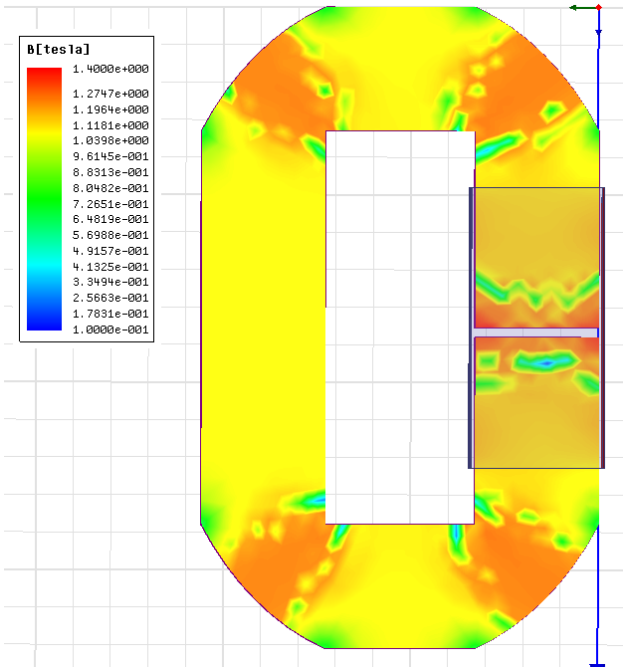


Fig. 9.13: Proposed hybrid transformer design.

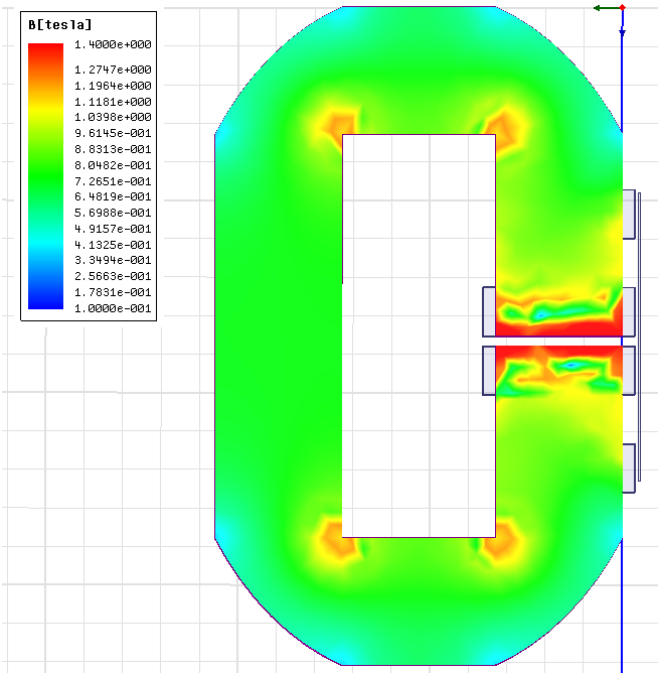
For the core designed using SC2068M1, the cross section area of the permanent magnet should be 28 cm^2. Such a permanent magnet has a magnetic force larger than 100 lbs, which is very difficult and dangerous to work with. For the final design, three pairs of IMNB1122 Neodymium bars are used, each of which has a dimension of 3" x 0.5" x 0.13". Two pairs are placed on the outside of the core, and one pair is placed inside the core window.

Finite element analysis simulation is performed for both the conventional design (magnetics only) and the hybrid design (magnetics with permanent magnets). The simulation results are shown in Fig. 9.14. For both cases, the number of turns for the windings are 12,

and the windings are excited by 160 A current. As shown in the results, with the same excitation, the hybrid design has a much lower flux density due to the permanent magnet's flux cancelling effect.



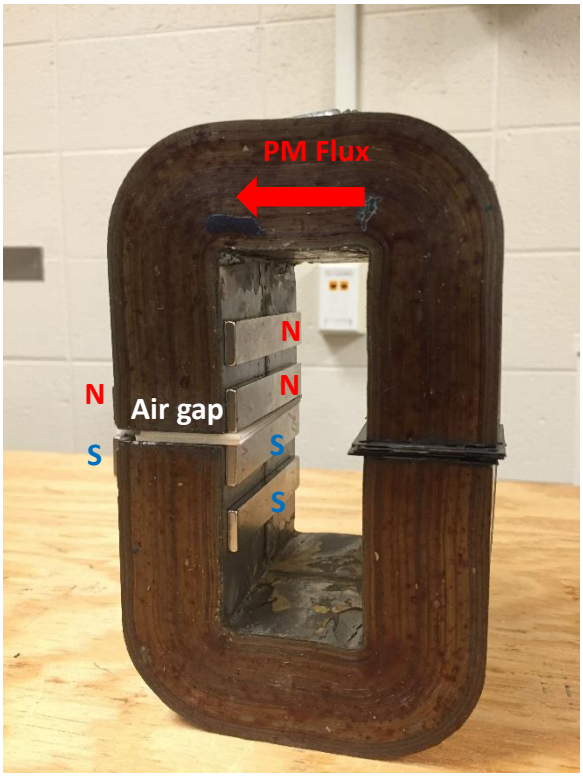
(a)



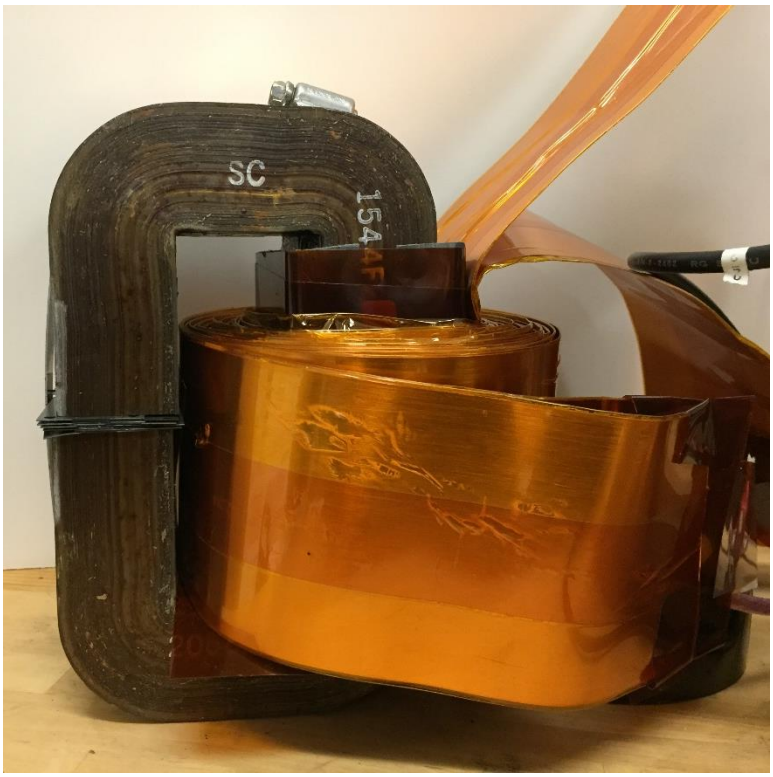
(b)

Fig. 9.14: Finite element analysis simulation for the two transformer designs: a) conventional transformer design with magnetics only; and b) hybrid transformer design with magnetics and permanent magnets.

The hybrid transformer is fabricated with the core SC2068M1. Fig. 9.15 (a) shows the placement of the three pairs of permanent magnets, and Fig. 9.15 (b) shows the final transformer with windings. The permanent magnets are placed in such a way that its flux tends to cancel the flux excited by the windings.



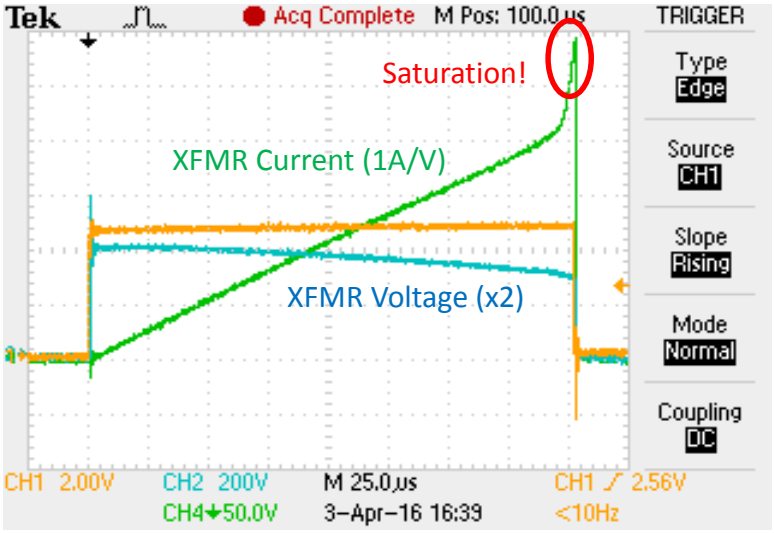
(a)



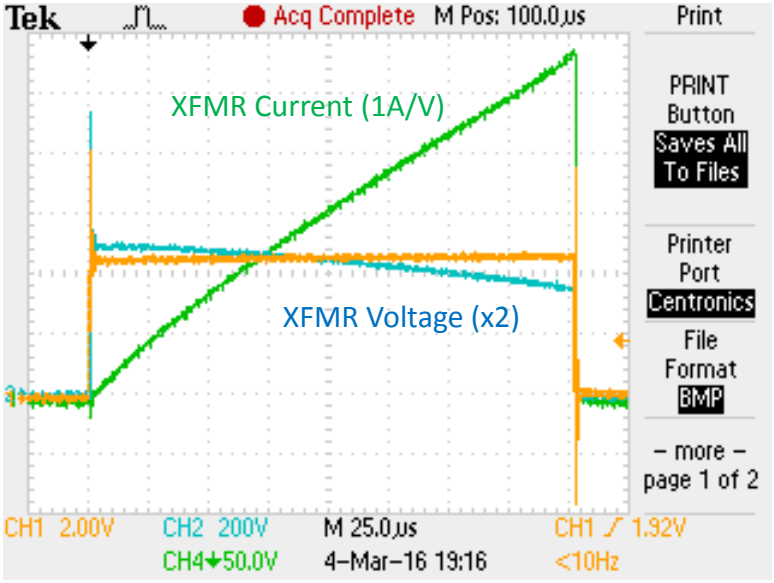
(b)

Fig. 9.15: Fabricated hybrid transformer: a) core and permanent magnets; and b) final fabricated hybrid transformer.

Then the two transformers, one with the magnetic core only and one with magnetic core and permanent magnets, are tested by injecting a current into them. The two transformers use the same core SC2068M1, and they both have 12 turns of windings. The current and voltage waveforms for the tests are shown in Fig. 9.16. For the conventional transformer, saturation is clearly indicated by the exponentially increasing current, which occurs after reaching a certain level. However, for the hybrid transformer, the current continuously increases without any saturation. Fig. 9.17 shows the calculated inductance versus current curves for these two transformers. As can be seen from these two curves, the conventional transformer magnetizing inductance quickly drops once the current exceeds 170 A, indicating saturation. However, for the hybrid transformer, the inductance is still maintained at a higher value even when the current reaches 270 A.

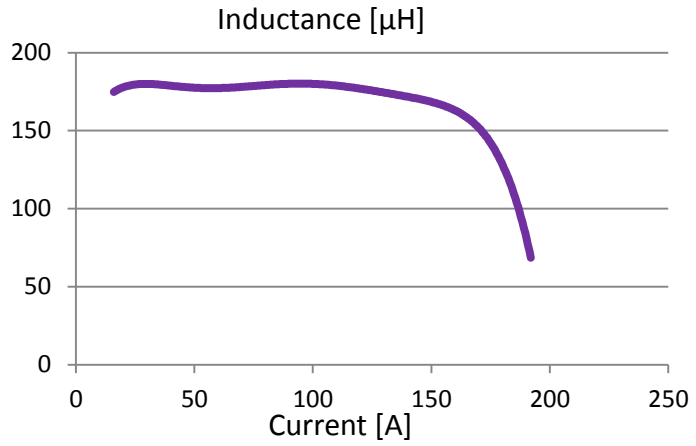


(a)

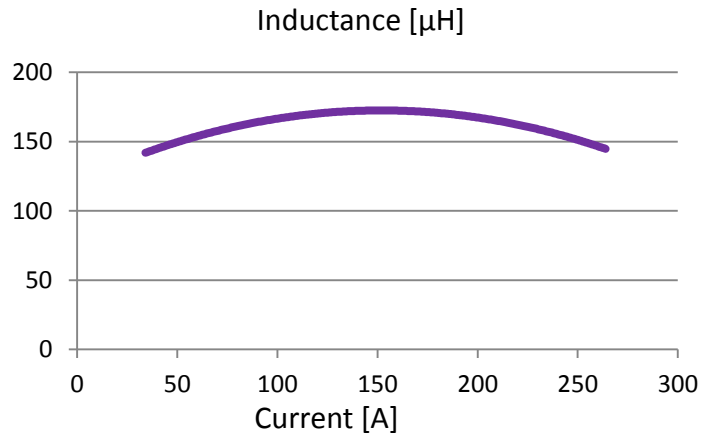


(b)

Fig. 9.16: Experimental current and voltage waveforms of testing the two transformers: a) conventional transformer with magnetic cores only; and b) hybrid transformer with magnetic cores and permanent magnets.



(a)



(b)

Fig. 9.17: Calculated magnetizing inductance versus current curves based on the results of Fig. 9.16: a) conventional transformer with magnetic cores only; and b) hybrid transformer with magnetic cores and permanent magnets.

Consider some inductance values from Fig. 9.17 for a comparison. The conventional design has a magnetizing inductance of 170 µH at 166 A and 160 µH at 176 A. While for the hybrid transformer design, it shows an inductance of 170 µH at 220 A and 160 µH at 240 A. Therefore, with the same size of the magnetic core, the hybrid transformer design can store 75 % more energy compared to the conventional design. In other words, to achieve the same energy storage, the hybrid transformer design can reduce core materials by 63%.

9.5. Conclusions

This chapter describes the detailed high-frequency transformer design. Two U-shape nano-crystalline cores are used for the transformer design with air gaps in between for dc energy storage to meet the design specifications as well as the objectives of achieving compact design, low core loss, and low winding loss. Windings made by wide copper foil offer low winding loss and also a design cost reduction compared to a litz-wire-based design. Primary and secondary windings are layered on top of each other with thin insulation in between to achieve a low leakage inductance. Two sets of windings are connected in parallel to achieve even lower copper loss. The detailed step-by-step design procedure is presented, which shows an estimated transformer efficiency of over 99%. Transformer characterization is performed to extract various parasitic elements including leakage inductance, self-winding capacitance, and winding-to-winding capacitance, and to evaluate the energy storage capability of the magnetizing inductance. Finally, a hybrid transformer design with pre-biased flux is explored. The hybrid design integrates the magnetic cores and permanent magnets, with the latter providing a dc flux bias for the former such that the usable B-H curve range of the magnetic cores can be extended. A hybrid-design based transformer is fabricated, and simulation as well as experimental tests are performed. Results show that, compared to the conventional design, the hybrid design can store 75% more energy with the same size core. Equivalently, to store the same amount of energy, the hybrid design can save core materials by 63%.

CHAPTER 10: SIMULATION AND EXPERIMENTAL VALIDATION

10.1. Introduction

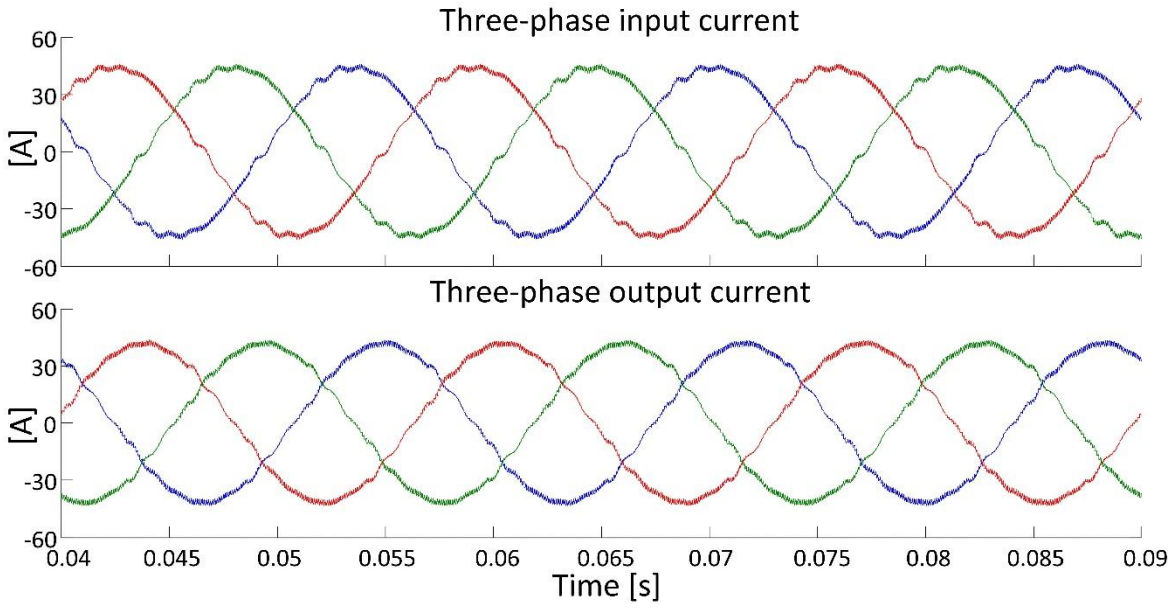
This chapter will first show preliminary simulation results of the S4T. To experimentally verify the proposed S4T, a three-phase 208 V / 10 kVA unit was designed, fabricated, and tested. This chapter presents the designed S4T unit, the system for testing the converter, and experimental results. In addition, as a unique application for the S4T, the converter can be operated as a low-voltage three-phase soft-switching dynamic VAr compensator, which is also demonstrated with the fabricated S4T prototype.

10.2. Simulation Results for the S4T

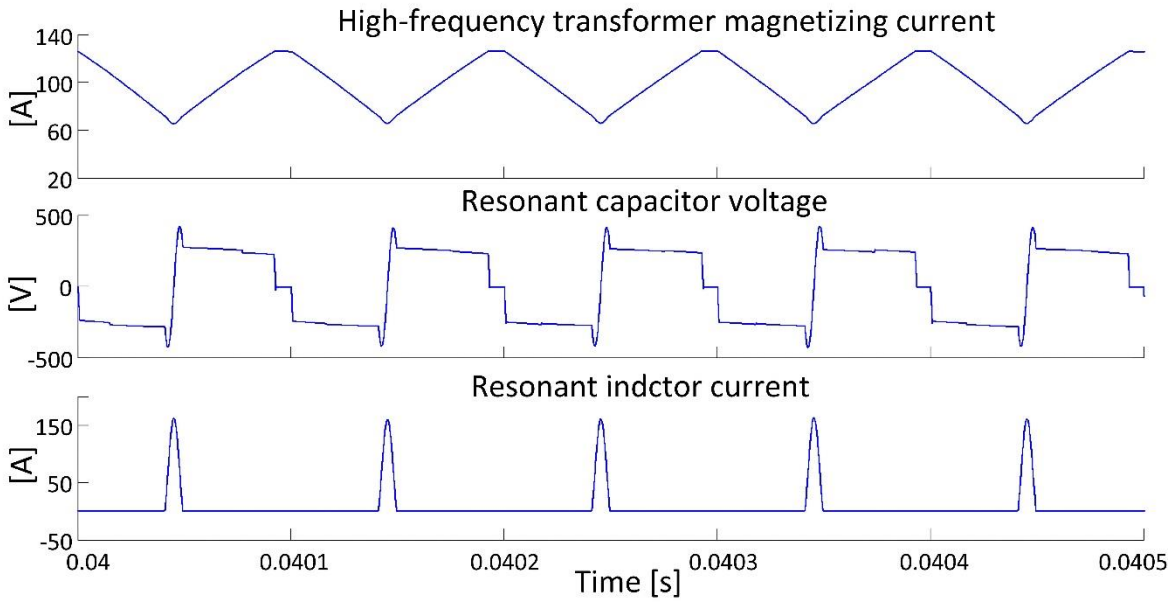
The operation of the proposed converter is validated through simulation. Parameters of the converter are shown in Table 10.1. Fig. 10.1 shows the simulation waveforms of input and output currents, high-frequency transformer magnetizing current, resonant capacitor voltage, and resonant inductor current.

Table 10.1: Simulation parameters of the S4T.

Power rating	Input/output voltage	Switching frequency	Magnetizing inductance
10 kVA	208 V	10 kHz	200 µH
Filter capacitor	Filter inductor	Resonant capacitor	Resonant inductor
60 µF	150 µH	0.4 µF	8 µH



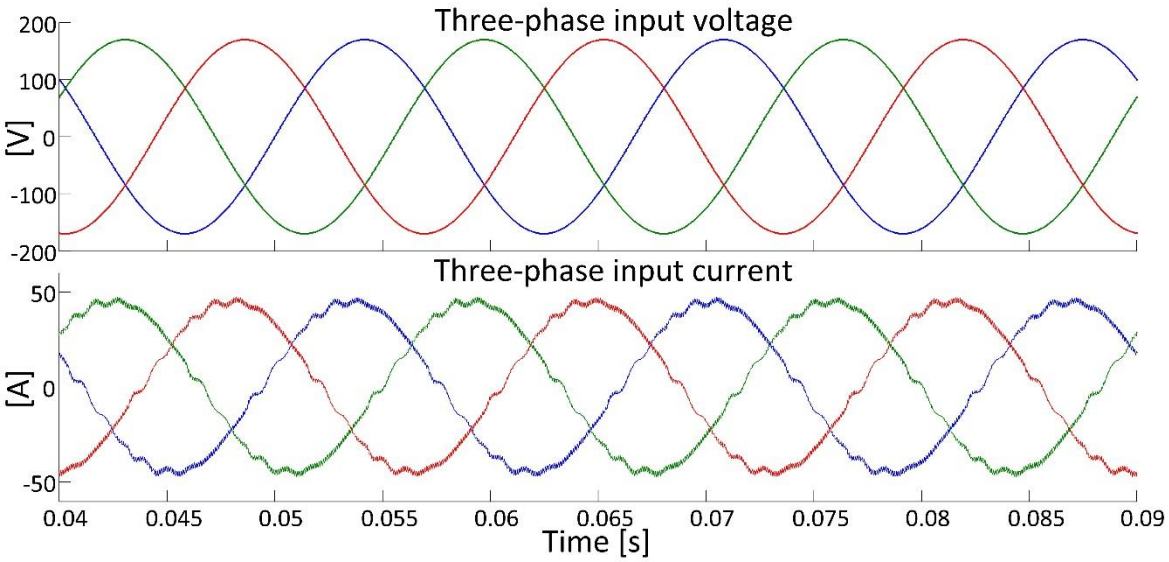
(a)



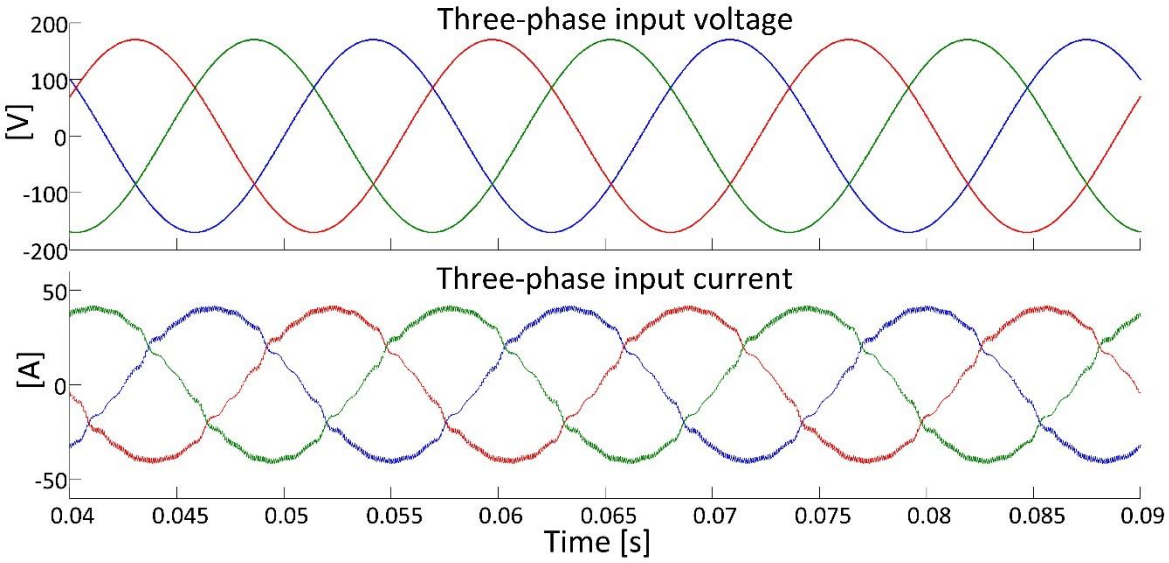
(b)

Fig. 10.1: Simulation waveforms for the S4T of: (a) three-phase input and output currents; and (b) high-frequency transformer magnetizing current, resonant capacitor voltage, and resonant inductor current.

Bidirectional power flow control is also simulated. Fig. 10.2 shows the simulation waveforms of the three-phase voltage and current on the input side when the power flows in forward direction and in reverse direction.



(a)



(b)

Fig. 10.2: Simulation waveforms of the three-phase voltage and current on the input side for the S4T when: (a) power flows in forward direction; and (b) power flows in reverse direction.

The S4T is then simulated with a 10 kW three-phase resistive load (three of 13 Ω resistors connected in delta) connected to the output side. Fig. 10.3 shows the simulation waveforms of the three-phase input current and the voltage across the resistive load. It can be seen that the load voltage is regulated at sinusoidal with very low harmonics.

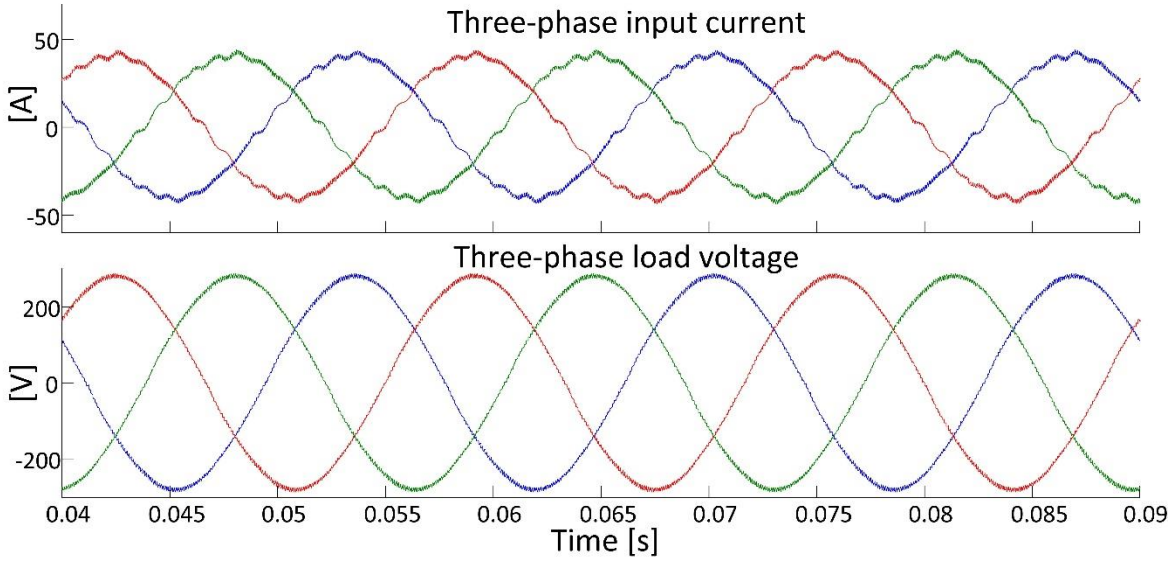


Fig. 10.3: Simulation waveforms of the three-phase input current and output voltage when a 10 kW resistive load is connected to the S4T output side.

Fig. 10.4 shows the simulation waveforms of the two winding currents within one switching cycle when considering a 2 μH transformer leakage inductance. The equivalent series resistance considering dc and ac copper loss is 16 mΩ, a value derived from the high-frequency transformer design that has been discussed in chapter 9. The waveform is recorded for the transition from state 2 to state 3 and then to state 4 of Fig. 6.12 (i.e., the magnetizing current transferred from the primary side bridge to the secondary side). It can be seen that during the transition, the two winding currents are slowly built up and driven down due to the resonance between the leakage inductance and the resonant capacitors, rather than having an abrupt change. Fig. 10.5 shows the simulation waveforms of the two resonant capacitors voltage when two diodes are connected in series with the transformer. The voltage waveforms of the two resonant capacitors are different from each other due to the leakage inductance effect.

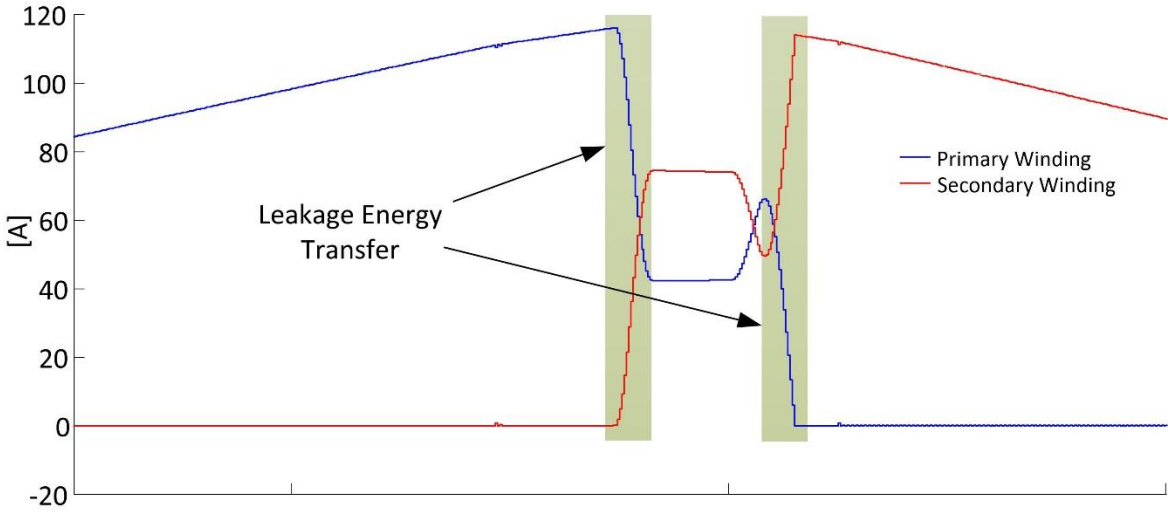


Fig. 10.4: Simulation waveforms of the two winding currents showing the leakage energy transfer.

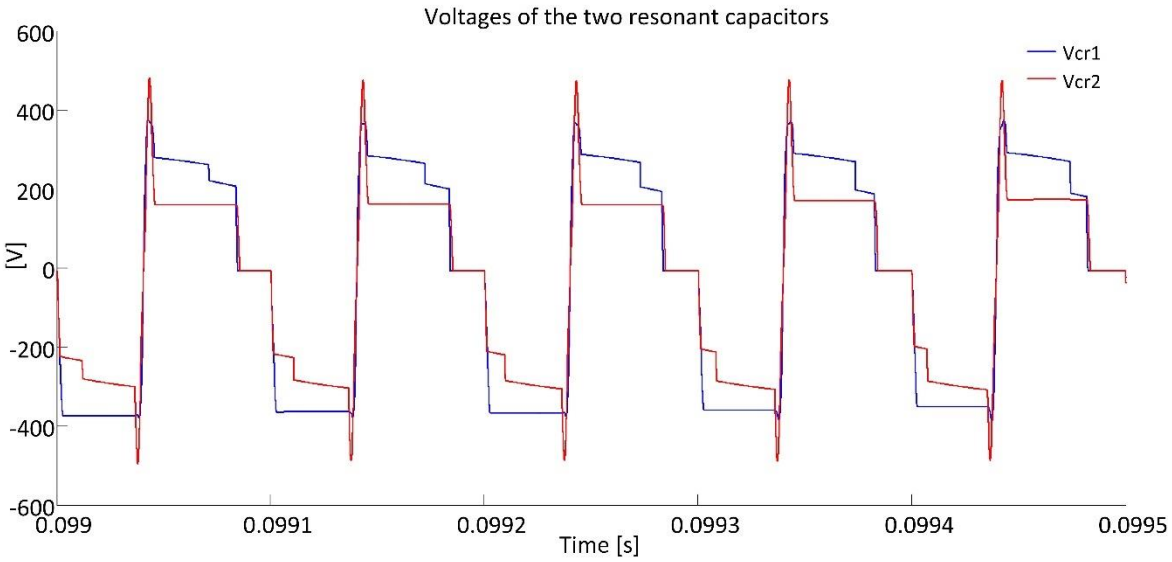


Fig. 10.5: Simulation voltage waveforms of the two resonant capacitors when considering transformer leakage inductance with diodes connected in series with the transformer.

10.3. Fabricated S4T Unit

A 208 V / 10 kVA S4T unit was fabricated in the lab for demonstration. This section describes the development of the S4T unit.

10.3.1. Power Stage of the Converter

The power stage of the S4T converter was designed on a multi-layer PCB board. Since the S4T has a symmetrical topology, only one PCB board design is required for the input/output converter bridge. Fig. 10.6 shows the circuit schematic that will be laid out onto

the PCB board. The board has connectors for the source/load, the high-frequency transformer, the gate drivers, the power supply, and the gate control signals. The board has footprints for TO-247 package such that the devices can be directly soldered onto the board. Other components such as capacitors, inductors, MOVs, snubbers, and sensors are also directly soldered onto the board. For each phase, the filter capacitors are composed of two large capacitors with a capacitance of 30 μF and two small capacitors with a capacitance of 2.2 μF, giving a total filtering capacitance of 64.4 μF for each phase. Large capacitors provide energy buffering for each switching cycle, while small capacitors provide a low-inductance path for the switching transient. The resonant capacitors consist of four small capacitors connected in parallel with a capacitance of 0.1 μF for each. Multiple capacitors connected in parallel provide a low equivalent parasitic inductance. TVS diodes are used to protect the device gate from over-voltage stress. Optional capacitors can also be soldered across the device gate terminal to reduce the device switching speed if necessary. Test points are provided for measuring and debugging purposes.

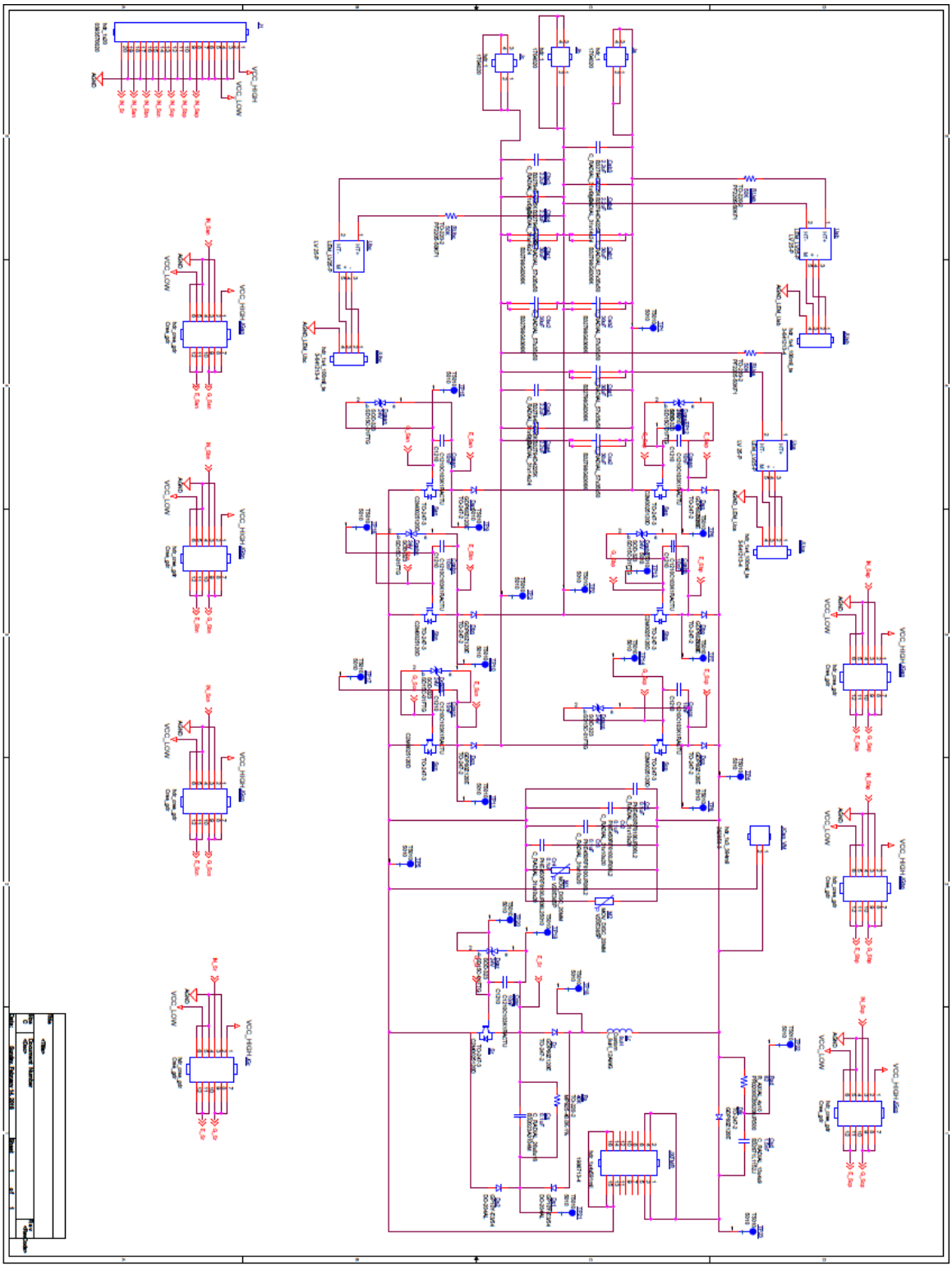
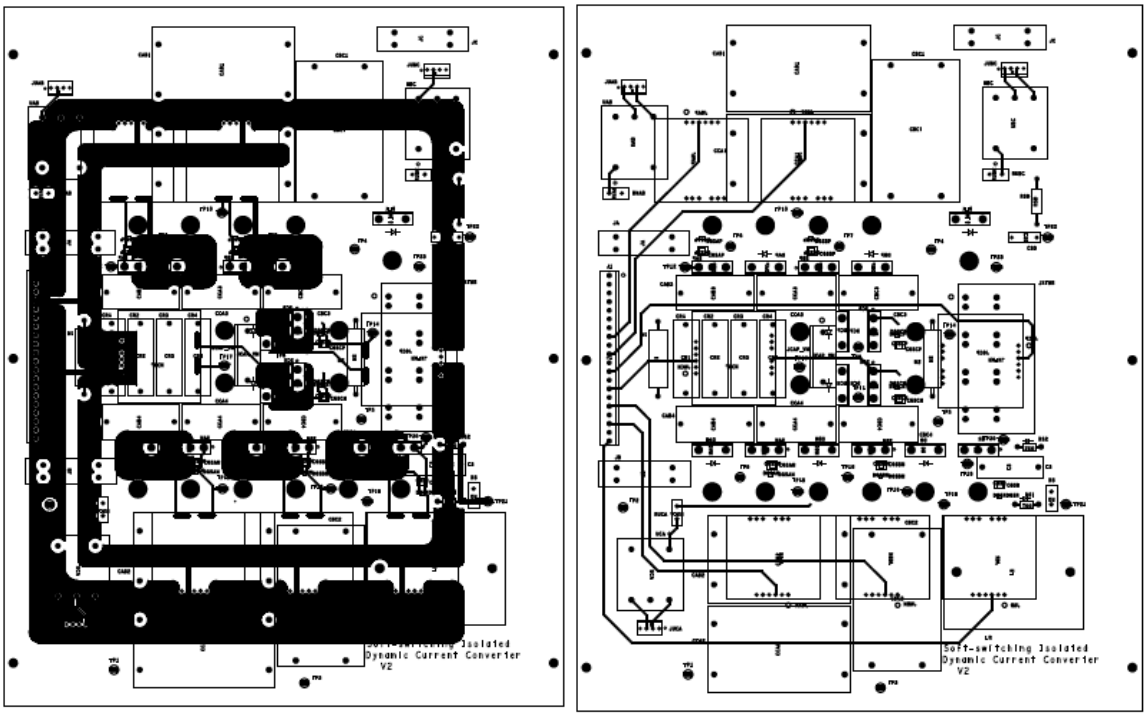


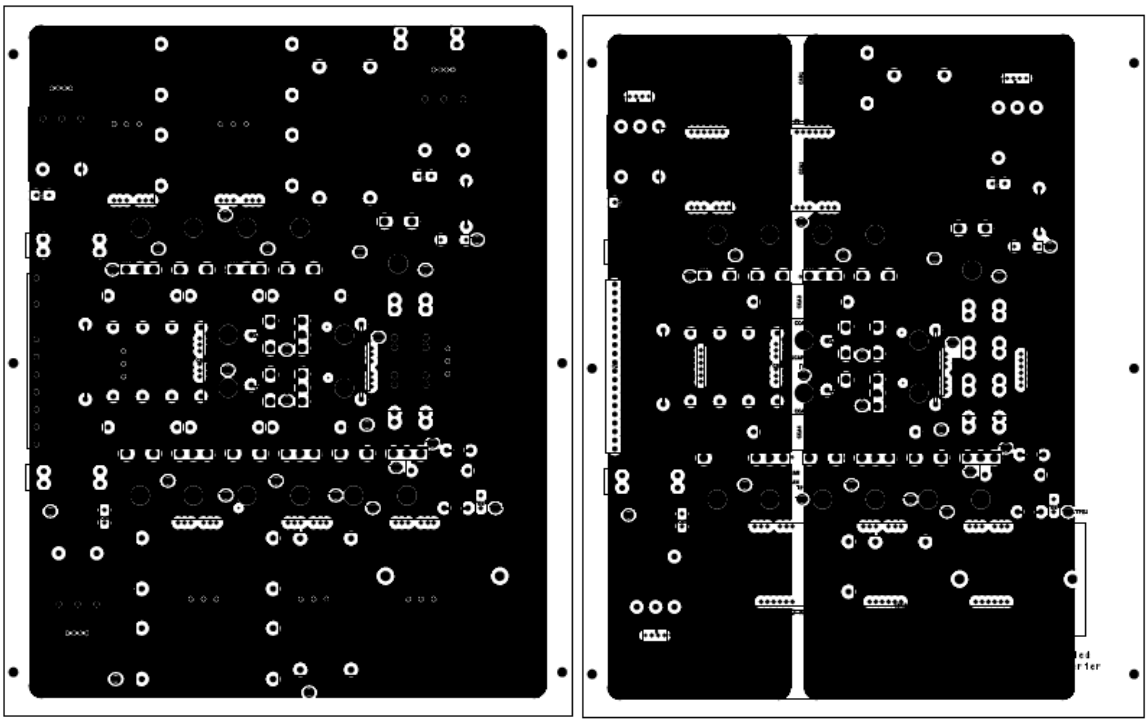
Fig. 10.6: Schematic of the board.

The PCB board is designed to have six layers: the top layer for the low-voltage supply, the second layer for gate control signals, the third layer for the ground plane, the fourth layer

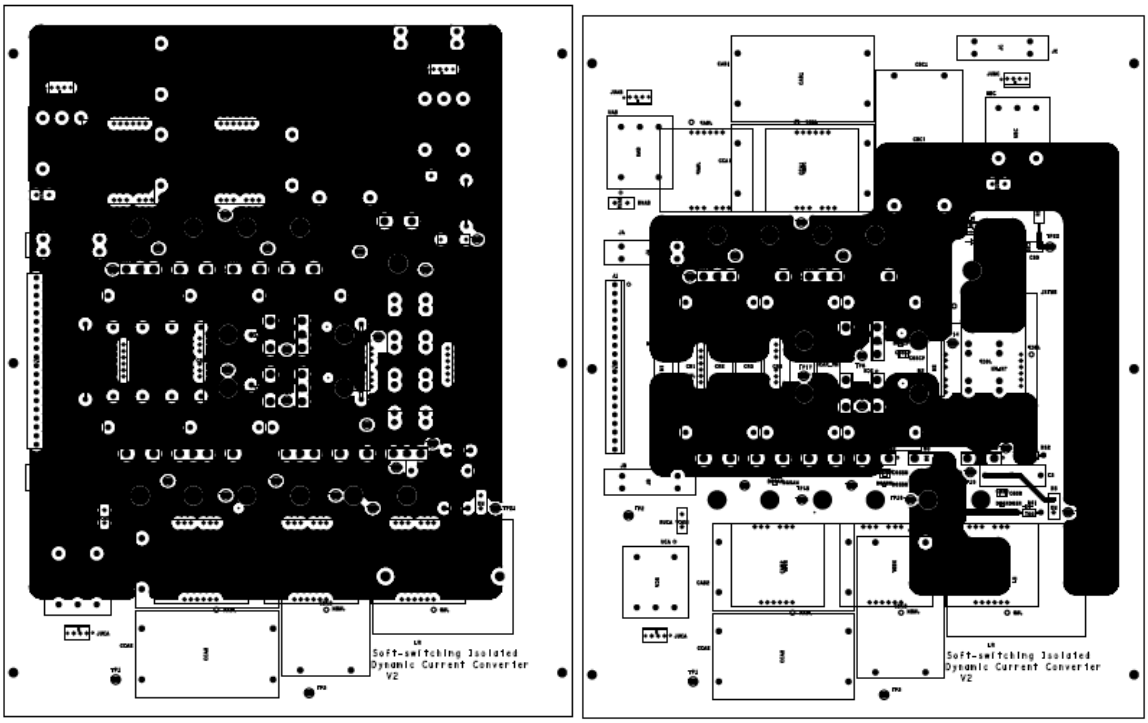
for phase *a* and phase *c* supplies, the fifth layer for phase *b* supply, and the sixth layer for the transformer positive and negative rails. The ground plane provides shielding for the gate control signals, isolating it from the EMI noise generated by the power planes. 6 oz copper is used for each layer to ensure that it can carry high enough current for the power planes. Eight mils of FR4, which has dielectric strength of 800-900V per mil, are used to provide enough insulation between layers. The final board has a total thickness of 93 mils. Fig. 10.7 shows the PCB layout for the S4T converter.



(a) **(b)**



(c) **(d)**



(e) **(f)**

Fig. 10.7: PCB layout for the S4T converter: a) 1st layer; b) 2nd layer; c) 3rd layer; d) 4th layer; e) 5th layer; and f) 6th layer.

10.3.2. Assembled Unit

Fig. 10.8 shows the conceptualized unit assembly for the S4T converter. The semiconductor devices should be attached closely to the heatsink to achieve effective heat dissipation. Since the case of the TO-247 devices are typically connected to its collector/drain terminal, an insulation layer is needed between the device and the heatsink. Aluminum oxide ceramic tile is used between the device and the heatsink to provide high-voltage insulation with high thermal conductivity. Devices are soldered onto the power-stage PCB boards while keeping the power connection leads as short as possible. Two separate power-stage and heatsink sets are fabricated for the S4T input and output bridge. The controller is mounted on top of the two power converters, with shielding to prevent it from the EMI noise.

Fig. 10.9 shows the final assembled S4T unit, for which the converters are mounted into an aluminum enclosure. The enclosure has three-phase power connections for the input and output on its one side, and has push-buttons and switches on the other side for various converter controls such as start-up, shut-down, and to increase/decrease the power level. The enclosure is connected to the ground potential for safety purposes.

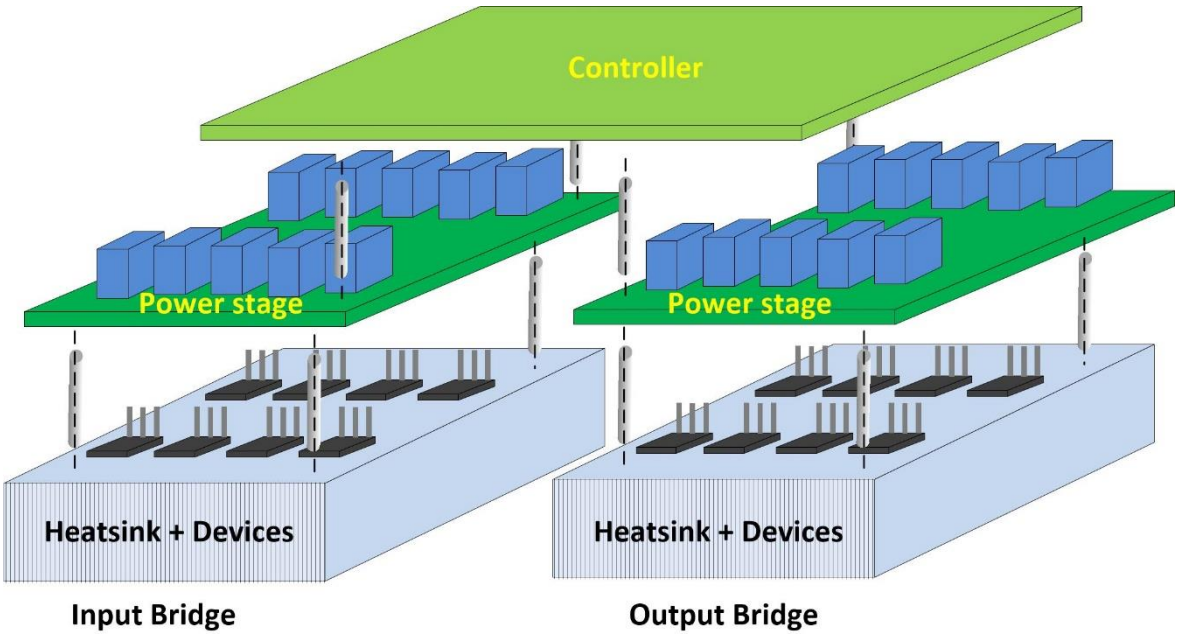
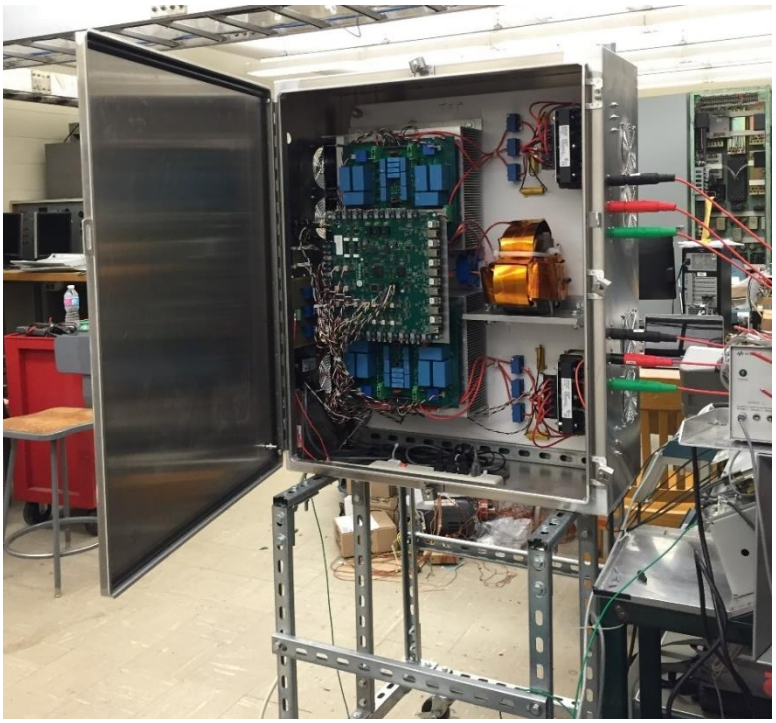
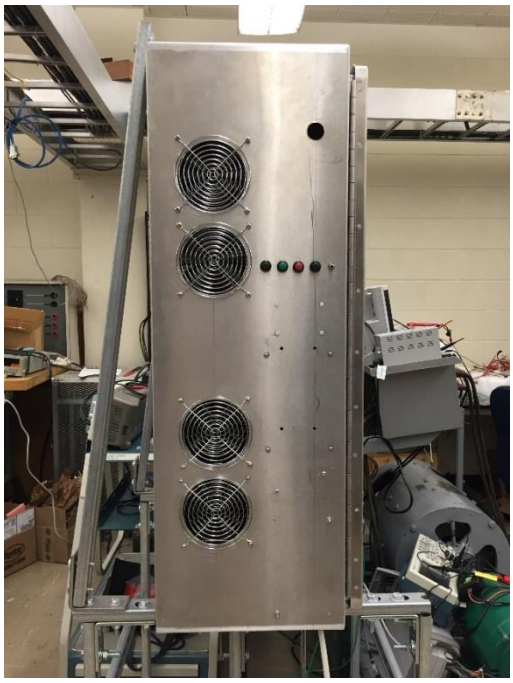


Fig. 10.8: Conceptualized unit assembling for the S4T converter.



(a)



(b) **(c)**

Fig. 10.9: Final assembled S4T unit: a) unit mounted into an aluminum enclosure; b) power connections for the three-phase input and output on one side; and c) push-buttons and switches on the other side for converter control.

10.4. System for Testing the Unit

The S4T unit is connected to a three-phase system to perform the test. Fig. 10.10 shows the schematic of the system wiring. A three-phase 230 V source is connected to a three-phase variable transformer through knife switches and circuit breakers. The variable transformer output voltage ranges from 0 to 480 V. Both the three-phase input and output terminals of the S4T are connected to the output of the variable transformer, with fuses installed on both sides. The S4T is running to circulate power from the input to the output, while the three-phase voltage source only provides active power to compensate for converter loss.

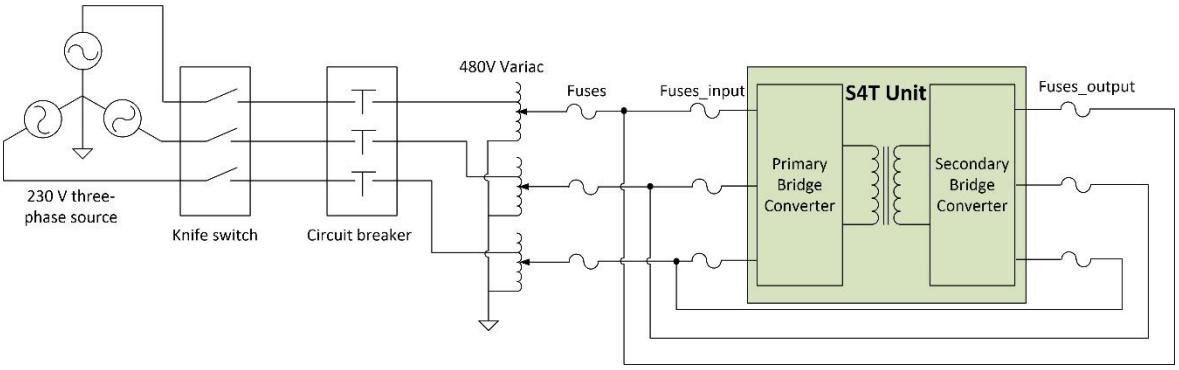


Fig. 10.10: System schematic for testing the S4T unit.

10.5. Experimental Results for the S4T

The S4T unit is first tested by connecting the input and output to the same supply to circulate power. Then the S4T unit is tested with three-phase resistive loads connected on its output side.

10.5.1. Power-Circulating Test

Both the input and the output are connected to the variable transformer to perform a power circulating test. The S4T unit is successfully tested at 208 V with a line current injection of 25.7 A, corresponding to a power level of 9.3 kVA. The transformer magnetizing current reaches a steady state level of 93 A, with a peak current of 117 A. Fig. 10.11 shows the experimental waveforms of the transformer magnetizing current, line current, and resonant capacitor voltage. Fig. 10.12 shows the waveform envelope of voltage across the

active devices and the voltage of the resonant capacitor. It can be seen that the device stress is limited within the envelope of the capacitor voltage. The resonant capacitor acts as a voltage clamp for all devices, which eliminates high-voltage spikes caused by parasitic elements. The zoomed-in cycle-to-cycle waveforms for magnetizing current, resonant capacitor voltage, and resonant inductor current are shown in Fig. 10.13, which closely matches the conceptualized waveforms and simulation waveforms. Fig. 10.14 shows the waveforms of one ZVS switching transient. It can be seen that before the device is turned on, the voltage across it already drops to zero, indicating zero turning-on loss. When the device is turned off, the voltage across it increases with a significantly reduced *dv/dt* rate, indicating a reduced turning-off loss.

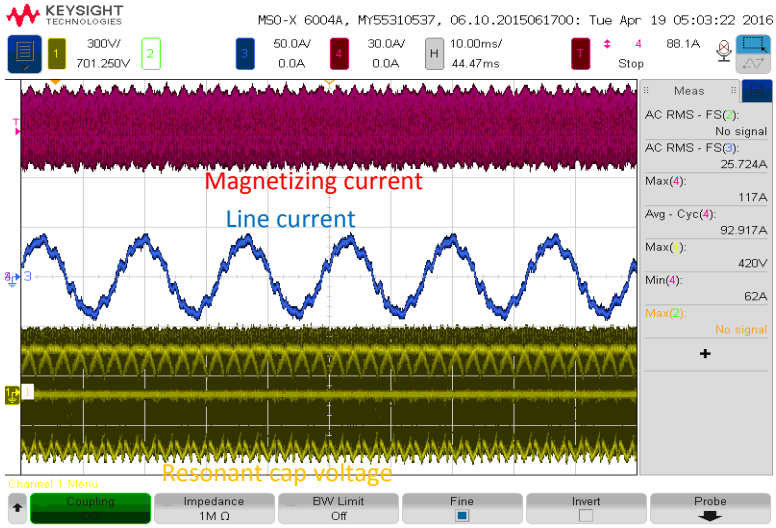


Fig. 10.11: Experimental waveforms of transformer magnetizing current (CH4, 30 A/div), line current (CH3, 50 A/div), and resonant capacitor voltage (CH1, 300V/div).

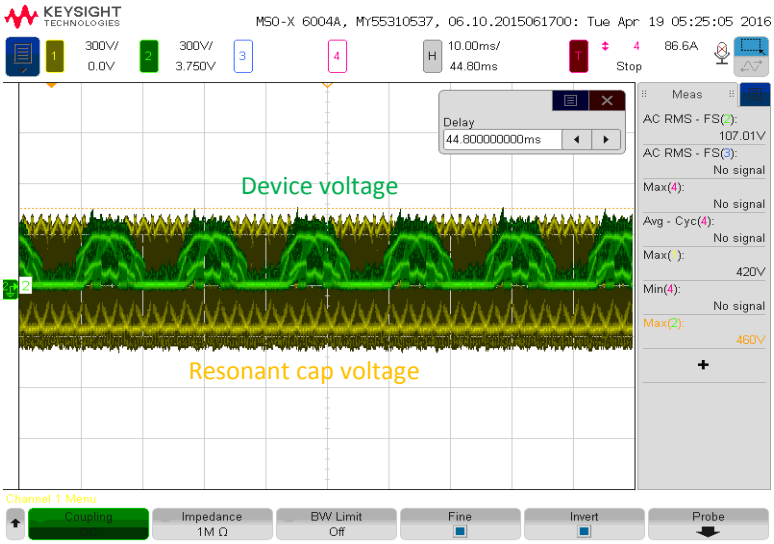


Fig. 10.12: Experimental waveforms of resonant capacitor voltage (CH1, 300 V/div) and device voltage (CH2, 300 V/div).

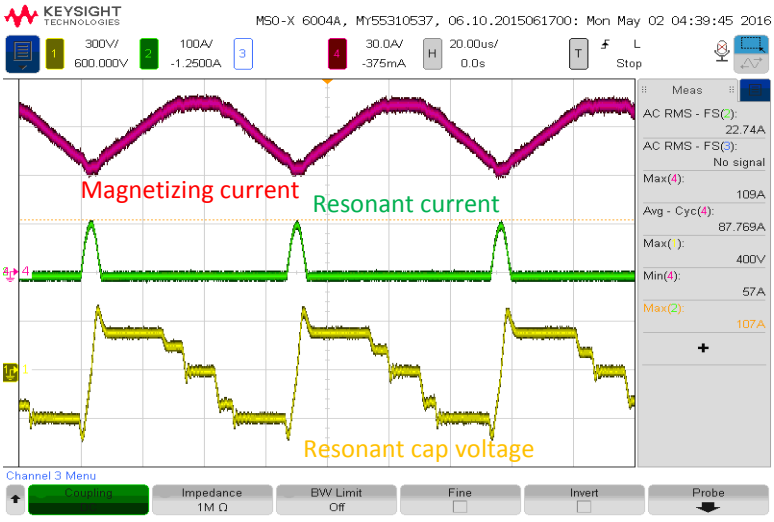


Fig. 10.13: Zoomed-in cycle-to-cycle waveforms for magnetizing current (CH4, 30 A/div), resonant capacitor voltage (CH1, 300 V/div), and resonant inductor current (CH2, 100 A/div).

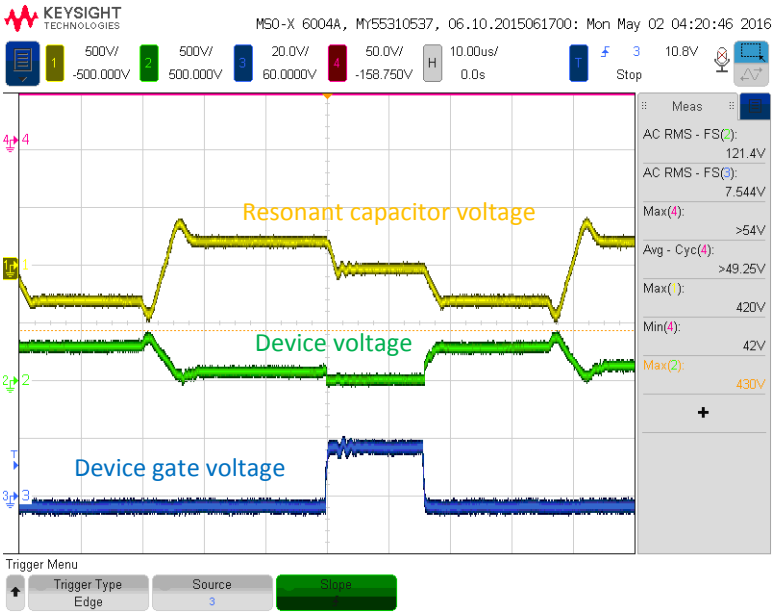
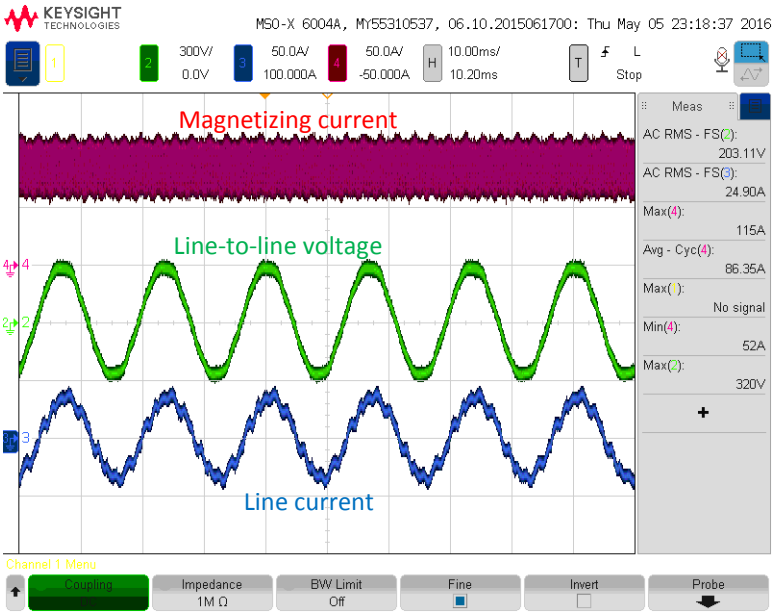
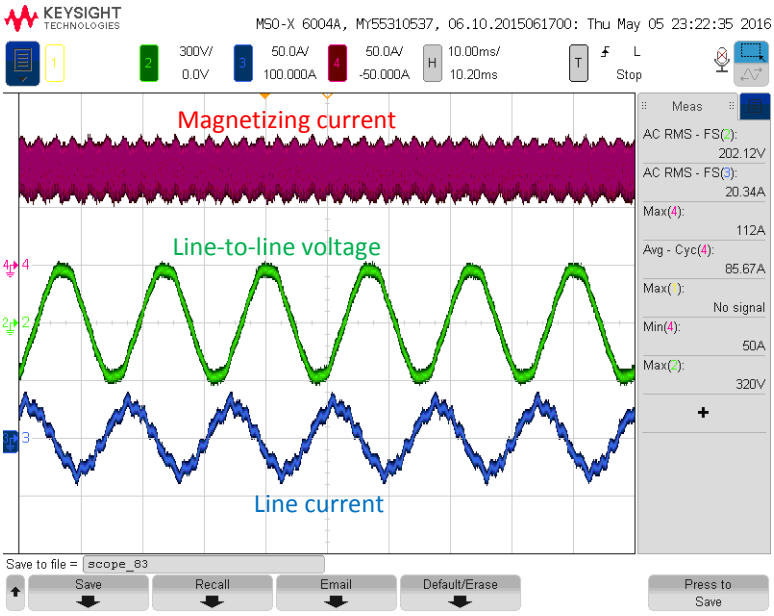


Fig. 10.14: One ZVS switching transient waveforms of resonant capacitor voltage (CH1, 500 V/div), device voltage (CH2, 500 V/div), and device gate voltage (CH3, 20 V/div).

The S4T is tested with power flow in both forward and reverse directions. Fig. 10.15 (a) shows the waveforms of the forward power flow, and Fig. 10.15 (b) shows the waveforms of the reverse power flow.



(a)



(b)

Fig. 10.15: Experimental waveforms of transformer magnetizing current (CH4, 50 A/div), line-to-line voltage (CH2, 300 V/div), and line current (CH3, 50 A/div) for two power flow directions: a) forward power flow; and b) reverse power flow).

10.5.2. Test with Resistive Loads

The S4T unit is then tested with a three-phase resistive load connected to the three-phase output on the secondary side. Three resistors are connected in delta and each one has a resistance of 22.6 Ω. Fig. 10.16 shows the experimental waveforms of the transformer magnetizing current and the current through the resistive loads. As shown in the figure, purely sinusoidal currents are injected to the load, in spite of the high-frequency ripples on the transformer magnetizing current.

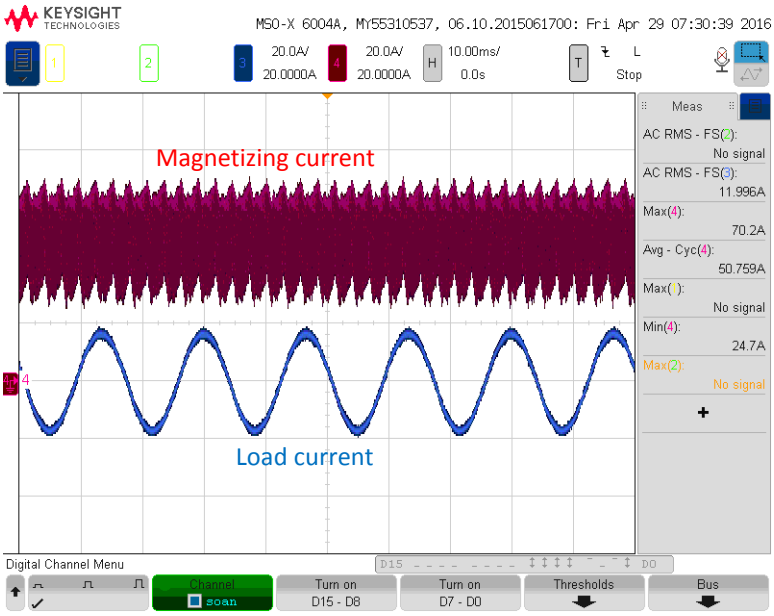


Fig. 10.16: Experimental waveforms of resistive loads test: transformer magnetizing current (CH4, 20 A/div) and current through the resistive load (CH3, 20 A/div).

10.6. Loss Measurement and Comparison

Converter loss was measured using Yokogawa. Fig. 10.17 shows the loss measurement results with different dc currents and line voltages. It can be seen that the converter loss increases with current as expected, but is almost purely independent of voltage levels. This clearly shows that ZVS condition is met for all devices and proves the soft-switching feature of the S4T. Based on this, it is predicted that the converter can achieve significantly higher efficiency at higher voltage and higher power levels.

Table 10.2 summarizes the comparison of various topologies to implement a three-phase 480 V/50 kVA solid state transformer with the switching frequency of 15 kHz. The comparison is for the S4T, the conventional DAB based multi-stage SST, and the low-frequency transformer with a rectifier and an inverter. Compared to the other two solutions, even though the device current rating for the S4T is 2 p.u., it does not have severe fault inrush current thanks to its inherent current limiting capability. The S4T really stands out with the features of lower device count, full-range of soft-switching, and higher efficiency. The S4T rated at 480 V / 50 kVA is expected to have much higher efficiency than the 208

V / 10 kVA unit, primarily because the unit is rated at a higher voltage and the device modules to be used have a much lower conduction voltage drop. Fig. 10.17 shows that the unit loss is independent of voltage levels, which also in turn indicates higher efficiency for a higher-voltage-rated unit.

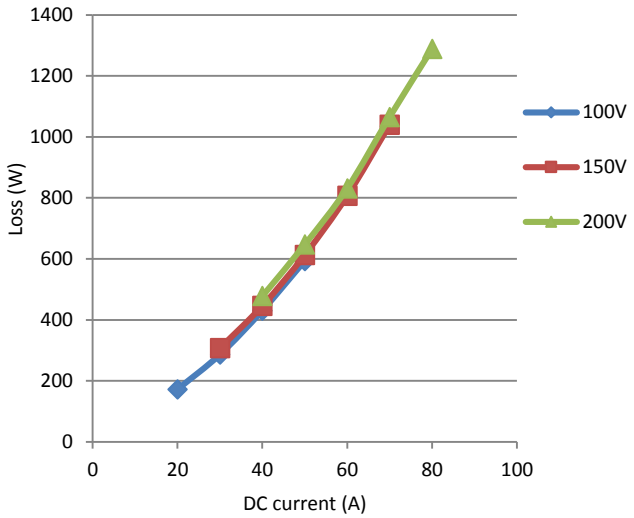


Fig. 10.17: Measured converter loss with different dc currents and line voltages.

Table 10.2: Comparison of S4T, conventional DAB based multi-stage SST, and low-frequency transformer with a rectifier and an inverter when implementing a three-phase 480 V/50 kVA solid state transformer with a switching frequency of 15 kHz.

Topology	Active Device Count	Soft-Switching	DC Caps	XFMR Frequency	Device V/I Rating	Fault Current	Projected Efficiency
Soft-switching solid state transformer (S4T)	12 (main) +2 (auxiliary)	Full range	–	15 kHz	1 p.u. / 2 p.u.	2 p.u.	97.4%
DAB based multi-stage SST	20	DC/DC only with a limited range	2	15 kHz	1 p.u. / 1 p.u.	> 10 p.u.	93%
Low-frequency transformer with rectifier and inverter	12	No	1	60 Hz	1 p.u. / 1 p.u.	> 10 p.u.	91.5%

10.7. A Unique Application as a Dynamic VAr Compensator

One extended application for the S4T is the dynamic VAr compensator. By only operating one side converter bridge while leaving the other side idle, the fabricated S4T runs as a low-voltage soft-switching dynamic VAr compensator, whose topology is shown in Fig. 10.18. The high-frequency transformer of the S4T acts as an inductor in this case.

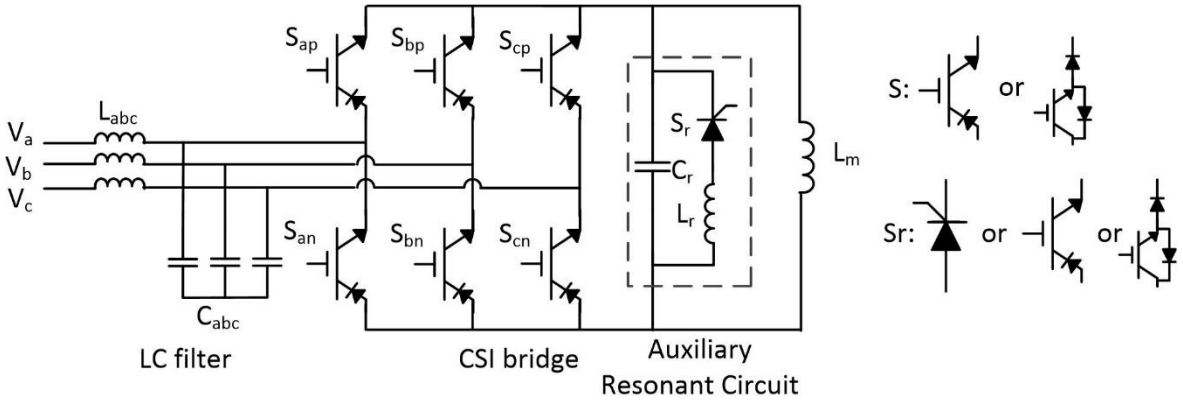


Fig. 10.18: Topology of the low-voltage soft-switching dynamic VAr compensator.

The operating principle of this low-voltage soft-switching dynamic VAr compensator is very similar to the S4T. The current through the inductor L_m is regulated at a constant dc value, and the main devices are switched under charge control to deliver reactive currents that are leading the voltages by 90^o to the three phase. The auxiliary resonant circuit provides ZVS conditions for all the main devices, in a manner that is the same as for the S4T.

Simulation is performed for the low-voltage soft-switching dynamic VAr compensator rated at 208 V / 10 kVAr. The main inductor has an inductance of 200 μH, and the switching frequency is 15 kHz. Fig. 10.19 shows the simulation waveforms of the three-phase voltage, converter injected current, and the inductor current. It can be seen that the converter injects a current which is leading the voltage by 90^o, and the inductor current is maintained at a dc level with high-frequency switching ripple on top of it. Fig. 10.20 shows the cycle-by-cycle waveforms of the inductor current, resonant inductor current, and resonant capacitor voltage.

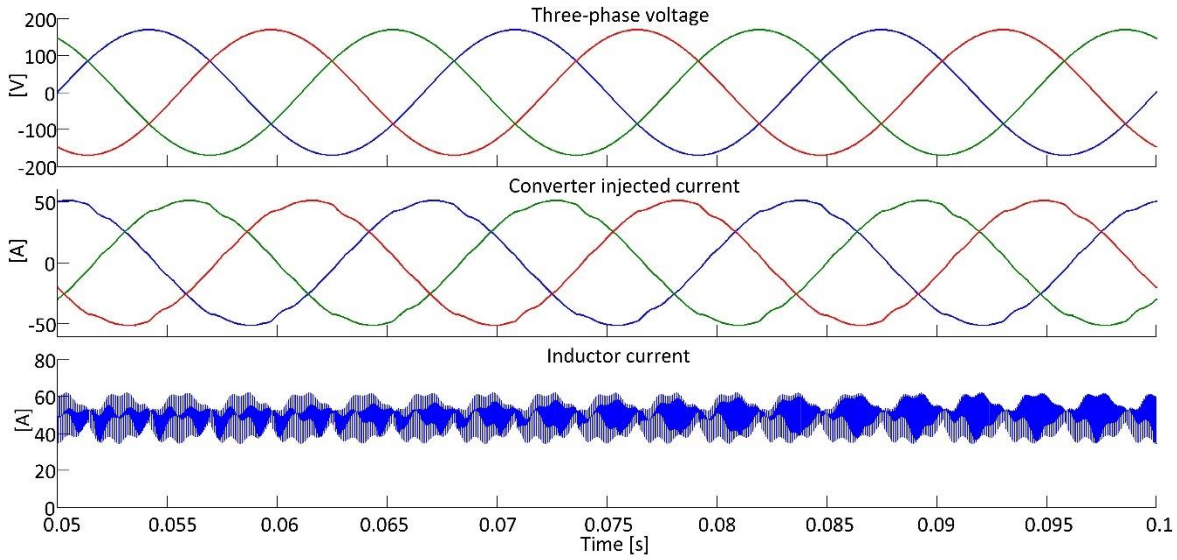


Fig. 10.19: Simulation results of the three-phase voltage, converter injected current, and inductor current for the low-voltage soft-switching dynamic VAr compensator.

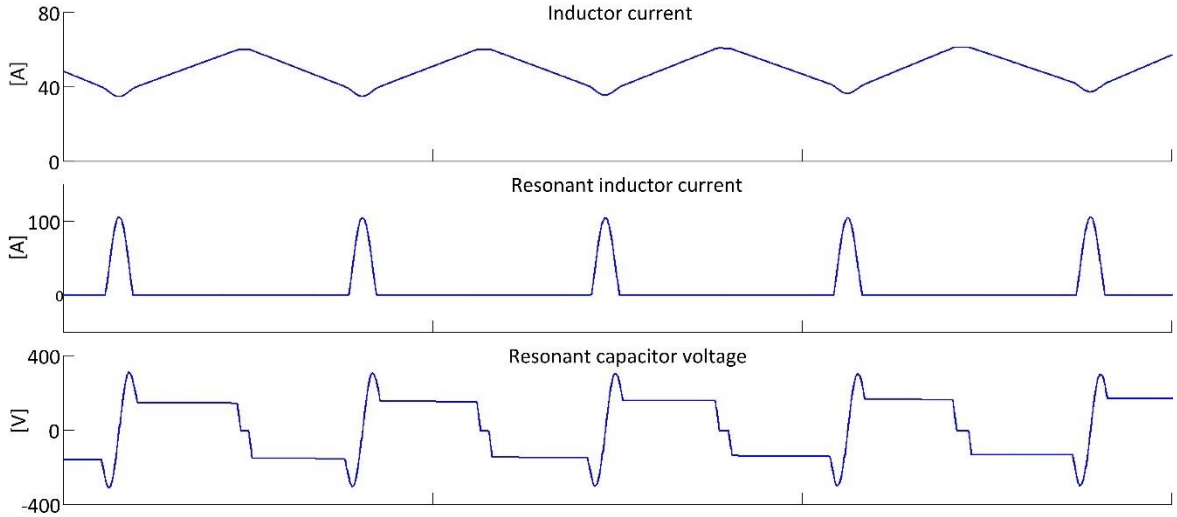


Fig. 10.20: Cycle-by-cycle waveforms of the inductor current, resonant inductor current, and resonant capacitor voltage for the low-voltage soft-switching dynamic VAr compensator.

Experimental results for the low-voltage soft-switching dynamic VAr compensator are shown below. Fig. 10.21 shows the experimental waveforms of the inductor current, the injected current to phase *a*, and line-to-line voltage V_{ab}. The line-to-line voltage is 208 V and the inject current is 32 A (RMS) in the waveforms, corresponding to a reactive power level of 11.5 kVAr. The dc current is regulated at around 65 A, with high-frequency switching ripples on top of it. Fig. 10.22 shows the waveform envelope of voltage across the active devices and the voltage of the resonant capacitor. The device stress is also limited within the

envelope of the resonant capacitor voltage, similar to that of the previous test. The zoomed-in cycle-by-cycle waveforms for the main inductor current, resonant capacitor voltage, and resonant inductor current are shown in Fig. 10.23, which closely match the simulation waveforms. Fig. 10.24 shows waveforms of one switching transient. It can be seen that when the device is turned off, the voltage across the device increases with a significantly reduced *dv/dt* rate. Before turning on, the voltage across the device already drops to zero. The waveform clearly shows ZVS transitions for the device.

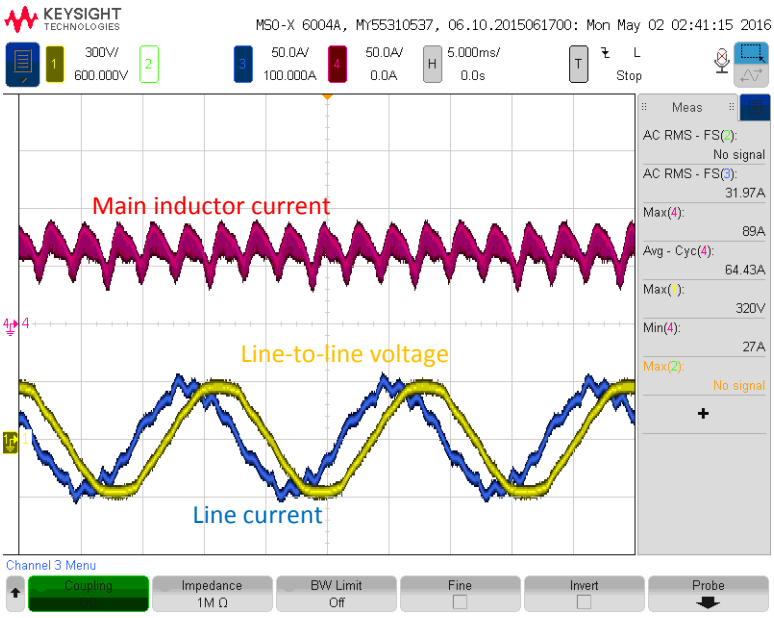


Fig. 10.21: Experimental waveforms of the inductor current (CH4, 50 A/div), the injected current to phase *a* (CH3, 50 A/div), and line-to-line voltage V_{ab} (CH1, 300 V/div) for the low-voltage soft-switching dynamic VAr compensator.

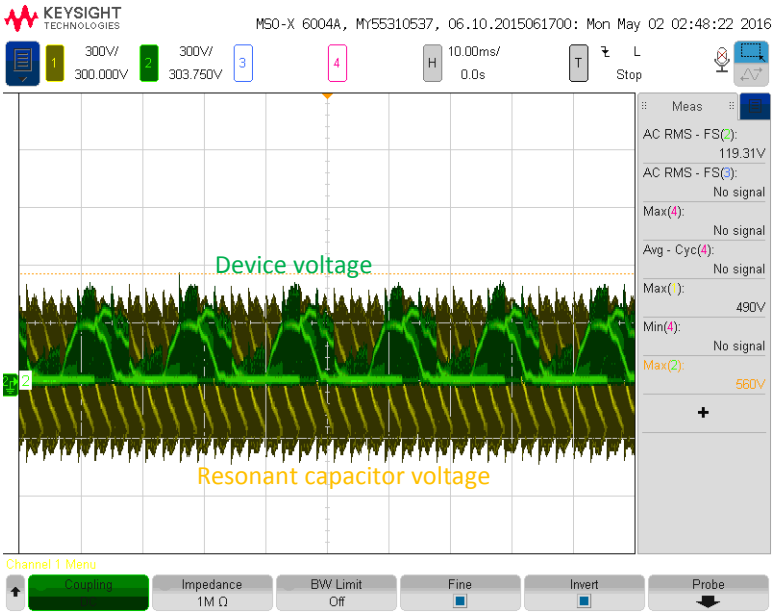


Fig. 10.22: Experimental waveforms of the voltage across a device (CH2, 300 V/div) and resonant capacitor voltage (CH1, 300 V/div) for the low-voltage soft-switching dynamic VAr compensator.

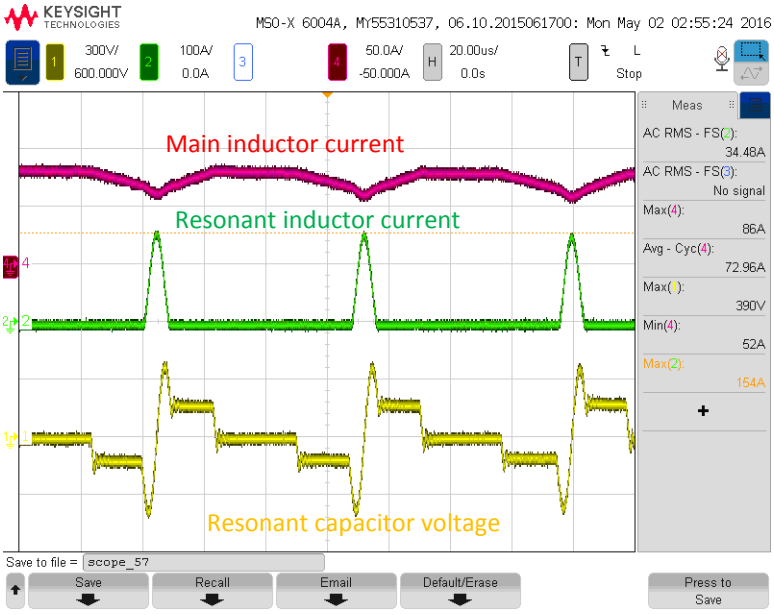


Fig. 10.23: Experimental waveforms of the inductor current (CH4, 50 A/div), resonant inductor current (CH2, 100 A/div), and resonant capacitor voltage (CH1, 300 V/div) for the low-voltage soft-switching dynamic VAr compensator.

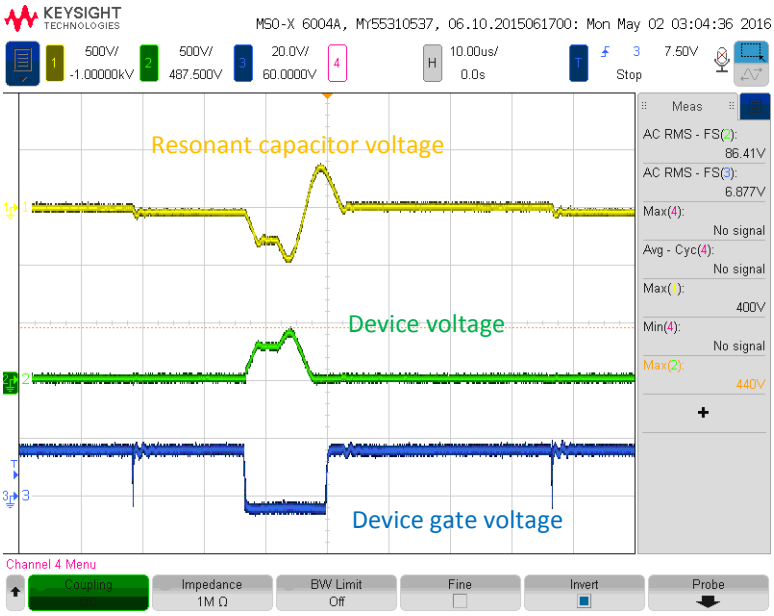


Fig. 10.24: Experimental waveforms of one ZVS transient: resonant capacitor voltage (CH1, 500 V/div), device voltage (CH2, 500 V/div), and gate voltage (CH3, 20 V/div) for the low-voltage soft-switching dynamic VAr compensator.

10.8. Conclusions

The functionality of the S4T is demonstrated through simulation and experiments. This chapter first shows simulation results for a 208 V / 10 kVA three-phase ac/ac S4T. It then presents the 10 kVA S4T unit fabricated in the lab. Mechanical assembling of the power stage and the unit, converter PCB layout, and the system for testing the unit are presented. The assembled S4T unit is first tested by circulating power, with both input and output terminals connected to the same supply. The S4T unit successfully demonstrates power regulation at 9.3 kVA. Power flows in both directions are tested. Then the S4T is tested with a three-phase delta-connected resistive load. The S4T losses at different voltage and current levels are measured using Yokogawa, which shows to be independent of voltage levels and thus indicates soft-switching features. A comparison is then presented among the S4T, the conventional DAB-based SST, and the low-frequency transformer with a rectifier and an inverter, which shows the S4T advantages of lower device count, full-range of soft switching, and higher efficiency. Finally, as an extended unique application, the S4T is configured as a

low-voltage three-phase soft-switching dynamic VAr compensator, and its function is demonstrated by operating one side converter bridge of the S4T.

CHAPTER 11: S4T OPERATION UNDER LOAD STEP-CHANGES, START-UP, SHUT-DOWN, AND FAULT CONDITIONS

11.1. Introduction

In addition to the steady state operation, the S4T also needs to operate properly under various transients such as load step-changes, converter start-up, shunt-down. Also, when system faults or converter faults occur, the converter should be able to protect itself without damaging any components. This chapter will describe the converter's operating principle under all these transients.

11.2. Load Step-Changes

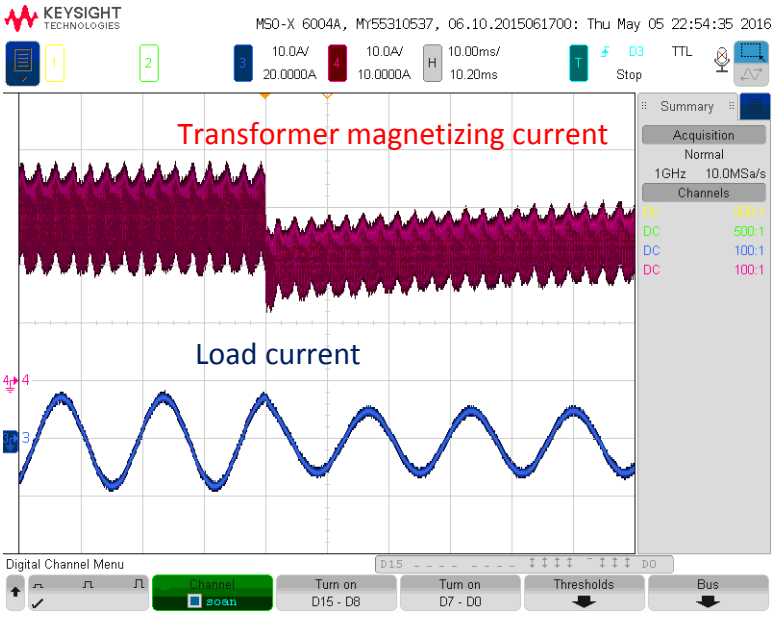
To optimize the S4T efficiency, the transformer magnetizing current level should be varied according to the load current level. In this way, the time period of the freewheeling state, which is only circulating the magnetizing current within the converter and incurs device conduction loss, can be reduced and thus the converter efficiency can be improved. For conventional CSIs, dynamically changing the dc current according to the load level can slow down the dynamic response due to the high inertia of the large inductor. However, for the S4T, the transformer magnetizing inductance is designed to be relatively small, a fact that reduces system inertia, without sacrificing the quality of input and output waveforms. As a result, the transformer magnetizing current can be built up and driven down to a new reference value within a few switching cycles. This makes it feasible to dynamically change the transformer magnetizing current without slowing down the response under load step-changes.

Fast dynamic change of the transformer magnetizing current according to the load level is achieved through a feed-forward loop that controls the magnetizing current, as shown previously in Fig. 7.3. When a load step-change occurs, I_{Di}^{*} can respond immediately thanks to the feed-forward loop of the output power, rather than being slowed down by the PI loop. The converter behavior under both load step-up and -down transients is presented as follows.

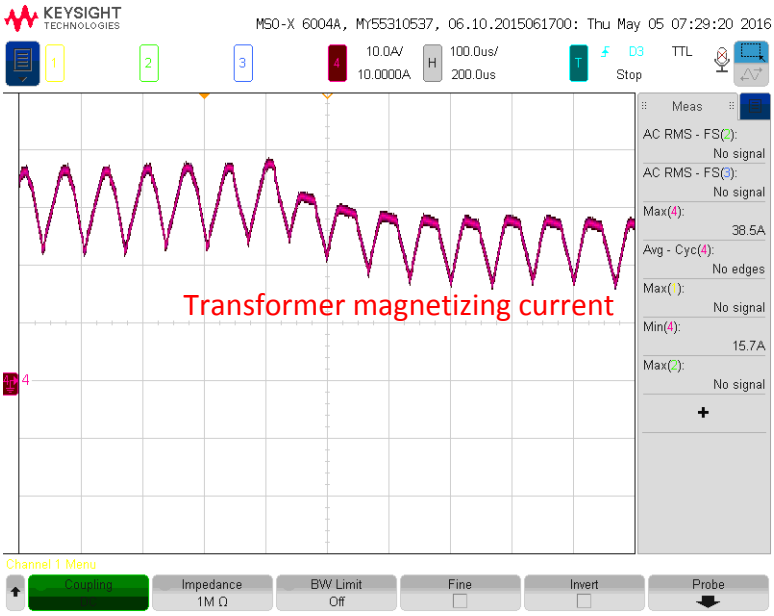
11.2.1. Load Step-Down

Transformer magnetizing current regulation under load step-down change is easy to achieve. Even without the feed-forward loop, the charge control modulation can immediately reduce the duty cycle of the active states to reduce the load current. As a result, the duty cycle of the freewheeling state will become larger. Then the PI loop brings the magnetizing current to the optimum level, which decreases the freewheeling state duration to the minimum. However, the feed-forward loop can expedite this transient process.

Fig. 11.1 shows the experimental results when the load current peak value decreases from 8 A to 5A. The transformer magnetizing current quickly changes from 30 A to 20 A to accommodate the load step-down change. As shown in the zoomed-in waveforms of Fig. 11.1 (b), the transformer magnetizing current is driven down to the new reference within three switching cycles, which shows a very fast dynamic response. This allows almost instantaneous response of the fundamental frequency load. Being able to operate a 20 A dc current instead of 30 A under light load conditions can reduce losses by over 33%.



(a)



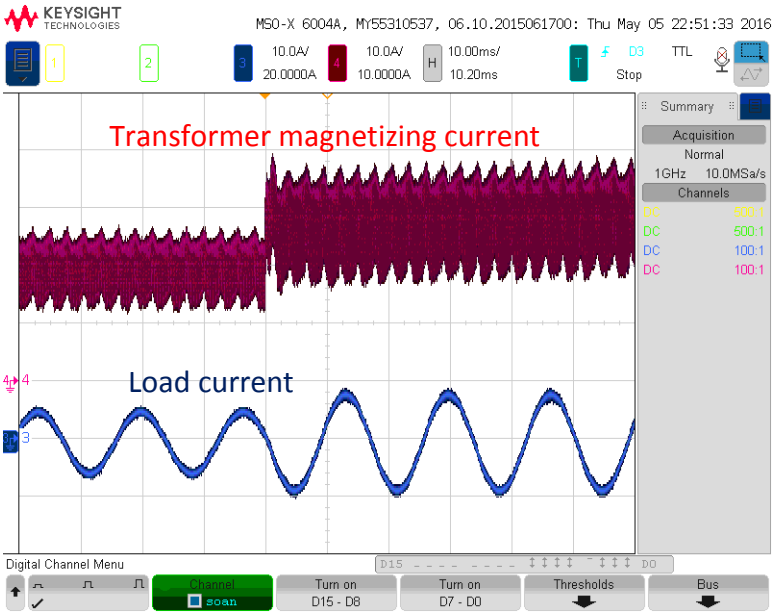
(b)

Fig. 11.1: Transient performance under load step-down change: a) transformer magnetizing current (CH4, 10 A/div) and load current (CH3, 10 A/div); and b) zoomed-in waveforms of the transformer magnetizing current (CH4, 10 A/div).

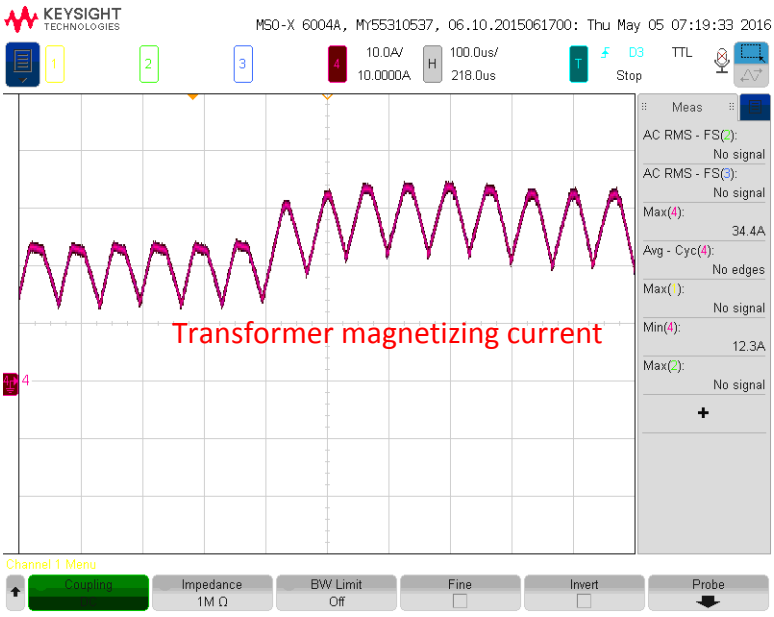
11.2.2. Load Step-Up

When load step-up occurs, the transformer magnetizing current should be quickly built up such that it can deliver enough energy to the load without causing any sag. In this case, I_{Di}^{*} quickly increases because of the feed-forward loop, and then the charge modulation control immediately increases the duty cycle of the input bridge such that more energy is being dumped into the transformer to build up the transformer magnetizing current. This process can also be accomplished within several switching cycles, ensuring fast dynamic response to the load step-up change.

Fig. 11.2 shows the experimental results when the load current peak value increases from 5 A to 8A. The transformer magnetizing current quickly increases from 20 A to 30 A to accommodate the load step-up change. As shown in the zoomed-in waveforms of Fig. 11.2 (b), the transformer magnetizing current is built up to the new reference within three switching cycles.



(a)



(b)

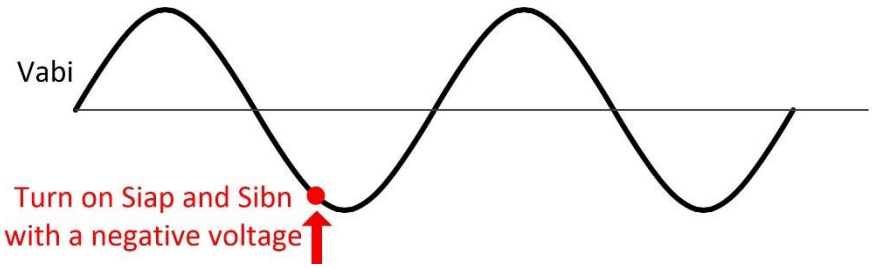
Fig. 11.2: Transient performance under load step-up change: a) transformer magnetizing current (CH4, 10 A/div) and load current (CH3, 10 A/div); and b) zoomed-in waveforms of the transformer magnetizing current (CH4, 10 A/div).

11.3. Converter Start-Up

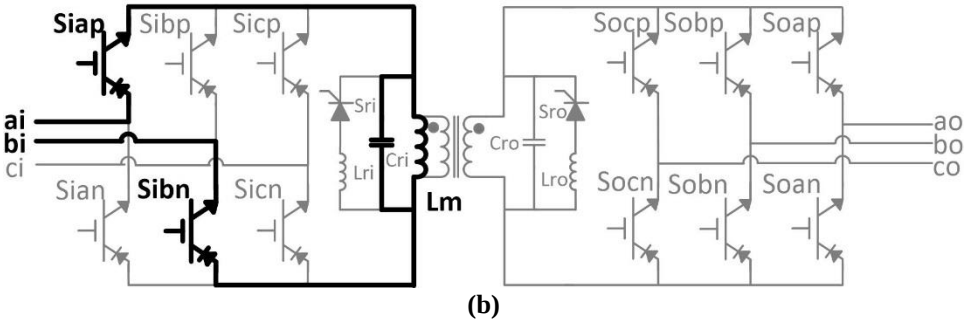
The S4T does not have large dc energy storage capacitors, as in the case of conventional voltage source converters. As a result, for the converter start-up, it does not need to design an external start-up circuit with large resistors and relays to avoid inrush current. However,

the S4T still has small resonant capacitors connected in shunt with the high-frequency transformer. Although they have very small capacitance value, typically from tens to several hundred nano-farads, hard start-up with a large line voltage directly applied across them still generates inrush current. The peak of the inrush current depends on the capacitance value and the parasitic inductance of the current loop, which is typically very small. Hard start-up with Si devices may be acceptable since these devices can typically withstand much higher short-circuit current, but it may be problematic for SiC devices since their short-circuit current withstanding capability is low. Therefore, it is necessary to operate the converter properly during start-up such that the inrush is avoided.

At start-up, the resonant capacitor voltage should be charged up without any inrush current. This can be achieved by turning on the devices whose corresponding input line-to-line voltage is negative. As shown in Fig. 11.3, devices S_{iap} and S_{ibn} are turned on when V_{abi} is negative. Devices do not conduct since they are reverse blocked. When the voltage V_{abi} crosses zero, S_{iap} and S_{ibn} start to conduct, and the capacitor voltage will be the same as V_{abi}. However, the resonant capacitors cannot be charged to its peak voltage by V_{abi} due to low impedance of the transformer magnetizing inductance. Assuming a 180 μH transformer magnetizing inductance, the corresponding impedance at line frequency is only 0.068 ohms. As a result, when the line voltage reaches its peak to fully charge the resonant capacitors, the transformer magnetizing current already reaches several thousand amperes, which is definitely not desired.



(a)



(b)

Fig. 11.3: Charging the resonant capacitors during start-up: a) input line-to-line voltage V_{abi}; and b) turn-on S_{iap} and S_{ibn} when V_{abi} is negative.

The proper way of charging resonant capacitors is by using the energy of the transformer magnetizing inductance. When V_{abi} crosses zero, S_{iap} and S_{ibn} start to conduct, and the transformer magnetizing inductance is charged by V_{abi}. The magnetizing current I_m will quickly increase due to the low impedance of the transformer magnetizing inductance. As soon as I_m reaches a certain level, S_{iap} and S_{ibn} are turned off, and I_m charges the resonant capacitors to decrease their voltage V_{cr} towards a negative value. Since resonant capacitors are quite small, I_m can charge it to a very large negative value. Then the cycle-by-cycle operation can start in a way similar to the steady state operation. The conceptualized start-up waveforms are shown in Fig. 11.4 as the input line-to-line voltage V_{abi}, the magnetizing current I_m, and the resonant capacitor voltage V_{cr} of the first switching cycle after the start-up. It should be noted that, even during the start-up procedure, all devices are switched under soft-switching conditions.

Fig. 11.5 shows the experimental results at the start-up. The external push button to start up the converter is triggered at an arbitrary instant. However, since the input line-to-line voltage of V_{abi} (green curve in Fig. 11.5) is positive at this moment, devices are not turned on. Once V_{abi} reaches a negative value, S_{iap} and S_{ibn} are turned on but they do not conduct. When V_{abi} crosses zero in a positive direction, S_{iap} and S_{ibn} are forward biased, and I_m quickly builds up. Once I_m reaches a certain level, the cycle-by-cycle operation starts. Zoomed-in waveforms of these two resonant capacitor voltages are shown in Fig. 11.5 (b).

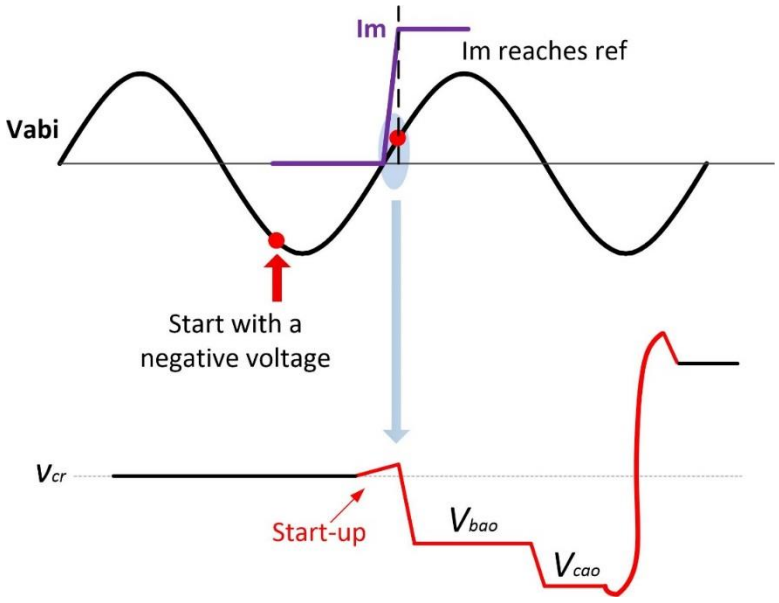
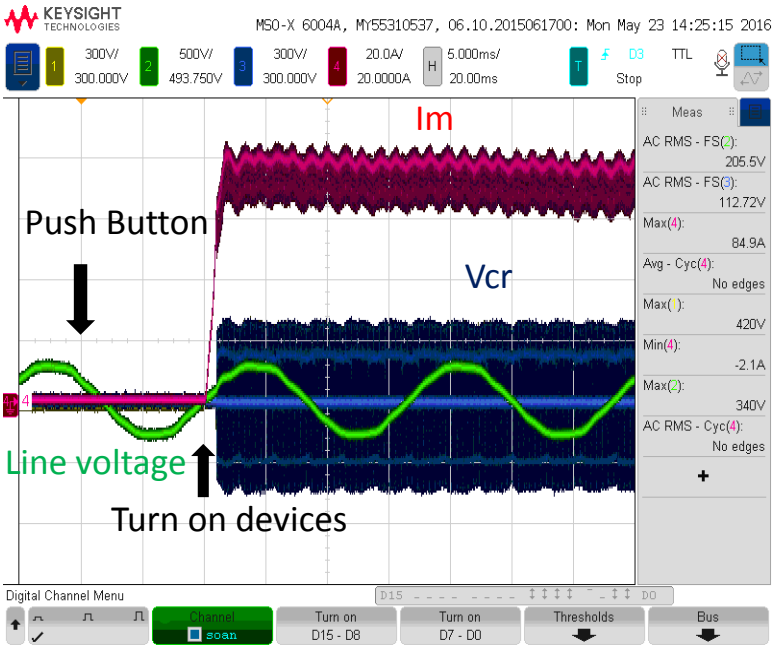
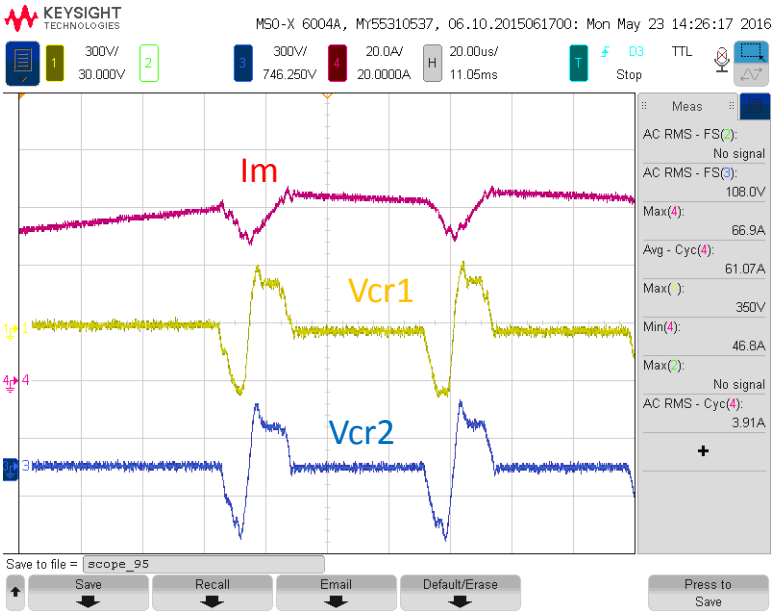


Fig. 11.4: Conceptualized start-up waveforms of input line-to-line voltage V_{abi}, the magnetizing current I_m, and the resonant capacitor voltage V_{cr} of the first switching cycle after the start-up.



(a)



(b)

Fig. 11.5: Start-up experimental waveforms of: a) input line-to-line voltage (CH2, 500 V/div), magnetizing current (CH4, 20 A/div), and resonant capacitor voltage (CH3, 300 V/div); and b) zoomed-in waveforms of the magnetizing current (CH4, 20 A/div) and two resonant capacitor voltages V_{cr1} (CH1, 300 V/div) and V_{cr2} (CH3, 300 V/div).

It should be noted that the start-up sequence can be initiated with any phase pair, e.g. phase *b* and phase *c*, or phase *c* and phase *a*, by turning on the devices corresponding to these phase legs. The start-up sequence remains the same as introduced before for these cases.

11.4. Converter Shut-Down

Normal converter shut-down is accomplished by turning on devices in the same leg. The magnetizing current is then circulating within this leg and starts to decrease towards zero due to the voltage drop across the devices. The shut-down operation can be performed by any of the device legs of the input and output bridges. However, only one device leg of the input or output bridge can be turned on (it can also simultaneously turn on a single device leg in the input and output bridge). Otherwise, the bridge will formulate a current flowing path from the input/output terminal to the transformer if two or more legs are turned on simultaneously, which will either develop a huge transformer magnetizing current by the source voltage due to the low impedance of the transformer magnetizing inductance, or

deliver a large dc current to the passive load. Fig. 11.6 shows that the converter is shut down by turning on devices S_{icp} and S_{icn}.

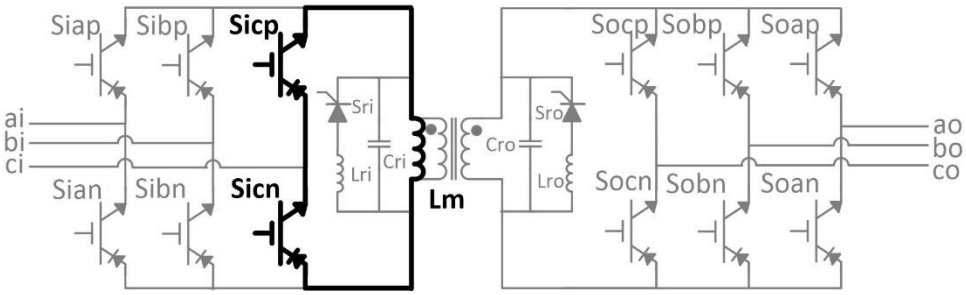


Fig. 11.6: Converter shut-down by turning on devices S_{icp} and S_{icn}.

However, converter shut-down cannot be performed at an arbitrary instant. Turning on devices within the same leg when the resonant capacitors have a negative voltage will develop inrush current through devices. Therefore, the shut-down sequence can only be activated when the capacitor voltage is positive. The allowed shut-down region with respect to the resonant capacitor voltage V_{cr} is shown in Fig. 11.7. If V_{cr} is positive, shut-down can be immediately started by turning on devices within the same leg. Since V_{cr} is positive, the devices are reverse blocked, and no current flows through them. Magnetizing current I_m then charges the capacitor, having V_{cr} decreases. Once V_{cr} drops to zero, devices conduct, and I_m circulates through the device leg and starts dropping towards zero. However, if a shut-down command is applied when V_{cr} is negative, the converter will continue its normal operation until V_{cr} turns positive, and then it will start the shut-down operation. It should be noted that during the shut-down procedure, devices are also operated under soft-switching conditions.

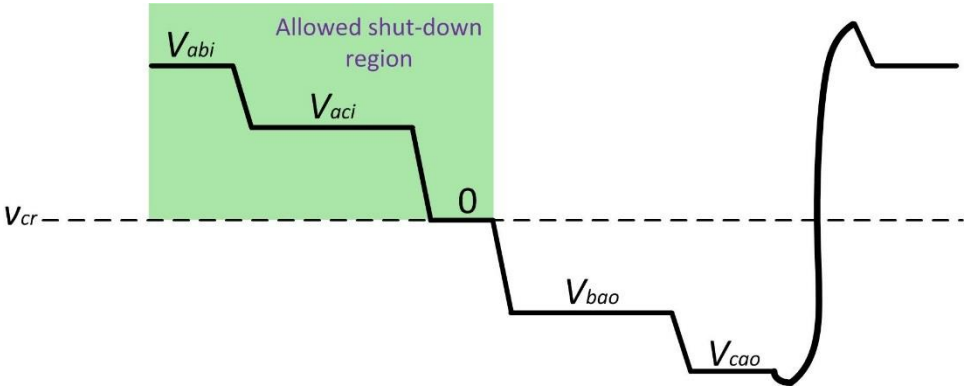


Fig. 11.7: Allowed shut-down region with respect to the resonant capacitor voltage.

Fig. 11.8 shows the experimental results during the converter shut-down. The external push button to shut down the converter is triggered at an arbitrary instant. However, since the capacitor voltage V_{cr} is negative at this moment, the shut-down sequence is not initiated. The converter continues its normal operation until V_{cr} turns positive. Then the devices are turned on, but they are reverse blocked. V_{cr} quickly drops to zero due to the charging effect of I_m. Devices are forward biased as soon as V_{cr} becomes zero. Then I_m circulates through these devices and decreases to zero.

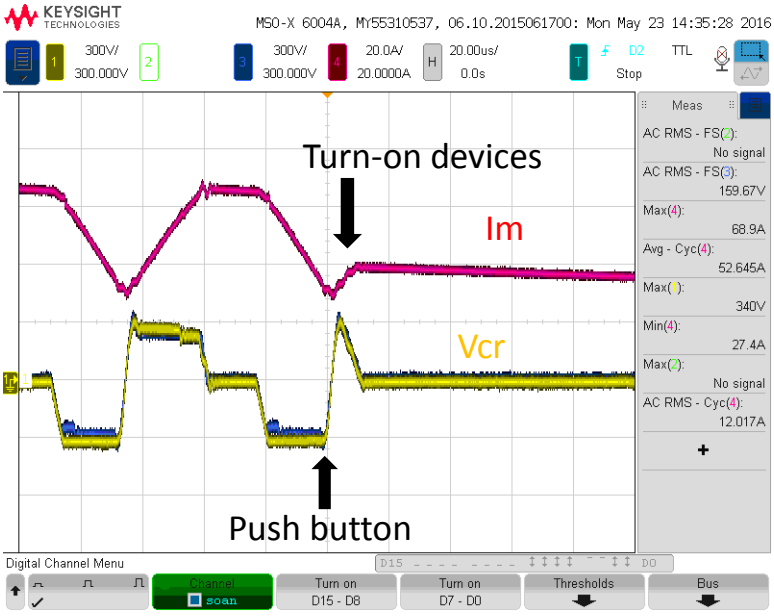


Fig. 11.8: Shut-down experimental waveforms of: magnetizing current (CH4, 20 A/div) and two resonant capacitor voltages V_{cr1} (CH1, 300 V/div) and V_{cr2} (CH3, 300 V/div).

11.5. Operation under Fault Conditions

During the converter operation, once any fault is detected, the converter will go to the fault mode by turning-on devices within the same leg to freewheel the transformer magnetizing current. Signals monitored to detect a fault are voltage and current of the input and output terminals, filter capacitor voltages of the input and output, transformer magnetizing current, and resonant capacitor voltages. All these parameters determine the current and voltage stress of semiconductor devices. Once they exceed a threshold value, the converter will switch to the freewheeling mode to shut-down the converter to protect itself.

Any open circuit fault in the input and output converter bridges, which is typically problematic for current source converters, is also well handled in the S4T. On the input and output terminal sides, the filter capacitors help clamp the over voltage appearing on the terminals. On the high-frequency transformer side, the two resonant capacitors act as a snubber to slow down the *dv/dt* upon any open circuit fault occurring that stops the magnetizing current flow.

Same as in the converter shut-down mode, when a fault is detected, only one device leg of the input or output bridge is turned on, or one device leg of both the input bridge and one of the output are simultaneously turned on, to start the freewheeling. Also, the corresponding devices are only turned on when V_{cr} is positive to avoid inrush current.

11.6. Conclusions

The S4T operations under load step-changes, start-up, shut-down, and fault conditions are presented. Due to the light inertia of the system, by using a feedforward loop in the controller, the S4T can dynamically change the dc current according to the load levels such that the efficiency is kept at an optimum level. The dc current can accomplish step changes within several switching cycles, causing no disturbance to the load demand. Converter operations under start-up and shut-down are also presented. The converter goes through soft start-up and shut down sequence without causing any inrush. The devices also operate under soft-switching conditions under these transients. Converter operation under fault conditions is also described, in which the converter will go through the soft shut-down procedure upon any fault being detected.

CHAPTER 12: SCALING TO MEDIUM VOLTAGE

12.1. Introduction

The absence of high-voltage-rated semiconductor devices sets the barrier for deploying the converters at the medium voltage level. Nowadays, the highest rated IGBTs available in the market are 7.2 kV with a very low switching frequency (< 1 kHz) capability. High-voltage SiC MOSFETs and IGBTs seem to be able to switch at a higher voltage level with lower switching loss, but they are still in the development phase and the high cost will be a major concern for widespread usage. For medium-voltage high-power converter design, existing solutions include connecting devices in series as discussed in [105] and [106], which have been used in pulse power applications. This technique faces many challenges since it requires complex designs of snubbers and gate drivers to make sure that all the series connected devices should equally share the voltage during both steady state and transient. Alternatively, multi-level converters, including various types of stacked H-bridge, neutral-diode clamped, and flying capacitor inverters, provide an alternative approach for high voltage scaling. Balance control of multi-level voltage source converters has been widely explored in [107]-[109].

The modularity of the proposed S4T lends itself to series and/or parallel stacking to reach medium voltage and high power level. Stacking low-voltage rated modules can extend the benefits of small size, fast dynamics, and low cost to the medium-voltage scale. However, the "low inertia" and strong coupling properties of the S4T impose more severe challenges for a stable operation. This chapter will present a robust voltage and power balance strategy for stacking the S4T modules.

12.2. Stacking to Medium Voltage and High Power

Fig. 12.1 shows the medium-voltage dc to three-phase ac stacked converter using the dc to single-phase ac converter modules. Four modules are connected in series on the single-phase ac side to configure a high-voltage single-phase ac, and three of these stacks compose

a high-voltage three-phase ac configuration. Modules are connected in parallel on the dc side to equally share the current. Fig. 12.2 shows the stacked three-phase ac to three-phase ac converter by using the three-phase ac to single phase ac converter modules. The three-phase ac side is connected in parallel, and the single-phase ac side is connected in series. Fig. 12.3 shows the stacked dynamic VAr compensator, in which all the modules are connected in series through stacking the low-frequency terminals. The modular dynamic VAr compensator shown in Fig. 12.3 will be described in greater details in section 12.3. Stacking low-voltage rated modules for medium voltage applications helps in reducing the system cost and maintaining the high-switching frequency for the devices, thereby retaining the fast dynamic response for medium-voltage power conversion.

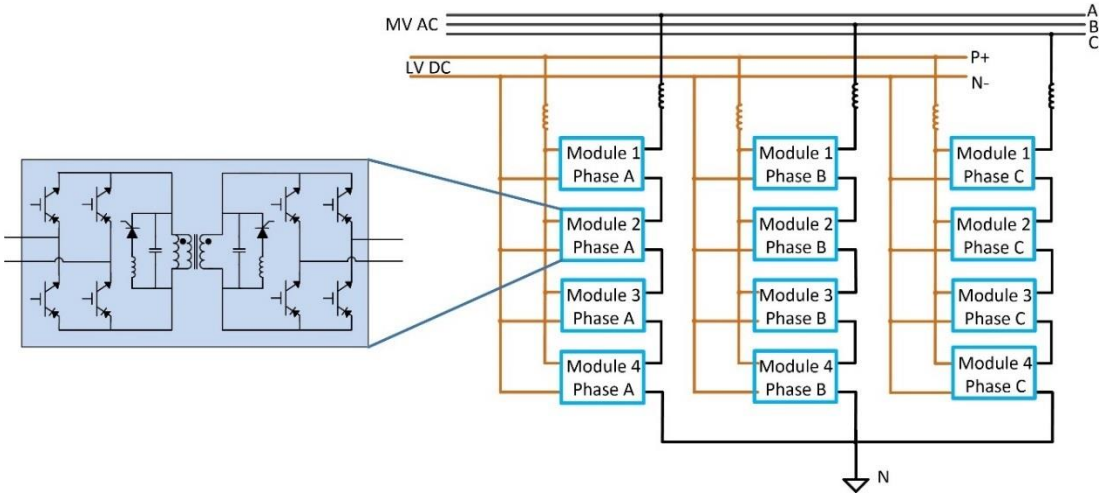


Fig. 12.1: Stacked dc to three-phase ac converter using dc to single-phase ac converter modules.

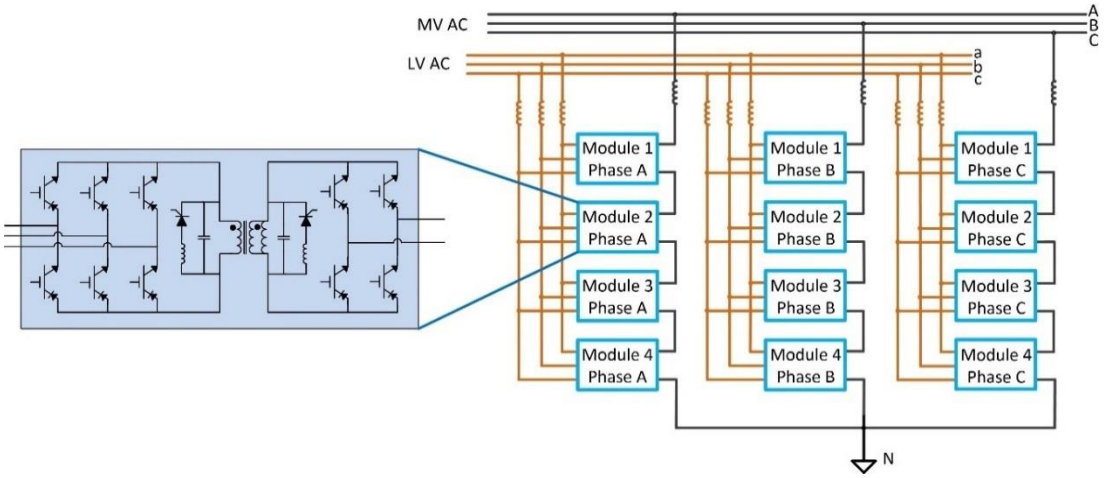


Fig. 12.2: Stacked three-phase ac to ac converter using three-phase ac to single-phase ac converter modules.

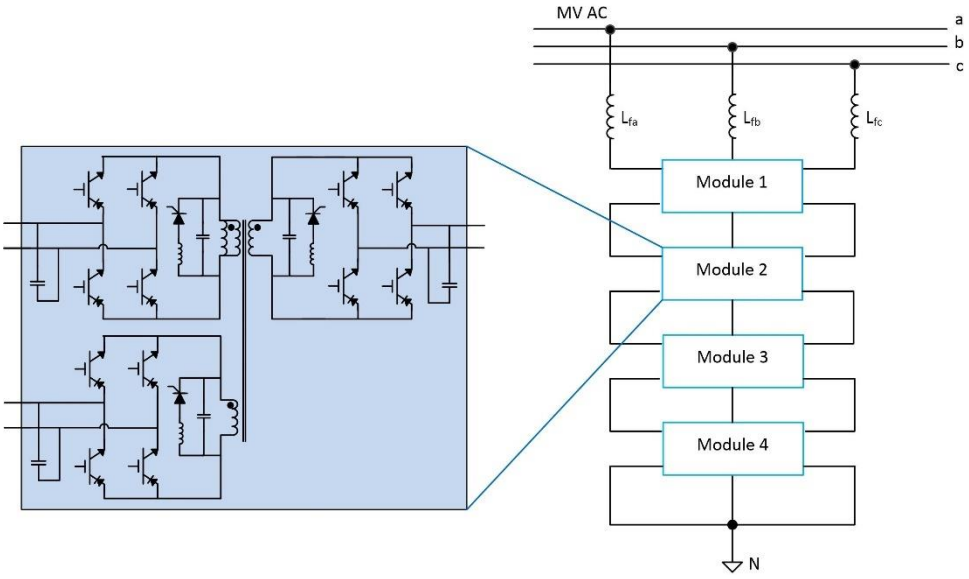


Fig. 12.3: Stacked dynamic VAr compensator modules.

Parallel stacking on the low-voltage high-current side can be easily achieved by providing equal current reference signals for each module and by using charge control to regulate that current. Phase shifting among stacked modules can be used to cancel the switching ripples, leading to a light filter design. However, series stacking on the high-voltage side needs to achieve dynamic voltage sharing among modules. Any voltage imbalance may cause instability and subsequent module failure. In addition, all the converter modules need to maintain a constant transformer magnetizing current, and meanwhile supply sinusoidal current injection to the grid. Due to the commonality of all the topologies, only the series stacking of the dynamic VAr compensators will be discussed here, while the same principle can be extended to stacking other S4T topologies. However, it is expected that controlling the series-stacked VAr compensator will be more difficult than to control the other two stacked SSTs shown in Fig. 12.1 and Fig. 12.2. This is because stacked SSTs have stiff voltage sources on the low voltage side, which can help stabilize the magnetizing current and maintain the voltage balance on the high-voltage side. In the following, the topology of the modular soft-switching dynamic VAr compensator will be first described. Then stacking of this modular converter will be discussed.

12.3. Modular Soft-Switching Dynamic VAr Compensator

This section will cover the topology, operating principle, analysis, control, and simulation results for the single module soft-switching dynamic VAr compensator. The stacking of this modular converter will be discussed in the next section.

12.3.1. Topology of the Single Module Soft-Switching Dynamic VAr Compensator

Fig. 12.4 shows the modular soft-switching dynamic VAr compensator topology for high-voltage applications. The single module topology, which is also a building block, consists of three single-phase CSI modules coupled together with a three-winding high-frequency transformer. Appropriate LC filters are configured around the three low-frequency ac terminals for suppressing switching harmonics. Similar to the low-voltage topology, three auxiliary resonant circuits are connected in parallel to the high-frequency transformer, one for each converter bridge to provide ZVS conditions for all of the main devices.

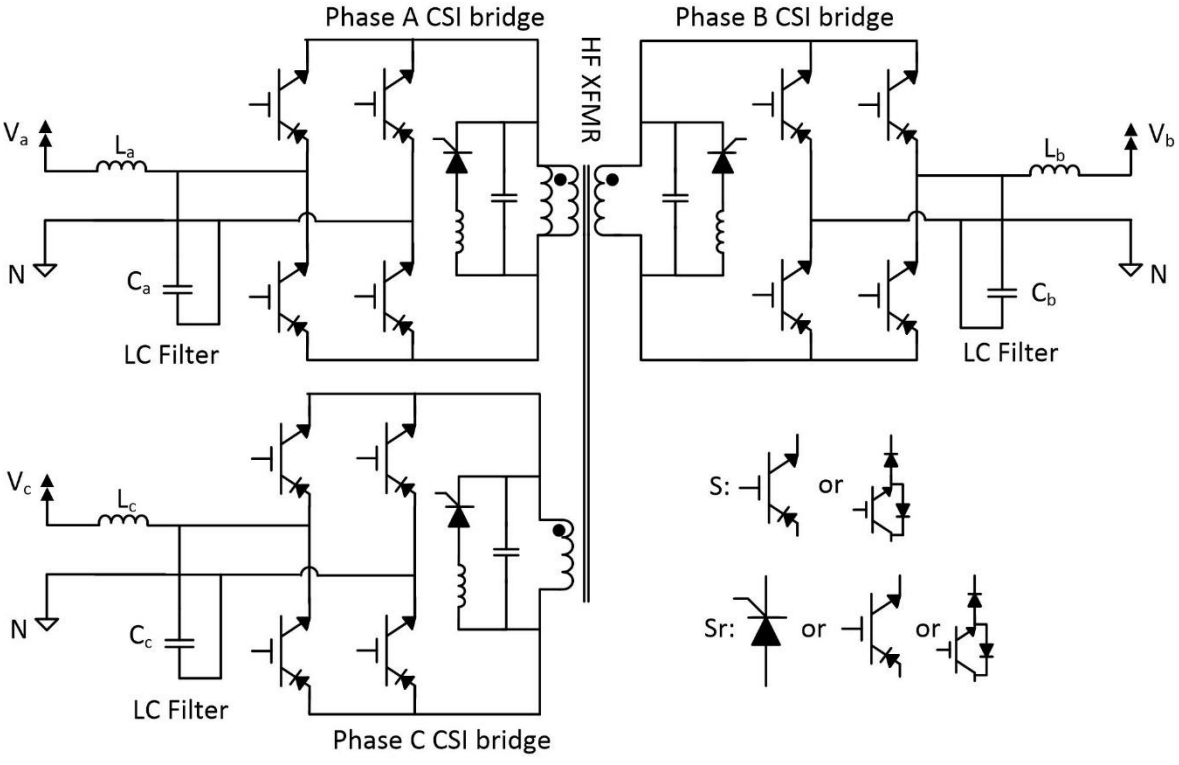


Fig. 12.4: Topology of the modular soft-switching Dynamic VAr Compensator for high-voltage applications.

12.3.2. Operating Principle of the Single Module Soft-Switching Dynamic VAr Compensator

When providing capacitive or leading reactive power, three-phase voltage and reference current waveforms are shown in Fig. 12.5, in which the current leads the voltage by 90°. The operating principle to provide inductive or lagging reactive power is similar and will not be described in detail again. Based on the polarity and magnitude of the current and voltage, the converter has 12 operating sectors and they are repeated every 2π radians. The phase voltage effect on the magnetizing current varies among the 12 sectors. For an instant t_0 as shown in Fig. 12.5, the three-phase current and voltage relationships are as shown in equation (12.1). The line-to-line voltage relationship is as shown in equation (12.2). The operating sequence for the three-phase follows the descending order of the voltage amplitude, which is *b*, *a*, and *c* according to the time instant t_0 of Fig. 12.5. Detailed operation is described below, with the corresponding circuit states and conceptualized waveforms shown in Fig. 12.6 and Fig. 12.7.

$$\begin{cases} |V_b| = |V_a| + |V_c| \\ |I_a| = |I_b| + |I_c| \\ V_a > 0, V_b < 0, V_c > 0 \\ I_a > 0, I_b < 0, I_c < 0 \end{cases} \tag{12.1}$$

$$\begin{cases} V_{ab} > 0 \\ V_{ac} < 0 \end{cases} \tag{12.2}$$

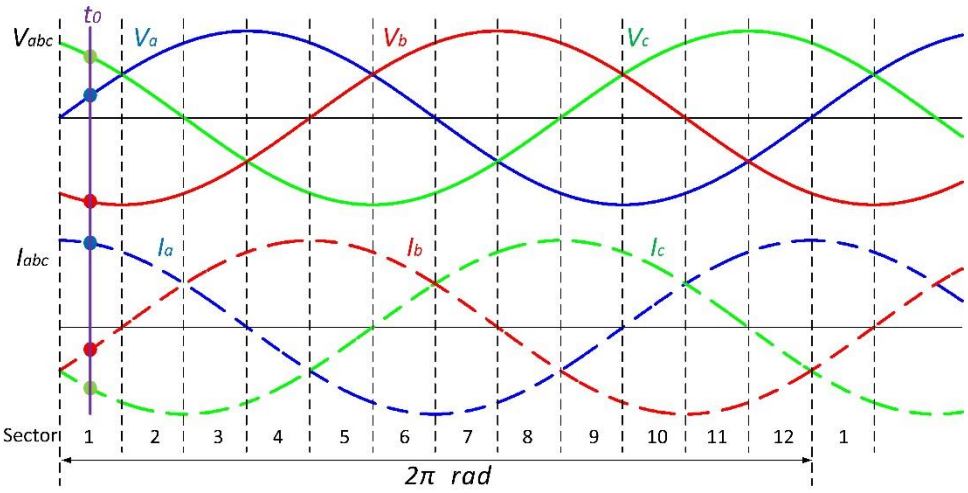


Fig. 12.5: Three-phase voltage and current waveforms with current leading voltage by 90°.

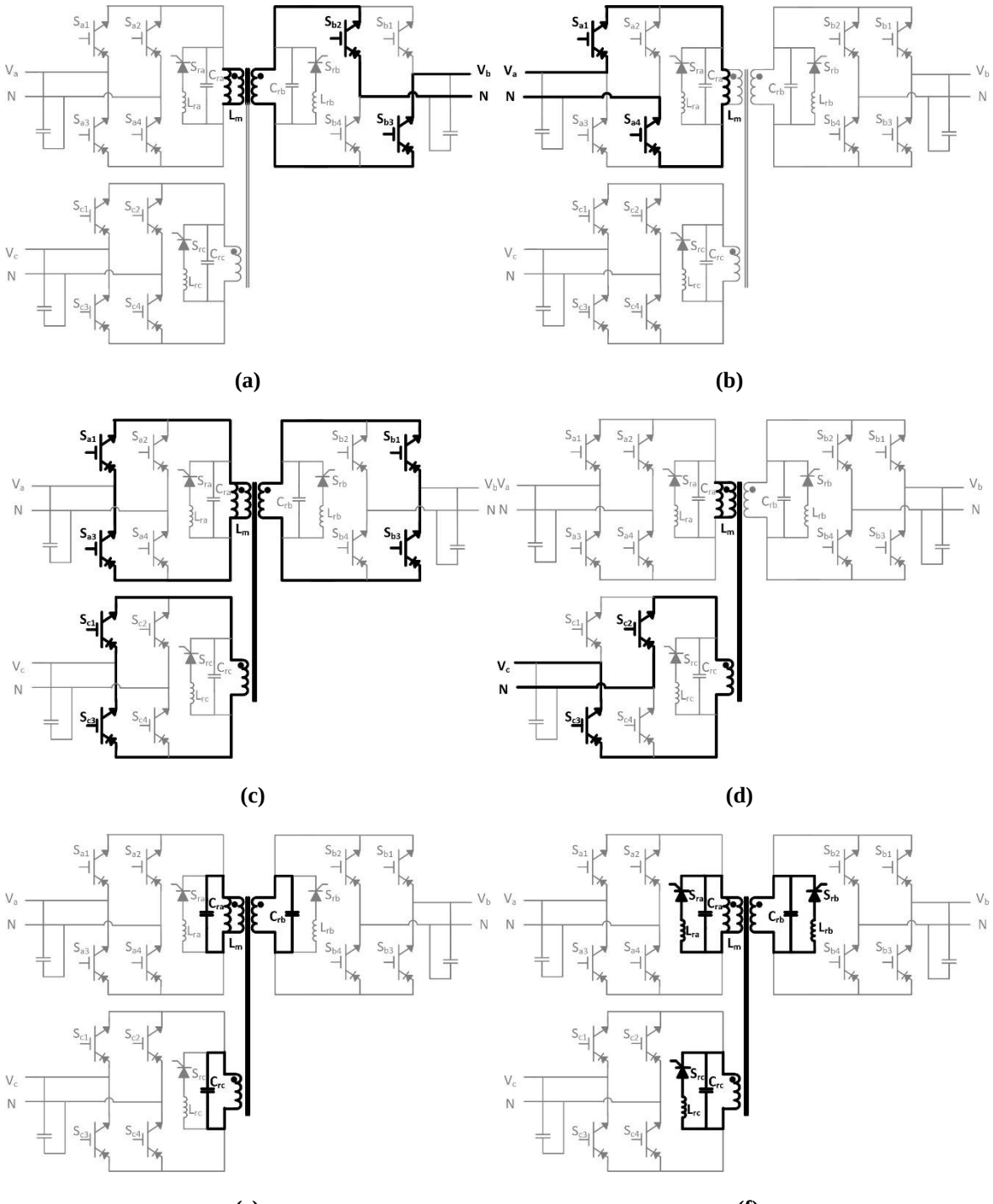


Fig. 12.6: Operating states over one switching cycle: (a) state 1 – charging the magnetizing inductance with the highest line-to-neutral voltage; (b) state 2 – charging the magnetizing inductance with the second line-to-neutral voltage; c) state 3 –freewheeling; (d) state 4 – discharging the magnetizing inductance with the negative line-to-neutral voltage; (e) state 0 – ZVS transition state; and (f) state 5 – resonant state.

A. State 1: Charging the magnetizing inductance with the highest line-to-neutral voltage (Fig. 12.6(a))

The transformer is connected to phase *b* and neutral by turning on S_{b2} and S_{b3}, according to the polarity of the phase *b* reference current. The voltage across the resonant capacitor, which is V_{Cr}, reaches the positive line-to-neutral voltage $-V_{bn}$ (V_{bn} is negative at this instant). The magnetizing inductance L_m is being charged by $-V_{bn}$, and thus the current i_m increases linearly. This state ends when the average current delivered to phase *b* over one switching cycle equals to its reference.

B. State 0: ZVS transition state (Fig. 12.6(e))

S_{b2} and S_{b3} are turned off, causing the magnetizing current to flow through the resonant capacitor, providing a significantly reduced *dv/dt* rate. S_{b2} and S_{b3} are turned off with zero switching loss. The resonant capacitor is charged by i_m and its voltage starts to drop from $-V_{bn}$. Within this state, the incoming device S_{a1} and S_{a4} can be gated on. However, there is no current flowing through the devices since V_{Cr} is larger than V_{an} and the devices are reverse blocked.

C. State 2: Charging the magnetizing inductance with the second line-to-neutral voltage (Fig. 12.6(b))

When V_{Cr} drops to a value equivalent to V_{an}, S_{a1} and S_{a4} conduct and thus the transformer is connected to phase *a* and neutral. Turning on S_{a1} and S_{a4} incurs no switching loss. V_{Cr} reaches the line-to-neutral voltage V_{an} (V_{an} is positive at this instant). The magnetizing inductance L_m is being charged by V_{an}, and thus the current i_m increases linearly. This state ends when the average current delivered to phase *a* over one switching cycle equals to its reference.

D. State 0: ZVS transition state (Fig. 12.6(e))

S_{a4} is turned off under ZVS conditions. The resonant capacitor is charged by i_m, and its voltage starts to drop towards zero. S_{a3} is gated on but the devices are reverse blocked since V_{cr} is larger than zero.

E. State 3: Freewheeling (Fig. 12.6(c))

When V_{Cr} drops to zero, S_{a1}, S_{a3}, S_{b1}, S_{b3}, S_{c1}, and S_{c3} conduct. The converter enters the freewheeling state. i_m flows through these devices rather than flowing to the output terminals. V_{cr} equals to zero at this state.

F. State 0: ZVS transition state (Fig. 12.6(e))

S_{a1}, S_{a3}, S_{b1}, S_{b3}, S_{c1}, and S_{c3} are turned off under ZVS conditions. The resonant capacitor is charged by i_m, and its voltage starts to drop towards a negative value.

G. State 4: Discharging the magnetizing inductance with the negative line-to-neutral voltage (Fig. 12.6(d))

S_{c2} and S_{c3} conduct under ZVS conditions, and L_m is being discharged by $-V_{cn}$. V_{cr} equals to $-V_{cn}$. This state ends when the average current delivered to phase *c* within one switching cycle equals to its reference.

H. State 0: ZVS transition state (Fig. 12.6(e))

S_{c2} and S_{c3} are turned off under ZVS conditions. The resonant capacitor is charged by i_m, and its voltage drops to a greater negative value. This state delivers more energy to the capacitor to make sure that V_{cr} can reach a voltage higher than $-V_{bn}$ after the resonant operation.

I. State 5: Resonant (Fig. 12.6(f))

Auxiliary switch S_r is turned on under ZCS condition to initiate the resonant operation between L_r and C_r. This state ends when the current through L_r drops to zero, and S_r is turned off under ZCS condition. As a result, the voltage polarity of C_r is reversed.

J. State 0: ZVS transition state (Fig. 12.6(e))

After the resonant operation, the capacitor voltage reaches a value larger than the line-to-neutral voltage $-V_{bn}$. Then the incoming devices S_{b2} and S_{b3} can be turned on under ZVS conditions. The resonant capacitor is charged by i_m until its voltage drops to a value equals to $-V_{bn}$, which starts the ZVS operation of next switching cycle.

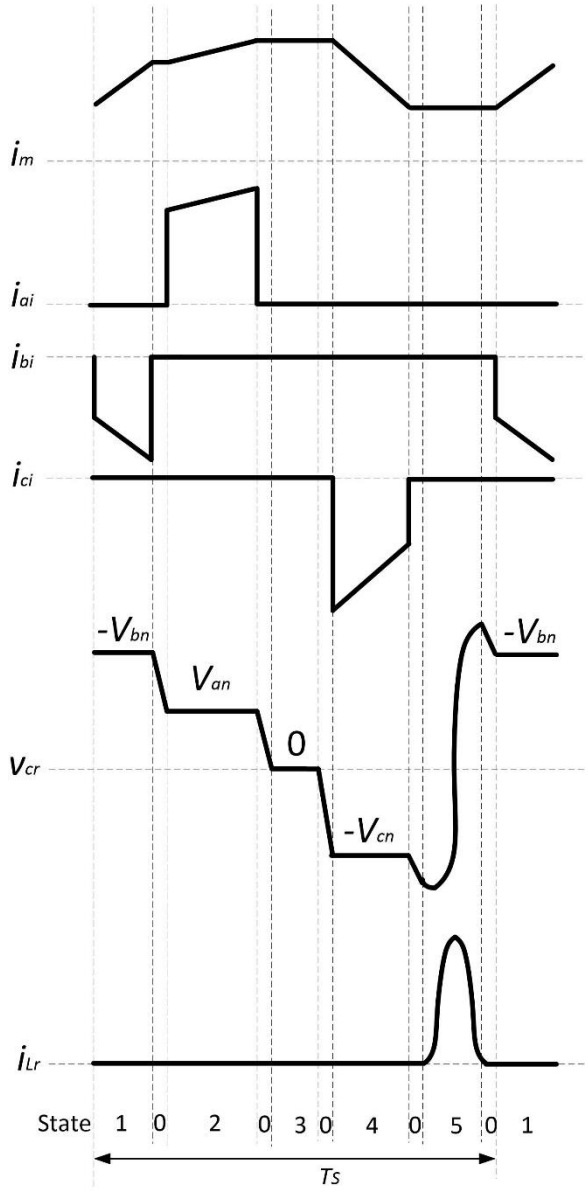


Fig. 12.7: Conceptualized waveforms (states 1 – 4 correspond to Fig. 12.6 (a) – (d); state 0 corresponds to Fig. 12.6 (e); and state 5 corresponds to Fig. 12.6 (f)).

12.3.3. Analysis of the Single Module Soft-Switching Dynamic VAr Compensator

Analysis is performed for the modular soft-switching dynamic VAr compensator to obtain the optimum dc current level, the average current ripple on the magnetizing inductance, and the conditions for ensuring CCM operation. The modular topology operation sequences over all three phases. It has three active states, which are governed by equation (12.3), in which t_a, t_b, t_c are the time durations for these three states. The voltage applied to the magnetizing inductance is the line-to-neutral voltage. Neglecting the ZVS transition state

and the resonant state, equation (12.4) should be valid to eliminate the freewheeling state when the phase that has the highest instantaneous line current reaches its peak I_p. Equation (12.5) is satisfied for a balanced three-phase system. Therefore, the optimum dc current for the magnetizing inductance can be derived as equation (12.6), in which the dc current should be equal to twice the peak value of the reference grid current.

$$\begin{cases} I_{m.opt} * t_a = |I_a| * T_S \\ I_{m.opt} * t_b = |I_b| * T_S \\ I_{m.opt} * t_c = |I_c| * T_S \end{cases} \tag{12.3}$$

$$t_a + t_b + t_c = T_S \tag{12.4}$$

$$|I_a| + |I_b| + |I_c| = 2 * max\left(|I_a|, |I_b|, |I_c|\right) \tag{12.5}$$

$$I_{m.opt} = 2I_p \tag{12.6}$$

The three-phase grid voltage, which is lagging the current by 90°, is defined by equation (12.7). The average values of the three-phase line currents and voltages applied to the magnetizing inductance over $\pi/6$ rad are calculated as equations (12.8) and (12.9). The average time period of phase *c* operation, shown in equation (12.10), can be derived from equations (12.3) and (12.4). Assuming an instant when phases *a* and *b* charge the magnetizing inductance while phase *c* discharges it, the average magnetizing current ripple is given by equation (12.11).

$$\begin{cases} V_a = V_p sin(\omega t) \\ V_b = V_p sin\left(\omega t - 2\pi/3\right) \\ V_c = V_p sin\left(\omega t + 2\pi/3\right) \end{cases} \tag{12.7}$$

$$\begin{cases} I_{a.ave} = \dfrac{6}{\pi} \int_0^{\pi/6} \left| I_p sin\left(\omega t + \dfrac{\pi}{2}\right) d(\omega t) \right| = \dfrac{3}{\pi} I_p \\ I_{b.ave} = \dfrac{6}{\pi} \int_0^{\pi/6} \left| I_p sin\left(\omega t - \dfrac{\pi}{6}\right) d(\omega t) \right| = \dfrac{3\left(2 - \sqrt{3}\right)}{\pi} I_p \\ I_{c.ave} = \dfrac{6}{\pi} \int_0^{\pi/6} \left| I_p sin\left(\omega t - \dfrac{5\pi}{6}\right) d(\omega t) \right| = \dfrac{3\left(\sqrt{3} - 1\right)}{\pi} I_p \end{cases} \tag{12.8}$$

$$\begin{cases} V_{a.ave} = \frac{6}{\pi}\int_0^{\pi/6}\left|V_p sin(\omega t)d(\omega t)\right| = \frac{3(2-\sqrt{3})}{\pi}V_p \\ V_{b.ave} = \frac{6}{\pi}\int_0^{\pi/6}\left|V_p sin\left(\omega t - \frac{2\pi}{3}\right)d(\omega t)\right| = \frac{3}{\pi}V_p \\ V_{c.ave} = \frac{6}{\pi}\int_0^{\pi/6}\left|V_p sin\left(\omega t + \frac{2\pi}{3}\right)d(\omega t)\right| = \frac{3(\sqrt{3}-1)}{\pi}V_p \end{cases} \tag{12.9}$$

$$t_{c.ave} = \frac{|I_{c.ave}|}{|I_{a.ave}|+|I_{b.ave}|+|I_{c.ave}|}T_S \tag{12.10}$$

$$\Delta I_{m.ave} = \frac{V_{c.ave} * t_{c.ave}}{L_m} = \frac{(6-3\sqrt{3})V_p}{\pi f_S L_m} \tag{12.11}$$

The magnetizing current has the maximum ripple at $\omega t=0$, thus three-phase instantaneous grid current and voltage are simplified as equations (12.12) and (12.13). The discharging time duration, which is t_c, is calculated as equation (12.14). Therefore, the peak magnetizing current ripple is shown as equation (12.15). To avoid DCM operation, the average dc current should be larger than half of this ripple, thus equation (12.16) should be satisfied.

$$\begin{cases} I_a = I_p \\ I_b = I_c = -\frac{1}{2}I_p \end{cases} \tag{12.12}$$

$$\begin{cases} V_a = 0 \\ V_b = -V_c = -\frac{\sqrt{3}}{2}V_p \end{cases} \tag{12.13}$$

$$t_c = \frac{|I_c|}{|I_a|+|I_b|+|I_c|}T_s \tag{12.14}$$

$$\Delta I_{m.max} = \frac{V_c t_c}{L_m} = \frac{\sqrt{3}V_p}{8 f_S L_m} \tag{12.15}$$

$$f_S L_m > \frac{\sqrt{3}V_p}{32 I_p} \tag{12.16}$$

12.3.4. Control of the Single Module Soft-Switching Dynamic VAr Compensator

Similar to the S4T, to maintain a compact and low-cost design, the magnetizing inductance, which carries a constant dc current, is designed to have a low inductance value. And charge-control-based modulation is used to control the converter, which can help maintain high-quality injections with large dc current ripple. Control of the converter consists of two loops, as shown in Fig. 12.8, in which the outer loop generates the three-phase current references and the inner loop controls device duty cycles based on the charge modulation. When synchronized with the three-phase line voltage, the *D* component of the grid current is used to regulate the magnetizing current at a constant dc level. The feedback loop generates I_D^* from dc current error Δi_m, and the compensator G_M, which can be a PI controller, is used to compensate the converter loss such that i_m is regulated at its reference I_m^*. The *Q* component of the three-phase current reference I_Q^* is set based on the required reactive power Q^* that needs to be injected. Then the three-phase reference currents are obtained through the *DQ-ABC* transformation, and they are fed into the inner control loop.

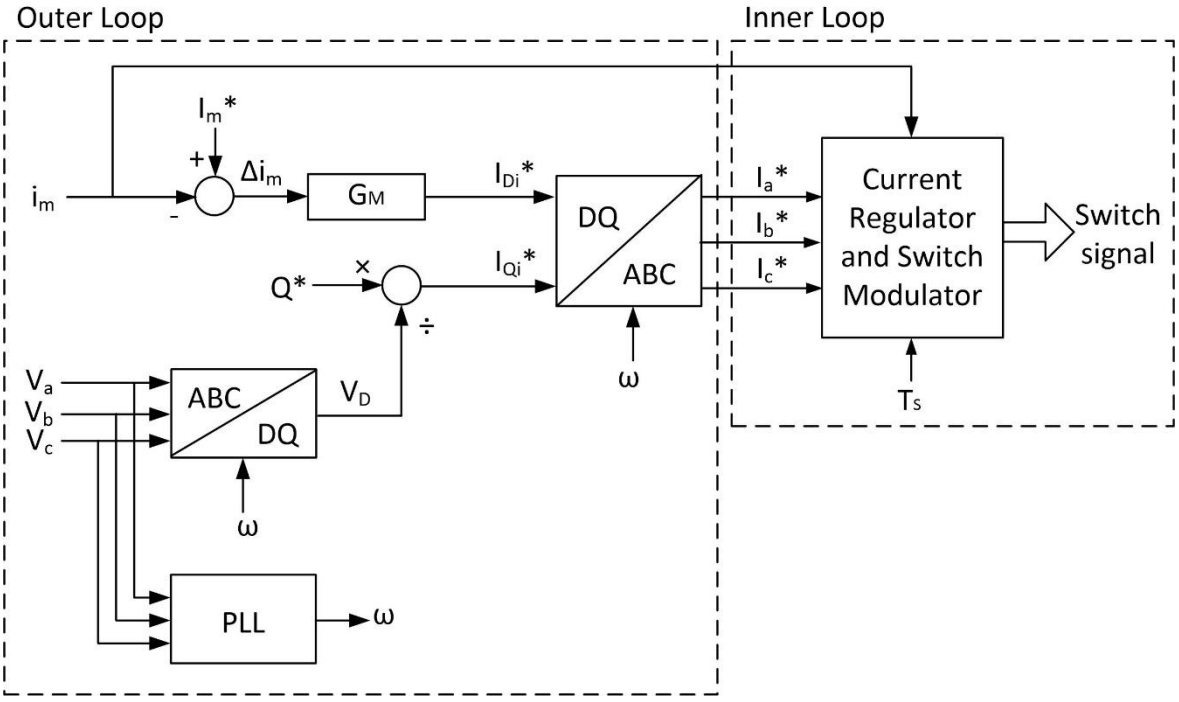


Fig. 12.8: Control architecture for the single-module soft-switching dynamic VAr compensator.

The inner loop is a charge control modulator, which continuously compares the actual charge delivered to each phase with the reference charge to determine the duty cycle of devices. The charge control for this modular soft-switching dynamic VAr compensator is the same as for the S4T, which will not be described in detail here again. The inner control loop for the modular dynamic VAr compensator is shown in Fig. 12.9. The bridge operation is sequenced consecutively such that a complete switching period consists of cycling through all three phases.

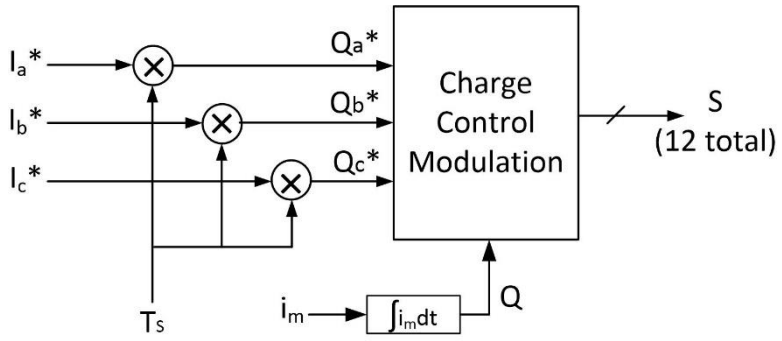


Fig. 12.9: Inner control loop for the modular soft-switching dynamic VAr compensator.

12.3.5. Simulation Results of the Single-Module Soft-Switching Dynamic VAr Compensator

Simulations are performed for the single-module soft-switching dynamic VAr compensator rated at 208 V / 10 kVAr. The transformer has a magnetizing inductance of 200 μH, and the switching frequency is 15 kHz. Fig. 12.10 shows the simulation waveforms of the three-phase voltage, converter-injected current, and the magnetizing current. It can be seen that the converter injects a current which is leading the voltage by 90^o, and the magnetizing current is maintained at a dc level with high-frequency switching ripple on top of it. Fig. 12.11 shows the zoomed-in waveforms of the magnetizing current, the resonant inductor current, and the resonant capacitor voltage. Compared to the low-voltage dynamic VAr compensator that was discussed in section 10.7, the dc current level of the modular topology is twice that of the low-voltage one. This is because the duty cycle of each bridge for the modular topology is always equal to or less than 0.5. However, the modular topology lends itself to stacking to high voltage, which is not possible with the low-voltage topology.

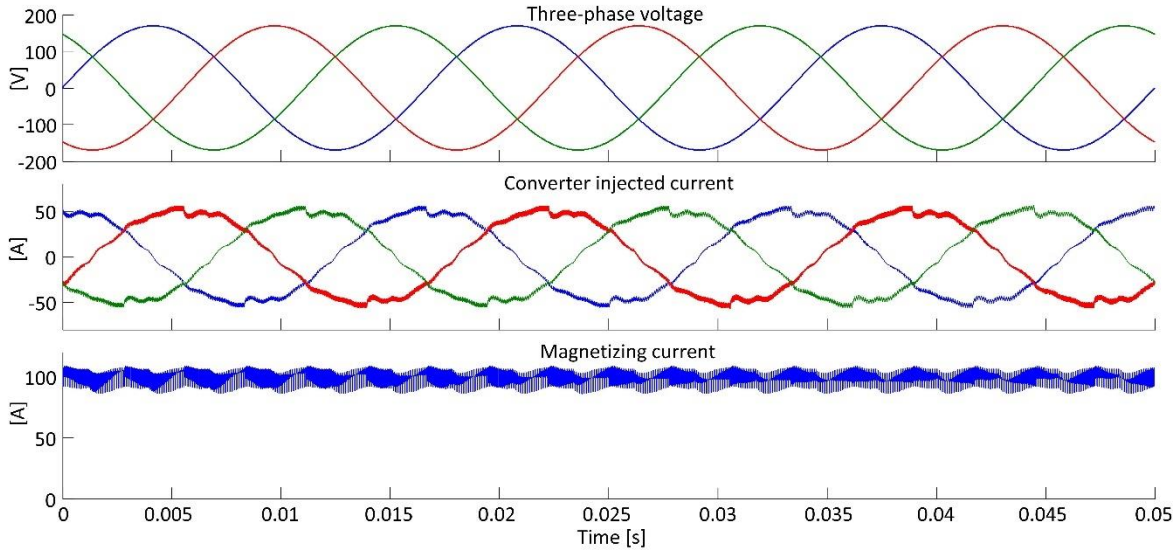


Fig. 12.10: Simulation results of the three-phase voltage, converter-injected current, and magnetizing current for the single-module soft-switching dynamic VAr compensator.

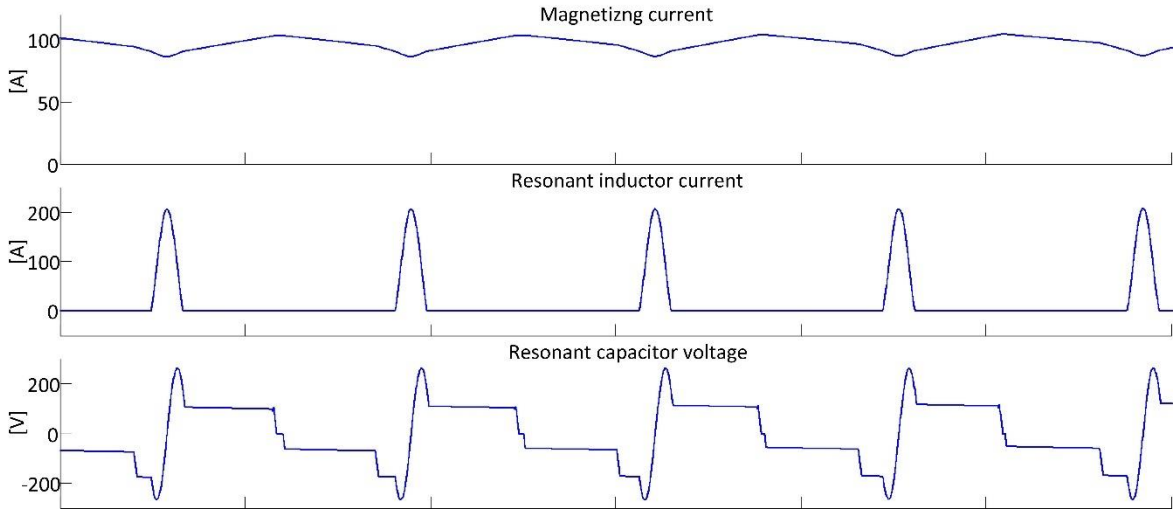


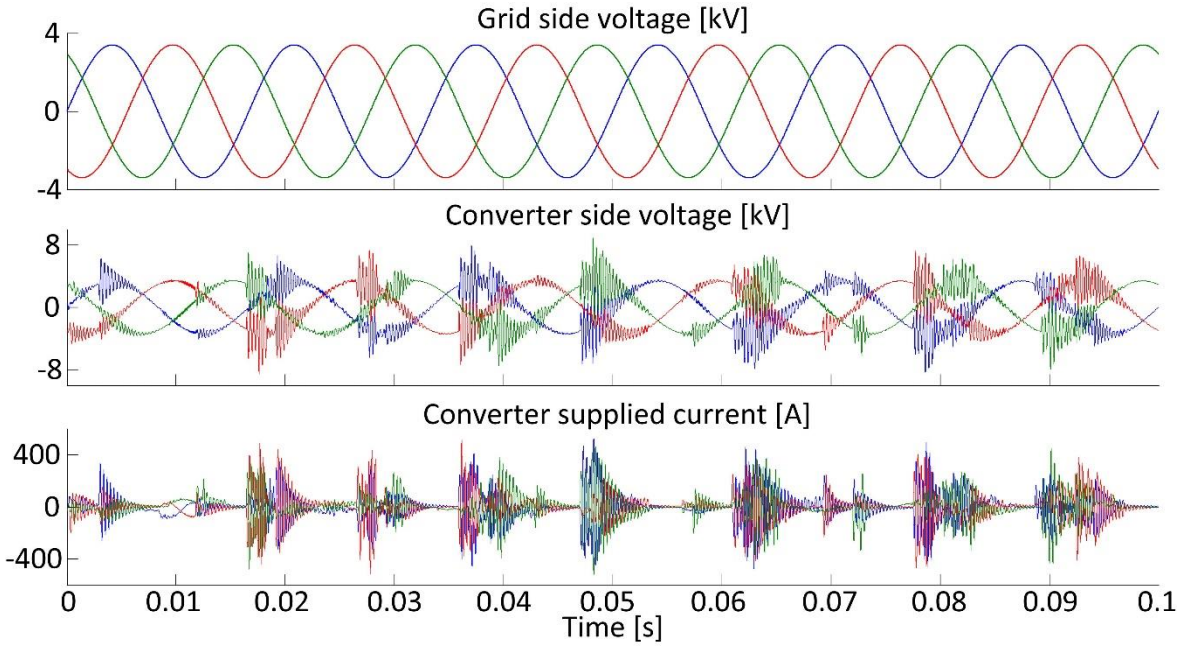
Fig. 12.11: Cycle-by-cycle waveforms of the magnetizing current, resonant inductor current, and resonant capacitor voltage for the single-module soft-switching dynamic VAr compensator.

12.4. Stability Issue of Converter Series Stacking

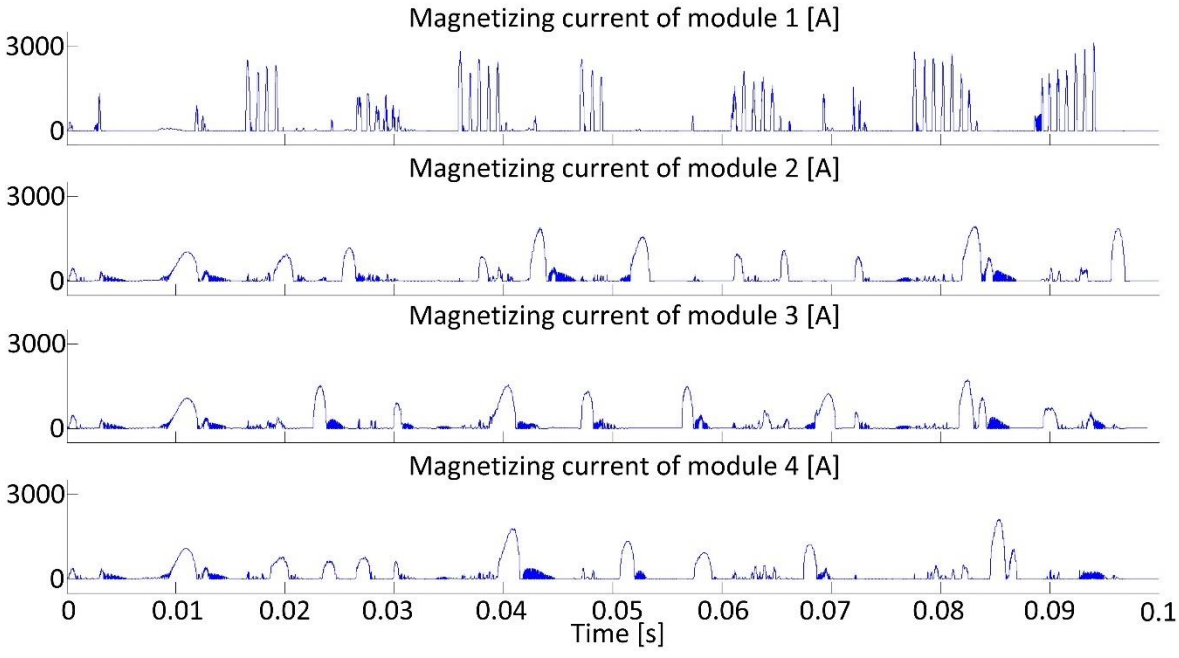
As shown in Fig. 12.3, the modular soft-switching dynamic VAr compensator that was discussed in section 12.3 can be connected in series to reach high voltage. Four modules are stacked to interface a 4.16 kV (line-to-line) three-phase ac system, as shown in Fig. 12.3. With equal voltage sharing, each module should regulate a RMS voltage of 600 V across its input. This enables using 1200 V or 1700 V IGBT for each module. If the stacked system

loses stability, the voltage across each module may go beyond the IGBTs rating and damage the converter.

For a single module, the control strategy defined in section 12.3 uses charge control to maintain a constant transformer magnetizing current and to regulate the input and output injections. If load voltage regulation is required, an outer voltage control loop is then added to the inner current loop. However, for series stacking, using this control strategy cannot maintain the voltage sharing among all the modules. Perfectly synchronous switching among all the modules cannot be guaranteed due to the differences of semiconductor switch characteristics, converter parasitic elements, and various latencies of controllers and gate drivers. Besides, phase shifting operation among modules is desirable to cancel the switching ripple, and thus reduce the line current harmonics and the filter size, while phase shifting will further exacerbate the voltage sharing issue. Therefore, the charge control in the form described in section 12.3 cannot be directly applied to the stacked system. Fig. 12.12 demonstrates the unstable operation of the stacked VAr compensator through simulation. Stacked VAr compensator is required to provide 300 kVAr reactive power, with 75 kVAr from each module. The transformer magnetizing current reference is set at 300A for each module with a switching frequency of 15 kHz. Two adjacent modules are phase-shifted by a quarter switching cycle to cancel the switching ripple. The stacked converter is operated with the charge modulation control described in section 12.3. Fig. 12.12 (a) shows the waveforms of the grid voltage, converter side voltage (before the filter inductor), and the converter supplied current. Fig. 12.12 (b) shows the magnetizing current waveforms of these four modules. Results show that the transformer magnetizing current, terminal voltages, and the converter supplied current cannot be stably controlled.



(a)



(b)

Fig. 12.12: Simulation waveforms to show unstable operation using conventional charge control for the stacked dynamic VAr compensator: a) waveforms of grid side voltage, converter side voltage, and converter supplied current, and (b) magnetizing current of four modules.

12.5. Control Strategy for Series Stacking Converters

To ensure stable operation, a robust control strategy must be developed. However, there are several challenges for stabilizing the series-stacked converter modules:

1) The system exhibits a property of “low inertia” since neither the high-frequency transformer nor the filter capacitor has large energy storage capability.

2) The converter itself has strong coupling effects among the filter capacitor voltage, supplied current, and the magnetizing current.

3) All the series-stacked modules are also strongly coupled through the low-frequency terminals since the same grid current flows through all modules, making the individual magnetizing current regulation for each module to be challenging.

To address all the above challenging issues, a robust control strategy for series stacking converter modules will be developed in this section. First and foremost, the terminal voltage sharing among all the modules has to be strictly maintained, which guarantees the safe operation of the converter module. Secondly, the transformer magnetizing current has to be regulated to ensure the system’s controllability. With these two conditions satisfied, the grid current is also regulated to be sinusoidal. Therefore, the proposed controller is composed of two control loops. The inner loop, which is a faster loop, will be used to regulate the voltage across each module and the magnetizing current on a switching cycle-to-cycle basis, and the outer loop that has slower dynamics is used to regulate the grid current. In the following, the auxiliary resonant circuit is omitted for simplification, since it is only involved in the ZVS transition of the devices while not impacting the steady state operation of the converter.

12.5.1. Inner Control Loop

Filter Capacitor Voltage Regulation

The inner control loop is responsible for regulating the filter capacitor voltage and the magnetizing current of each module at the reference value. For the S4T, the voltage stress of each device is the same as the filter capacitor voltage. Therefore, it is important to strictly regulate the filter capacitor voltage at each switching cycle such that the device is operated within its SOA. The capacitor voltage of each phase has a direct relationship with the duty cycle of that bridge. Take bridge A as an example, which is shown in Fig. 12.13. The green line is the current flow path when the bridge is operating. When the bridge is inactive, the

filter capacitor is charged by the grid current $I_{g,A}$. While when the bridge is active, it is discharged by a current equal to $I_m - I_{g,A}$. The filter capacitor voltage and current relationship is governed by equations (12.17) and (12.18). To achieve a strict voltage regulation of the filter capacitor, a deadbeat control strategy is used here, as illustrated in Fig. 12.14. At the start of each bridge operation, the transformer magnetizing current I_m and the grid current $I_{g,A}$ are sensed. The capacitor voltage error $\Delta V_{cap.A}$ is calculated as the reference voltage minus the present capacitor voltage of this phase. Then equation (12.18) is used to determine the duty cycle. The next bridge operation will start in the same manner. In this way, at the end of each bridge operation period, the filter capacitor voltages reach the reference.

$$I_{cap.A} = I_{g.A} - m * I_m \tag{12.17}$$

where m=1 when bridge A is active; m=0 when the bridge A is inactive.

$$\frac{I_{cap.A} * D_A^{'} T_S}{C} = \Delta V_{cap.A} \tag{12.18}$$

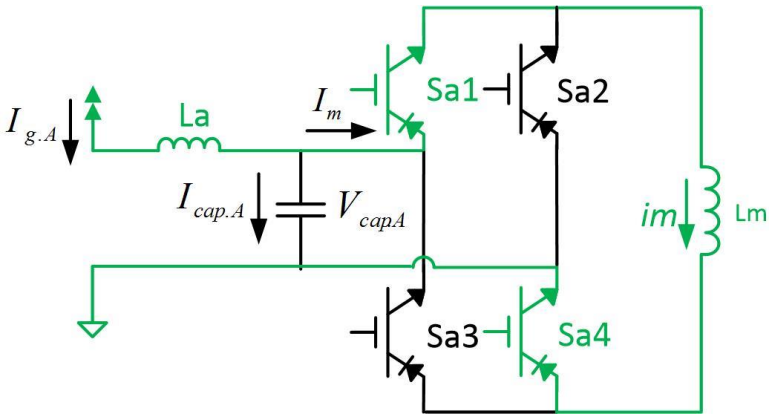


Fig. 12.13: Simplified phase A bridge configuration.

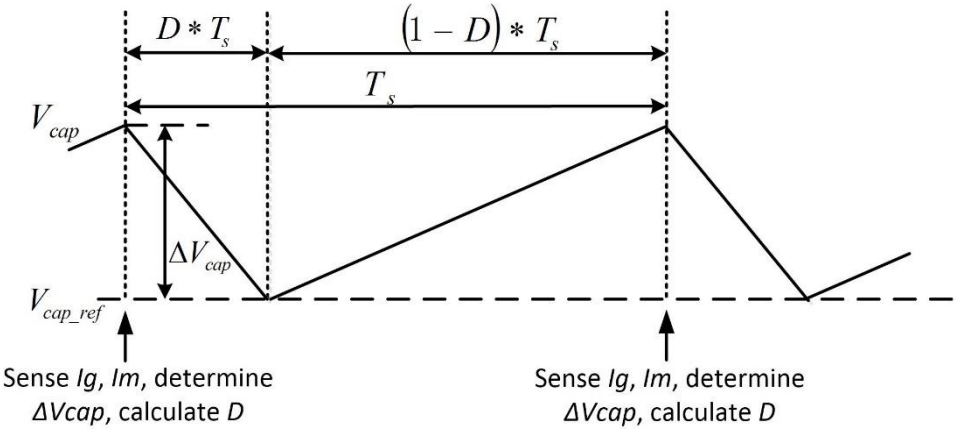


Fig. 12.14: Principle of controlling the filter capacitor voltage.

Fig. 12.15 shows the simulation waveforms of the filter capacitor voltage based on the proposed deadbeat control strategy. The black line in the figure is the reference voltage for each module, which envelops the actual filter capacitor voltage, indicating a tight voltage regulation. However, there is always a steady-state error between the filter capacitor voltage fundamental value and the reference, which will result in a deviation on the active and reactive power control as well as some grid current harmonics. This can be compensated for and improved by the outer loop controller, which will be discussed later.

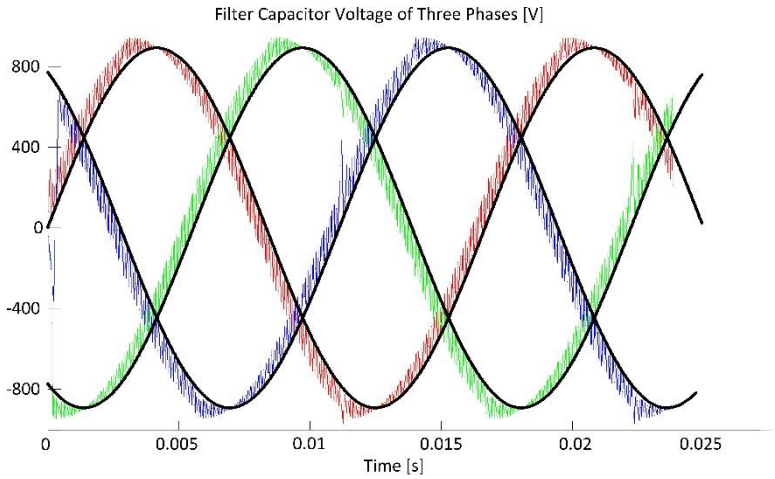


Fig. 12.15: Simulation waveforms of the filter capacitor voltage to show the tight voltage regulation.

Magnetizing Current Regulation

For the conventional charge control modulation that is used to control a single converter module, the converter extracts energy from the grid to compensate for the converter loss in order to maintain the magnetizing current at a constant dc level. If the magnetizing current

is lower than the reference, the *d* component of the grid current reference will be increased to extract more active power from the source. While if it is higher than the reference, the *d* value will be decreased. However, for the stacked converter, modules may have different compensation requirements, i.e., the magnetizing current of one module may be higher than the reference while lower for other modules. However, the same grid current will flow through all the series connected modules. In this case, regulating the magnetizing current of all the modules using the same grid current may not be achievable. Instead, it is proposed here to use the energy stored in the filter capacitors for each module to regulate the magnetizing current. However, this regulation has to be performed on a cycle-to-cycle basis, since the energy storage within the filter capacitor is very low. At each switching cycle, only a fraction of the filter capacitor energy is used to regulate the magnetizing current such that the filter capacitor voltage will not largely deviate from its reference, and this is also accomplished by the inner control loop.

The transformer magnetizing inductance is being charged and discharged by the three phases over one switching cycle. The change of the magnetizing current after one switching cycle is given in equation (12.19). Therefore, to dynamically change the magnetizing current, the duty cycle of each phase is slightly varied over subsequent switching cycles. To increase the magnetizing current, the duty cycles of the phase(s) that tend to charge the magnetizing inductance are slightly increased while the duty cycles of the phase(s) that tend to discharge it are slightly decreased. Similarly, the magnetizing current can be reduced in an opposite manner. It should be noted that the duty cycle variation to compensate the magnetizing current will drive the filter capacitor away from its reference. However, this is acceptable as long as this deviation is within a limit.

$$\Delta I_m = \sum_{\Phi} V_{cap.\Phi} D_{\Phi} T_S ; \left(\Phi = A, B, C\right) \tag{12.19}$$

To elaborate on the principle of regulating I_m, Fig. 12.16 shows the method of increasing I_m within one switching cycle. Assuming at this time instant, the current and voltage of phases A and B have the same polarity, while for phase C they are different. This means,

within this switching cycle, phases A and B tend to charge the transformer magnetizing inductance and phase C tends to discharge it. Therefore, increasing I_m can be realized through increasing the duty cycle of phase A or B, or decreasing that of phase C, or through the combination of all these three. Since compensating the magnetizing current using the energy stored within the filter capacitor will slightly change the filter capacitor voltage, to balance the three phases, it is preferred to use the energy from all three phases to regulate I_m. Fig. 12.16 shows that at the time instant t_0, the controller tries to increase I_m by ΔI_m through extending duty cycles of phases A and B, and shortening the duty cycle of phase C. As a result, all these three phase voltages will deviate from the reference, shown as the red line. This deviation is acceptable since the compensation requirement for I_m is very small. In the figure, *t(+)* denotes the active time period for a phase and *t(0)* represents the idle time period.

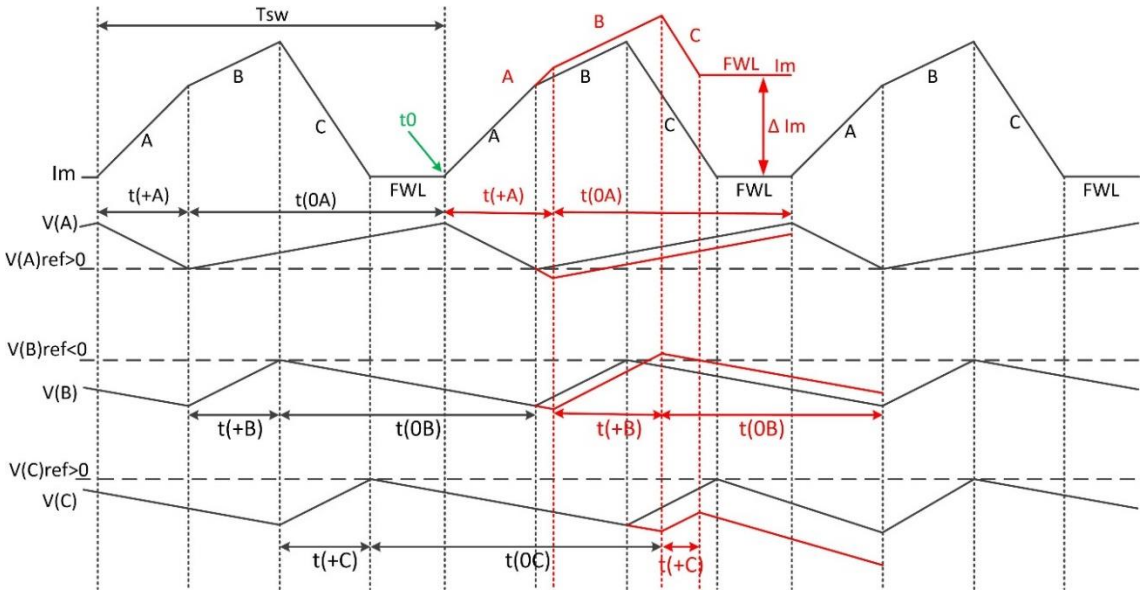


Fig. 12.16: Principle of increasing the magnetizing current within one switching cycle.

The algorithm of regulating I_m is defined as below. At the beginning of a switching cycle, the required compensation ΔI_m is calculated as equation (12.20). Then the compensation effort from each phase is determined by equation (12.21), for which the energy stored in the filter capacitors of all the three phases are used to regulate the magnetizing current. Then the

duty cycle changes to achieve this compensation is given by equation (12.22), in which $V_{cap.\phi}$ is the measured filter capacitor voltage of one phase at the beginning of each switching cycle.

$$\Delta I_m = I_m^* - I_m \tag{12.20}$$

$$\Delta I_{m.\phi} = \Delta I_m * \frac{I_\phi^*}{\sum_{\phi=A,B,C} I_\phi^*} \tag{12.21}$$

$$\Delta D_\phi = \frac{L_m}{V_{cap.\phi} T_{sw}} \Delta I_{m.\phi} \tag{12.22}$$

Complete Inner Control Loop

The inner control loop determines the duty cycle of each phase to achieve filter capacitor voltage control and magnetizing current regulation for each switching cycle. At the beginning of each switching cycle, the duty cycle for regulating the filter capacitor voltage is calculated as equations (12.17) and (12.18), and a small duty cycle variation for compensating the magnetizing current is calculated as equations (12.20) – (12.22). Finally, the desired duty cycle for bridge operation is given by equation (12.23). Fig. 12.17 shows the complete inner loop controller block diagram for phase A, and the same one applies to phases B and C.

$$D_A = D_A^{'} + \Delta D_A \tag{12.23}$$

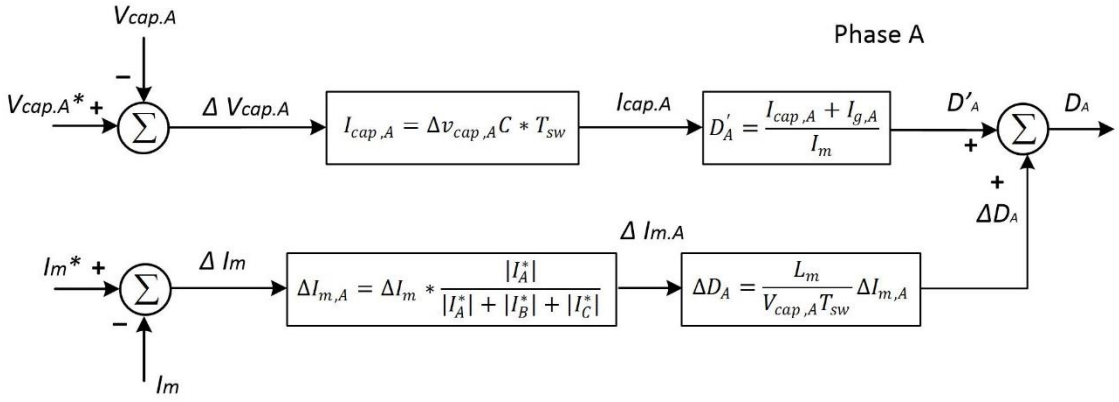


Fig. 12.17: Inner control loop for the series-stacked converter.

12.5.2. Outer Control Loop

The outer loop controller provides the capacitor voltage reference for the inner loop and is responsible in controlling the grid current and regulating the magnetizing current of all

four modules in steady state. However, the control strategy for regulating the filter capacitor voltage defined in the previous section generates third-order harmonics on the capacitor voltage, which will result in third-order harmonics on the grid current. This will also need to be addressed by refining the outer loop controller.

The outer loop indirectly regulates the grid current by controlling the filter capacitor voltage, which is analogous to the indirect current control of voltage source converters. In this control scheme, the *q* component of the grid current reference determines the reactive power to be injected into the grid, and the *d* component corresponds to the active power flow. Meanwhile, a decoupled current control loop is required to remove the i_q and i_d coupling effect caused by the filter inductor. For the series-stacked converter system, i_d component is used to regulate the magnetizing current of all four modules on a steady-state basis. The required i_d component that needs to be injected corresponds to the error between the summation of I_m of all four modules and the summation of I_m references, i.e., the overall system's compensation requirement for the magnetizing current. The voltage reference for all the four modules is calculated in the outer loop, divided by four to get the reference for each module, and then passed to the inner loop controller.

For the inner loop controller defined in the previous section, the filter capacitor voltage waveforms are enveloped by the reference voltage, as shown in Fig. 12.15. This means that the resulted filter capacitor voltage fundamental component does not equal to the reference. The difference between them causes errors on both the voltage amplitude and phase angle, which will affect the active and reactive power flow. These steady state errors of the active and reactive power can be automatically compensated for by the outer loop. The voltage reference generated by the outer loop will vary accordingly to compensate for these errors. However, the above difference also causes low order harmonics on the filter capacitor voltage. Fig. 12.18 plots the harmonics spectrum of the filter capacitor voltage using the proposed deadbeat control strategy. It shows that except for the harmonics order at the switching frequency, the filter capacitor voltage also exhibits relatively high third-order

harmonics. Simulation results also show significant 3rd harmonics on the grid current due to the filter capacitor voltage harmonics. These 3rd harmonics can be suppressed using a series connected 3rd order passive filter, while it will increase the system cost. Besides, the inductors and capacitors of the filter cannot be exactly tuned at this frequency. A more practical approach to eliminate the harmonics is by refining the controller.

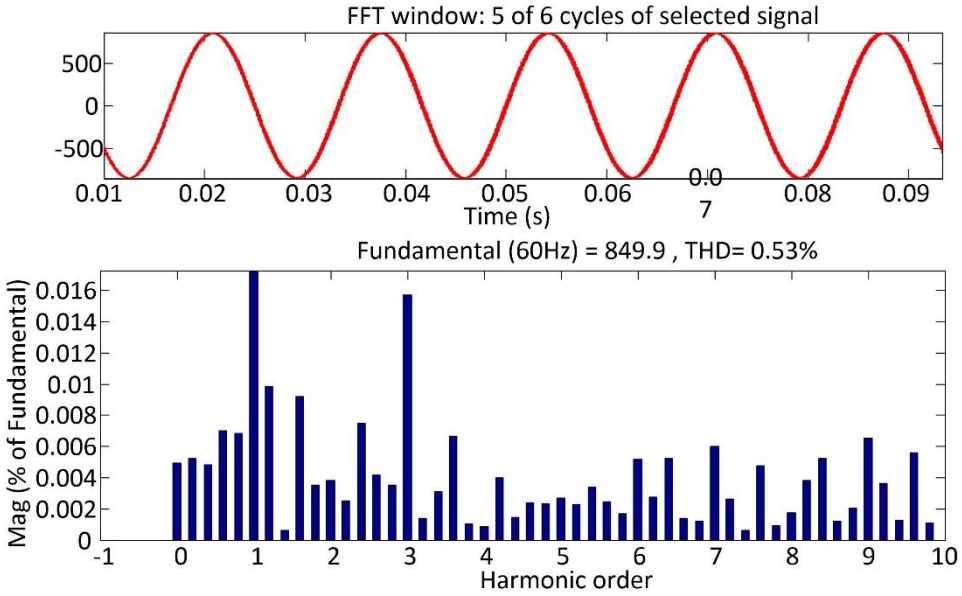


Fig. 12.18: Harmonics spectrum of the filter capacitor voltage when using the proposed deadbeat control strategy.

The stacked converter indirectly controls the grid current by controlling the filter capacitor voltage. Therefore, the filter capacitor can be modeled as a controllable voltage source. The equivalent circuit for each phase on the ac side is shown in Fig. 12.19, in which $V_{cap.f}$ is the fundamental voltage of the filter capacitor, and $V_{cap.h}$ is the harmonics component. These two components are generated from the filter capacitor voltage control scheme defined in the previous section with a voltage reference of V_{cap}^{*}. The presence of $V_{cap.h}$ generates a harmonic current $I_{g.h}$ flowing through the filter inductor. One approach to remove it is by adding another harmonics voltage component with an opposite phase to cancel the effect of $V_{cap.h}$, which is $-V_{h}^{*}$ as shown in Fig. 12.19. Since the impedance of the filter inductor for the fundamental component is very low, the corresponding voltage drop across the inductor can be neglected. Then the harmonic voltage of the filter capacitor is

approximately equal to the filter inductor voltage, as expressed in equation (12.24). Therefore, the added harmonics voltage reference is given by equation (12.25), in which the coefficient *K* determines the harmonics cancelling effort and should be chosen properly to achieve the lowest harmonics on the grid current. Since only the 3rd harmonics is dominant, the controller will only filter out these harmonics. The complete outer loop controller with active harmonics cancellation is shown in Fig. 12.20.

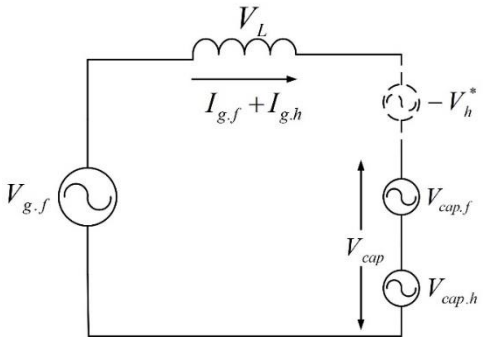


Fig. 12.19: Equivalent circuit for each phase on the ac side.

$$V_{cap.h} = V_{cap} - V_{cap.f} \approx V_{cap} - V_{g.f} = V_L \tag{12.24}$$

$$V_h^* = K * V_{cap.h} = K * V_L \tag{12.25}$$

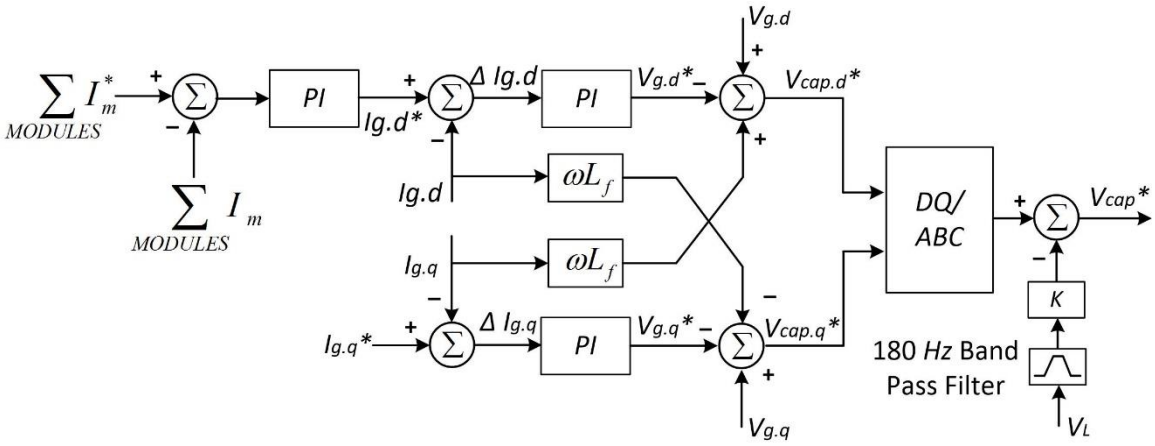


Fig. 12.20: Outer control loop for the series-stacked converter.

12.5.3. Complete Controller for the Stacked Converter

Fig. 12.21 shows the entire control block diagram for the stacked VAr Compensator. The outer loop determines the filter capacitor voltage reference based on the indirect grid current control and the overall transformer magnetizing current compensation requirement

as well as the harmonics cancelling effect, all of which has been covered in section 12.5.2. Then this capacitor voltage reference is divided by the number of modules to get the filter capacitor voltage reference for each module. The inner loop controller then uses the deadbeat controller described in section 12.5.1 to regulate the filter capacitor voltages and the transformer magnetizing current on a switching cycle-to-cycle basis for each module. Although only the control strategy for the stacked dynamic VAr compensator is presented, the same principle applies to all the other topologies that have been presented in chapter 6.

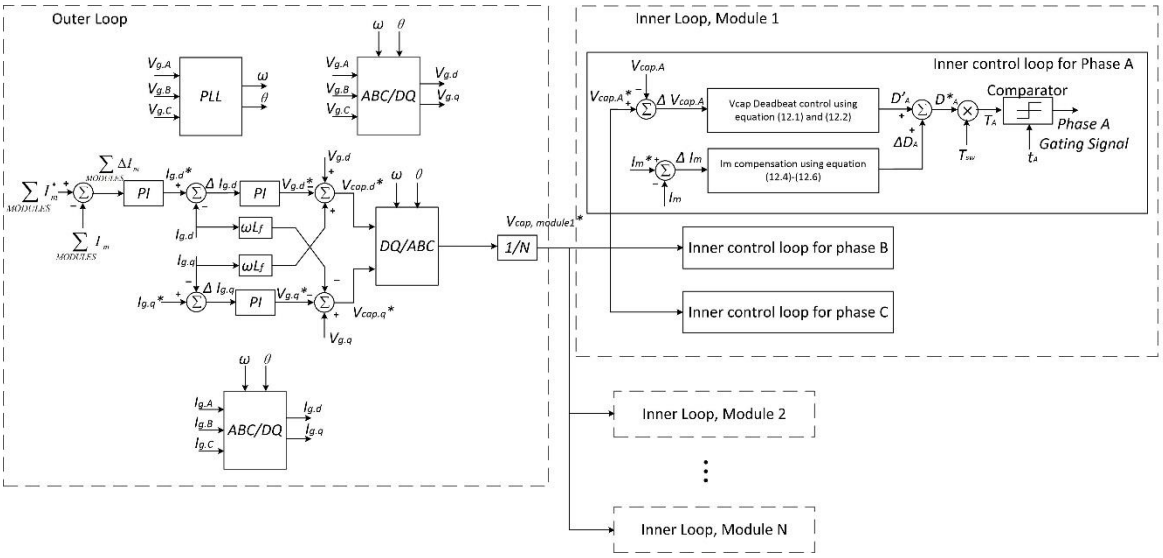
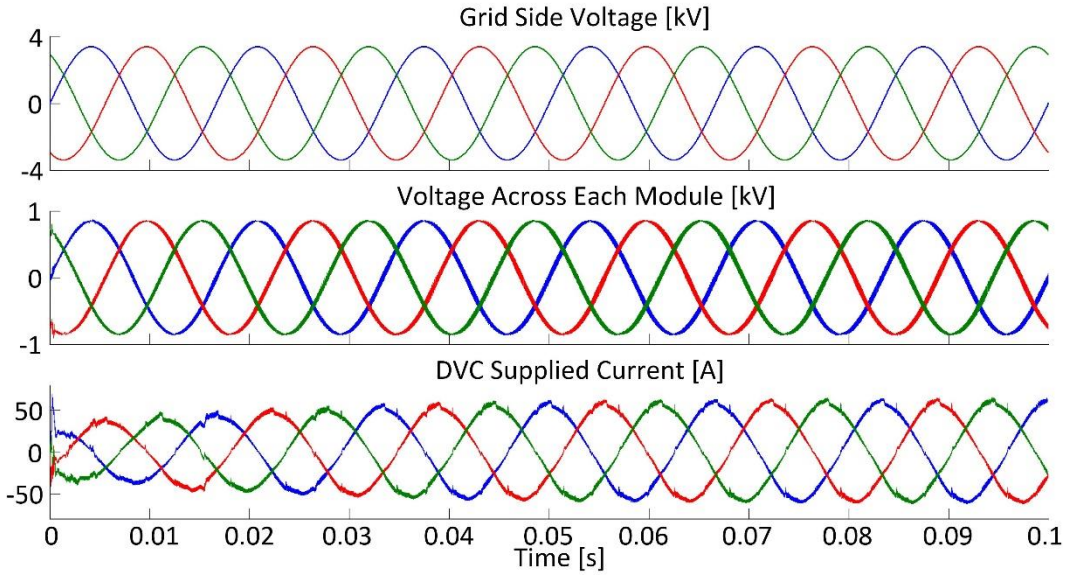


Fig. 12.21: Complete control diagram for the series-stacked converter.

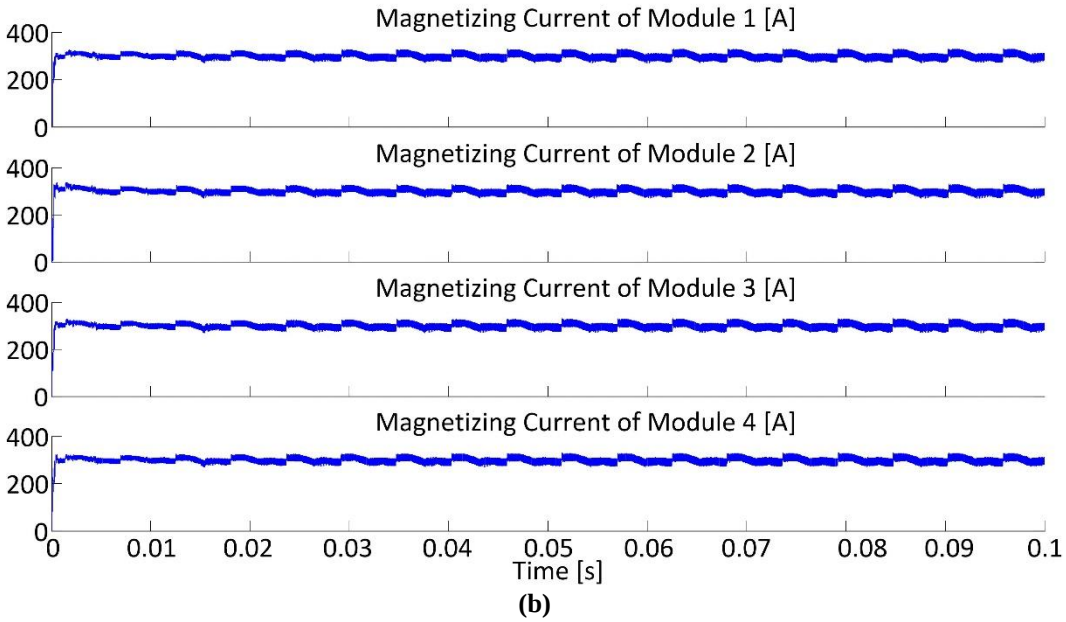
12.6. Simulation Results

To verify the control strategy, the stacked dynamic VAr compensator that is configured with four series-connected modules is simulated. The stacked converter is connected to a three-phase ac system with a line-to-line RMS voltage of 4160 V, through a three-phase lumped filter inductor of 300 μH. Each module has a filter capacitance of 20 μF on each phase. The high-frequency transformer of each module has a magnetizing inductance of 150 μH. Each module is controlled to equally share the ac voltage, and the transformer magnetizing current is regulated at 300 A. The stacked system is required to inject a total reactive power of 300 kVAr, 75 kVAr from each module. The converter is running at a switching frequency of 15 kHz. Adjacent modules are running with a phase shift of 1/4 switching cycle, aimed to reduce the switching harmonics on the grid current. Fig. 12.22 (a)

shows the waveforms of the grid side voltage (line-to-neutral), voltage across each module, and the converter supplied current. Fig. 12.22 (b) shows the magnetizing currents of all the four modules. Waveforms show that, with the proposed controller, equal voltage sharing is achieved for all the stacked modules, and all the magnetizing currents are well regulated at the references. Meanwhile, the stacked converter provides the desired reactive power with low harmonics on the current.



(a)



(b)

Fig. 12.22: Simulation waveforms to show stable operation using the proposed control strategy for the stacked converter: a) waveforms of grid side voltage, converter side voltage, and converter supplied current, and (b) magnetizing current of four modules.

12.7. Conclusions

The modularity of the S4T allows it to be series and/or parallel stacked to reach medium voltage and high power levels. However, series stacking converters faces great challenges in equally sharing the voltage and stabilizing the converter operation. Using the conventional charge control modulation method to control the stacked system leads to unstable operation. This chapter uses the modular soft-switching dynamic VAr compensator as an example to demonstrate the operation of the stacked converters. Description of the modular soft-switching dynamic VAr compensator topology is first given. Simulation results shows that the conventional charge control for the single module cannot be directly used to control the stacked converter. As a result, a robust multi-loop control strategy is developed. The outer loop of the proposed controller determines the filter capacitor voltage reference based on the indirect grid current control and the overall transformer magnetizing current compensation requirement on the steady-state basis, along with active harmonics filtering functionality. The inner loop uses the proposed deadbeat controller to regulate the filter capacitor voltages and the transformer magnetizing current on a switching cycle-to-cycle basis for each module. Simulation results for the series-stacked dynamic VAr compensator show the efficacy of the proposed control strategy.

CHAPTER 13: CONCLUSIONS AND RECOMMENDATIONS FOR FUTURE WORK

13.1. Conclusions

This dissertation has presented soft-switching topologies to implement solid-state transformers. The proposed topology has a simple and symmetrical architecture, minimal device and component count in the power flow path, with small-rated auxiliary components that enable the soft switching property. Two topologies were presented, a zero-current-switching solid state transformer in which all devices are switched under ZCS conditions and the converter can be designed with half-controlled devices such as SCRs, and a zero-voltage-switching version in which all devices are switched under ZVS conditions. The ZVS topology exhibits simpler operating principles, controllable *dv/dt* rates, no device reverse recovery issue, and higher efficiency. Thus the ZVS topology was selected as the design and analysis target.

Unlike the DAB converter, the small-rated auxiliary resonant circuit helps the S4T realize ZVS conditions for all its main devices over the entire load range, and features controlled *dv/dt* and *di/dt* rates. Further, it can realize dc, single- or multi-phase ac on the input/output at arbitrary frequencies and power factors with sinusoidal voltages and low EMI. Various topology variations have been shown as dc/single-phase ac to dc/single-phase ac, dc/single-phase ac to three-phase ac, dc/single-phase ac to three-phase four-wire ac, and three-phase three-wire ac to three-phase four-wire ac, as well as multi-terminal topologies, acting as a universal converter with the same operating principle to achieve ZVS conditions. It should be noted that the proposed auxiliary resonant converter can be used for any type of current source converters to provide ZVS conditions for their devices.

The converter shows simple control and benign shut down under fault and failure modes, and is relatively insensitive to key parameters such as transformer leakage inductance. The converter operating principle is simple in that the ZVS transition occurs automatically

without the need for precisely controlling devices at specified time instants, and it retains the fixed-frequency PWM capability. Cycle-by-cycle charge modulation control allows compact transformer design while maintaining high-quality voltage regulation on the input and the output. In addition, the S4T offers several very important features that conventional VSIs and CSIs do not have: 1) the converter does not require any intentionally added dead time or overlap time for device transitions; 2) there is no severe inrush current when devices on the same leg are turned on simultaneously by fault; 3) devices do not suffer from catastrophic voltage stress when interrupting the inductive current flowing path; 4) reduced *dv/dt* rate significantly mitigates all the hard-switching issues such as resonance, spikes, noise, and EMI; 5) protection of the devices is extremely easy due to the low *dv/dt* rate.

The converter also has fast dynamic response under load transients, start-up, and shut-down because of its low inertia property. The converter can finish the transient operation within several switching cycles, causing no delay for the load demands. Start-up and shut-down procedures also occur in a soft manner, without any inrush current generated.

The high-frequency transformer is a key element for the solid state transformer. Detailed design procedures were presented to achieve low core loss and low copper loss. In addition, the dc flux feature of the S4T presents the feasibility of using permanent magnets to provide a pre-biased dc flux such that the energy storage capability of the magnetic cores can be significantly improved. This dissertation presented a hybrid transformer design methodology to integrate permanent magnets and magnetic cores, which can reduce the core volume by over 50%.

Besides the proposed S4T converter for active power transfer, this dissertation also presented potential applications for the S4T, including two soft-switching dynamic VAr compensator topologies that are derived from the S4T, one based on a conventional three-phase current source inverter (CSI) and the other one configured with three individual full-bridge CSIs coupled through an inductor or a high-frequency transformer. The latter topology can potentially be scaled to higher voltage levels by stacking the modules in series.

Similar to the S4T, both topologies achieve full range of ZVS conditions for all the main devices and avoid using electrolytic capacitors for temporary energy storage, which enhances the reliability and avoids inrush current.

Series and/or parallel stacking the S4T modules can reach medium-voltage high-power levels, thanks to the modularity of the S4T converter. However, the low inertia and strong coupling properties impose challenges of stabilizing the stacked system. This dissertation also presented a robust multi-loop control strategy for the stacked converter system, whose efficacy is verified through simulation. The proposed control strategy can be extended to control any type of series-stacked current source converters.

Finally, experimental validation was obtained with a proof of concept prototype rated at 208 volts/ 10 kVA. A detailed comparison was done among the proposed S4T, the conventional multi-stage SST, and the low-frequency transformer with a rectifier and an inverter, showing the S4T's prominent advantages of low component count, full SST functionalities, and high efficiency.

13.2. Summary of Contributions

As a summary, this research has achieved the following:

- Proposed a soft-switching solid state transformer topology that has the features of minimal two-stage conversion with low device count, soft-switching features for all devices at full range, four-quadrant operation with voltage buck and boost capabilities, arbitrary power factors and frequencies for the input and the output, eliminating the dc energy storage capacitors to avoid inrush current and improve reliability, fast dynamic response to transients, ease of control to achieve soft-switching operation, flexible configurations for two- or multi-terminal dc, single- and multi-phase ac systems such that acting as a universal converter, and

modular design to scale to medium voltage and high power levels through series and/or parallel stacking the converter modules.

- The proposed auxiliary resonant circuit for the S4T can be used for any type of current source converter to achieve zero-voltage-switching.
- Presented the S4T operating principle, control, detailed analysis, leakage impact, and auxiliary resonant circuit.
- Presented the detailed power stage design and the auxiliary resonant circuit design.
- Presented the high-frequency transformer design that achieves compact size, low loss, low leakage, and high insulation levels.
- Proposed a hybrid high-frequency transformer design methodology that integrates permanent magnets and magnetics to reduce the transformer core volume.
- Presented two soft-switching Dynamic VAr compensator topologies that are derived from the S4T.
- Experimentally demonstrated the functionality of the proposed S4T with a 208 V / 10 kVA unit. Comparison with other topologies was also given.
- Proposed a robust control methodology for the series-stacked converter modules such that the S4T can be scaled up to medium voltage level.

13.3. Recommendations for Future Work

13.3.1. Experimental Demonstration on a High-Power Level

Preliminary study shows that the proposed S4T can reach an efficiency of over 97% when designing at 480 V / 50 kVA, even with low cost Silicon devices. It should be noted that a higher voltage rated unit can exhibit even higher efficiency, since the S4T loss is independent of the voltage levels. Till now, the back-to-back solution could not reach this efficiency due to the multi-stage conversion. Low converter loss also helps to achieve a much

more compact converter design because of the low thermal burden on the cooling system. Therefore, it is desirable to develop a higher-power-rated S4T unit with compact size and high efficiency.

13.3.2. Design with Reverse-Blocking IGBTs

Using reverse-blocking IGBTs can help achieve a compact design and low conduction loss. RB-IGBT usually shows higher switching and reverse recovery losses compared to conventional two-quadrant devices. However, since all the S4T devices are operated under ZVS conditions and the reverse recovery is not a concern, designing a S4T unit with RB-IGBTs should be able to achieve better performance.

13.3.3. Low-Cost High-Frequency Transformer Design

To achieve low loss for the high-frequency transformer, the nano-crystalline material is used to design the core. However, the cost of such material is seven to ten times greater than that of the amorphous-iron and ferrite. The ferrite shows comparable core loss as the nano-crystalline, but with a much lower saturation flux density. A hybrid transformer methodology has been explored, resulting in significant improvement in the energy storage capability of magnetic cores by using permanent magnets. Therefore, it is suggested to use this proposed method to design a ferrite-based transformer, which exhibits low cost and compact size, and thus helps to meet the low-cost target for some applications, such as motor drives.

13.3.4. Functional Demonstration for DC, Single-Phase AC, and Multi-Port

The S4T shows a universal power conversion capability, and topologies for dc, single- or multi-phase ac, and multi-terminal conversion have been presented. All the topologies work under the same operating principle while maintaining ZVS conditions for all the main devices. Experimental validation of these varied topologies is helpful in the exploration of more applications such as renewable integration and energy storage.

13.3.5. Motor Drive Application

The S4T can be operated with arbitrary power factors and frequencies for the input and the output, along with the capability of four-quadrant operation. In addition, direct control of the current allows the feasibility of fast regulating the flux of the motor. It is suggested to load the S4T with a motor to demonstrate four-quadrant operations.

13.3.6. Demonstration of Medium-Voltage Operation

In this research, the control strategy for the series-stacked S4T converter has been developed to robustly stabilize the series-stacked converter system, which is desired for medium-voltage applications. Because of the universal power conversion capability of the S4T, it can seamlessly integrate all types of sources and loads such as PV, wind, battery, and motors in utilities. The emerging high-voltage SiC MOSFETs and IGBTs that are rated over 10 kV also make the converter design at the utility voltage level to be feasible. In addition, the soft-switching feature of the S4T significantly mitigates the problems associated with high *di/dt* and *dv/dt* rates for the SiC devices. It is thus beneficial to explore the S4T converter design for utility applications. Beyond that, the high-frequency transformer design that needs to withstand the over 100 kV basic-insulation-level (BIL) while still maintaining acceptable leakage should be explored.

APPENDIX A: BILL OF MATERIAL FOR THE S4T CONVERTER

Item	Quant.	Ref. Des.	Value	Description	Manufacturer	Manufacturer P/N
1	7	Sap, Sbp, Scp, San, Sbn, Scn, Sr	IGBT / MOSFET	IGBT 1200V 100A 535W TO247 or MOSFET N-CH 1200V 90A TO-247	ON Semiconductor or Cree	NGTB50N120FL2WG or C2M0025120D
2	8	Dap, Dbp, Dcp, Dan, Dbn, Dcn, Dr, Dlk	Diode	DIODE SCHOTT 1.2KV 60A TO247-2	Global Power Technologies	GDP60Z120E
3	2	Ds1, Ds2	Diode	DIODE GEN PURP 1.6KV 1A DO204AL	Vishay Semiconductor	GP10Y-E3/54
4	7	Dgsap, Dgsbp, Dgscp, Dgsan, Dgsbn, Dgscn, Dgsr	TVS diode	TVS DIODE 15VWM 31VC SOD323	Littelfuse	SD15C-01FTG
5	6	Cab1, Cab2, Cbc1, Cbc2, Cca1, Cca2	30 µF	30µF Film Capacitor 350V 875V Polypropylene	EPCOS	B32798G8306K
6	6	Cab3, Cab4, Cbc3, Cbc4, Cca3, Cca4	2.2 µF	2.2µF Film Capacitor 400V 1050V	EPCOS	B32794D4225K
7	4	Cr1, Cr2, Cr3, Cr4	0.1 µF	0.1µF Film Capacitor 650V 1600V	Kemet	PHE450RF6100JR06L2
8	7	Cgsap, Cgsbp, Cgscp, Cgsan, Cgsbn, Cgscn, Cgsr	10 nF	10000pF 100V Ceramic Capacitor X7R 1210	Kemet	C1210C103K1RACTU
9	1	Cs	0.1 µF	0.1µF Film Capacitor 300V 1500V	EPCOS	B32023A3104M
10	1	Csd	1.5 nF	1500pF Film Capacitor 600V 1600V	EPCOS	B32671L1152J
11	3	RUab, RUbc, RUca	50 k	RES 50K OHM 50W 1% TO220	Riedon	PF2205-50KF1
12	1	Rs	40 k	RES 40K OHM 25W 1% TO220	Caddock Electronics	MP925-40.0K-1%
13	1	Rsd	62	RES 62 OHM 2W 5% AXIAL	Vishay BC Components	PR02000206209JR500
14	3	Uab, Ubc, Uca	3	TRANSDUCR VOLTAG CLOSE LOOP 10MA	LEM USA	LV 25-P
15	23	TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP11, TP12, TP13, TP14, TP15, TP16, TP17, TP18, TP19, TP20, TP21, TP22, TP23	Test point	TEST POINT PC MULTI PURPOSE RED	Keystone Electronics	5010
16	1	Lr	Inductor	Resonant Inductor	–	Custom designed
17	2	M1, M2	MOV	VARISTOR 620V 10KA DISC 20MM	Littelfuse	V20E385P
18	1	JXFMR	Terminal block	CONN TERM BLOCK PWR 15MM 4POS	TE Connectivity	1986713-4
19	1	JCap_VM	Terminal block	TERM BLOCK 3POS SIDE ENTRY 10MM	TE Connectivity	282858-3

20	3	JUab, JUbc, JUca	4-pin header	4 Positions Header, Unshrouded Connector	TE Connectivity	3-641213-4
21	3	Ja, Jb, Jc	Terminal block	CONN TERM BLK HI CURRENT 1POS	Phoenix Contact	1704020
22	7	JGap, JGbp, JGcp, JGan, JGbn, JGcn, JGr	Gate driver board	MOSFET, Bridge Drivers Evaluation Board	Cree	CRD-001
23	3	CT	Current transducer for line current	SENSOR CURRENT HALL 100A AC/DC	LEM USA	HAS 100-S
24	1	CT	Current transducer for dc current	SENSOR CURRENT HALL 500A AC/DC	LEM USA	LF 505-S
25	1	Filter inductor	Filter	Three-phase line inductor 220 μH, 46.2 A	AUTOMATIONDIRECT	LR-2015
26	3	Fuse	Fuse	Fuses 480VAC/300VDC 60A	Bussmann	SC-60
27	3	Fuse holder	Fuse holder	Fuse holder 1P class G	Bussmann	G30060-1CR
28	3	Resistor	Damping resistor	RES CHAS MNT 3 OHM 1% 50W	Stackpole Electronics	KAL50FB3R00
29	1	Heatsink	Heatsink	Bonded fin heat sinks with fans	C&H Technology	CH5117
30	15	Ceramic tile	Ceramic tile for cooling devices	Aluminum oxide wafers	Fischer Elektronik	AOS2182471
31	1	AC/DC converter	AC/DC converter	AC/DC CONVERTER 9V 15W	XP Power	ECL15US09-S

APPENDIX B: PUBLICATIONS AND PATENTS

Journal Papers:

[1] H. Chen, A. Prasai, and D. Divan, "Dyna-C: A Minimal Topology for Bi-Directional Solid State Transformers," *IEEE Transactions on Power Electronics*, in press.

[2] H. Chen, A. Prasai, R. Moghe, and K. Chintakrinda, and D. Divan, "A 50 kVA Three-phase Solid-State Transformer Based on the Minimal Topology: Dyna-C," *IEEE Transactions on Power Electronics*, vol. 31, no. 12, pp. 8126-8137, Dec. 2016.

[3] H. Chen, A. Prasai, and D. Divan, "A Modular Isolated Topology for Instantaneous Reactive Power Compensation," *IEEE Transactions on Power Electronics*, in press.

[4] H. Chen, A. Iyer, R. Harley, and D. Divan, "Dynamic Grid Power Routing using Controllable Network Transformers (CNT) with Decoupled Closed-Loop Controller," *IEEE Transactions on Industry Applications*, vol. 51, no. 3, pp. 2361-2372, May 2015.

Conference Papers:

[1] H. Chen, and D. Divan, "A Soft-Switching Dynamic VAr Compensator," in *IEEE Applied Power Electronics Conference (APEC)*, 2017.

[2] H. Chen, and D. Divan, "High-Frequency Transformer Design for the Soft-Switching Solid State Transformer (S4T)," in *IEEE Applied Power Electronics Conference (APEC)*, 2017.

[3] H. Chen, and D. Divan, "Soft-Switching Solid-State Transformer (S4T)," in *IEEE Energy Conversion Congress and Exposition (ECCE)*, 2016.

[4] H. Chen, R.P. Kandula, A. Prasai, J. Schatz, and D. Divan, "Flexible Transformers for Distribution Grid Control," in *IEEE Energy Conversion Congress and Exposition (ECCE)*, 2016.

[5] R.P. Kandula, H. Chen, A. Prasai, F. Lambert, J. Schatz, and D. Divan, "Field Upgradable Transformer: A Fractionally-Rated Voltage Regulator for the Distribution System," in *IEEE Energy Conversion Congress and Exposition (ECCE)*, 2016.

[6] R.P. Kandula, H. Chen, A. Prasai, F. lambert, T. Heidel, C. Schauder, J. Schatz, T. Powell, D. Divan, "Field Test Results for a 12.47 kV 3-phase 1 MVA Power Router," in *IEEE Energy Conversion Congress and Exposition (ECCE)*, 2016.

[7] H. Chen, A. Prasai, and D. Divan, "An Isolated Topology for Reactive Power Compensation with a Modularized Dynamic-Current Building-Block," in *IEEE Applied Power Electronics Conference (APEC)*, 2016, pp. 1437-1442.

[8] H. Chen, and D. Divan, "High Speed Switching Issues of High Power Rated Silicon-Carbide Devices and the Mitigation Methods," in *IEEE Energy Conversion Congress and Exposition (ECCE)*, 2015, pp. 2254-2260

[9] R.P. Kandula, A. Prasai, H. Chen, R. Mayor, F. Lambert, T. Heidel, C. Schauder, and D. Divan, "Design Considerations and Experimental Results for a 12.47-kV 3-Phase 1 MVA Power Router," in *IEEE Energy Conversion Congress and Exposition (ECCE)*, 2015, pp. 5000-5007.

[10] H. Chen, A. Iyer, R. Harley, and D. Divan, "Decoupled Closed-Loop Power Flow Control for the Controllable Network Transformers (CNT)," in *IEEE Applied Power Electronics Conference (APEC)*, 2014, pp. 2148-2155.

[11] H. Chen, A. Prasai, and D. Divan, "Stacked Modular Isolated Dynamic Current Source Converters for Medium Voltage Applications," in *IEEE Applied Power Electronics Conference (APEC)*, 2014, pp. 2278-2285.

[12] A. Prasai, H. Chen, and D. Divan, "Dyna-C: A Topology for a Bi-directional Solid-State Transformer," in *IEEE Applied Power Electronics Conference (APEC)*, 2014, pp. 2278-2285.

[13] A. Prasai, H. Chen, R. Moghe, Z. Wolanski, K. Chintakrinda, A. Zhou, J.C. Llambes, and D. Divan, "Dyna-C: Experimental Results for a 50 kVA 3-Phase to 3-Phase Solid State Transformer," in *IEEE Applied Power Electronics Conference (APEC)*, 2014, pp. 2271-2277.

Patent:

[1] H. Chen and D. Divan, "Soft Switching Solid State Transformer," U.S. Patent Filed with USPTO.

REFERENCES

[1] "Large power transformers and the U. S. electric grid," *Report of Office of Electricity Delivery and Energy Reliability*, 2014.

[2] "2014 renewable energy data book," *Report of U.S. Department of Energy*, 2014.

[3] "Solid state transformer market by product (power, traction, & distribution), application (alternative power generation, electric vehicle charging stations, & others), & geography (North America, Europe, Asia-Pacific, & RoW) – forecast to 2020," *Report by marketsnadmarkets.com*, 2015.

[4] W. McMurray, "Power converter circuits having a high frequency link," U. S. Patent 3,581,212, 1970.

[5] R.W.A.A. De Doncker, D.M. Divan, and M.H. Kheraluwala, "A three-phase soft-switched high-power-density DC/DC converter for high-power applications," *IEEE Transactions on Industry Applications*, vol. 27, no. 1, pp. 63-73, January 1991.

[6] J. Everts, J. Van den Keybus, F. Krismer, J. Driesen, and J.W. Kolar, "Switching control strategy for full ZVS soft-switching operation of a dual active bridge AC/DC converter," in *IEEE Applied Power Electronics Conference and Exposition*, 2012, pp. 1048-1055.

[7] R. King, and T.A. Stuart, "A normalized model for the half-bridge series resonant converter," *IEEE Transactions on Aerospace and Electronic Systems*, vol. AES-17, no. 2, pp. 190-198, March 1981.

[8] R.J.King, and T.A. Stuart, "Modeling the full-bridge series-resonant power converter," *IEEE Transactions on Aerospace and Electronic Systems*, vol. AES-18, no. 4, pp. 449-459, July 1982.

[9] A.F. Witulski, and R.W. Erickson, "Design of the series resonant converter for minimum component stress," *IEEE Transactions on Aerospace and Electronic Systems*, vol. AES-22, no. 4, pp. 356-363, July 1986.

[10] V.T. Ranganathan, P.D. Ziogas, and Victor R. Stefanovic, "A regulated DC-DC voltage source converter using a high frequency link," *IEEE Transactions on Industry Applications*, vol. IA-18, no. 3, pp. 279-287, May 1982.

[11] M.C.W. Lindmark, "Switch-mode power supply", U. S. Patent 4,097,773, June 27, 1978.

[12] Y.–G. Kang, and A.K. Upadhyay, "Analysis and design of a half-bridge parallel resonant converter," *IEEE Transactions on Power Electronics*, vol. 3, no. 3, pp. 254-265, July 1988.

[13] R.L. Steigerwald, "A comparison of half-bridge resonant converter topologies," *IEEE Transactions on Power Electronics*, vol. 3, no. 2, pp. 174-182, April 1988.

[14] R.L. Steigerwald, "High-frequency resonant transistor DC-DC converters," *IEEE Transactions on Industrial Electronics*, vol. IE-31, no. 2, pp. 181-191, May 1984.

[15] A.K.S. Bhat, "Analysis and design of a series-parallel resonant converter," *IEEE Transactions on Power Electronics*, vol. 8, no. 1, pp. 1-11, January 1993.

[16] B. Yang, F.C. Lee, A.J. Zhang, and G. Huang, "LLC resonant converter for front end DC/DC conversion," in *IEEE Applied Power Electronics Conference and Exposition*, 2002, pp. 1108-1112.

[17] G. Pledl, M. Tauer, and D. Buecherl, "Theory of operation, design procedure and simulation of a bidirectional LLC resonant converter for vehicular applications," in *IEEE Vehicle Power and Propulsion Conference*, 2010, pp. 1-5.

[18] C. Zhao, D. Dujic, A. Mester, J.K. Steinke, M. Weiss, S. Lewdeni-Schmid, T. Chaudhuri, and P. Stefanutti, "Power electronic traction transformer-medium voltage prototype," *IEEE Transactions on Industrial Electronics*, vol. 61, no. 7, pp. 3257-3268, July 2014.

[19] I. Yamato, N. Tokunaga, Y. Matsuda, H. Amano, and Y. Suzuki, "New conversion system for UPS using high frequency link," in *IEEE Annual Power Electronics Specialists Conference*, 1988, pp. 658-663.

[20] J. Garcia, M.A. Dalla-Costa, A. Kirsten, D. Gacio, and P. Quintana, "Study of a flyback-based stage as grid interface topology for micro-generation applications," in *IEEE International Power Electronics and Motion Control Conference*, 2012, pp. LS7a.2-1-LS7a.2-6.

[21] J. Garcia, M.A. Dalla-Costa, A.L. Kirsten, D. Gacio, and A.J. Calleja, "A novel flyback-based input PFC stage for electronic ballasts in lighting applications," *IEEE Transactions on Industry Applications*, vol. 49, no. 2, pp. 769-777, March 2013.

[22] M.F. de Melo, A.L. Kirsten, M.A. Dalla Costa, J. Garcia, and P.J. Quintana, "Bidirectional flyback converter connected to the grid and applied to a distributed microgeneration and street lighting system," in *IEEE Industry Applications Society Annual Meeting*, 2014, pp. 1-6.

[23] A.L. Kirsten, T.B. Marchesan, M.A. Dalla Costa, and R.N. do Prado, "Resonant technique for bidirectional flyback converter," *Electronics Letters*, vol. 45, no. 25, pp. 1345-1346, December 2009.

[24] K. Vangen, T. Melaa, and A.K. Adnanes, "Soft-switched high-frequency, high power DC/AC converter with IGBT," in *IEEE Power Electronics Specialists Conference*, 1992, pp. 26-33.

[25] H.A. Toliyat, A. Balakrishnan, M. Amirabadi, and W. Alexander, "Soft switched ac-link AC/AC and AC/DC buck-boost converter," in *IEEE Power Electronics Specialists Conference,* 2008, pp. 4168-4176.

[26] M. Amirabadi, H.A. Toliyat, and W.C. Alexander, "Single-phase soft-switching AC-link buck-boost converter," in *Applied Power Electronics Conference and Exposition,* 2014, pp. 2192-2199.

[27] D. Divan, A. Prasai, and H. Chen, "Isolated dynamic current converters," U.S. Patent US 9,065,321 B2, Aug. 8, 2013.

[28] A. Prasai, H. Chen, and D. Divan, "Dyna-C: a topology for a bi-directional solid-state transformer," in *IEEE Applied Power Electronics Conference and Exposition*, 2014, pp. 1219-1226.

[29] A. Prasai, H. Chen, R. Moghe, Z. Wolanski, K. Chintakrinda, A. Zhou, J.C. Llambes, and D. Divan, "Dyna-C: experimental results for a 50 kVA 3-phase to 3-phase solid state transformer," in *IEEE Applied Power Electronics Conference and Exposition*, 2014, pp. 2271-2277.

[30] H. Chen, A. Prasai, and D. Divan, "Stacked modular isolated dynamic current source converters for medium voltage applications," in *IEEE Applied Power Electronics Conference and Exposition,* 2014, pp. 2278-2285.

[31] W. McMurray, "Selection of snubbers and clamps to optimize the design of transistor switching converters," *IEEE Transactions on Industry Applications*, vol. IA-16, no. 4, pp. 513-523, July 1980.

[32] R. Watson, F.C. Lee, and G.C. Hua, "Utilization of an active-clamp circuit to achieve soft switching in flyback converters," *IEEE Transactions on Power Electronics*, vol. 11, no. 1, pp. 162-169, January 1996.

[33] M.N. Kheraluwala, R.W. Gascoigne, D.M. Divan, and E.D. Baumann, "Performance characterization of a high-power dual active bridge DC-to-DC converter," *IEEE Transactions on Industry Applications*, vol. 28, no. 6, pp. 1294-1301, November 1992.

[34] K. Vangen, T. Melaa, S. Bergsmark, and R. Nilsen, "Efficient high-frequency soft-switched converter with signal processor control," in *IEEE Telecommunications Energy Conference*, 1991, pp. 631-639.

[35] H. Zhou, and A.M. Khambadkone, "Hybrid modulation for dual-active-bridge bidirectional converter with extended power range for ultracapacitor application," *IEEE Transactions on Industry Applications*, vol. 45, no. 4, pp. 1434-1442, July 2009.

[36] H. Bai, and C. Mi, "Eliminate reactive power and increase system efficiency of isolated bidirectional dual-active-bridge DC-DC converters using novel dual-phase-shift control," *IEEE Transactions on Power Electronics*, vol. 23, no. 6, pp. 2905-2914, November 2008.

[37] F. Krismer, S. Round, and J.W. Kolar, "Performance optimization of a high current dual active bridge with a wide operating voltage range," in *IEEE Power Electronics Specialists Conference,* 2006, pp. 1-7.

[38] N.D. Weise, G. Castelino, K. Basu, and N. Mohan, "A single-stage dual-active-bridge-based soft switched AC-DC converter with open-loop power factor correction and other advanced features," *IEEE Transactions on Power Electronics*, vol. 29, no. 8, pp. 4007-4016, August 2014.

[39] T. Kawabata, K. Honjo, N. Sashida, K. Sanada, and M. Koyama, "High frequency link DC/AC converter with PWM cycloconverter," in *IEEE Industry Applications Society Annual Meeting*, 1990, pp. 1119-1124.

[40] M.A. Moonem, and H. Krishnaswami, "Analysis of dual active bridge based power electronics transformer as a three-phase inverter," in *IEEE Industrial Annual Conference*, 2012, pp. 238-243.

[41] I. Pecelj, S. de Haan, and J. Ferreira, "Three-phase active bridge inverter-3PAB," in *IEEE International Conference on Power Electronics, Drives and Energy Systems*, 2014, pp. 1-6.

[42] R. Limpaecher, and R. Rodriguez, "Resonant link PFN charger and modulator power supply," in *IEEE International Pulsed Power Conference*, 2007, pp. 1495-1499.

[43] M. Amirabadi, H.A. Toliyat, and W.C. Alexander, "Battery-utility interface using soft switched ac link supporting low voltage ride through," in *IEEE Energy Conversion Congress and Exposition*, 2009, pp. 2606-2613.

[44] M. Amirabadi, A. Balakrishnan, H.A. Toliyat, and W. Alexander, "Soft switched ac-link direct-connect photovoltaic inverter," in *IEEE International Conference on Sustainable Energy Technologies*, 2008, pp. 116-120.

[45] M. Amirabadi, A. Balakrishnan, H.A. Toliyat, and W.C. Alexander, "High-frequency AC-Link PV inverter," *IEEE Transactions on Industrial Electronics*, vol. 61, no. 1, pp. 281-291, January 2014.

[46] H. Cha, and P.N. Enjeti, "A new soft switching direct converter for residential fuel cell power system," in *IEEE Industry Application Conference*, 2004, pp. 1172-1177.

[47] S. Ostlund, "Reduction of transformer rated power and line current harmonics in a primary switched converter system for traction applications," in *IEEE European Conference on Power Electronics and Applications*, 1993, pp. 112-119.

[48] S. Bhattacharya, T. Zhao, G. Wang, S. Dutta, S. Baek, Y. Du, B. Parkhideh, X. Zhou, and A.Q. Huang, "Design and development of generation-I silicon based solid state transformer," in *IEEE Applied Power Electronics Conference and Exposition*, 2010, pp. 1666-1673.

[49] M. Sabahi, S.H. Hosseini, M.B. Sharifian, A.Y. Goharrizi, and G.B. Gharehpetian, "Zero-voltage switching bi-directional power electronic transformer," *IET Power Electronics*, vol. 3, no. 5, pp. 818-828, September 2010.

[50] W. McMurray, "The thyristor electronic transformer: a power converter using a high-frequency link," *IEEE Transactions on Industry and General Applications*, vol. IGA-7, no.4, pp. 451-457, July 1971.

[51] M. Kang, P.N. Enjeti, and I.J. Pitel, "Analysis and design of electronic transformers for electric power distribution system," *IEEE Transactions on Power Electronics*, vol. 14, no. 6, pp. 1133-1141, November 1999.

[52] J. Hoyo, H. Calleja, and J. Arau, "Study of an AC-AC flyback converter operating in DCM," in *IEEE Power Electronics Specialist Conference*, 2003, pp. 683-688.

[53] C. Daolian, "Novel current-mode AC/AC converters with high-frequency AC link," *IEEE Transactions on Industrial Electronics*, vol. 55, no. 1, pp. 30-37, January 2008.

[54] H. Qin, and J.W. Kimball, "Ac-ac dual active bridge converter for solid state transformer," in *IEEE Energy Conversion Congress and Exposition*, 2009, pp. 3039-3044.

[55] H. Qin, and J.W. Kimball, "Solid-state transformer architecture using AC-AC dual-active-bridge converter," *IEEE Transactions on Industrial Electronics*, vol. 60, no. 9, pp. 3720-3730, September 2013.

[56] T. Zhao, L. Yang, J. Wang, and A.Q. Huang, "270 kVA solid state transformer based on 10 kV SiC power devices," in *IEEE Electric Ship Technologies Symposium*, 2007, pp. 145-149.

[57] C. Leung, S. Dutta, S. Baek, and S. Bhattacharya, "Design considerations of high voltage and high frequency three phase transformer for solid state transformer application," in *IEEE Energy Conversion Congress and Exposition*, 2010, pp. 1551-1558.

[58] X. She, A.Q. Huang, F. Wang, and R. Burgos, "Wind energy system with integrated functions of active power transfer, reactive power compensation, and voltage conversion," *IEEE Transactions on Industrial Electronics*, vol. 60, no.10, pp. 4512-4524, October 2013.

[59] J. Shi, W. Gou, H. Yuan, T. Zhao, and A.Q. Huang, "Research on voltage and power balance control for cascaded modular solid-state transformer," *IEEE Transactions on Power Electronics*, vol. 26, no. 4, pp. 1154-1166, April 2011.

[60] H. Ju Cha, and P.N. Enjeti, "A three-phase AC/AC high-frequency link matrix converter for VSCF applications," in *IEEE Power Electronics Specialist Conference*, 2003, pp. 1971-1976.

[61] J. Kolar, and G. Ortiz, "Solid-state-transformers: key components of future traction and smart grid systems," in *Proc. of the International Power Electronics Conference*, 2014.

[62] K. Basu, A. Shahani, A.K. Sahoo, and N. Mohan, "A single-stage solid-state transformer for PWM AC drive with source-based commutation of leakage energy," *IEEE Transactions on Power Electronics*, vol. 30, no. 3, pp. 1734-1746, March 2015.

[63] M.D. Manjrekar, R. Kieferndorf, and G. Venkataramanan, "Power Electronic transformers for utility applications," in *IEEE Industry Applications Conference*, 2000, pp. 2496-2502.

[64] I. Evans, R. Limpaecher, and A. Dillon, "Power the way – a paper on AC link TM technology for 21st century HVDC transmission," in *IEEE Energy 2030 Conference*, 2008, pp. 1-11.

[65] R. Limpaecher, and E.R. Limpaecher, "Charge transfer apparatus and method therefore," U. S. Patent 9, 329, 596, 2000.

[66] H. Chen, "Close loop control system for var compensator," Varentec Report, San Jose, CA, 2011.

[67] H. Keyhani, and H.A. Toliyat, "Isolated ZVS high-frequency-link AC-AC converter with a reduced switch count," *IEEE Transactions on Power Electronics*, vol. 29, no. 8, pp. 4156-4166, August 2014.

[68] H. Keyhani, H.A. Toliyat, M. Harfman-Todorovic, R. Lai, and R. Datta, "An isolated resonant AC-Link three-phase AC-AC converter using a single HF transformer," *IEEE Transactions on Industrial Electronics*, vol. 61, no. 10, pp. 5174-5183, October 2014.

[69] S. Dutta, and S.R.S. Bhattacharya, "Integration of multi-terminal DC to DC hub architecture with solid state transformer for renewable energy integration," in *IEEE Energy Conversion Congress and Exposition*, 2013, pp. 4793-4800.

[70] M. Amirabadi, H.A. Toliyat, and W.C. Alexander, "A multiport AC link PV inverter with reduced size and weight for stand-alone application," *IEEE Transactions on Industry Applications*, vol. 49, no. 5, pp. 2217-2228, September 2013.

[71] H.S. Krishnamoorthy, D. Rana, P. Garg, P.N. Enjeti, and I.J. Pitel, "Wind turbine generator-battery energy storage utility interface converter topology with medium-frequency transformer link," *IEEE Transactions on Power Electronics*, vol. 29, no. 8, pp. 4146-4155, August 2014.

[72] J.L. Duarte, M. Hendrix, and M.G. Simoes, "Three-port bidirectional converter for hybrid fuel cell systems," *IEEE Transactions on Power Electronics*, vol. 22, no. 2, pp. 480-487, March 2007.

[73] H. Tao, J.L. Duarte, and H.A.M. Hendrix, "Three-port triple-half-bridge bidirectional converter with zero-voltage switching," *IEEE Transactions on Power Electronics*, vol. 23, no. 2, pp. 782-792, March 2008.

[74] S. Madhusoodhanan, S. Bhattacharya, and K. Hatua, "Control technique for 15 kV SiC IGBT based active front end converter of a 13.8 kV grid tied 100 kVA transformerless intelligent power substation," in *IEEE Energy Conversion Congress and Exposition*, 2013, pp. 4697-4704.

[75] S. Falcones, X. Mao, and R. Ayyanar, "Topology comparison for solid state transformer implementation," in *IEEE PES General Meeting*, 2010, pp. 1-8.

[76] J.W. Kolar, and J. Huber, "Solid-state transformer – key design challenges, applicability, and future concepts," Professional Seminar in *IEEE Applied Power Electronics Conference and Exposition*, 2016.

[77] K.D.T. Ngo, "Topology and analysis in pwm inversion, rectification and cycloconversion," Ph.D. dissertation, California Institute of Technology, May 1984.

[78] A. Lindemann, "A new IGBT with reverse blocking capability," *IXYS Application Note IXAN0049*, 2001.

[79] A. De, S. Roy, S. Bhattacharya, and D. Divan, "Performance analysis and characterization of current switch under reverse voltage commutation, overlap voltage bump and zero current switching," in *IEEE Applied Power Electronics Conference and Exposition*, 2013, pp. 2429-2435.

[80] A. Kurnia, H. Cherradi, and D. Divan, "Impact of IGBT behavior on design optimization of soft switching inverter topologies," *IEEE Transactions on Industry Applications*, vol. 31, no.2, pp. 280-286, Mar. 1995.

[81] Fairchild, "IGBT Basics 1," Application Note 9016, Feb. 2001.

[82] Fairchild, "MOSFET Basics," Application Note 9010, Sep. 2013.

[83] Cree, "Design considerations for designing with Cree SiC modules part 1. Understanding the effects of parasitic inductance," Application Note, 2013.

[84] Meetechniek, "Measuring self-inductance and ESR," Application Note, 2014.

[85] N. Mohan, T. Undeland, and W. Robbins, *Power electronics converters, applications and design*, Wiley, New York, 2002.

[86] Infineon, "Influence of stray inductance on high-efficiency IGBT based inverter designs," Application Note, 2010.

[87] Mitsubishi, "General considerations for IGBT and intelligent power modules," Application Note, Sep. 1998.

[88] J. Dodge, "Eliminating parasitic oscillation between parallel MOSFETs," Advanced Power Technology Application Note APT-0402, Mar. 2004.

[89] R. Burra, S. Mazumder, and R. Huang, "DV/DT related spurious gate turn-on of bidirectional switches in a high-frequency cycloconverter," *IEEE Transactions on Power Electronics*, vol. 20, no.6, pp. 1237-1243, Nov. 2005.

[90] Cree, "CAS100H12AM1, 1.2 kV, 100 A silicon carbide half-bridge module," CAS100H12AM1 datasheet, 2014.

[91] Semikron, "Semikron structure of power modules," Semikron Application Note.

[92] D. Divan, "The resonant DC link converter - a new concept in static power conversion," *IEEE Transactions on Industry Applications*, vol. 25, no.2, pp. 317-325, Mar. 1989.

[93] D. Divan, and G. Skibinski, "Zero-switching-loss inverters for high-power applications," *IEEE Transactions on Industry Applications*, vol. 25, no.4, pp. 634-643, Jul. 1989.

[94] J. He, and N. Mohan, "Parallel resonant DC link circuit - a novel zero switching loss topology with minimum voltage stresses," *IEEE Transactions on Power Electronics*, vol. 6, no.4, pp. 687-694, Oct..

[95] S. Chen, and T.A. Lipo, "A novel soft-switched PWM inverter for AC motor drives," *IEEE Transactions on Power Electronics*, vol. 11, no.4, pp. 653-659, Jul. 1996.

[96] K. Wang. D. Boroyevich, and F.C. Lee, "Charge control of three-phase buck PWM rectifiers," in *IEEE Applied Power Electronics Conference and Exposition*, 2000, pp. 824-831.

[97] Michele Sclocchi, "Input filter design for switching power supplies," Texas Instruments application note, 2011.

[98] M.S. Rauls, D.W. Novotny, and D. Divan, "Design considerations for high frequency co-axial winding power transformers," in *IEEE Industry Applications Society Annual Meeting*, 1991, pp. 946-952.

[99] M.S. Rauls, D.W. Novotny, D. Divan, R.R. Bacon, and R.W. Gascoigne, "Multi-turn high frequency co-axial winding power transformers," in *IEEE Industry Applications Society Annual Meeting*, 1992, pp. 956-963.

[100] G. Shane, "Permanent magnet inductor design for reduced mass inductive components," Ph.D. dissertation, Dept. Elect. Eng., Purdue Univ., West Lafayette, IN, 2012.

[101] Total Magnetic Solutions, "Permanent magnet design guidelines," Available online: http://www.magnetsales.com/design/DesignG.htm.

[102] P. Pieteris, "Permanent Magnet DC Inductor." Patent US20100194512 (A1). Aug. 5, 2010.

[103] T. Ishibashi and K. Terasono, "DC Reactor and Inverter Device." Patent JP2007123596 (A). May 17, 2007.

[104] R. Tominaga, "D.C. Reactor." Patent EP0744757 (B1). Jul. 12, 1995.

[105] J. Kim, B. Min, S.V. Shenderey, "High voltage pulsed power supply using IGBT stacks," *IEEE Transactions on Dielectrics and Electrical Insulation*, vol. 14, no.4, pp. 921-926, Aug, 2007.

[106] J.G. Kulpin, "A 100 kilovolt phase control thyristor switch stack," in *IEEE International Power Modulators and High Voltage Conference*, 2008, pp. 378-380.

[107] M. Hagiwara, and H. Akagi, "Control and experiment of pulsewidth-modulated modular multilevel converters," *IEEE Transactions on Power Electronics*, vol. 24, no.7, pp. 1737-1746, Jul. 2009.

[108] F. Peng, "A generalized multilevel inverter topology with self voltage balancing," *IEEE Transactions on Industry Applications*, vol. 37, no.2, pp. 611-618, Mar. 2001.

[109] M. Saeedifard, and R. Iravani, "Dynamic performance of a modular multilevel back-to-back HVDC system," *IEEE Transactions on Power Delivery*, vol. 25, no.4, pp. 2903-2912, Oct. 2010.

[110] S. Inoue, and H. Akagi, "A bidirectional isolated dc-dc converter as a core circuit of the next-generation medium-voltage power conversion system," *IEEE Transactions on Power Electronics*, vol. 22, no.2, pp. 535-542, Mar. 2007.

[111] Magnetics® datasheet, "Ferrite core materials summary."

[112] Metglas® datasheet, "Powerlite inductor cores."

[113] W. Shen, "Design of high-density transformers for high-frequency high-power converters," Ph.D. dissertation, ECE, Virginia Tech, Blacksburg, VA, 2006.

[114] MK magnetics Inc. datasheet, "Nanocrystalline characteristics curves."

[115] Texas Instrument application note, "Magnetics design 5 – inductor and flyback transformer design."

VITA

Hao Chen was born in China in 1987. He received his B.S. degree in electrical engineering from the Nanjing University of Science and Technology in Nanjing, China, in 2008, and his M.S. degree in electrical engineering from the Illinois Institute of Technology in Chicago, in 2010.

From 2010 to 2012, he was an electrical engineer at Varentec in San Jose, California, where he worked on various projects including solid state transformers, dynamic VAr compensators, and voltage control for distribution systems.

Since January 2013, he has been working toward his Ph.D. degree in electrical engineering at the Georgia Institute of Technology, under the supervision of Dr. Deepak Divan. He has been working on several projects including soft-switching solid-state transformers, power flow controllers for utilities, distribution grid control, and wide-band-gap device characterization and design.

He is the author/coauthor of over 20 journal and conference papers as well as three patents, an active reviewer of several IEEE transaction journals and conferences, and a student member of IEEE. He is the recipient of best presentation award of IEEE Applied Power Electronics Conference and Exposition (APEC) in both 2014 and 2016.