Teaching Hardware Reverse Engineering: Educational Guidelines and Practical Insights

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Abstract—Since underlying hardware components form the basis of trust in virtually any computing system, security failures in hardware pose a devastating threat to our daily lives. Hardware reverse engineering is commonly employed by security engineers in order to identify security vulnerabilities, to detect IP violations, or to conduct very-large-scale integration (VLSI) failure analysis. Even though industry and the scientific community demand experts with expertise in hardware reverse engineering, there is a lack of educational offerings, and existing training is almost entirely unstructured and on the job. To the best of our knowledge, we have developed the first course to systematically teach students hardware reverse engineering based on insights from the fields of educational research, cognitive science, and hardware security. The contribution of our work is threefold: (1) we propose underlying educational guidelines for practice-oriented courses which teach hardware reverse engineering; (2) we develop such a lab course with a special focus on gate-level netlist reverse engineering and provide the required tools to support it; (3) we conduct an educational evaluation of our pilot course. Based on our results, we provide valuable insights on the structure and content necessary to design and teach future courses on hardware reverse engineering.

Keywords—hardware reverse engineering, educational guidelines

I. INTRODUCTION

In a world in which interconnected digital systems permeate almost all facets of our lives, IT security constitutes a major challenge for governments, individuals, and society at large. Even though various software layers employ a number of security mechanisms, hardware components are the basis of trust in virtually any computing system. Security failures at the hardware layer can have catastrophic consequences for the safety and security of computing systems as recently demonstrated by Spectre [1] and Meltdown [2].

There are a number of reasons why inspecting digital hardware is highly desirable in a security context. First, malicious manipulations (e.g., hardware Trojans and backdoors) can compromise the security of an entire system [3]. Since modern Application Specific Integrated Circuit (ASIC) design and fabrication processes are globally distributed, various (untrusted) stakeholders have access to valuable hardware

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designs and are thus able to commit piracy and perform malicious manipulations [4]. Second, low-quality counterfeits of integrated circuits pose serious security and safety risks, e.g., in mission-critical systems in aerospace or the power grid [5], [6]. Third, it is estimated that semiconductor companies face losses in the range of several billion US dollars in global revenue due to hardware piracy [7]. In this context, hardware reverse engineering experts play an essential role in helping companies detect violation of Intellectual Property (IP) in hardware designs.

The continuous evolution of a digital society shaped by a rapidly expanding Internet of Things (IoT) and the proliferation of cyber-physical systems has created a high demand for IT security experts with a solid background in hardware reverse engineering. Nevertheless, there is an almost complete lack of educational offerings in the hardware reverse engineering field. Moreover, the topic of how to optimally structure an educational program that aims to teach hardware reverse engineering skills has not been extensively explored. Currently, hardware reverse engineering training happens almost entirely on the job and is restricted to a relatively small number of entities: Government agencies (for defensive and offensive purposes), large semiconductor companies (for competitive and failure analysis), and a small number of specialized hardware analysis companies. We argue that materially limited access to reverse engineering specialists leaves companies and institutions less able to identify and respond to hardware vulnerabilities, which in turn makes them more susceptible to exploitation and attack. We propose mitigating this industry-wide deficit of hardware reverse engineers through the integration of hardware reverse engineering training into existing security programs.

Goal and Contribution. In this paper, we motivate our work by sketching the high demand for experts in hardware reverse engineering and the surprising lack of educational courses. We then provide an introduction to the various elements essential to effectively teaching hardware reverse engineering which include technical knowledge, insights from the fields of educational research and cognitive science, and the utility of graphical representations, which play a crucial role in the field.

Based on this foundation, we propose educational guidelines for hardware reverse engineering courses, which we in turn used to create and conduct such a course. Finally, we present an educational evaluation of the pilot course, held in the winter term 2017/2018 at the Ruhr-Universität Bochum, Germany. In summary our contributions are:

- Educational Guidelines. To the best of our knowledge, we have designed the first structured guidelines to teach hardware reverse engineering with a particular focus on gate-level netlist reverse engineering. Since the effective use of both graphical and textual representations is essential in the hardware reverse engineering field, our guidelines incorporate structures to support connectionmaking processes between both types of representations. Our guidelines lay the foundation for a course structure that enables the acquisition of conceptual competencies such as sensemaking (e.g., skills to choose the meaningful parts of a hardware design) or perceptional competencies (e.g., abilities to immediately grasp the meaning of a graphical representation). These competencies support students' learning from graphical and textual representations, and their development in the context of learning hardware reverse engineering is consequentially essential.
- Lab Course. Based on the proposed guidelines, we create
 a lab course consisting of five different projects with a
 special focus on gate-level netlist reverse engineering. We
 introduce our educational software environment based on
 the interactive tool HAL, which provides both textual and
 graphical representations of gate-level netlists.
- Educational Evaluation. We provide valuable insights into the structure and content necessary to teach future courses in this area by conducting an educational evaluation, which considers perceived task difficulty, mental effort, and the level of relevant prior knowledge of the course participants. Based on the results, we derive methods for teaching and designing future courses on hardware reverse engineering.

II. TECHNICAL BACKGROUND

The term *reverse engineering* relates to the processes of extracting knowledge or design information from anything man-made in order to comprehend its inner structure [8]. In the context of hardware security [9], security engineers (as well as adversaries) are forced to employ reverse engineering to make sense of a proprietary hardware design (e.g., to identify security vulnerabilities or security-circuitry for Trojan insertion [10]). During this task, analysis of the gate-level netlist is a crucial step for human reverse engineers [11].

Gate-level Netlists. Synthesis tools convert Register Transfer Level (RTL) descriptions of hardware designs into representations of the (Boolean) logic gates of the target gate library and their connectivity [12]. Such representations are called gate-level netlists. A simple example of a gate-level netlist in (1) graphical representation and the equivalent (2) textual representation can be found in Fig. 1.

During the different synthesis steps, valuable high-level information such as (1) meaningful descriptive information (e.g., names and comments), (2) boundaries of implemented modules, and (3) module hierarchies is lost. In practice, this loss of information highly complicates the reverse engineering process [13].

In real-world settings, analysts can obtain gate-level netlists in several scenarios: (1) through chip-level reverse engineering in the case of a given ASIC (involving steps such as decapsulation and delayering) [14], (2) through bitstream reverse engineering in the case of Field Programmable Gate Arrays (FPGAs) [15], or (3) by direct access at a foundry or through bribery or theft.

Tools. Similar to complex hardware design processes, hardware reverse engineering requires tools to automate time-consuming tasks and simplify steps for human analysts (e.g., through different representation forms). In particular, the latter is important for teaching this topic to novices in this area. Even though several tools exist in the industrial sector [14], [16], such programs are typically not publicly available. In anticipation of Section IV, we selected the hardware reverse engineering tool HAL [17] as our educational software environment since it provides a rich-featured interactive Graphical User Interface (GUI) suited for manual analysis, graph-based visual representations of gate-level netlists, and built-in extensibility for the integration of custom functionalities.

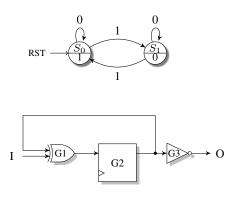
Representations. Various representational forms are involved during hardware design processes as well as reverse engineering processes. For example, during design and implementation phases, simulation waveforms are typically analyzed for debugging purposes. During gate-level netlist reverse engineering, textual forms or graph-based representational forms are analyzed, see Fig. 1. Therefore, the process of hardware reverse engineering necessitates the utilization of graphical representations.

III. EDUCATIONAL GUIDELINES

In order to derive guidelines for the structure of courses which allow effective teaching of hardware reverse engineering, we first summarize relevant current background in educational research and cognitive science regarding learning with graphical and textual representations.

A. Pedagogical Background

Both textual and graphical representations play a central role in hardware reverse engineering (see II). From a pedagogical point of view, two major challenges have to be solved to teach hardware reverse engineering effectively: (1) Students need support in learning from and working with domain-specific graphical representations, and (2) students' connection-making abilities between textual and graphical representations need to be facilitated. To this end, we analyze relevant current background in educational research, which provides guidance as to how these two challenges can be met. Note that the cognitive theory of multimedia learning [18], [19], and the integrated model of text and picture comprehension [20] distinguish between learning from graphical and from textual representations. This distinction is based on the processing of text in the verbal part of the working memory [21], [22],



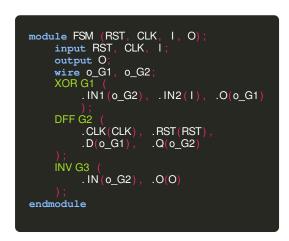


Fig. 1. Example Moore Finite State Machine (FSM) circuit as state transition graph (upper left) with associated gate-level netlist in (1) visual graph-based representation (lower left), and (2) textual representation with an exemplary gate library in Verilog (right).

and the processing of graphical representations in the visual part [21], [22]. Thus, these different processing pathways cause different demands for an educational course structure, in which graphical and textual representations are combined.

1) Opportunities and Challenges – Learning with Graphical Representations: Prior educational research outlined opportunities for as well as challenges with learning from graphical representations. Schnotz [23] showed that graphical representations can support students' learning success by making abstract concepts more accessible. Additionally, graphical representations can depict supplementary information [24], [25] which enables students to build a deeper understanding of novel content [26]. Sociocultural theories consider graphical representations as an important form of scientific communication [27], [28]. Despite their value in supporting students' learning processes, graphical representations can also be challenging for students. One of the main challenges in this context is the representational dilemma [24], [29], [30]. A representational dilemma exists when students have to learn new content knowledge they do not yet understand from graphical representations they also do not yet understand [30]. To overcome this challenge and benefit from graphical representations, it is necessary for students to develop specific competencies. These competencies support students in recognizing how graphical representations depict relevant information in order to solve a task or to learn new content. Thus, it is essential to consider how the development of specific competencies can be supported by the structure of the course. In the following, the specific competencies to overcome the representational dilemma and to benefit from domainspecific graphical representations will be addressed. Based on educational research, we outline how these competencies can be acquired to reach the two goals of (1) enabling students' learning from and working with graphical representations, and (2) facilitating students' connection-making abilities between textual and graphical representations.

2) Competencies for Learning from and Working with Graphical Representations: According to cognitive learning theories, students have to acquire representational competencies to overcome the representational dilemma [29], [31]–[34]. Representational competencies are defined as the skills and knowledge applied to interpret and use graphical representations [35]. Cognitive learning theories distinguish two types of representational competencies: (1) conceptual competencies, and (2) perceptual competencies. Prior findings showed that these two types of representational competencies are linked to learning processes with graphical representations [18]–[20], [23], [30] and are consequently relevant for educational guidelines.

Conceptual Competencies: Sensemaking. Conceptual competencies describe a set of skills and practices that enable students to relate graphical representations to prior knowledge, to draw inferences based on graphical representations, and to choose the most suitable graphical representation which contains the information necessary to complete a task [30], [36]. The process of choosing the relevant parts of a graphical representation for solving a problem depends on the students' ability to identify meaningful visual features. Koedinger et al. [37] showed that students' development of conceptual competencies is based on sensemaking processes. Dougherty et al. [38] described sensemaking as a process in which a person combines various information and ideas in a meaningful way. Sensemaking processes are verbally mediated [30], [37], [39], [40] and explicit since students need to willfully engage in verbal explanations [41].

Perceptual Competencies: Fluency. Perceptual competencies are defined as the ability to immediately detect the meaning of a graphical representation. The immediate detection of relevant information from a graphical representation is accomplished effortlessly and efficiently through an improved ability to recognize visual patterns [18]–[20], [23], [42]. Perceptual competencies include the concept of fluency in recognizing and processing information from and about the graphical representation [43]. The acquisition of perceptual competencies does not require direct instruction, but rather

experience-based learning through the repetition of numerous examples [42], [44]–[46].

3) Competencies for Connection-Making Abilities: Besides representational competencies, which are necessary to benefit from graphical representations, students have to acquire skills and knowledge about how to glean information from textual and graphical representations in tandem. The main phenomena here are the ways in which the graphical representation constrains the understanding of the text as well as the mechanisms by which text and graphics complement each other to convey relevant information [24], [25]. Acquiring competencies in connectionmaking between the textual and graphical representations is essential; since both types of representation depict relevant information in gate-level netlists (see Fig. 1). Schnotz and Bannert [47] outlined that text and picture comprehension are goal-oriented processes, in which the individual actively selects and handles verbal and graphical information to construct mental representations to complete the task at hand. The general assumption that adding graphics to a text improves the learning process overlooks the fact that graphical representations can be redundant to the accompanying text or dependent on the level of prior knowledge of the learners. Prior findings showed that learners with low prior knowledge benefit from combining textual and graphical representations, whereas learners with high prior knowledge also seem to be able to learn content from text alone [47]. The learning processes for acquiring connection-making abilities are described as verbally mediated sensemaking processes that use graphical representations in authentic tasks [30].

In summary, hardware reverse engineering processes are greatly facilitated by working with textual and graphical representations of gate-level netlists. Consequently, a course imparting content from and skills in this field has to integrate these two forms of representations. Prior educational research has shown that learning with graphical representations can be beneficial and challenging at the same time. To overcome these challenges, students have to acquire specific competencies. These can be acquired in different ways, which have to be considered while designing content and structure of a new course. Based on these demands we propose four guidelines for an educational course which teaches hardware reverse engineering.

B. Educational Guidelines for Teaching Hardware Reverse Engineering

- (1) Integration of Graphical Representations. By drawing upon educational research, we have summarized how graphical representations can enable access to complex concepts [23] and support students' learning processes. Since working with graphical representations is a common practice in hardware reverse engineering, graphical representations should be an integral part of a course which teaches reverse engineering.
- (2) Instructional Support to Develop Conceptual Competencies. Working with graphical representations can be challenging for students, especially when they are using representations for the first time. To overcome the represen-

tational dilemma, special instructional support is needed [30] to acquire conceptual competencies based on the activation of sensemaking processes [37]. Consequently, instructional support to acquire conceptual competencies needs to engage students in active reasoning, for example by prompting students to self-explain how they used a graphical representation or by engaging in discussions with other students about solving a task [30], [37], [48].

- (3) Support to Develop Perceptual Competencies. When integrating graphical representations into a course it is important to support the development of students' fluencyability to recognize the meaning of a graphical representation immediately. Based on prior findings, the development of perceptual competencies is not based on instructional support but on experience-based learning with repetition of numerous examples [30], [42], [44]–[46]. Hence, an educational course in hardware reverse engineering should involve repetitive exercises of working with the graphical representations to support students in developing fluency for detecting relevant patterns therein.
- (4) Instructional Support to Develop Connection-Making Abilities. Since gate-level netlists can be represented both graphically and textually, it is important to enable students to develop abilities for connection-making between the two different forms of representation. Students have to learn how text and graphics complement and constrain one another. Since the development of connection-making abilities is based on verbally mediated sensemaking processes [30], students should reflect and explain their solutions verbally during lectures.

IV. EDUCATIONAL RESEARCH AS THE FOUNDATION FOR A REVERSE ENGINEERING LAB COURSE

We now provide details of the practice-oriented hardware reverse engineering course. Prior to the course and task descriptions in Section IV-B, we first introduce the educational software environment based on the interactive gate-level netlist reverse engineering and manipulation tool HAL [17] (Section IV-A).

A. Educational Software Environment

HAL assists users in the reverse engineering of complex gate-level netlists and its extensibility allows for the development of custom plugins. In particular, HAL employs an interactive GUI to provide both textual and graph-based representation of the gate-level netlist under inspection. We stress that a GUI is of major importance in manual reverse engineering since making sense of complex or even relatively small hardware circuits consisting of a few hundred gates is considerably easier with a graph-based representation than it is with an inflexible textual representation.

Relevance with Respect to Guidelines. We want to emphasize that HAL supports *Guideline 1* as defined in Section III-B, e.g. by providing a learning environment, which integrates graphical and textual representations of gate-level netlists.

Since hardware reverse engineering requires hands-on experience, we decided to offer a 3 ECTS credit point lab course to final year bachelor's and master's students of our IT security programs. Since their relevant prior knowledge does not differ, course requirements are equal for both groups. While the course provides an overview of the multi-layered chip-level reverse engineering processes and hardware security in general, the main learning objectives focus on gate-level netlist reverse engineering using HAL. In order to assure real-world relevance, we also invited two industry experts who presented specific hardware reverse engineering projects.

Structure. To facilitate our students' learning success, the course consists of five projects (minimum grade to pass: 75%) which have to be completed individually by each participant. Each project lasts three weeks and contains the following subtasks: (1) the reading of relevant scientific papers, (2) pen & paper exercises, and (3) practical reverse engineering tasks. The reading and understanding of 1-2 scientific papers conveys relevant content for subsequent tasks while the pen & paper exercises support reproduction and internalization of relevant information. The acquired knowledge is first applied to smallscale examples, and subsequently in more complex contexts during the practical reverse engineering tasks. At the beginning of each project, theoretical and practical background is taught in one introductory session and after the submission deadline, solutions are discussed and students are encouraged to present their approaches to the class in another session. In total, 12 sessions are held during the 15-week winter term: 10 project sessions and 2 invited sessions.

Relevance with Respect to Guidelines. The project design supports students as they develop perceptual competencies as defined in *Guideline 3*, e.g. through repeated tasks involving the use of graphical representations. Furthermore, the course structure satisfies *Guidelines 2* and *4*, e.g. by encouraging active discussions during our lab sessions.

- 1) Project 1 Standard Cell Reverse Engineering: To understand the goals and needs of hardware reverse engineering, students first have to acquire general knowledge of hardware security by answering questions drawn from two comprehensive works [49], [50] which cover topics ranging from the semiconductor supply chain structure, to hardware design flow, to threat models. Both the pen & paper and the practical exercises focus on standard cell reverse engineering, which is an essential element of chip-level reverse engineering. Once a standard cell is identified, the analyst can employ an image recognition algorithm to find all other occurrences of the same standard cell. This leads to a higher level of abstraction and thus makes it easier to understand the circuit functionality [50]. In the practical assignment, students reverse engineer standard cells from the Integrated Circuit (IC) layout of an Advanced Encryption Standard (AES) IP core and subsequently utilize KLayout [51] to automatically extract a gate-level netlist.
- 2) Project 2 Netlist Reverse Engineering: In this exercise, the gate-level netlist analysis and manipulation tool HAL is introduced to the students. In addition to ASICs, widely-used

FPGAs lend themselves to reverse engineering. Since FPGAs enable the students to directly test circuit manipulations as performed in later tasks, we provide the relevant background on the security of Static Random Access Memory (SRAM)based FPGAs and outline the major challenges of gate-level netlist reverse engineering [13], [52]. The pen & paper exercise involves the analysis and reverse engineering of Look-Up Table (LUT) contents in order to comprehend how combinational circuits are realized on an FPGA. In the practical assignment, students must decrypt a given ciphertext, which has been processed by a simple proprietary cryptographic encryption algorithm with a known key. In order to implement the decryption function, students have to analyze the datapath of the encryption algorithm realized by the design under consideration. which is given in the form of a gate-level netlist. More precisely, they have to analyze cryptographic Sboxes (implemented in LUTs) and assemble the corresponding inverse Sboxes for the decryption function. Sboxes are small tables which are central components of modern ciphers.

- 3) Project 3 FSM Reverse Engineering: Since the control logic of most digital systems is implemented by Finite State Machines (FSMs), this project focuses on FSM reverse engineering in a realistic scenario. The FSM control signals are of particular interest to the reverse engineer because these signals steer the datapath modules of the design or communicate to other FSMs. Through the integration of scientific papers [53], [54], we taught students the fundamentals of constructing FSM circuits in hardware and the algorithmic identification of FSMs from gate-level netlists. In the pen & paper assignment, the students have to recover the possible states, draw the state transition graph, and derive further high-level information, e.g. the FSM encoding, from a gate-level description of a small FSM. An example for such an FSM is depicted in Fig. 1. In the practical assignment, students have to reverse engineer the control logic from a slightly modified variant of the proprietary cipher from Project 2 with the goal of determining the number of iterated rounds which are executed by the cipher. After identifying the combinational logic gates and signals of which the FSM is composed, they define the state transition graph and deduce the function of each state.
- 4) Project 4 Crypto Reverse Engineering: While Projects 2 and 3 focus on (a) acquiring knowledge, (b) learning and implementing basic reverse engineering strategies, and (c) becoming familiar with the handling of HAL, Project 4 aims at the application of these skills in the context of a realworld implementation of the Advanced Encryption Standard (AES) on an FPGA. AES is the most widely used encryption algorithm. Initially, a brief overview of the AES standard and the fundamental concepts of AES hardware architectures are provided to the students [55]. Usually, Sboxes are implemented on FPGAs utilizing LUTs and multiplexers. In the pen & paper exercise, students reverse engineer a small circuit implementing one column of a 4 bit Sbox. Subsequently, they sketch the hardware implementation of an AES Sbox and calculate the number of potential input permutations for the AES Sbox. In the practical assignment, students have to extract a hard-coded

key from a real-world AES core to decrypt a given ciphertext. After deriving high-level information like the functionality (encryption or decryption), the presence of the key schedule, the key length, and the hardware architecture (iterative or pipelined), they have to write a HAL plugin to identify the Sbox logic, since the Sboxes serve as a potential anchor for attacks on the hard-coded key. Finally, the hard-coded key is extracted through manipulation of the underlying circuit (insertion of a hardware Trojan) or through exhaustive reverse engineering.

5) Project 5 - Reverse Engineering vs. Obfuscation: This project introduces hardware obfuscation as a potential countermeasure to IP theft and reverse engineering to the students [9]. Control flow obfuscation methods are discussed as a specific example of obfuscation methods on the netlist-level. The reading briefly introduces a weak FSM-based obfuscation method utilizing so-called obfuscated states that have to be passed in correct order before the original states appear [56]. In the combined pen & paper and practical assignments, students defeat the introduced obfuscation method through using structural reverse engineering and manipulation of the gate-level netlist. Students are equipped with a gate-level netlist and the corresponding bitstream that is implementing the aforementioned obfuscation scheme. While the bitstream implements the obfuscated FSM on a small FPGA, the students can control the FSM directly via UART, and hence test the successfulness of their attempts by receiving a visual feedback from an LED. To accomplish this task, students have to manipulate the gate-level netlist file with HAL and synthesize it to the proprietary bitstream using the vendor toolchain.

V. EVALUATION – METHODS AND RESULTS

A. Methods

To the best of our knowledge, the proposed course is the first to teach domain-specific knowledge in hardware reverse engineering with a particular focus on gate-level netlist reverse engineering incorporating educational theory. One already existing course for teaching hardware reverse engineering [57] was developed and conducted by Yener and Zonenberg, but did not focus on gate-level netlist reverse engineering in particular.

Because of our unique focus on teaching gate-level netlist reverse engineering we could not draw much educational guidance from existing courses. This resulted in the need to perform a thorough course evaluation to gain deeper insights for future lectures in this field. Overall, 10 students participated in the pilot course. All of them were enrolled in IT Security programs at Ruhr-Universität Bochum, Germany. Five students (all male; mean age 22.2 years; 3 on bachelor's level; 2 on master's level) consented to the analysis of their data within the context of this educational evaluation.

The main goals of our evaluation were: to understand how challenging the projects were and to what extent their difficulty was dependent upon the students' prior level of knowledge, to assess whether the workload corresponding to each individual project was adequate, to determine if HAL and its graphical representations supported the learning process, and to identify

what other difficulties, if any, the students encountered. In the following, we introduce the evaluative methods we used, summarize the results, and highlight implications for future courses on hardware reverse engineering.

1) Relevant Prior Knowledge: We designed our projects and introductory lectures based upon assumptions about the students' level of prior knowledge of relevant topics. By measuring their level of prior knowledge, we were able to detect knowledge gaps which explain difficulties they encountered and help us revise the course for future iterations. We used two methods to measure the level of relevant prior knowledge. The first method consisted of three self-developed items including the following questions: "How highly do you rate your level of prior knowledge in hardware reverse engineering?" Students had been asked to rate their answer on a 5-point *Likert* Scale [58], ranging from "very low (1)" to "very high (5)". The other two items "How much theoretical exposure to hardware reverse engineering have you had?" and "How much practical experience in hardware reverse engineering do you have?" had to be answered on a 5-point Likert scale [58], ranging from "very much (1)" to "not at all (5)". Additionally, students were asked to provide information about any relevant courses they successfully completed.

2) Cognitive Load – Mental Effort and Perceived Task Difficulty: Besides the level of prior knowledge, we measured mental effort and perceived task difficulty. The methods used in this study are common in current research on cognitive load [59] by means of two subjective rating scales. The first scale was the mental effort rating scale [60]. We asked students to rate their invested amount of mental effort on a 7-point Likert Scale [58], ranging from "very low mental effort (1)" to "very high mental effort (7)" [59]. Another commonly used scale to measure cognitive load is the perceived task difficulty scale [61]–[64]. Students were asked to rate the perceived task difficulty on a 7-point Likert Scale [58], ranging from "very easy (1)" to "very difficult (7)".

B. Results

In summary, all 10 students completed the course successfully. In the following, we present and discuss the results of the 5 students who consented to evaluation. Here we would like to note that we did not attempt to determine the probability of successful course completion in our analysis. As stated before, students had to reach at least 75% to pass a single project and all 10 students reached between 80-100% in each project. Based on this structure, the probability of successful course completion has no explanatory power.

To set the particular focus of the evaluation on the novel hardware reverse engineering tasks, students were asked to rate projects 3-5. Those three projects included real-world hardware reverse engineering tasks with growing complexity. Note that project 1 and 2 were important to introduce hardware reverse engineering in general and the educational software HAL in particular, but did not include real-world hardware reverse engineering tasks. Thus, they were excluded from the evaluation of this course.

Table I
DESCRIPTIVE ANALYSIS OF PRIOR KNOWLEDGE WITH MEANS AND STANDARD DEVIATIONS

| | Prior Knowledge | Theoretical Experiences | Practical Experiences |
|-----------|-----------------|-------------------------|-----------------------|
| Mean (SD) | 2.00 (1.00) | 4.20 (.84) | 4.60 (.55) |

Table II
DESCRIPTIVE ANALYSIS OF PERCEIVED TASK DIFFICULTY AND MENTAL EFFORT WITH MEANS AND STANDARD DEVIATIONS

| | Perceived Task Difficulty | Mental Effort |
|-----------|---------------------------|---------------|
| Project 3 | 3.60 (1.14) | 4.20 (.84) |
| Project 4 | 3.60 (.89) | 4.40 (.85) |
| Project 5 | 5.20 (.45) | 5.60 (.89) |

Level of Relevant Prior Knowledge. Most of the students had low theoretical knowledge and barely any practical experience in hardware reverse engineering. Table I illustrates the results of a descriptive analysis with means and standard deviation (SD). In addition, most of the students had not completed relevant coursework and consequently had gaps in domain-specific topics like the application of Boolean functions or the implementation of cryptographic schemes.

Level of Mental Effort and Task Difficulty. Table II summarizes the descriptive analysis of cognitive load. Means and standard deviations revealed moderate levels of perceived task difficulty and mental effort.

VI. DISCUSSION AND IMPLICATIONS

All 10 students successfully passed the pilot course. First, this result supports the assumption that the course and its foundation based on the educational guidelines contribute to teaching hardware reverse engineering successfully. Project 5 included the most complex task which is reflected in higher means of perceived task difficulty and mental effort. Although the task complexity gradually increases from project 3 to project 5, all students successfully passed each single task which leads to the inference that the course structure contributes to learning hardware reverse engineering efficiently.

Second, the combination of graphical and textual representations as integrated in the course supported the students' learning success by making abstract concepts in hardware reverse engineering more accessible. Third, the course structure and the inclusion of instructional support facilitated the acquisition of relevant competencies and connection-making abilities, which are necessary to learn from and work with graphical and textual representations as used in HAL.

Course Restructuring – Closing Prior Knowledge Gaps. Despite the successful implementation of the pilot course, the challenges presented by the students' lack of relevant knowledge prior to beginning the course merits further discussion. Through their feedback, we determined that the students had knowledge gaps in relevant content area, which caused them to invest more time than we had intended to complete the projects. To provide greater support for students' learning processes, we decided to partially restructure the material of our course in the future. Instead of a single practice-oriented lab course, we are

currently designing a new series which includes fundamental background on the hardware design processes in Lectures 1-6 (from [12]). From there, Lectures 7-12 will holistically capture the multi-layer hardware reverse engineering process (e.g., from [11], [14], [49], [50], [52], [65]). We also set an appropriate incentive that reflects the expected workload by offering 5 ECTS credit points for successful participation in the lectures, in addition to 3 ECTS for the lab part of the course.

To test the course structure and to obtain deeper insights into the learning processes of a broader student population, we plan to offer the modified course for the first time at the University of Massachusetts Amherst, USA, and Ruhr-Universität Bochum, Germany, in the first six weeks (2 lectures per week) of the 2018/19 winter term. In the last 9 weeks of the semester, we will offer our lab course. We expect our students to satisfy the shorter project time limits (2 instead of 3 weeks) thanks to their significantly higher prior knowledge in relevant topics.

VII. CONCLUSION

In this paper, we highlighted the necessity of security engineers' and system designers' acquisition of solid hardware reverse engineering skills. Even though there is an increasing demand for specialists in this area, we identified a lack of educational courses which make hardware reverse engineering more accessible to students by teaching fundamental background content in a well-structured and practice-oriented fashion.

To this end, we formulated course structure guidelines based on insights gleaned from the fields of educational research and cognitive science which led to the development of a novel course on hardware reverse engineering with particular focus on gate-level netlist reverse engineering. Based on the educational evaluation of our first pilot lab course, we identified important aspects of future improvements to course content, particularly the incorporation of fundamental background knowledge of hardware design processes, an area in which students were lacking.

REFERENCES

- P. Kocher, D. Genkin, D. Gruss, et al., "Spectre Attacks: Exploiting Speculative Execution," CoRR, vol. abs/1801.01203, 2018.
- [2] M. Lipp, M. Schwarz, D. Gruss, et al., "Meltdown," CoRR, vol. abs/1801.01207, 2018.
- [3] G. T. Becker et al., "Stealthy Dopant-level Hardware Trojans," in CHES, pp. 197–214, Springer, 2013.
- [4] M. Rostami et al., "A Primer on Hardware Security: Models, Methods, and Metrics," Proc. of the IEEE, vol. 102, no. 8, pp. 1283–1295, 2014.
- [5] U. Guin, K. Huang, D. DiMase, et al., "Counterfeit integrated circuits: A rising threat in the global semiconductor supply chain," Proc. of the IEEE, vol. 102, pp. 1207–1228, Aug 2014.
- [6] U. Guin, D. DiMase, and M. Tehranipoor, "Counterfeit integrated circuits: Detection, avoidance, and the challenges ahead," *J. of Electron. Testing*, vol. 30, pp. 9–23, Feb 2014.

- [7] M. Pecht and S. Tiku, "Bogus: Electronic manufacturing and consumers confront a rising tide of counterfeit electronics," *IEEE Spectrum*, vol. 43, pp. 37–46, May 2006.
- [8] M. G. Rekoff, "On Reverse Engineering," IEEE Trans. on Systems, Man, and Cybern., no. 2, pp. 244–252, 1985.
- [9] B. Shakya et al., Introduction to Hardware Obfuscation: Motivation, Methods and Evaluation, pp. 3–32. Springer, 2017.
- [10] S. Wallat et al., "A Look at the Dark Side of Hardware Reverse Engineering – A Case Study," in IVSW, 2017.
- [11] M. Fyrbiak *et al.*, "Hardware Reverse Engineering: Overview and Open Challenges," in *IVSW*, 2017.
- [12] N. Weste and D. Harris, CMOS VLSI Design: A Circuits and Systems Perspective. USA: Addison-Wesley Publishing Company, 4th ed., 2010.
- [13] P. Subramanyan et al., "Reverse Engineering Digital Circuits Using Structural and Functional Analyses," *IEEE Trans. Emerging Topics Comput.*, vol. 2, no. 1, pp. 63–80, 2014.
- [14] R. Torrance, "The State-of-the-Art in IC Reverse Engineering," in CHES, pp. 363–381, Springer, 2009.
- [15] J.-B. Note and É. Rannaud, "From the bitstream to the netlist," in ACM FPGA, pp. 264–264, 2008.
- [16] Texplained. https://www.texplained.com/process. [Online; accessed 19-May-2017].
- [17] M. Fyrbiak et al., "HAL- The Missing Piece of the Puzzle for Hardware Reverse Engineering, Trojan Detection and Insertion," *IEEE Trans. on Dependable and Secure Computing*, pp. 1–1, 2018.
- [18] R. E. Mayer, "Cognitive Theory of Multimedia Learning," The Cambridge Handbook of Multimedia Learning, pp. 31–48, 2005.
- [19] R. E. Mayer, "Cognitive Theory of Multimedia Learning," *The Cambridge Handbook of Multimedia Learning*, vol. 2, pp. 31–48, 2009.
- [20] W. Schnotz, "An Integrated Model of Text and Picture Comprehension.," The Cambridge handbook of multimedia learning., pp. 49–69, 2005.
- [21] A. Baddeley, "Working Memory," Sci., vol. 255, pp. 556–559, 1992.
- [22] A. Baddeley, "Working Memory: Theories, Models, and Controversies," Annu. Review of Psychology., vol. 63, pp. 1–29, 2012.
- [23] W. Schnotz, "An Integrated Model of Text and Picture Comprehension," The Cambridge Handbook of Multimedia Learning, vol. 2, pp. 72–103, 2014
- [24] S. Ainsworth, "DeFT: A Conceptual Framework for Considering Learning with Multiple Representations," *Learning and Instruction*, vol. 16, pp. 183–198, 2006.
- [25] S. Ainsworth, "The Multiple Representation Principle in Multimedia Learning," The Cambridge Handbook of Multimedia Learning, p. 464, 2014.
- [26] T. Seufert, "Supporting Coherence Formation in Learning from Multiple Representations," *Learning and Instruction*, vol. 2, pp. 227–237, 2003.
- [27] R. Kozma et al., "The Roles of Representations and Tools in the Chemistry Laboratory and Their Implications for Chemistry Learning," The J. of the Learning Sci., vol. 9, no. 2, pp. 105–143, 2000.
- [28] J. V. Wertsch et al., "Saying more than you know in instructional settings.," Theories of Learning and Stud. of Instructional Practice., pp. 153–166, 2014.
- [29] K. W. McElhaney et al., "Evidence for Effective Uses of Dynamic Visualisations in Science Curriculum Materials," Stud. in Sci. Educ., vol. 51, no. 1, pp. 49–85, 2015.
- [30] M. A. Rau, "Conditions for the Effectiveness of Multiple Visual Representations in Enhancing STEM Learning," Educ. Psychology Review., vol. 29, no. 4, pp. 717–761, 2017.
- [31] J. K. Gilbert, "Visualization: A Metacognitive Skill in Science and Science Education," Visualization in Sci. Educ., pp. 9–27, 2005.
- [32] J. K. Gilbert, "Visualization: An emergent field of practice and enquiry in science education.," Visualization: Theory and Practice in Sci. Educ., pp. 3–24, 2008.
- [33] S. Ainsworth, The Educational Value of Multiple-representations when Learning Complex Scientific Concepts, pp. 191–208. Dordrecht: Springer Netherlands, 2008.
- [34] A. J. de Jong *et al.*, "Acquiring Knowledge in Science and Mathematics: The Use of Multiple Representations in Technology Based Learning Environments," *Learning with Multiple Representations*, 1998.
- [35] J. H. Sim and other, "Representational Competence in Chemistry: A Comparison Between Students with Different Levels of Understanding of Basic Chemical Concepts and Chemical Representations.," Cogent Educ., vol. 1, no. 1, 2005.

- [36] V. Michalchik et al., "Representational Resources for Constructing Shared Understandings in the High School Chemistry Classroom," Visualization: Theory and Practice in Sci. Educ., pp. 233–282, 2008.
- [37] K. R. Koedinger *et al.*, "The Knowledge Learning Instruction Framework: Bridging the Science-Practice Chasm to Enhance Robust Student Learning," *Cognitive Sci.*, pp. 757–798, 2012.
- [38] D. S. Dougherty et al., "Sensemaking and Emotions in Organizations: Accounting for Emotions in a Rational(ized) Context," Communication Stud., pp. 215–238, 2006.
- [39] M. T. Chi et al., "Selfexplanations: How Students Study and Use Examples in Learning to Solve Problems," Cognitive Sci., pp. 145–182, 1989.
- [40] D. Gentner, "Structure-mapping: A Theoretical Framework for Analogy," Cognitive Sci., pp. 155–170, 1983.
- [41] A. A. diSessa and other, "Meta-representation: An Introduction," The J. of Math. Behavior, pp. 385–398, 2000.
- [42] E. J. Gibson, Principles of Perceptual Learning and Development. Pearson College Div, 1996.
- [43] A. J. Rocke, Image and Reality: Kekule, Kopp, and the Scientific Imagination. University of Chicago Press, 2010.
- [44] E. J. Gibson, "Perceptual Learning in Development: Some Basic Concepts," *Ecological Psychology*, pp. 295–302, 2000.
- [45] P. J. Kellman and other, "Perceptual Learning, Cognition, and Expertise," Psychology of Learning and Motivation, pp. 117–165, 2013.
- [46] H. B. Richman et al., "Perceptual and Memory Processes in the Acquisition of Expert Performance: The EPAM Model," The Road to Excellence: The Acquisition of Expert Performance in the Arts and Sci., Sports, and Games, pp. 167–187, 1996.
- [47] W. Schnotz and other, "Construction and Interference in Learning from Multiple Representation," *Learning and Instruction*, pp. 141–156, 2003.
- [48] L. Fiorella and other, "Eight Ways to Promote Generative Learning," Educ. Psychology Review., pp. 1–25, 2015.
- [49] M. Rostami, F. Koushanfar, and R. Karri, "A Primer on Hardware Security: Models, Methods, and Metrics," *Proc. of the IEEE*, vol. 102, no. 8, pp. 1283–1295, 2014.
- [50] S. E. Quadir et al., "A Survey on Chip to System Reverse Engineering," JETC, vol. 13, pp. 6:1–6:34, 2016.
- [51] M. Köfferlein, "KLayout." https://www.klayout.de/. [Online; accessed 08-May-2018].
- [52] S. M. Trimberger and J. J. Moore, "FPGA Security: Motivations, Features, and Applications," *Proc. of the IEEE*, vol. 102, no. 8, pp. 1248–1265, 2014.
- [53] Y. Shi et al., "A Highly Efficient Method for Extracting FSMs from Flattened Gate-Level Netlist," in ISCAS, pp. 2610–2613, 2010.
- [54] T. Meade et al., "Netlist Reverse Engineering for High-Level Functionality Reconstruction," in ASP-DAC, pp. 655–660, 2016.
- [55] Rodriguez-Henriquez et al., Cryptographic Algorithms on Reconfigurable Hardware. Springer Publishing Company, Incorporated, 1st ed., 2010.
- [56] R. S. Chakraborty et al., "Security against hardware Trojan through a novel application of design obfuscation," in ICCAD, pp. 113–116, 2009.
- [57] B. Yener and other, "CSCI 4974 / 6974 Hardware Reverse Engineering." http://security.cs.rpi.edu/courses/hwre-spring2014/. [Online; accessed 2014].
- [58] R. Likert, "A Technique for the Measurement of Attitudes," Archives of Psychology., 1932.
- [59] A. Schmeck et al., "Measuring Cognitive Load with Subjective Rating Scales During Problem Solving: Differences Between Immediate and Delayed Ratings," *Instructional Sci.*, vol. 43, pp. 93–114, 2015.
- [60] F. G. Paas, "Training Strategies for Attaining Transfer of Problem-solving Skill in Statistics: A Cognitive-load Approach," J. of Educ. Psychology., vol. 84, pp. 429–434, 1992.
- [61] O. Bratfisch et al., Perceived Item-Difficulty in Three Tests of Intellectual Performance Capacity. ERIC Clearinghouse, 1972.
- [62] S. Kalyuga et al., "Managing Split-attention and Redundancy in Multimedia Instruction," Appl. Cognitive Psychology, vol. 13, pp. 351– 371, 1999.
- [63] N. Marcus et al., "Understanding Instructions," J. of Educ. Psychology, vol. 88, pp. 49–63, 1996.
- [64] F. Paas et al., "Cognitive Load Theory and Instructional Design: Recent Developments," Educ. Psychologist, vol. 38, pp. 1–4, 2003.
- [65] M. C. Hansen et al., "Unveiling the ISCAS-85 Benchmarks: A Case Study in Reverse Engineering," *IEEE Design & Test of Comp.*, vol. 16, no. 3, pp. 72–80, 1999.