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Modulation Techniques for a Modified Three-Phase Quasi-Switched Boost Inverter with Common-Mode Voltage Reduction

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ABSTRACT In a single-stage buck-boost quasi-switched boost inverter (qSBI), the shoot-through state insertion causes high amplitude common-mode voltage. Consequently, the qSBI becomes less attractive in transformerless photovoltaic (PV) systems. In this paper, a novel space vector pulse-width modulation for a modified qSBI is introduced to reduce the magnitude of common-mode voltage and push the modulation index up to 1. By properly choosing the shoot-through interval time, shoot-through states are considered to be inserted for boosting voltage and also reducing the THD value of the output voltage. The mathematical analysis and operating principles of the converter are discussed and verified through PSIM simulations. Finally, an experimental prototype is validated based on a TMS320F28335 DSP microcontroller and a DE0-Nano FPGA digital control platform.

INDEX TERMS Z-source inverter, quasi-switched boost inverter, single-stage inverter, common-mode voltage, transformerless PV system, space vector pulse-width modulation.

I. INTRODUCTION

Distributed generation has emerged as an effective way to use different renewable energy sources such as photovoltaics (PVs), wind power, and fuel cell stacks for enhancing reliability, reducing emissions, and improving additional power quality benefits. In distributed generation applications, PV power systems are particularly attractive, and their generation costs have been reduced continuously in recent years [1]-[2]. Therefore, grid-connected PV inverters need to be carefully designed to improve system performance in terms of low cost, lightweight, high efficiency, and small size [3]-[4]. The grid-connected inverters can be generally classified as transformerless and galvanic isolation systems. A combined high-frequency transformer in the DC side or a low-frequency bulky transformer in the AC grid side is usually used to achieve the galvanic isolation and improve the safety. However, transformer-based PV inverters are heavy and bulky with a high cost and high loss. Therefore, transformerless PV inverters have received more attention in both academic and industrial fields [4]-[6]. To interface PV systems to the grid, voltage source inverters (VSIs) are the most established DC to AC power converter in any electric power systems. Moreover, an additional boost DC-DC converter might be mandatory if the output voltage of the PV panels is not high enough under all the operating conditions. In order to prevent the short-circuiting of the DC-link bus, a deadtime must be used in the H-bridge inverter, which inevitably increases the THD value at the output side. In recent years, single-stage Z-source and quasi-Z-source power inverters (ZS/qZSIs) [7]-[10] with buck/ boost characteristic have been introduced with some advantages in PV applications. Because of the continuous input current and lower voltage stresses across capacitors, the qZSIs have been used widely in distributed generation systems [8]-[10]. However, the size and weight of qZSIs are still large because of using two qZS-inductors and two qZS-capacitors in the Z-source network. In order to reduce the size and weight of the inverter package, a study on quasi-switched boost inverters (qSBIs) of embedded and DC-link types was

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presented in [11]. The qSBIs overcome qZSIs in terms of reduced size, weight, and power losses for high boost applications [12]. Compared to the DC-link types, the embedded types have more interesting and competitive solutions in the PV applications due to the continuous input current characteristic and relatively high voltage gain. However, when a wider input voltage range is needed for a PV system related to the buck voltage ability or a low voltage boost requirement, the embedded qSBI cannot respond well, as presented in [13]-[14]. In order to overcome this limitation, an active qSBI has been proposed by combining the qZS and qSB topologies [15]-[16]. However, many components are required in these Z-networks, which leads to reduce efficiency and increase cost.

To enhance the voltage range of an embedded qSBI and reduce the number of passive elements with reference to the active qZSI, a two-switch qSBI (2S-qSBI) was introduced and verified in [17]-[18], that required two extra switches in the qSB-network, as depicted in Fig. 1. Compared with other impedance-source inverters, the 2S-qSBI solution has great attention for PV systems due to its attractive merits in terms of the wide input voltage operation, continuous input current, and system volume.

In a transformerless PV inverter, common-mode voltages (CMVs) will be generated while the inverter is being operated. The CMV with high magnitude, high frequency, and slew rate *dv*/*dt* will lead to the leakage current on the stray capacitors between PV panels [19]. For safety consideration, the leakage current should be repressed within an allowable value to guarantee the safety requirement. Leakage current reduction is helpful in reducing possible extra power losses, slowing the degradation of PV panels, and improving grid current quality. The leakage current can be reduced by modifying the PWM strategies to reduce the CMV amplitude. The CMV reduction technologies for the conventional VSIs can be categorized into system topology reconfiguration [20]-[23] and carrier-based PWM technique modification [24]-[27]. The inverter system can be modified by changing some active or passive elements in the topology. For example, the H8 topology with adding two more switches [20], the three-phase topology using three zero-voltage rectifier modules [21], and four-leg inverter [22] are all structural solutions for CMV reduction. Furthermore, a common-mode passive filter that utilizes passive-filter networks to eliminate the high-frequency leakage current to the AC stage was discussed in [23]. Under this circumstance, the filter does not change the CMV level, but it blocks the leakage current in a specific bandwidth. Overall, these topology-oriented approaches have disadvantages of being more complex, high cost, and increasing the total power loss.

Recently, the carrier and modulation-based solutions have been discussed to reduce the CMV without hardware changing. The CMV and common-mode current (CMC) reduction methods presented in [24]-[25] can be considered as modified-carrier solutions. These techniques can reduce the high-frequency harmonics of the CMV. However, the THD value

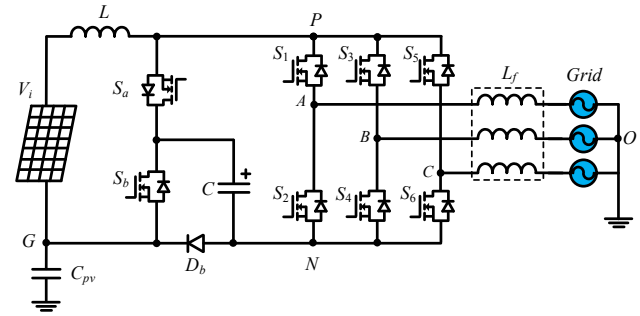

FIGURE 1. Three-phase 2S-qSBI for PV system.

of the output voltage is high, and the software implementations of these methods are complicated and need a high-performance microcontroller. Active zero state-space vector PWM (AZ-SVPWM), remote state SVPWM (RS-SVPWM), and near state SVPWM (NS-SVPWM) are the most popular modulation-based CMV reduction methods. These modulation methods have been discussed in many research works [26]–[28]. For AZ-SVPWM, the traditional zero states of the inverter are replaced by two active vectors in opposite directions with the same time as zero vector. Like the conventional SVM and discontinuous SVM (DSVM), the modulation index of AZ-SVPWM is linear. However, the THD of the output voltage is high, and bipolar line-to-line voltages appear in the AZ-SVPWM. In NS-SVPWM, three adjacent vectors are used in each switching cycle to synthesize the reference voltage. Under AZ-SVPWM and NS-SVPWM methods, the peak-to-peak value of CMV is successfully decreased from V_{PN} to $V_{PN}/3$, where V_{PN} is the peak DC-link voltage. Nevertheless, the modulation index of NS-SVPWM is linear between 0.66 and 1. Unlike the AZ-SVPWM and NS-SVPWM, the RS-PWSVM strategy can keep the CMV constant by selecting only odd active vectors or even active vectors. However, the modulation index of RSSVM strategies cannot go over 0.57. Because the shoot-through (ST) vectors during each switching cycle are required, none of the aforementioned modulation-based methods is ideal for single-stage power inverters. In [29], the CMV reduction three-phase ZSI was proposed by applying the RS-SVPWM strategy. In this method, an extra diode is added to the negative terminal of the PV source to provide the isolation between the PV panels and the inverter during ST states. However, the modulation index is limited to 0.57 in this case. In the same way, a three-phase ZSI with two extra switches was introduced in [30] to eliminate the CMV. However, the modulation index is also kept up only to 0.57. In [31], a three-phase ZSI with a modified NS-SVPWM strategy was presented. By applying the modified NS-SVPWM, the magnitude CMV of three-phase ZSI is reduced to VPN/3. However, the modulation index in this case is limited within 0.66 and 1. This is not a competitive solution for wide voltage range applications. The modified HERIC-based ZSI/ qZSI topologies with two extra controlled switches and diodes were

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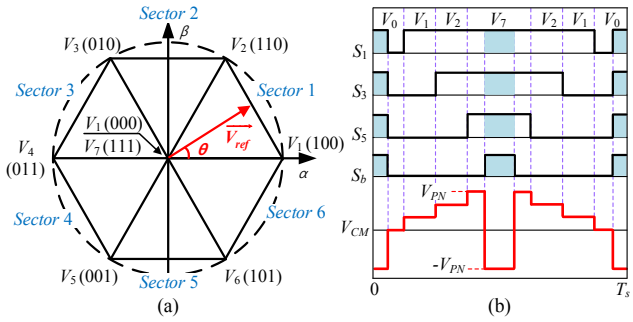

FIGURE 2. The SVM-based strategy for 2S-qSBI. (a) Space vector diagram; (b) Switching pattern of 2S-qSBI in sector 1.

TABLE I
CMV VALUES FOR DIFFERENT VECTORS OF 2S-QSBI

Vector	V_{CMV}	
	SVM Method	AZ-SVPWM Methods
$\overrightarrow{V_1}$, $\overrightarrow{V_3}$, $\overrightarrow{V_5}$ (Odd vectors)	$V_{PN}/3$	$V_{PN}/3$
$\overrightarrow{V_2}$, $\overrightarrow{V_4}$, $\overrightarrow{V_6}$ (Even vectors)	$2V_{PN}/3$	$2V_{PN}/3$
$\overrightarrow{V_0}$ (zero vector)	0	NA
$\overrightarrow{V_7}$ (zero vector)	V_{PN}	NA
$\overrightarrow{V_{sh}}$ (ST vector)	$-V_{PN}$	$-V_{PN}$

NA: Not applicable.

discussed in [32] to reduce the CMV/ CMC. Nevertheless, these solutions will cause a high voltage stress on semiconductor devices of the three-phase system. The qZSI T-type three-level inverter with CMV reduction has been proposed in [33]-[34], which consists of two qZSI modules and more active switches in the H-bridge circuit. Consequently, it results in high component-count and complex control when compared with a two-level inverter system. Similarly, the ZS four-leg inverter was presented in [35] to achieve constant CMV with complex control and high cost. The CMV reduction based on PWM modification for the three-phase qZSI was studied in [36]-[37]. The odd vectors were used to keep CMV constant, and the modulation index is really low in this method [36]. The method introduced in [37] can effectively reduce the leakage current. However, a notch filter should be added to the system, and the CMV waveform is not improved so much when compared with the conventional SVM method. Currently, there is not any work that discusses the CMV problems of three-phase transformerless PV qSBI systems.

The objective of this paper is to propose novel AZ-SVPWM schemes in a modified 2S-qSBI (M2S-qSBI). In the M2S-qSBI, an extra inductor is connected to the negative terminal of the PV panels. However, the total inductance value of the qSB inductors in the M2S-qSBI is equal to that of the qSB inductor in the conventional 2S-qSBI. Like conventional SVM, the proposed CMV reduction strategies can operate with a modulation index up to 1. In these proposed methods, the ST states are inserted within zero vector interval time to guarantee voltage boosting and also to reduce the output voltage distortion. Furthermore, the M2S-qSBI with the proposed modulation is considered with competitive solutions in PV applications due to its continuous input current characteristic and relatively wide voltage range operation. The proposed PWM methods are also useful for other topologies such as the continuous input current qSBI/ qZSI in [12]-[13].

II. SVM SCHEMES FOR TWO-SWITCH QUASI-SWITCHED BOOST INVERTER

A. CONVENTIONAL SVM SCHEME FOR 2S-qSBI

In a conventional SVM method, six active vectors ($\overrightarrow{V_1} - \overrightarrow{V_6}$) and two zero vectors ($\overrightarrow{V_0}$ and $\overrightarrow{V_7}$) are used to synthesize reference vector. Like the qSBI, the 2S-qSBI has two operating modes: One is the ST mode, where at least one H-bridge leg is turned on; and the other one is the non-ST mode, where the 2S-qSBI works as a conventional VSI. In addition to the eight switching states of a VSI, the ST states are used for the 2S-qSBI. The ST states are inserted into the SVM for all H-bridge legs. Fig. 2 depicts the voltage space vectors for the 2S-qSBI. Moreover, the CMV for three phases *A*, *B*, and *C* is defined by the following equation.

$$V_{CM} = V_{NG} + \frac{(V_{AN} + V_{BN} + V_{CN})}{3}, \quad (1)$$

where V_{AN}, V_{BN}, and V_{CN} are the voltages between nodes *A*-*N*, *B*-*N*, and *C*-*N*, repectively.

To define the CMV of the 2S-qSBI, Table I shows the switching states and the CMV values. By using (1), the CMV value will be changed every time when a different space vector is used. The odd, even, and zero vectors are applied as the conventional SVM. It can be concluded that the peak-to-peak amplitude of CMV under the conventional SVM control is really high and equal to $2V_{PN}$. The high fluctuations in the CMV waveform cause a large leakage current in the grid-connected PV systems [5].

B. CONVENTIONAL AZ-SVPWM SCHEME FOR 2S-qSBI

In the AZ-SVPWMs, the modulation index can vary in full range like the conventional SVM strategy. The AZ-SVPWMs use the same active vectors to establish the reference voltage vector as the conventional SVM method. In detail, the active vectors are considered to synthesize the reference vector. By applying the AZ-SVPWM methods to the 2S-qSBI, the CMV values of the 2S-qSBI can be observed in Table I. However, the peak-to-peak amplitude of CMV in 2S-qSBI is still high and equal to $5V_{PN}/3$.

III. MODIFIED TWO-SWITCH QUASI-SWITCHED BOOST INVERTER (M2S-QSBI) FOR CMV REDUCTION

A. OPERATING PRINCIPLE OF M2S-QSBI

Fig. 3(a) shows a M2S-qSBI with a reconfiguration of an input inductor in the qSB-network. Consequently, one more inductor is connected to the negative side of the DC input source. Like the 2S-qSBI, the M2S-qSBI has two modes of operation, as seen in Figs. 3(b)-3(c). The ST state is brought into the circuit by applying the ST pulses to switch S_b and all

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switches of H-bridge inverter. The following equations are obtained as

$$\begin{cases} v_{L1} = L_1 \dfrac{di_{in}}{dt} = \dfrac{L_1(V_i + V_C)}{L_1 + L_2} \\ v_{L2} = L_2 \dfrac{di_{in}}{dt} = \dfrac{L_2(V_i + V_C)}{L_1 + L_2} \\ C\dfrac{dV_C}{dt} = -I_{in}, \end{cases} \tag{2}$$

On the other hand, when the inverter is operated under the non-ST mode, switch S_b is turned off, and switch S_a is turned on. The following equations are obtained for this operating mode

$$\begin{cases} v_{L1} = L_1 \dfrac{di_{in}}{dt} = \dfrac{L_1(V_i - V_C)}{L_1 + L_2} \\ v_{L2} = L_2 \dfrac{di_{in}}{dt} = \dfrac{L_2(V_i - V_C)}{L_1 + L_2} \\ C\dfrac{dV_C}{dt} = I_{in} - i_{PN}, \end{cases} \tag{3}$$

In the steady-state analysis, the DC-link voltage, V_{PN} and the average input current are defined as

$$\begin{cases} V_{PN} = V_C = \dfrac{V_i}{1 - 2D_{ST}} \\ I_L = \dfrac{(1 - D_{ST})i_{PN}}{1 - 2D_{ST}}, \end{cases} \tag{4}$$

where D_{ST} is the ST duty cycle.

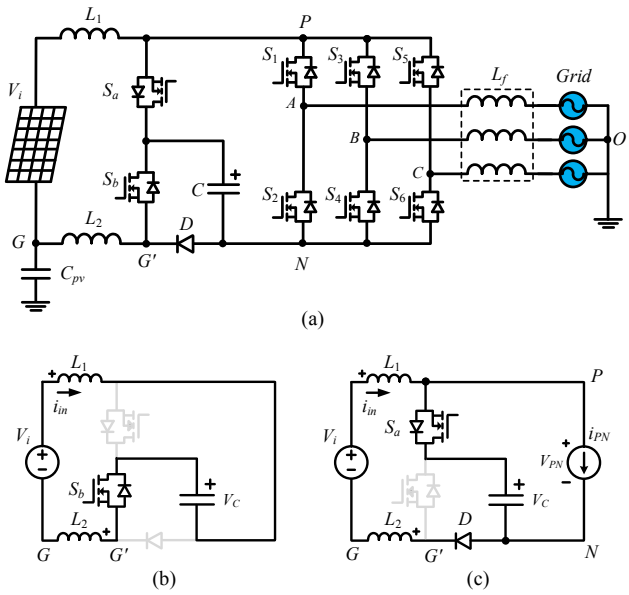

FIGURE 3. Three-phase M2S-qSBI. (a) Main circuit, and it's equivalent circuits during (b) ST mode and (c) non-ST mode.

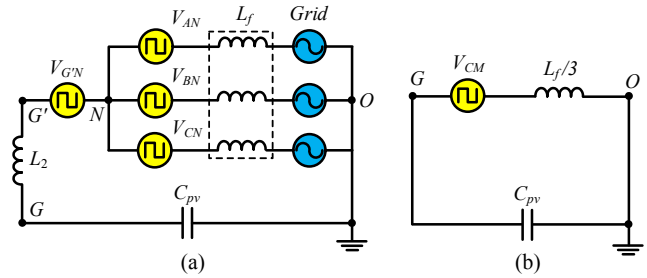

FIGURE 4. Common-mode model of three-phase M2S-qSBI. (a) Equivalent model and (b) Simplified model.

TABLE II
CMV VALUES FOR M2S-QSBI WITH K = 2/3 AND 5/6

Vector	CMV (k = 2/3)	CMV (k = 5/6)
Odd vectors	$2V_i/3 - V_{PN}/3$	$5V_i/6 - V_{PN}/2$
Even vectors	$2V_i/3$	$5V_i/6 - V_{PN}/6$
ST vector	$2V_i/3 - V_{PN}/3$	$5V_i/6 - V_{PN}/6$

B. COMMON-MODE MODEL

From Fig. 3(a), the common-mode loop model of the three-phase M2S-qSBI PV system is obtained. The equivalent and simplified CMV loop models of the M2S-qSBI system are drawn in Fig. 4(a) and Fig. 4(b), respectively. The voltage between nodes N and G is the total voltage of $V_{NG'}$ and V_{L2}. From the values in Table I, V_{NG} can be given by

$$V_{NG} = \begin{cases} kV_i + (k-1)V_{PN} & \text{ST state} \\ k(V_i - V_{PN}) & \text{Non-ST state,} \end{cases} \tag{5}$$

where $k = L_2/(L_1+L_2)$ and $k \in [0, 1)$.

The CMV (V_{CM}) of the M2S-qSBI can be determined as follows

$$V_{CM} = V_{OG} = V_{ON} + V_{NG}. \tag{6}$$

C. CMV ANALYSIS FOR M2S-QSBI

From (5) and (6), the CMV values in switching states of the M2S-qSBI can be derived. When ST states are not applied to the M2S-qSBI, the CMV of M2S-qSBI is generated as that of the mentioned AZ-SVPWM methods. The CMV of M2S-qSBI in non-ST states is as follows

$$V_{CM} = \begin{cases} \dfrac{V_C}{3} + k(V_i - V_C) \\ \dfrac{2V_C}{3} + k(V_i - V_C). \end{cases} \tag{7}$$

According to (7), the variation of CMV is $V_{PN}/3$ with all values of k.

In contrast, when the ST states are inserted into two opposite active vectors, one higher level of the CMV appears in each ST state. Thus, the CMV will increase when the ST state is used. The CMV of M2S-qSBI with ST states insertion can be rewritten

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$$V_{CM}=\begin{cases}-V_{PN}+k\left(V_i+V_{PN}\right) & \text{in ST vector}\\ \dfrac{V_{PN}}{3}+k\left(V_i-V_{PN}\right) & \text{in odd vectors}\\ \dfrac{2V_{PN}}{3}+k\left(V_i-V_{PN}\right) & \text{in even vectors,}\end{cases} \tag{8}$$

From (8), it can be seen that the variation value of CMV can be minimined by using the optimal value of ratio k. To keep the CMV variation in a low value of $V_{PN}/3$, the value of k should be 2/3 or 5/6. Table II shows the CMV of the M2S-qSBI with k = 2/3 and 5/6.

IV. IMPLEMENT OF THE PROPOSED AZ-SVPWM SCHEMES FOR M2S-QSBI

In the conventional AZ-SVPWM-1 and 3 methods, the number of commutations within a PWM cycle are six, while it is ten in the conventional AZ-SVPWM-2 method, which leads to occur high switching loss of H-bridge switches. Moreover, the AZ-SVPWM-2 and 3 methods need to have the simultaneous commutations in different legs of the H-bridge. This is difficult to realize in practice because these are the time delay differences between gate drivers and non-ideal semiconductor devices [25]-[27]. Thus, the proposed CMV reduction solution for the M2S-qSBI is based on the AZ-SVPWM-1 method. The M2S-qSBI reference voltage vector is determined as

$$\overrightarrow{V_{ref}}=\overrightarrow{V_1}\frac{T_1}{T_s}+\overrightarrow{V_2}\frac{T_2}{T_s}+\overrightarrow{V_3}\frac{T_z}{2T_s}+\overrightarrow{V_6}\frac{T_z}{2T_s}, \tag{9}$$

where T_1, T_2, and T_s are the time intervals of vectors $\overrightarrow{V_1}$ and $\overrightarrow{V_2}$, and the control cycle, respectively. T_z is the total time intervals of $\overrightarrow{V_3}$ and $\overrightarrow{V_6}$.

The time intervals of $\overrightarrow{V_1}$, $\overrightarrow{V_2}$, $\overrightarrow{V_3}$, and $\overrightarrow{V_6}$ can be found as

$$\begin{cases}T_1=M\cdot T_s\cdot\sin(\dfrac{\pi}{3}-\theta)\\ T_2=M\cdot T_s\cdot\sin(\theta)\\ T_z=T_s-T_1-T_2,\end{cases} \tag{10}$$

where θ is the inclined angle.

The modulation index, M, is defined as

$$M=\sqrt{3}V_{ref}/V_{PN}, \tag{11}$$

where V_{ref} is the peak value of the output phase voltage.

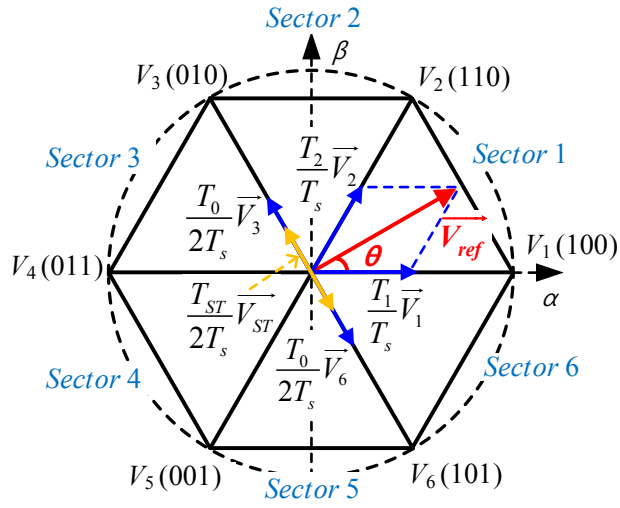

FIGURE 5. Space vector diagram of the proposed AZST-SVM method for M2S-qSBI.

A. AZSVM-BASED STRATEGY FOR M2S-QSBI IN NON-ST STATES

Taking sector 1 as an example, AZ-SVPWM-1 utilizes the sequence as V_3–V_2–V_1–V_6–V_1–V_2–V_3, involving only 60° jumps during every commutation. As mentioned in the conventional AZ-SVPWM-1 scheme for the M2S-qSBI in the non-ST state, two opposite vectors $\overrightarrow{V_3}$ and $\overrightarrow{V_6}$ are used to replace $\overrightarrow{V_0}$. Therefore, the dwell times of $\overrightarrow{V_3}$ and $\overrightarrow{V_6}$ can be calculated as $T_3 = T_6 = T_z/2$. Based on (7), the variation of CMV is always equal to $V_{PN}/3$. Because the ST states are not employed, the M2S-qSBI under conventional AZ-SVPWM-1 modulation operates in a buck mode.

B. INSERTION OF ST STATES

When the ST states are considered being inserted into the aforementioned switching sequences, the M2S-qSBI has six active vectors, and one additional ST vector. For the M2S-qSBI, the space vector diagram of the proposed ST-insertion-based AZ-SVPWM (AZST-SVM) scheme is demonstrated in Fig. 5. Regarding the aforementioned space vector diagram, the ST states are inserted into two near opposing active vectors $\overrightarrow{V_3}$ and $\overrightarrow{V_6}$. The switching sequences in the other sectors of the proposed AZST-SVMs can be also obtained in Table III. Referring to (9), the modified volt-second balance principle can be determined as

$$\begin{cases}\overrightarrow{V_{ref}}=\overrightarrow{V_1}\dfrac{T_1}{T_s}+\overrightarrow{V_2}\dfrac{T_2}{T_s}+\overrightarrow{V_3}\dfrac{T_0}{2T_s}+\overrightarrow{V_6}\dfrac{T_0}{2T_s}+\overrightarrow{V_{ST}}\dfrac{T_{ST}}{T_s}\\ T_s=T_1+T_2+T_0+T_{ST}.\end{cases} \tag{12}$$

where $\overrightarrow{V_{sh}}$ and T_0 is the ST voltage vector and total time intervals of $\overrightarrow{V_3}$, $\overrightarrow{V_6}$ after the ST state insertion.

The dwell times of $\overrightarrow{V_1}$, $\overrightarrow{V_2}$, $\overrightarrow{V_3}$ and $\overrightarrow{V_6}$ can be rewritte

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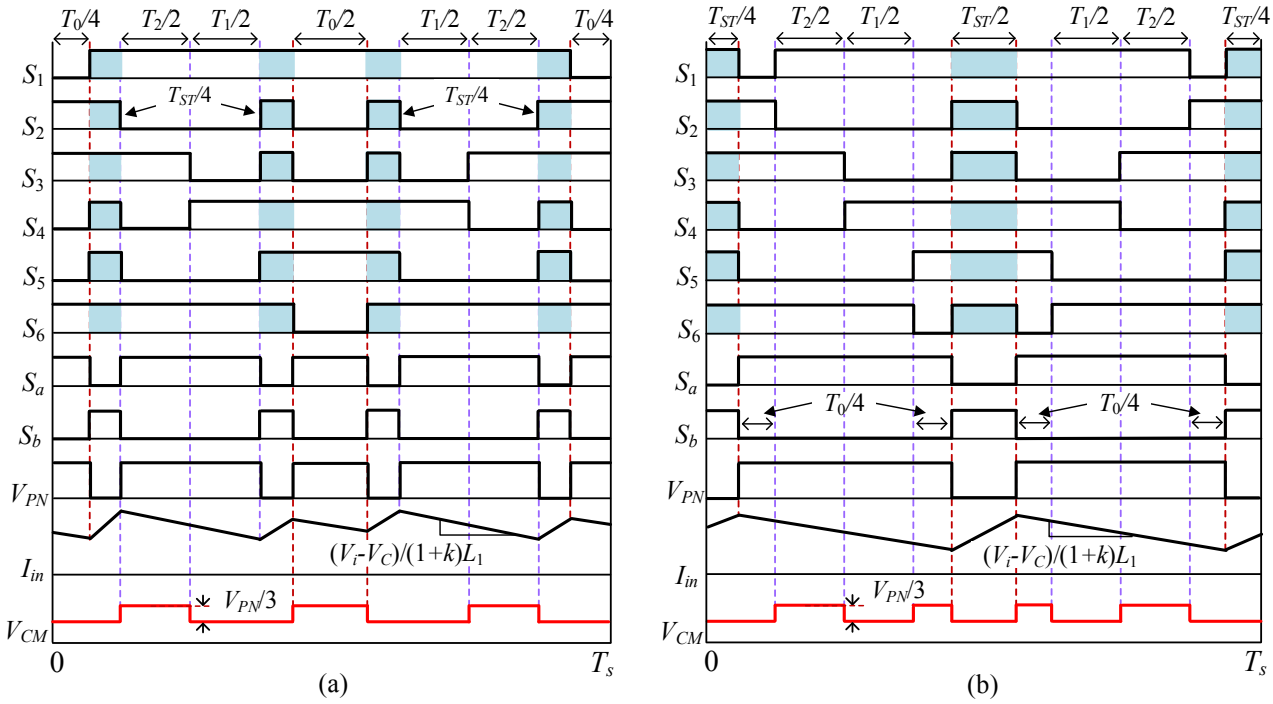

FIGURE 6. Switching sequences of the proposed AZST-SVM methods with k = 2/3 for M2S-qSBI in Sector 1. (a) AZST-SVM4, and (b) AZST-SVM2.

TABLE III
SWITCHING SEQUENCES OF THE PROPOSED AZST-SVMS

Sector	Switching sequence	
	Proposed AZST-SVM4	Proposed AZST-SVM2
1	V_3–V_{ST}–V_2–V_1–V_{ST}–V_6–V_{ST}–V_1–V_2–V_{ST}–V_3	V_{ST}–V_3–V_2–V_1–V_6–V_{ST}–V_6–V_1–V_2–V_3–V_{ST}
2	V_1–V_{ST}–V_2–V_3–V_{ST}–V_4–V_{ST}–V_3–V_2–V_{ST}–V_1	V_{ST}–V_1–V_2–V_3–V_4–V_{ST}–V_4–V_3–V_2–V_1–V_{ST}
3	V_5–V_{ST}–V_4–V_3–V_{ST}–V_2–V_{ST}–V_3–V_4–V_{ST}–V_5	V_{ST}–V_5–V_4–V_3–V_2–V_{ST}–V_2–V_3–V_4–V_5–V_{ST}
4	V_3–V_{ST}–V_4–V_5–V_{ST}–V_6–V_{ST}–V_5–V_4–V_{ST}–V_3	V_{ST}–V_3–V_4–V_5–V_6–V_{ST}–V_6–V_5–V_4–V_3–V_{ST}
5	V_1–V_{ST}–V_6–V_5–V_{ST}–V_4–V_{ST}–V_5–V_6–V_{ST}–V_1	V_{ST}–V_1–V_6–V_5–V_4–V_{ST}–V_4–V_5–V_6–V_1–V_{ST}
6	V_5–V_{ST}–V_6–V_1–V_{ST}–V_2–V_{ST}–V_1–V_6–V_{ST}–V_5	V_{ST}–V_5–V_6–V_1–V_2–V_{ST}–V_2–V_1–V_6–V_5–V_{ST}

$$\begin{cases} T_1 = M \cdot T_s \cdot \sin(\dfrac{\pi}{3} - \theta) \\ T_2 = M \cdot T_s \cdot \sin(\theta) \\ T_3 = T_6 = \dfrac{T_0}{2} = \dfrac{T_z - T_{ST}}{2}, \end{cases} \tag{13}$$

where T_{ST} is the interval time of ST state, and $T_{ST} = D_{ST}T_s$.

Fig. 6 illustrates the different types of ST insertion switching patterns for the M2S-qSBI with k = 2/3 as an example. In the proposed AZST-SVM4 method, the desired total ST is equally divided into four parts per one control cycle and the value of time interval is equal to $T_{ST}/4$, as seen in Fig. 6(a). On the other way, the proposed AZST-SVM2 method has two parts per one control cycle, and the time interval of each part is $T_{ST}/2$. When compared with the proposed AZST-SVM4 method, the switching loss on switches with the AZST-SVM2 method can be reduced. However, the peak-to-peak input current ripple of the M2S-qSBI under the proposed AZST-SVM2 method is higher than that under the proposed AZST-SVM4 method.

As described in [9], the modulation index and the desired total ST duty cycle should be satisfied as

$$M + D_{sh} \le 1. \tag{14}$$

In order to ease the process of switching state selection, the switching sequences of the proposed AZST-SVM methods are summarized in Tables III. Note that, the ST-state insertion is applied to all switches of H-bridge inverter.

V. PARAMETER DESIGN OF M2S-QSBI

A. INDUCTANCE SELECTION

In the design guideline, the inductance selection is only based on the high-frequency ripple requirement. From Fig. 6, the peak-to-peak ripple inductor current with the proposed AZST-SVM4 and AZST-SVM2 methods are the largest in the non-ST states. From (3), we have the equation for the AZST-SVM methods as

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TABLE IV
PARAMETERS FOR POWER LOSS CALCULATION

Parameters	M2S-qSBI
Inductors	r_{L1} = 0.12 Ω and r_{L2} = 0.24 Ω Core part number: CM777125 (142 nH/N^2)
ESR of capacitor	240 mΩ
Switches	IPW60R045CPA (600 V, 60 A, R_{DSon} = 45 mΩ)
Diode	DSEC60-06A (600 V, 30 A, V_F = 1.6 V)

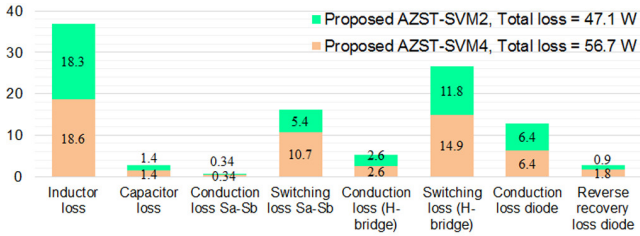

FIGURE 7. Power loss contribution of M2S-qSBI under the proposed AZST-SVMs.

$$(1+k)L_1\frac{di_{in}}{dt}=V_i-V_C. \tag{15}$$

Substituting (4) into (15), the inductance values of L_1 and L_2 in the proposed M2S-qSBI with the AZST-SVM4 method are calculated as

$$\begin{cases} L_1=\dfrac{D_{sh}\cdot M\cdot V_i\cdot(1-k)\cdot T_s}{(1-2D)\Delta I_L} \\ L_2=\dfrac{D_{sh}\cdot M\cdot V_i\cdot k\cdot T_s}{(1-2D)\Delta I_L}. \end{cases} \tag{16}$$

The inductance values of L_1 and L_2 in the proposed M2S-qSBI with the AZST-SVM2 method are determined as

$$\begin{cases} L_1=\dfrac{D_{sh}(1-D_{sh})\cdot(1-k)\cdot V_i\cdot T_s}{(1-2D)\Delta I_L} \\ L_2=\dfrac{D_{sh}(1-D_{sh})\cdot k\cdot V_i\cdot T_s}{(1-2D)\Delta I_L}, \end{cases} \tag{17}$$

where ΔI_L is the inductor ripple current.

From (16) and (17), it can be seen that the total of inductances L_1 and L_2 is equal to the inductor in qSB-network of the 2S-qSBI.

B. CAPACITANCE SELECTION

In the proposed AZST-SVM4 method, the peak-to-peak voltage ripple of a capacitor during the non-ST time interval is the largest. On the other hand, the proposed AZST-SVM2 method produces the highest peak-to-peak voltage ripple under the ST state. From (2)-(4), the capacitance of the capacitor in the AZST-SVM methods can be given as

$$\begin{cases} C=\dfrac{D_{sh}\cdot P_o\cdot M\cdot T_s}{2(1-D_{sh})V_i\cdot\Delta V_C} & \text{for AZST-SVM4} \\ C=\dfrac{D_{sh}\cdot P_o\cdot T_s}{2V_i\cdot\Delta V_C} & \text{for AZST-SVM2.} \end{cases} \tag{18}$$

where ΔV_C and P_o are the given capacitor voltage ripple and the output power, respectively.

C. SWITCHING LOSS ANALYSIS

To verify the characteristic of the proposed AZST-SVMs for M2S-qSBI, the power loss analysis is also determined. The power losses of the power switches, diodes, inductors, and capacitor are calculated as presented in [13], [16]. Because the conducting time and conducting current of the proposed AZST-SVM4 are the same as the proposed AZST-SVM2, only the switching loss of the semiconductor devices is presented in this section to perform the power loss analysis. The switching losses of MOSFETs in the proposed AZST-SVM4 are calculated as

$$\begin{cases} P_{SW\_Sa}=V_{PN}\cdot(I_{in}-i_o)\cdot 4f_S\cdot\dfrac{t_{on\_S}+t_{off\_S}}{2} \\ P_{con\_Sb}=V_{PN}\cdot I_{in}\cdot 4f_S\cdot\dfrac{t_{on\_S}+t_{off\_S}}{2} \\ P_{sw\_H}=\dfrac{3}{\pi}\displaystyle\int_0^{\pi}V_{PN}\cdot i_o\cdot\frac{t_{on\_S}+t_{off\_S}}{2}\cdot f_s\cdot d\omega t \\ \quad +8\cdot V_{PN}\cdot\dfrac{I_{in}}{3}\cdot f_s\cdot\dfrac{t_{on\_S}+t_{off\_S}}{2}+3\cdot Q_{rrb}\cdot V_{PN}\cdot f_s, \end{cases} \tag{19}$$

The switching losses of MOSFETs in the proposed AZST-SVM2 are given

$$\begin{cases} P_{sw\_Sa}=V_{PN}\cdot(I_{in}-i_o)\cdot 2f_s\cdot\dfrac{t_{on\_S}+t_{off\_S}}{2} \\ P_{sw\_Sb}=V_{PN}\cdot I_{in}\cdot 2f_s\cdot\dfrac{t_{on\_S}+t_{off\_S}}{2} \\ P_{SW\_H}=\dfrac{3}{\pi}\displaystyle\int_0^{\pi}V_{PN}\cdot i_o\cdot\frac{t_{on\_S}+t_{off\_S}}{2}\cdot f_s\cdot d\omega t \\ \quad +6\cdot V_{PN}\cdot\dfrac{I_{in}}{3}\cdot f_s\cdot\dfrac{t_{on\_S}+t_{off\_S}}{2}+3\cdot Q_{rrb}\cdot V_{PN}\cdot f_s, \end{cases} \tag{20}$$

where f_s, t_{on_S}, t_{off_S} are the switching frequency, the turn-on and turn-off delay times of MOSFET S_a and S_b, respectively.

The switching loss of the diode is determined

$$\begin{cases} P_{rrD}=Q_{rr}\cdot V_{PN}\cdot 4f_s, & \text{for AZST-SVM4} \\ P_{rrD}=Q_{rr}\cdot V_{PN}\cdot 2f_s, & \text{for AZST-SVM2.} \end{cases} \tag{21}$$

Table IV shows the parameters of the M2S-qSBI with the proposed AZST-SVMs for power loss calculation. Based on the parameters given in Tables IV, the power loss can be calculated. The input voltage and switching frequency are 250 V and 10 kHz, whereas the output phase voltage is 110 Vrms. Fig. 7 shows the power loss breakdown comparison between the two proposed methods when V_i = 250 V, f_s = 10 kHz, V_o = 110 Vrms and P_o = 1100 W. As shown in Fig. 7, the conduction loss of component in AZST-SVM4 is equal to that of AZST-SVM2. This is because the component conduction times in both the proposed methods are the same. However, the total loss of the AZST-SVM4 is higher than

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TABLE V
PARAMETERS USED FOR SIMULATION AND EXPERIMENT

Parameters		Values
Input voltage range		150 V ~ 350 V
Operating input voltage		250 V
DC-link voltage		360 V
Output power rating		1.1 kW
Output phase voltage		110 Vrms/ 50 Hz
Inductors	L_1	1 mH
	L_2	2 mH
	L_f	1.5 mH
Capacitors	C	470 µF/ 400 V
	C_f	20 µF
PWM carrier frequency		10 kHz

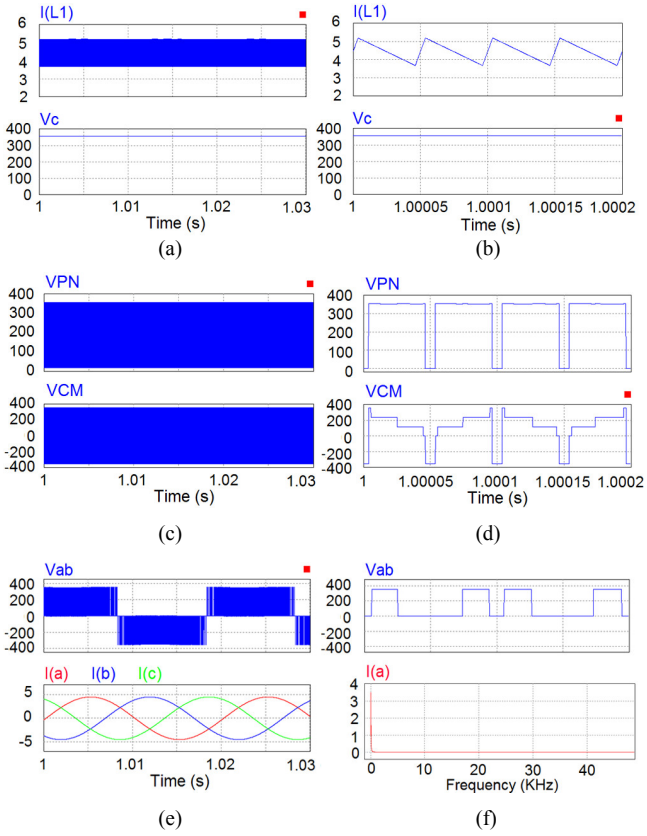

FIGURE 8. Simulation results of 2S-qSBI under the conventional SVM method. (a)-(b) Input current, qSB capacitor-*C* voltage, (c)-(d) DC-link voltage, common-mode voltage, (e) v_{ab} voltage, output currents, and (f) an enlargement of v_{ab} and FFT of i_a.

that of the AZST-SVM2 because the switching loss of the AZST-SVM4 is higher than that of the AZST-SVM2. In the proposed AZST-SVM4, the total ST state is divided into four parts per one control cycle, but it is only two parts per one control cycle in the proposed AZST-SVM2.

VI. SIMULATION AND EXPERIMENTAL VERIFICATIONS

A. SIMULATION RESULTS

In order to validate the effectiveness of the M2S-qSBI with the proposed AZST-SVM methods, PSIM simulation studies are carried out. The system parameters used for simulation are summarized in Table V. From Table V, $k = 2/3$ is taken as a default value, the qSB-inductance values are chosen 1 mH and 2 mH, while the qSB-capacitor is 470 µF. The sampling time is 100 µs. The ON-resistance of MOSFET is

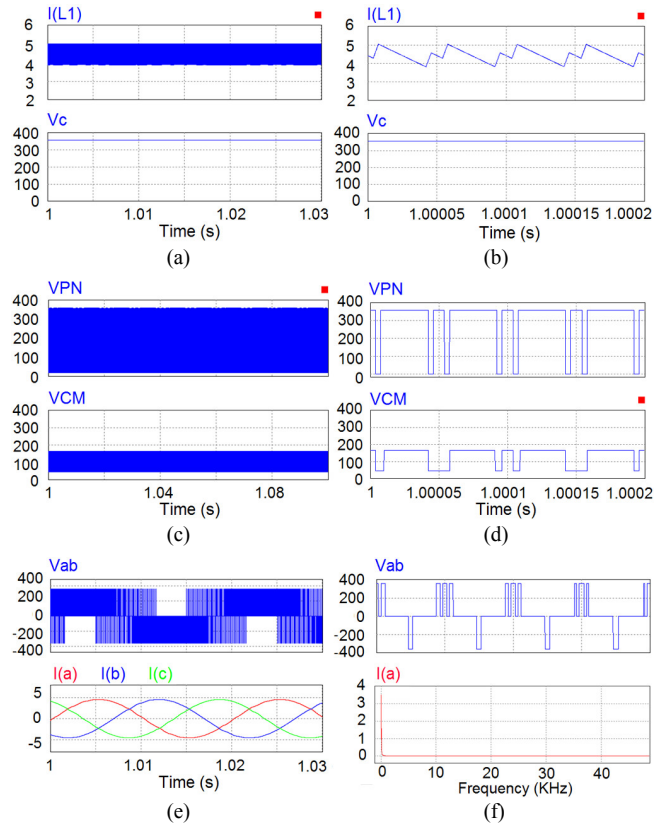

FIGURE 9. Simulation results of M2S-qSBI under the proposed AZST-SVM4 method. (a)-(b) Input current, qSB capacitor-C voltage, (c)-(d) DC-link voltage, common-mode voltage, (e) v_{ab} voltage, output currents, and (f) an enlargement of v_{ab} and FFT of i_a.

set to 45 mΩ for all switches, and the voltage drop on diodes is set to 1.6 V.

First, an inductive load with $R_l = 35\ \Omega$ and $L_l = 8$ mH is used to test the 2S-qSBI and M2S-qSBI. The LC-filter consisting of $L_f = 1.5$ mH and $C_f = 20$ µF is connected to the output of the inverter. Simulation waveforms of the input current, DC-link voltage, output v_{ab} voltage, and output currents are depicted by Figs. 8-10. For the 2S-qSBI with the conventional SVM, the input voltage is 250 V and the ST duty cycle of 0.16 is executed to generate 360 V DC-link voltage. The modulation index of 0.78 is set to produce an output phase voltage of 110 Vrms, as shown in Fig. 7. From Fig. 8(e), the RMS and THD values of the output currents are measured 3.26 A and 1.15%, respectively. The CMV of the 2S-qSBI with under the conventional SVM methods is 709 V, as depicted in Fig. 8(d). For both the proposed AZST-SVM methods, the applied input voltage is also 250 V; hence, an ST duty cycle and modulation index, are 0.16 and 0.78, respectively. It can be seen that the input current ripple of the M2S-qSBI with the proposed AZST-SVM4 is lower than that with the AZST-SVM2 method, as shown in Figs. 9(b) and 10(b). The qSB-capacitor voltage is around 355 V, as given in Figs. 9(a) and 10(a). The CMV of the M2S-qSBI with under the AZST-SVM methods is 117 V that is equal to 33.3% of the DC-link voltage, as shown in Figs. 9(c) and 10(c). The RMS and THD values of the output currents are around 3.25 A and 1.29%, respectively.

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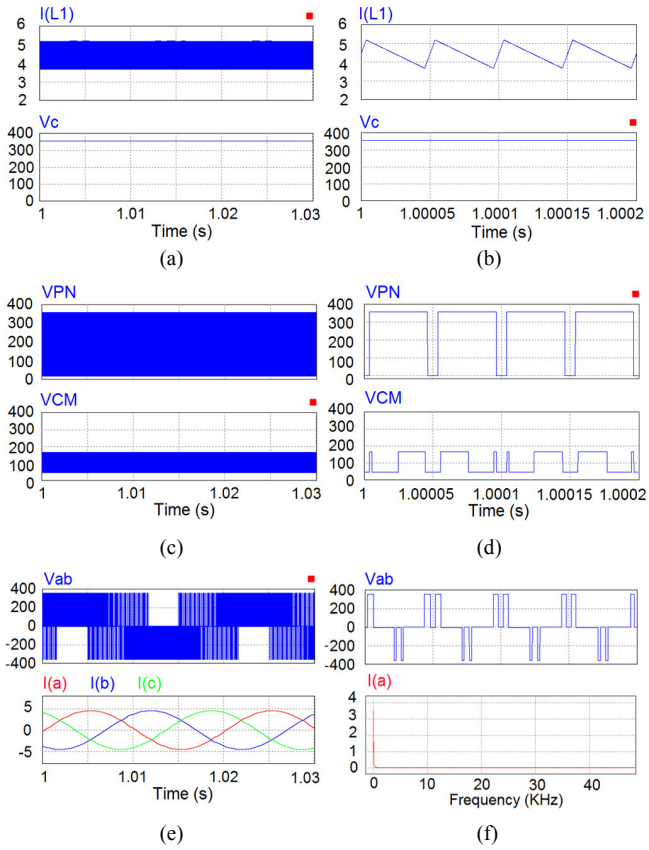

FIGURE 10. Simulation results of M2S-qSBI under the proposed AZST-SVM2 method. (a)-(b) Input current, qSB capacitor-*C* voltage, (c)-(d) DC-link voltage, common-mode voltage, (e) v_{ab} voltage, output currents, and (f) an enlargement of v_{ab} and FFT of i_a.

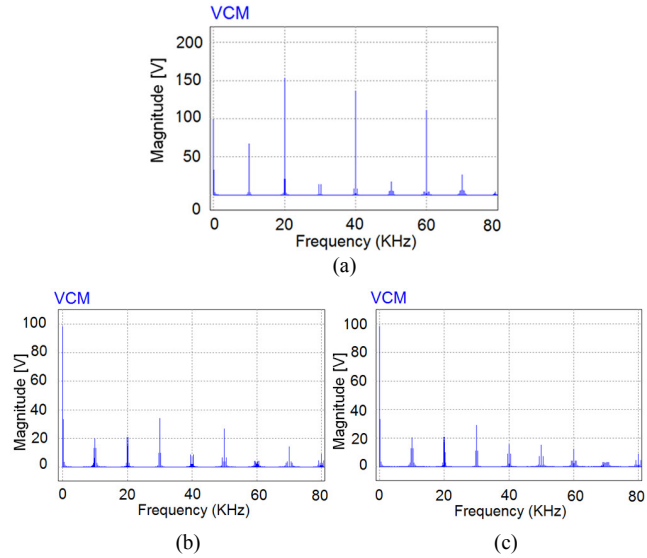

FIGURE 11. FFT of CMV: (a) the 2S-qSBI under the conventional SVM, M2S-qSBI under (b) the proposed AZST-SVM4, and (c) the proposed AZST-SVM2 methods.

Fig. 11 demonstrates the fast Fourier transform (FFT) spectrum of CMV of the conventional SVM-based 2S-qSBI the M2S-qSBI under the various modulation methods. It can be observed that the amplitudes of CMV at high frequency

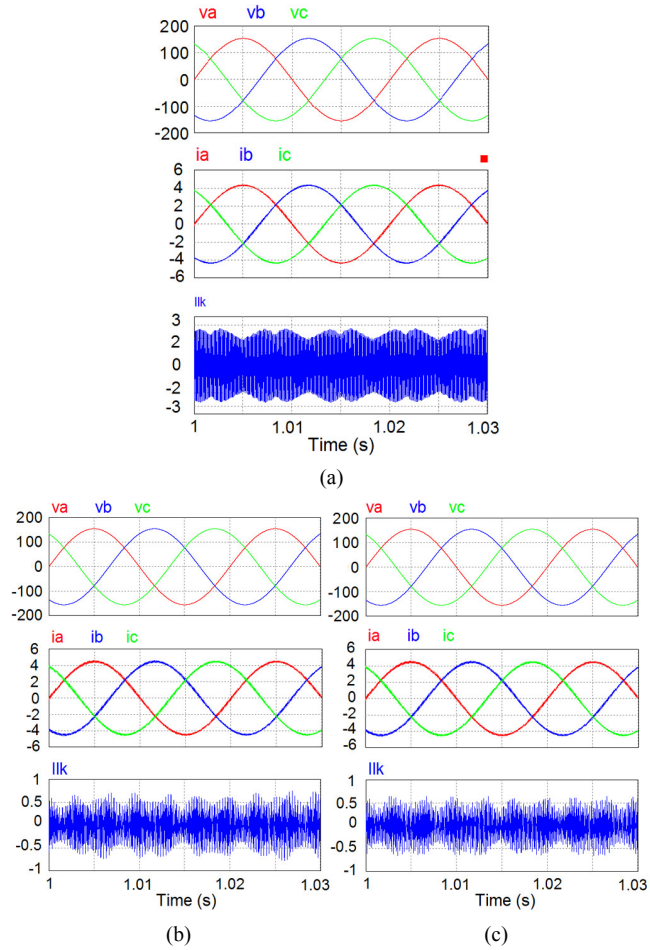

FIGURE 12. Grid voltage, output current, and leakage current for (a) the conventional SVM-based 2S-qSBI, (b) the proposed AZST-SVM4 and (c) the proposed AZST-SVM2 methods.

TABLE VI
COMPARISON RESULTS FOR SVM 2S-QSBI AND PROPOSED M2S-QSBI WITH AZST-SVM METHODS (BEFORE FILTER)

Method	M	ΔI_{in}	THD_i	THD_v	CMV
SVM	0.78	1.51 A	15.6%	79.7%	709 V
Proposed AZST-SVM4	0.78	1.2 A	23.2%	93.2%	117 V
Proposed AZST-SVM2	0.78	1.49 A	23.7%	93.3%	117 V

under the proposed modulation methods is low, which leads to reduce the leakage current.

Secondly, the 2S-qSBI and M2S-qSBI is tested in the grid connection mode. They are connected to the grid of 110 V/50 Hz. Three inductors L_f of 15 mH, as shown in Fig. 1 and Fig. 3, is connected between the grid and the inverter. The stray capacitor between the PV and ground C_{PV} is 220 nF. In the whole control system, the control of DC and AC sides are executed separately. For the DC-side control, the DC input voltage is measured and fed back through a low-pass filter to calculate the average value of the ST duty cycle, D_{ST}. This value is obtained according to the relationship of the peak value of the DC-link voltage and the DC input voltage, derived in (4). In the other word, the DC-link voltage is kept constant at 360 V. In order to connect to the grid, a phase-

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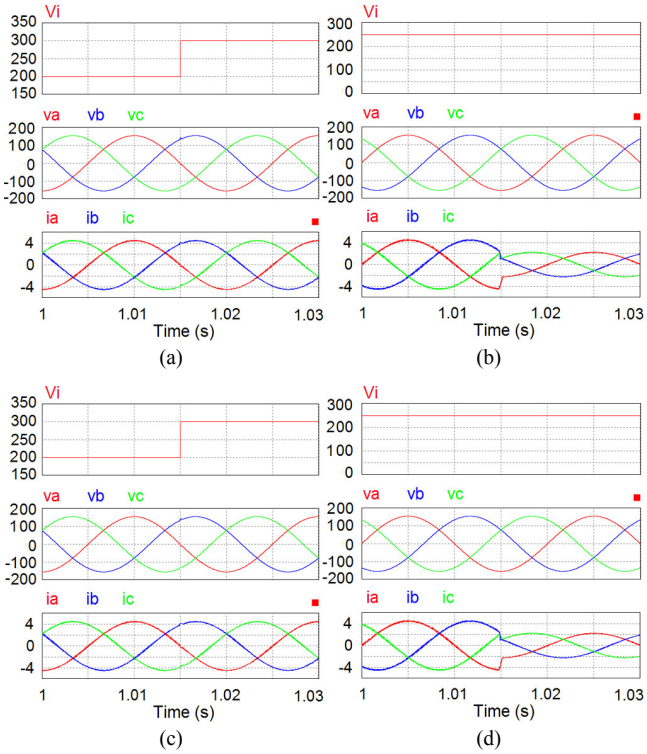

FIGURE 13. Simulation results of M2S-qSBI under the AZST-SVMs when the input voltage and load are changed. (a)-(b) Proposed AZST-SVM4; (c)-(d) Proposed AZST-SVM2.

locked loop based on *dq* transformation is derived for achieving synchronization with the grid. Fig. 12 provides the simulation results of the grid voltage and current and the leakage current under the conventional SVM-based 2S-qSBI and the M2S-qSBI with the proposed AZST-SVM methods. The root mean square (RMS) value of leakage current of the 2S-qSBI with the conventional SVM is 1.7 A. Due to the limited CMV, the RMS value of leakage current of the M2S-qSBI with the proposed AZST-SVM4 and AZST-SVM2 methods are 289 mA and 284 mA, respectively, which are lower than the permissible 300 mA stated in the VDE 0126-1-1 standard [38]. As depicted in Fig. 12, the output current THD value of the M2S-qSBI under the AZST-SVM4 and AZST-SVM2 methods is 2.2% and 2.3%, respectively. The THD values of M2S-qSBI under the proposed AZST-SVMs is higher than those of the SVM-based qSBI.

The simulation results comparison of the SVM-based 2S-qSBI and the M2S-qSBI with proposed AZST-SVM methods are summarized in Table VI. In general, the SVM-based 2S-qSBI and M2S-qSBI with the proposed AZST-SVM methods operate at $M = 0.78$ and $D_{ST} = 0.15$. The input current ripple of the M2S-qSBI with the proposed AZST-SVM4 method is lower than that with the proposed AZST-SVM2 method and SVM-based 2S-qSBI. This is because the number of ST-behaviors in the AZST-SVM4 is double that of AZST-SVM2 and conventional SVM. The output voltage and current THD values before the filter in the proposed M2S-qSBI with AZST-SVMs are higher than those in the SVM-based 2S-qSBI

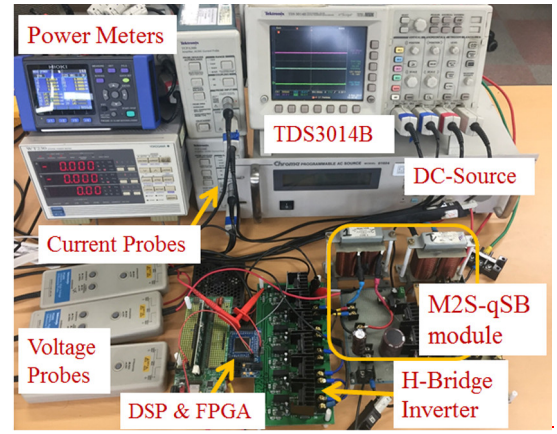

FIGURE 14. A picture of the experimental setup.

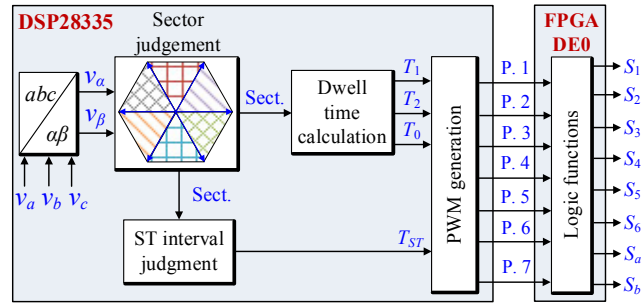

FIGURE 15. Implementation block diagram.

method. However, the peak-to-peak CMV value of the M2S-qSBI with the proposed AZST-SVM methods is significantly reduced to 117 V in comparison to 709 V in the SVM-based 2S-qSBI. Fig. 13 shows the dynamic responses of the M2S-qSBI with the proposed AZST-SVMs. As depicted in Figs. 13(a) and 13(c), the output power is kept at 1.1 kW when the input voltage suddenly jumps from 200 V to 300 V. Figs. 13(b) and 13(d) show the simulation waveforms when the output power increases from 500 W to 1.1 kW while the input voltage is kept at 250 V.

B. EXPERIMENTAL RESULTS

In order to evaluate the performance of the proposed AZST-SVM methods for the M2S-qSBI, a laboratory prototype of 1.1 kW three-phase 2S-qSBI and M2S-qSBI has been experimentally implemented. The modulation algorithms are implemented in discrete time using the TMS320F28335 DSP microcontroller, and the logic operations are executed by a DE0-Nano FPGA. Fig. 14 depicts a picture of the experimental setup. DSP TMS320F28335 and FPGA DE0 were used to generate the PWM1 to PWM7 signals as shown in Fig. 15. Three-phase AC reference voltages are sampled and transformed into DC components via *abc*/*αβ* transformation. In the proposed AZST-SVMs, based on Fig. 15, the sector number and shoot-through interval can be determined. According to (12) and (13), the dwell times of selected voltage vectors are calculated. Then, the switching sequences are decided, and the PWM generation block of DSP is executed.

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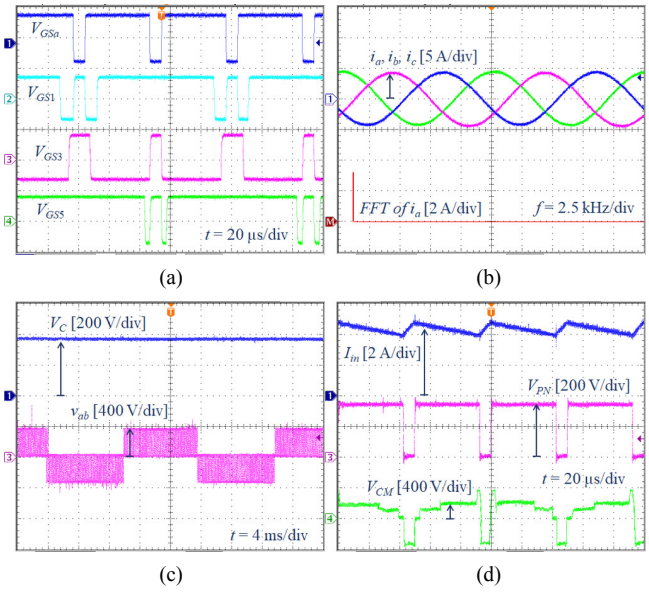

FIGURE 16. Experimental output waveforms of 2S-qSBI under the conventional SVM method. (a) Gate signals of S_a, S_1, S_3, and S_5; (b) output i_a, i_b, i_c currents and FFT spectrum; (c) qSB-capacitor voltage, line-to-line vab voltage; (d) input current, DC-link voltage, and common-mode voltage.

Finally, the control signals for switches are combined with the generated DSP PWM signals from FPGA DE0 to control the converter. Fig. 14 depicts a picture of the experimental setup. DSP TMS320F28335 and FPGA DE0 were used to generate the PWM1 to PWM7 signals as shown in Fig. 15. Three-phase AC reference voltages are sampled and transformed into DC components via abc/αβ transformation. In the proposed AZST-SVMs, based on Fig. 15, the sector number and shoot-through interval can be determined. According to (12) and (13), the dwell times of selected voltage vectors are calculated. Then, the switching sequences are decided, and the PWM generation block of DSP is executed. Finally, the control signals for switches are combined with the generated DSP PWM signals from FPGA DE0 to control the converter. The experiment used the same parameters as those in the simulation. Due to the limitation of the laboratory, only the inductive load is considered for validating the performance of the M2S-qSBI. Eight CoolMOS IPW60R045CPA MOSFETs are used for the switches, and DSEC60-06A is used for the qSB-diode. In the conventional SVM-based 2S-qSBI, one inductor of 3 mH was used to connect between the input DC-source and qSB-module, as presented in Fig. 1. As depicted in Fig. 16, the control signals of three upper switches are shown with the ST duty cycle of 0.16. The output currents are 3.4 A and their THD values are about 1.1%. As shown in Fig. 16(d), the CMV of the 2S-qSBI under the conventional SVM method varies from -352 V to 354 V, which is double of the DC-link voltage.

Figs. 17 and 18 show the experimental waveforms under the proposed AZST-SVM4 and AZST-SVM2 strategies, respectively. As highlighted in Fig. 17(a), the control signals of the upper switches are implemented with the ST states

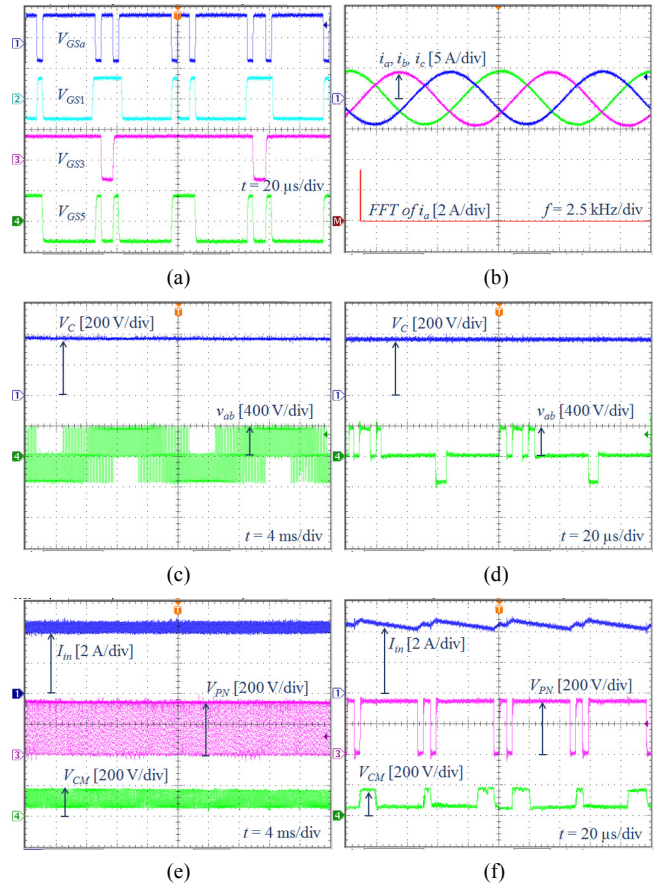

FIGURE 17. Experimental output waveforms of M2S-qSBI under the proposed AZST-SVM4 method. (a) Gate signals of S_a, S_1, S_3, and S_5; (b) output i_a, i_b, i_c currents and FFT spectrum; (c) qSB-capacitor voltage, line-to-line vab voltage; (d) an enlarge of (c); (e) input current, DC-link voltage, and common-mode voltage; (f) an enlarge of (e).

inserted in sector 3, and with the same order depicted in sector 1. Note that the desired total ST state is nearly equal to 0.16. The RMS values of the output currents are 3.3 A and their THD values are all about 1.5% in both the proposed AZST-SVM methods. The DC-link voltage of the M2S-qSBI under the proposed AZST-SVM methods is boosted to 357 V from the input voltage DC source of 250 V, as seen in Figs. 17(c) and 18(c). It can be observed that the input current ripple of the M2S-qSBI with the proposed AZST-SVM4 method is less than in the case of the proposed AZST-SVM2 method, as shown in Figs. 17(f) and 18(f). As demonstrated in Figs. 17(e) and 18(e), the CMV of the M2S-qSBI under the proposed AZST-SVM methods varies from 50 V to 169 V with a range of 119 V, which is 33.3% of the DC-link voltage. As shown in the zoomed-in view in Figs. 17(f) and 18(f), the CMV levels during powering states $\overrightarrow{V_1}$, $\overrightarrow{V_3}$, $\overrightarrow{V_5}$ and $\overrightarrow{V_{sh}}$ are fixed at 50 V. The CMV during powering states $\overrightarrow{V_2}$, $\overrightarrow{V_4}$, and $\overrightarrow{V_6}$ is 169 V. This is because the k value is selected as 2/3. If the k value is chosen at 5/6, the magnitude CMV of the proposed AZST-SVMs is also equal to 33% of the DC-link voltage. The good agreement can be seen between the simulation and experimental verifications, showing that the theoretical analysis used in the simulations are valid.

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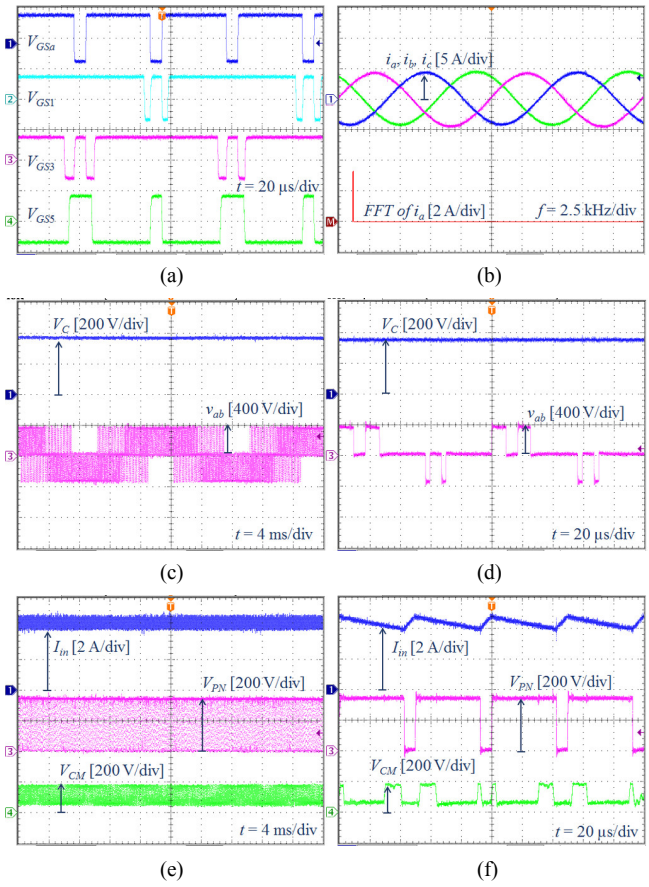

FIGURE 18. Experimental output waveforms of M2S-qSBI under the proposed AZST-SVM2 method. (a) Gate signals of S_a, S_1, S_3, and S_5; (b) output i_a, i_b, i_c currents and FFT spectrum; (c) qSB-capacitor voltage, line-to-line vab voltage; (d) an enlarge of (c); (e) input current, DC-link voltage, and common-mode voltage; (f) an enlarge of (e).

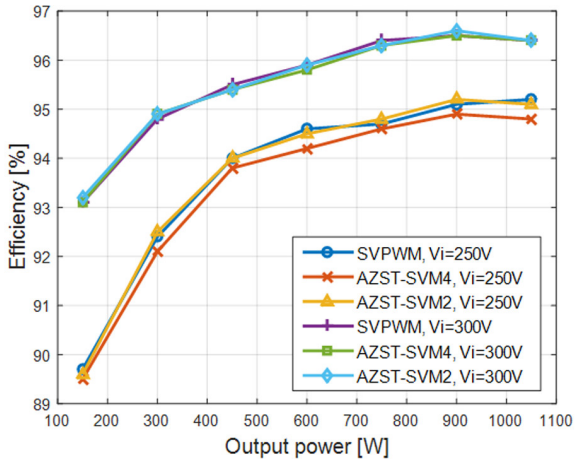

FIGURE 19. Efficiency measurement of the M2S-qSBI under proposed AZST-SVM methods.

Fig. 19 shows the efficiency measurements for both the conventional SVM-based 2S-qSBI and the proposed AZST-SVM methods at the same input voltage and the same conditions specified in Table III. In the case of the conventional SVM, the efficiency is about the same as the proposed AZST-SVM2. The maximum efficiency at the input voltage of 300 V of the proposed AZST-SVM4 and AZST-SVM2 methods are 96.5% and 96.7%, respectively. It can be seen that the efficiency of the proposed AZST-SVM2 method is slightly higher than that of the proposed AZST-SVM4 method. This is because the proposed AZST-SVM4 gets a higher switching loss caused by the ST states.

VII. CONCLUSION

In this paper, two modulation strategies have been proposed for a three-phase M2S-qSBI PV system to reduce the CMV. By using the introduced CMVR strategies, the instantaneous peak-to-peak of CMV is approximately 33.33% of the DC-link voltage. The proposed AZST-SVM methods can be implemented like a conventional SVM by adding ST states to the space vectors. In the M2S-qSBI, the CMV in both the proposed AZST-SVM methods is equal to 16.67% of the CMV in the conventional SVM-based 2S-qSBI. However, the proposed AZST-SVMs have a higher THD level of the output voltage and current than those of the conventional SVM. Moreover, compared with the proposed AZST-SVM2 method, the proposed AZST-SVM4 method has a lower peak-to-peak input current ripple. However, the efficiency of the proposed AZST-SVM2 method is slightly higher than that of the proposed AZST-SVM4 method. The M2S-qSBI under the both proposed AZST-SVM methods has been analyzed and simulated using a PSIM model. Finally, a 1.1-kW three-phase inverter prototype has been implemented. The actual experimental results have validated the proposed approaches and theoretical analysis.

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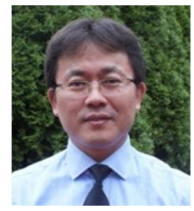

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