A 100 GBPS LDPC DECODER FOR THE IEEE 802.11AY

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Introduction

802.11ay is the amendment to the 802.11 standard that enables Wi-Fi devices to achieve 100 Gbps using the unlicensed mm-Wave (60 GHz) band at comparable ranges to todays commercial 60 GHz devices based on the 802.11ad standard.

The target throughput in 802.11ay single stream is 44 Gbps for 256-QAM, while 176 Gbps for MIMO 4 streams.

The QC LDPC codes for 802.11ay is derived from 802.11ad by lifting. There are two code length 672, 1344, each has 5 different rates.

The goal of the work is to design a standard compliant LDPC decoder for 802.11ay with high throughput, high energy and area efficiency.

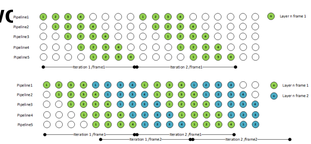
Background/SOA

➢ **A. Full row parallel layered decoding**

- check node parallelism = Z
- bit node parallelism = N
- pipelined architecture
- Converge speed Niter

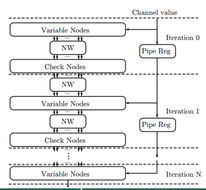
➢ **B. Frame interleaved two**

- check node parallelism = Z
- bit node parallelism = N
- pipelined architecture
- 2 frames interleaved
- Converge speed 2*Niter



➢ **C. Unrolling two-phase decoding**

- check node parallelism = N-K
- bit node parallelism = N
- pipelined architecture
- HW unrolled for different iteration
- Converge speed 2*Niter



	A	B	C
Throughput @ N=1K 28nm	Multi-Gbps	Multi-Gbps to 10s Gbps	100s Gbps
Flexibility in rate	Yes	Yes	NO
code length	No limitation	No limitation	1-2K
Early termination	Yes	Yes	Difficult

Table 1. SOA comparison

Methods

➢ **Frame interleaved architecture for layered decoding**

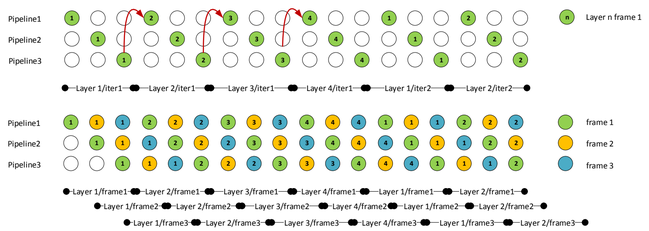


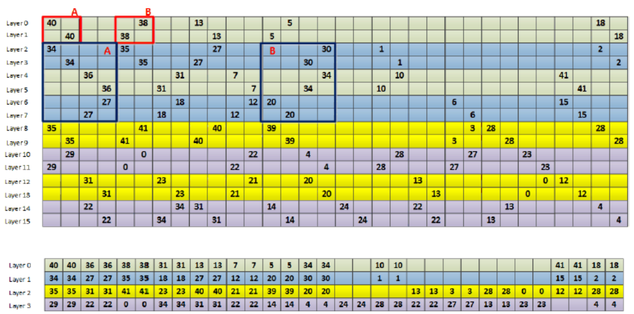
Figure 1. timing of full row parallel layered decoding normal vs. frame interleaved

☺Layered decoding requires less storage than two phase decoding
☺Layered decoding has fast convergence speed than two phase decoding
☺Frame interleaved schedule increases pipeline utilization hence increase throughput
☺Frame interleaved schedule increases HW utilization. Logic is shared for 3 frames, hence increase area and energy efficiency

➢ **Compress layers**

$$Throughput = \frac{N_{frame} * N * CLK_{frequency}}{N_{layer} * N_{pipeline\ stage} * N_{iteration}}$$

☹ Problem: Throughput drops at low rate



☺By adding simple switch network, several layers can be compressed. HW only take N_pipeline cycles to process message passing for 4 layers.

➢ **Advanced technology**

New technology (e.g. 16nm and 7nm) brings smaller area, higher clock speed and low power.
Eg. compared to TSMC's 20nm SoC process, 16/12nm is 50 % faster and consumes 60% less power at the same speed.

http://www.tsmc.com/english/dedicatedFoundry/technology/logic.htm

Results

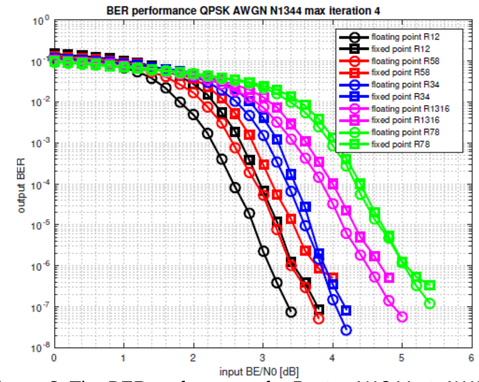


Figure 2. The BER performance for 5 rates N1344 at AWGN channel

	This work		ASSCC[20]	ISSCC[19]	ISTC[12]	VLSI[23]
Standard	802.11ay		802.11ad	802.11ad	802.11ad	802.11ad
Code length	1344/672		672	672	672	672
Algorithm	Layered		Layered	Two-phase	Two-phase	Two-phase
VFU/CFU parallelism	1344/42		336/42	672/42	672/546	672/42
Frame pipeline	YES		NO	YES	NO	YES
Unrolling	NO		NO	NO	YES	NO
No. cores	1		4	1	1	1
Support rates	10		4	4	1	4
Quantization	4		4	5	4	4
Implementation	logical synthesis		chip	chip	chip	chip
Technology	16nm	28nm	28nm	28nm	65nm	28nm
Work frequency	1000 MHz	600 MHz	470 MHz	150 MHz	257 MHz	202 MHz
Throughput (Gbps)	112@4it	67@4it	18@4it	12@3.75it	160@9it	6.78@10it
Area (sqmm)	0.19	0.42	0.78	0.63	12	1.99
VDD (V)	0.8	0.9	0.9	1.1	1.2	0.9
Power@ rate	R13/16	R13/16	R1/2	R1/2	R13/16	R13/16
Power@ SNR (db)	3.5 7	3.5 7	high	5	unknown	unknown
Early stop	NO YES	NO YES	YES	NO	NO	YES
Latency (ns)	36@4it 9@1it	60@4it 12@1it	138@4it	320@4it	35@9it	317@10it
Power (mW)	408 163	406 141	166	180	5360	104
Energy efficiency (pJ/iter)	3.64 1.45	6.05 2.10	18.4	15	33.5	15.34
Area efficiency (Gbps/sqmm)	589 589	160 160	23.58	19.05	13.6	3.41

Table 2. Comparison with SOA

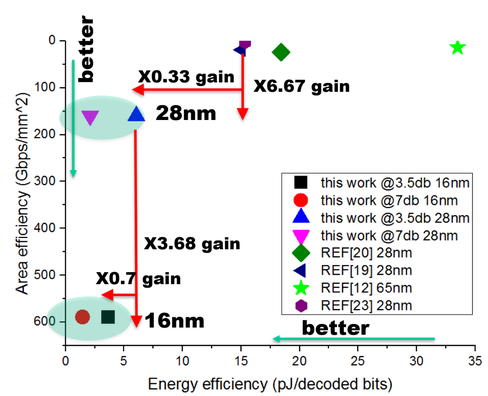


Figure 3. Comparison with SOA

Conclusion

A full row-based layered LDPC decoder with frame interleaved schedule is proposed for 802.11ay, implemented in 16 nm FinFET as well as 28 nm CMOS. The proposed architecture is flexible to support all coding rates and early stop as well.

The implemented results show significant improvement in throughput, area and energy efficient when compared to SOA. These performance gains are related to the architecture improvements and advanced technology.

Future work

➢ **Optimization data control to enable new frame feed in pipeline when one frame finished decoding**

➢ **Design new LDPC codes with longer code length to increase decoding throughput**

➢ **Multi-core solution to target 1 Tbps throughput**

Reference

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[23] M. Milicevic , et al "A Multi-Gb/s Frame-Interleaved LDPC Decoder With Path-Unrolled Message Passing in 28-nm CMOS", IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018

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