

PEFP: Efficient k -hop Constrained s - t Simple Path Enumeration on FPGA

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Abstract—Graph plays a vital role in representing entities and their relationships in a variety of fields, such as e-commerce networks, social networks and biological networks. Given two vertices s and t , one of the fundamental problems in graph databases is to investigate the relationships between s and t . A well-studied problem in such area is k -hop constrained s - t simple path enumeration. Nevertheless, all existing algorithms targeting this problem follow the DFS-based paradigm, which cannot scale up well. Moreover, using hardware devices like FPGA to accelerate graph computation has become popular. Motivated by this, in this paper, we propose the first FPGA-based algorithm PEPF to solve the problem of k -hop constrained s - t simple path enumeration efficiently. On the host side, we propose a preprocessing algorithm Pre-BFS to reduce the graph size and search space. On the FPGA side in PEPF, we propose a novel DFS-based batching technique to save on-chip memory efficiently. In addition, we also propose caching techniques to cache necessary data in BRAM, which overcome the latency bottleneck brought by the read/write operations from/to FPGA DRAM. Finally, we propose a data separation technique to enable dataflow optimization for the path verification module; hence the sub-stages in that module can be executed in parallel. Comprehensive experiments show that PEPF outperforms the state-of-the-art algorithm JOIN by more than 1 order of magnitude by average, and up to 2 orders of magnitude in terms of preprocessing time, query processing time and total time, respectively.

I. INTRODUCTION

Graph is a ubiquitous structure modeling entities and their relationships in various areas like e-commerce networks, social networks and biological networks [1], [2], [3]. One of the fundamental and important problems in graph databases is k -hop constrained s - t path enumeration [4], [5]; that is, given a directed and unlabelled graph G , source node s , target node t , and hop constraint k , we aim to enumerate all s - t paths such that the number of hops of each path is no more than k . In this paper, same as many existing studies on this problem, we only consider the *simple* path (i.e., a path with no repeated nodes) since a path containing cycles is less interesting and may significantly increase the total number of s - t paths. Note that for presentation simplicity, we abbreviate s - t k -hop constrained simple path as s - t k -path in this paper.

During s - t k -path computation, we have to frequently access neighbors of vertices in the graph. Real-life graphs usually follow power-law random distribution; that is, most vertices have a small degree, while some have a large degree [6]. However, modern CPUs are not an ideal way to deal with such data accesses: they do not offer high parallelism, and their caches do not work effectively for irregular graph processing that has little or no temporal and spatial locality. GPUs, on

the other hand, offer massive parallelism, but the performance can be significantly affected when the internal cores do not execute the same instruction (i.e., warp divergence), which is common in graphs with varying degrees [7].

FPGA has shown its substantial advantages over multi-core CPU in terms of parallelism [8]. For instance, one FPGA card can easily parallelize a loop with 1,000 iterations, while we have to find a host equipped with 1,000 CPU cores to offer the same parallelism. In addition, compared with GPU, FPGA is more energy-efficient, and can handle irregular graph processing with more stable parallelism by fully exploiting its pipeline mechanism [7]. Therefore, in this paper, we reconsider the problem of s - t k -path enumeration on FPGA.

Applications. We introduce the applications of s - t k -path enumeration on FPGA as follows.

- *E-commerce Networks.* A cycle in e-commerce networks indicates that there might exist fraudulent activities among the participants [9]. To detect such activities, Alibaba Group has developed a system in [5]; that is, when a new transaction is submitted from account t to account s , the system will perform s - t k -path enumeration to report all newly produced cycles. Since response time is very critical to the fraud detection system, it is necessary to speed up the s - t k -path queries in e-commerce networks. In this paper, we choose FPGA due to its parallel and re-programmable properties.
- *Social Networks.* For two users s and t in a social network, we may wonder to what extent t is influenced by or similar with s [10]. One can achieve this by enumerating all the simple paths from s to t with hop constraint k . As querying the s - t k -paths in a vast social network is very time-consuming, it is essential to accelerate such queries using FPGA.
- *Biological Networks.* It is known that s - t k -path enumeration is one of the most important pathway queries in biological networks [11]; that is, given two substances s and t , one can figure out the chains of interactions from s to t by enumerating all paths from s to t with hop constraint k . As biological networks are quite sensitive to the response time of pathway queries, it is necessary to accelerate s - t k -path queries through FPGA.

We have to emphasize that, besides the hop constraint, we can for sure impose other constraints to s - t path queries. For instance, one can apply label constraints to the vertices in social networks such that only specific types of users will be considered. Note that although we study the problem of s - t k -path enumeration in unlabelled graphs in this paper,

our solutions can be easily extended to solve it in labelled graphs; that is, we can deal with the label constraints in preprocessing stage to filter out the vertices and edges that satisfy the constraints.

Challenges. We present the challenges of solving the problem of s - t k -path enumeration on FPGA as follows.

- *Exponential Search Space and Expensive Verification Cost.* The main challenge of s - t k -path enumeration is the huge search space even if k is very small, because the number of results grows exponentially w.r.t k . Moreover, the tremendous number of intermediate results incurs expensive cost for path verification, which ensures that there are no repeated vertices along the path. It is inefficient in both response time and memory usage to simply enumerate all s - t k -paths with duplicate vertices, and then verify them.
- *Non-trivial Implementation on FPGA.* Due to the huge intermediate results using BFS-based framework, all existing solutions follow the DFS-based paradigm for better performance [4], [5], [12], [13]. However, DFS-based algorithms cannot be pipelined on FPGA because of the data dependencies among iterations. Thus existing algorithms cannot be straightforwardly implemented on FPGA. In addition, since CPU usually has an order of higher frequency than FPGA, it requires careful design on FPGA to achieve better performance than CPU.
- *Limited FPGA on-chip Memory.* Although BFS-based algorithms can be pipelined on FPGA, there is very limited FPGA on-chip memory (BRAM); hence, we have to frequently transfer intermediate results between BRAM and FPGA's external memory (DRAM) when using BFS-based paradigm, which significantly affects the overall performance. Therefore, one of the biggest challenges of solving this problem comes from how to deal with the huge intermediate data on FPGA efficiently to achieve good performance.

Consequently, it is rather challenging to design an efficient s - t k -path enumeration algorithm on FPGA that tames both computational hardness and on-chip memory bottleneck.

Contributions. Our contributions in this paper are summarized as follows:

- To the best of our knowledge, none of the existing s - t k -path enumeration algorithms can be directly adapted to the FPGA side. Therefore, we are the first to propose an efficient algorithm to solve this challenging problem on FPGA.
- On the host side, we develop a preprocessing algorithm **Pre-BFS** that can not only greatly reduce the search space in finding s - t k -paths, but also can finish in satisfactory time.
- On the FPGA side, we design an efficient algorithm **PEFP**. In PEFP, we first propose a novel DFS-based batching technique *Batch-DFS* to overcome the FPGA on-chip memory bottleneck. Then we further propose *caching* techniques to improve the read/write latency by reducing memory accesses to DRAM. Finally, we propose a *data separation* technique to fully parallelize the path verification module.
- We conduct comprehensive experiments on 12 real datasets to demonstrate the superior performance of our proposed algorithm PEFP compared with the state-of-the-art algorithm JOIN, where PEFP runs on the Xilinx Alveo U200 FPGA

card¹. More specifically, the experimental results show that PEFP outperforms JOIN by more than 1 order of magnitude by average, and up to 2 orders of magnitude in terms of preprocessing time, query processing time and total time, respectively.

Roadmap. The rest of the paper is organized as follows. Section II surveys important related works. Section III gives the formal definition of the problem studied in this paper, and introduces the existing solutions. Section IV presents the overall framework. We then propose our software preprocessing algorithm in Section V and hardware implementation details in Section VI. Extensive experiments are conducted in Section VII. Finally, Section VIII concludes the paper.

II. RELATED WORK

In this section, we review closely related works.

A. Simple Path Enumeration and Counting

There are many existing works studying the problem of enumerating s - t simple paths (e.g., [14], [15], [16]). However, what they focus on is how to construct a succinct presentation of these simple paths, thus we can efficiently enumerate the simple paths without explicitly storing each path. Note that their algorithms are not competitive for the problem of s - t simple path enumeration, and can only handle small graphs with thousands of vertices. Birmele *et. al* studied the problem of s - t simple path enumeration in [17], but the solution they proposed can only handle undirected graphs.

The counting of s - t simple paths is also a well-known $\#P$ hard problem, which has been extensively studied with different approaches such as recursive expressions of an adjacency matrix (e.g., [18], [19]). However, their counting approaches cannot be extended to efficiently enumerate hop-constrained simple paths in a trivial manner without materializing the paths during the computation, which will easily blow up the main memory even for a small k .

B. Shortest Path Enumeration

Given two vertices s and t in a graph, the end-to-end shortest path computation from s to t is one of the most important graph queries. In addition to the classical s - t shortest path computation, there are several variants where a set of paths are considered.

The problem of top- k' shortest paths has been intensively studied in the literatures (e.g., [20], [21]). To solve s - t k -path enumeration problem, we can keep on invoking the top- k' shortest simple path algorithm by increasing k' until the shortest path detected exceeds the distance threshold k . However, this naive method is not competitive because we have to enforce the output order of the paths according to their distances.

A considerable number of literatures have been published studying the constrained shortest path problem recently (e.g., [22], [23]). This problem can be defined as finding the shortest path between two vertices on a network whenever the traversal of any arc/vertex consumes certain resources. The problem of diversified shortest path has been intensively

¹<https://www.xilinx.com/products/boards-and-kits/alveo/u200.html>

Notation	Definition
G, G_{rev}	a graph, its reverse graph
V, E	graph vertex set, edge set
$p, v \rightsquigarrow v'$	a path, a path from v to v'
s, t, k	source and target vertex, hop constraint
s - t k -path	k -hop constrained path from s to t
$len(p)$	length of path p , where $len(p) = p - 1$
$sd(v, v')$	shortest distance from v to v'
$sd(v, v' p)$	shortest distance from v to v' without touching any vertex in $V(p)$
$bar[u]$	shortest distance from u to t
\mathcal{P}	path set of buffer area in BRAM
\mathcal{P}'	path set of processing area in BRAM
\mathcal{P}_D	path set in DRAM
$\mathcal{S}[i]$	one hop successors of path $\mathcal{P}'[i]$

TABLE I
SUMMARY OF NOTATIONS

studied in the literatures as well (e.g., [24], [25]), which consider both distance and diversity of s - t shortest paths. However, due to their focus on identifying the shortest paths, they cannot be adapted to s - t k -path enumeration in a trivial manner.

C. Shortest Path Computation on FPGA

Recently there emerge many literatures aiming at accelerating shortest path computation on FPGA (see [7] for a survey). Tommiska et al. [26] implemented single source shortest path (SSSP) algorithm on FPGA using adjacency matrix stored in BRAM, which limits its graph size that can be handled. Unlike the previous approach, Zhou et al. [27] solved SSSP with the graph stored in DRAM and the algorithm is fully pipelined. Bondhugula et al. [28] proposed to solve all-pairs-shortest-paths (APSP) problem on FPGA, which is to find shortest path between all pairs of vertices in the graph. The graph is stored in DRAM and only when the required slices of graph are streamed to BRAM. Betkaoui et al. [29] studied APSP for unweighted graphs by running BFS from each vertex, and its key idea for optimizing memory accesses is to use BRAM for random memory accesses and use DRAM for sequential accesses. Nevertheless, none of these algorithms can be directly adapted to s - t k -path enumeration problem because they can only identify the shortest paths rather than enumerate all s - t k -paths.

III. PRELIMINARY

In this section, we first give the formal definition of s - t k -hop constrained simple path enumeration problem, then we present a brief introduction to the existing solutions, namely T-DFS [12], T-DFS2 [13], HP-Index [5], and JOIN [4]. We summarize important notations in TABLE I.

A. Problem Definition

A directed graph G is represented as $G = (V, E)$, where $V(G)$ is the vertex set of G , and $E(G) \subseteq V(G) \times V(G)$ is the directed edge set of G . If the context is clear, we use **successor** or **neighbor** to refer “out-going neighbor”. Let G_{rev} denote the reverse graph of G , where $V(G_{rev}) = V(G)$ and for each edge $(v_1, v_2) \in E(G)$, there is a corresponding edge $(v_2, v_1) \in E(G_{rev})$. We say G' is an induced subgraph of G if $V(G') \subseteq V(G)$ and $E(G') = \{(v_1, v_2) | (v_1, v_2) \in E(G), v_1 \in V(G') \wedge v_2 \in V(G')\}$. A path p from vertex v to vertex v' is a sequence of vertices $v = v_0, v_1, \dots, v_n = v'$ such that for each

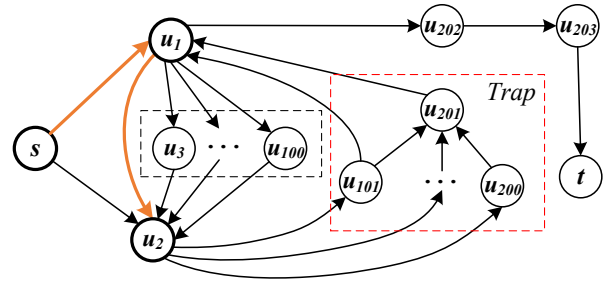


Fig. 1. Key Idea of BC-DFS with $k = 7$

$i \in [0, n-1], (v_i, v_{i+1}) \in E(G)$. We use $p(v, v')$ or $p(v \rightsquigarrow v')$ to denote a path from v to v' . A simple path is a loop-free path that contains no duplicate nodes. We use **path** to refer “simple path” if the context is clear. The length of a path p is denoted as $len(p)$, where $len(p) = |p| - 1$. We say path p is a k -hop constrained path if it satisfies $len(p) \leq k$. Given two vertices $v, v' \in V(G)$ and a path p , we use $sd(v, v')$ to denote the shortest distance from v to v' , and use $sd(v, v'|p)$ to denote the shortest distance from v to v' without touching any vertex in $V(p)$. We say u is a successor of path p if u is an out-going neighbor of the last vertex in p .

Problem Statement. In this paper, we study the FPGA-based k -hop constrained s - t simple path enumeration problem. Specifically, given a directed and unlabelled graph G , source vertex s , target vertex t , and hop constraint k , we use \mathcal{R} to represent the paths such that $\mathcal{R} = \{p \mid len(p) \leq k, p \text{ is a simple path and } p \text{ starts with } s \text{ and ends with } t\}$. We target developing FPGA-based algorithms to efficiently enumerate all paths in \mathcal{R} .

B. Existing Solutions

T-DFS and T-DFS2. In [12], T-DFS is proposed to solve s - t k -path enumeration problem in directed graphs. T-DFS carefully explores the out-going neighbors of a vertex and ensures that every search branch comes up with at least one s - t k -path, which is the art of “never fall in the trap”. Specifically, given a current path p , T-DFS aggressively computes the shortest distance $sd(u, t|p)$ for each successor u of p , and u will not be explored if $len(p) + 1 + sd(u, t|p) > k$. T-DFS2 [13] follows the same aggressive verification strategy as T-DFS, while it can reduce shortest path distance computation by skipping some vertices associated with only one output in the following search. Nevertheless, T-DFS and T-DFS2 show poor performance in practice due to the expensive verification cost [4].

HP-Index. In [5], a novel indexing technique HP-Index is proposed to continuously maintain the pairwise paths among hot points (i.e., vertices with high degree). Enumerating all s - t k -paths in HP-Index can be concluded as follows: (1) Perform DFS from s with search depth at most k , and record the path and backtrack when encountering a hot point; (2) Perform a reverse DFS from t in the same way; (3) Find the indexed paths among the hot points involved in the above computation; (4) Concatenate the paths from steps (1), (2) and (3) to identify s - t k -paths. It is reported in [4] that HP-Index can only achieve good performance on the extremely skewed graph dataset which has relatively small number of s - t k -paths.

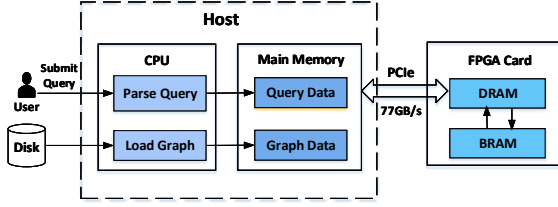


Fig. 2. Overall Framework of CPU-FPGA System

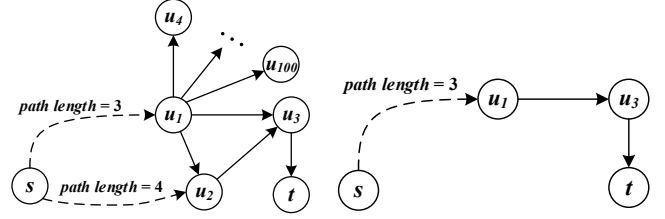
JOIN. Peng et al. [4] proposed the state-of-the-art algorithm JOIN to enumerate all s - t k -paths in a directed and unlabelled graph. JOIN designs an efficient pruning technique BC-DFS motivated by “never fall in the same trap twice through learning from mistakes”. The idea of BC-DFS is shown in Fig. 1, where the hop constraint k is set to 7. We regard the current path p as a stack S . In Fig. 1, node s, u_1 and u_2 have been pushed into S . After finishing DFS with S , we know that there is no valid s - t k -path w.r.t S . Then BC-DFS will set $u_2.bar = k + 1 - len(S)$, which is 6 in this example. When u_2 is unstacked and we push u_3 into the stack, it will not fall in the same “trap” like u_2 did before because it will check if $len(S) + 1 + u_2.bar \leq k$ holds. In this example, $len(S) + 1 + u_2.bar = 2 + 1 + 6 = 9 > 7$, hence u_2 will be pruned by u_3, \dots, u_{100} when s and u_1 are in the stack, which significantly reduces the search space.

Given a path $p = (u_1, \dots, u_n)$, its middle vertex is the $\lceil \frac{n}{2} \rceil$ -th vertex. To avoid duplicate search, JOIN follows “joining two paths” framework by exploiting the middle vertices of s - t k -paths. Its procedures can be concluded as follows: (1) Compute all middle vertices of s - t k -paths, denoted by \mathcal{M} ; (2) Add a virtual vertex t' and put an edge (u, t') for each $u \in \mathcal{M}$; (3) Compute s - t' ($\lceil \frac{k}{2} \rceil + 1$)-paths P_l using BC-DFS; (4) Add a virtual vertex s' and put an edge (s', u) for each $u \in \mathcal{M}$; (5) Compute s' - t ($\lfloor \frac{k}{2} \rfloor + 1$)-paths P_r using BC-DFS; (6) Join P_l and P_r to obtain the final results, where the join key is the node $u \in \mathcal{M}$, and a result path is valid iff it is a simple path and u is its middle vertex. Consequently, JOIN outperforms all existing algorithms, namely T-DFS [12], T-DFS2 [13], and HP-Index [5].

IV. FRAMEWORK OVERVIEW

In this section, we present our system’s overall framework to solve the problem of s - t k -path enumeration. The overview of the system architecture is illustrated in Fig. 2. The workflow of the system can be concluded as follows:

- 1) On the host side, the user first specifies the graph file, then the host loads the corresponding graph data and stores it in main memory. Once the graph loading process is finished, the host is ready to handle path queries submitted by user;
- 2) When a new query comes in, the host parses the query to extract s, t and k ;
- 3) The host starts its preprocessing computation (for further details see Section V) to prepare the necessary data that will be transferred to FPGA DRAM.
- 4) Based on the preprocessing, the host transfers the prepared data to FPGA DRAM through PCIe bus in DMA mode;
- 5) Once all the input data arrive at DRAM, FPGA can start its computation to find all valid s - t k -paths and return them



(a) Graph G

(b) Induced Subgraph after Removing Invalid Nodes with $k = 5$

Fig. 3. Example of Preprocessing

to the host side through PCIe. The computation details on FPGA will be introduced in Section VI.

V. SOFTWARE PREPROCESSING

In this section, we present the preprocessing details on the host side. We first give a brief introduction to the preprocessing technique of the state-of-the-art algorithm JOIN. Then we propose our optimized preprocessing technique to further reduce the search space for future path expansion and verification.

Preprocessing aims to compute and prepare necessary data for a given algorithm. As for preprocessing in JOIN, a k -hop BFS is first conducted from source vertex s to compute $sd(s, u)$ on G . Similarly, JOIN computes $sd(u, t)$ by conducting k -hop BFS from t on G_{rev} . The shortest distance of those vertices that have not been touched during BFS is set to $k + 1$. After finishing preprocessing, JOIN can start s - t k -path computation, which is introduced in subsection III-B.

Having investigated the preprocessing idea of JOIN, we find it can be optimized based on the following Theorem.

Theorem 1: Given shortest distance maps sd_s and sd_t , where $sd_s[v] = sd(s, v)$ and $sd_t[v] = sd(v, t)$ for any $v \in V(G)$, performing s - t k -path enumeration on original graph G is equivalent to doing it on subgraph $G' \subseteq G$, where G' is induced by the node set $\mathcal{N} \subseteq V(G)$ such that for each $u \in \mathcal{N}$, $sd_s[u] + sd_t[u] \leq k$.

Proof: Suppose there exists a valid s - t k -path p that contains a node u , where u is not in G' . Thus we have $sd_s[u] + sd_t[u] > k$, which contradicts the premise $len(p) \leq k$. Hence the theorem holds. ■

As illustrated in Fig. 3(a), when we set $k = 5$, 5-hop BFS from s will include the whole graph G . Although u_4, \dots, u_{100} cannot reach t , they will still be visited in JOIN during BC-DFS, which results in useless search. After we remove the invalid nodes such that $sd_s[u] + sd_t[u] > 5$, the induced subgraph is shown in Fig. 3(b), where u_2, u_4, \dots, u_{100} and their corresponding edges are removed, hence the search space is greatly reduced.

Next, we show that a $(k - 1)$ -hop bidirectional BFS on G is enough for preprocessing as follows.

We call a vertex u is valid in preprocessing iff $sd_s[u] + sd_t[u] \leq k$. We use G_{k-1} and G_k to denote the induced subgraph after running $(k - 1)$ -hop and k -hop bidirectional BFS on G , respectively. We show that $(k - 1)$ -hop bidirectional BFS is enough by proving $V(G_{k-1})$ contains all valid vertices.

Proof: Suppose there is a valid vertex u such that $u \in V(G_k)$ and $u \notin V(G_{k-1})$. Let V' denote the vertices that k -hop bidirectional BFS can touch while $(k - 1)$ -hop cannot. It is obvious that $V' = \{u | sd_s[u] = k \text{ or } sd_t[u] = k\}$.

Nevertheless, if u is a valid node and $sd_s[u] = k$, then we have $u = t$, which contradicts the premise that $u \notin V(G_{k-1})$ because $t \in V(G_{k-1})$. Similarly, if u is a valid node and $sd_t[u] = k$, then we have $u = s$, which contradicts the premise that $u \notin V(G_{k-1})$ because $s \in V(G_{k-1})$. Thus, $V(G_{k-1})$ includes all valid vertices. ■

Based on the above observations, we propose our preprocessing algorithm **Pre-BFS** which only needs to do $(k-1)$ -hop bidirectional BFS to obtain the induced subgraph G' as follows.

- 1) Perform $(k-1)$ -hop BFS from s on G to compute sd_s .
- 2) Perform $(k-1)$ -hop BFS from t on G_{rev} to compute sd_t ;
- 3) For each node $u \in sd_s \cap sd_t$, if $sd_s[u] + sd_t[u] \leq k$ holds, then we put it into node set \mathcal{N} .
- 4) Return the subgraph G' induced by \mathcal{N} in G .

When the preprocessing procedure is finished, we will send s , t , sd_t and G' to FPGA DRAM, where G' is stored using ‘‘Compressed Sparse Row’’ (CSR) format [30]. Note that we call sd_t as barrier (denoted as bar) in the rest of the paper.

VI. HARDWARE IMPLEMENTATION

In this section, we first introduce our proposed algorithm **PEFP** to solve s - t k -hop constrained Path Enumeration on **FPGA**. Then we present several optimizations to improve the performance of PEPF by fully utilizing the characteristics of FPGA.

A. PEPF

PEFP adopts the BFS-based paradigm, because BFS naturally enjoys great parallelism such as performing concurrent expansion for some intermediate results in a certain round. Therefore, we can easily apply pipeline optimizations to BFS-based algorithms to fully utilize the parallelism of FPGA.

In general, PEPF follows the **expansion-and-verification** framework, which can be dissected into three steps: (1) Expand the intermediate paths with one-hop successor vertices; (2) Verify if each expanded path is a valid path; (3) Write back the valid paths to the intermediate path set. The algorithm terminates when the intermediate path set is empty.

The details of PEPF are shown in Algorithm 1. Given source vertex s , target vertex t , hop constraint k , barrier bar and graph G , the algorithm computes and outputs all s - t k -paths. We first initialize intermediate path set \mathcal{P} , \mathcal{P}' , \mathcal{P}_D , and one-hop successors set \mathcal{S} with empty set (Line 1), where \mathcal{P}' is a batch of paths fetched from \mathcal{P} , \mathcal{P}_D represents the intermediate path set in DRAM, and $\mathcal{S}[i]$ denotes the one-hop successor vertex set of the i -th path in \mathcal{P}' (denoted as $\mathcal{P}'[i]$). Then we push a path into \mathcal{P}' consisting of just one vertex s (Line 2). If \mathcal{P}' is not empty, for each path $\mathcal{P}'[i] \in \mathcal{P}'$, we get its one-hop successors and put them into $\mathcal{S}[i]$ (Line 3-5). Next, we verify each successor $nbr \in \mathcal{S}[i]$ for every $\mathcal{P}'[i] \in \mathcal{P}'$ using Algorithm 2 (Line 6-9). If nbr is a valid successor for $\mathcal{P}'[i]$, a new intermediate path p will be generated and put into \mathcal{P} by concatenating nbr to $\mathcal{P}'[i]$ (Line 10-12). Note that when the size of \mathcal{P} reaches our predefined threshold, we will flush \mathcal{P} to DRAM to avoid BRAM overflow (Line 13-14). After all paths in \mathcal{P} have been processed in this batch, we fetch next batch of paths into \mathcal{P}' using Algorithm 3 (Line 15). PEPF terminates when \mathcal{P}' is empty (Line 3).

Given an intermediate path p , its one-hop successor u , target vertex t , hop constraint k and its barrier b_u , the verification module of checking whether u is a valid successor for p includes three stages, which is shown in Algorithm 2: (1) The first stage is **target check**. If u equals to target vertex t , then we output a new result path p' by concatenating u to p and return *false* (Line 1-4); (2) The second stage is **barrier check**. If $len(p) + 1 + b_u > k$, then we return *false* as it does not satisfy the hop constraint (Line 5-6); (3) The third stage is **visited check**. If u has already appeared in p , then we return *false* (Line 7-8). If u passes the validity check of the three stages, we can say u is a valid successor of p (Line 9).

Algorithm 1: PEPF(s, t, k, bar, G)

```

Input :  $s$  : source vertex
          $t$  : target vertex
          $k$  : hop constraint
          $bar$  : barrier array
          $G$  : graph

Output : All  $s$ - $t$   $k$ -paths
1  $\mathcal{P} \leftarrow \emptyset$ ;  $\mathcal{P}' \leftarrow \emptyset$ ;  $\mathcal{P}_D \leftarrow \emptyset$ ;  $\mathcal{S} \leftarrow \emptyset$ ;
2  $\mathcal{P}' \text{.push}(\{s\})$ ;
3 while  $\mathcal{P}' \neq \emptyset$  do
4   forall  $\mathcal{P}'[i] \in \mathcal{P}'$  do
5      $\mathcal{S}[i] \leftarrow$  one-hop successor vertices of  $\mathcal{P}'[i]$  in  $G$ ;
6   forall  $\mathcal{S}[i] \in \mathcal{S}$  do
7     forall  $\mathcal{S}[i][j] \in \mathcal{S}[i]$  do
8        $nbr \leftarrow \mathcal{S}[i][j]$ ;
9        $isValid \leftarrow \text{Verify}(\mathcal{P}'[i], nbr, t, k, bar[nbr])$ ;
10      if  $isValid == true$  then
11         $p \leftarrow \mathcal{P}'[i] \text{.push}(nbr)$ ;
12         $\mathcal{P} \text{.push}(p)$ ;
13      if  $\mathcal{P}$  is full then
14        Flush  $\mathcal{P}$  to  $\mathcal{P}_D$ ;
15  $\mathcal{P}' \leftarrow \text{NextBatch}(\mathcal{P}, \mathcal{P}_D)$ ;

```

Algorithm 2: Verify(p, u, t, k, b_u)

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Input :  $p$  : path  $p$ 
          $u$  : a successor of path  $p$ 
          $t$  : target vertex
          $k$  : hop constraint
          $b_u$  : barrier of vertex  $u$ 

Output :  $isValid$  : if  $u$  is a valid successor of  $p$ 
1 if  $u == t$  then /* Target Check */
2    $p' \leftarrow p \text{.push}(u)$ ;
3   output  $p'$ ;
4   return false;
5 if  $len(p) + 1 + b_u > k$  then /* Barrier Check */
6   return false;
7 if  $u$  is contained in path  $p$  then /* Visited Check */
8   return false;
9 return true;

```

Correctness. In Section V, we have correctly calculated barrier data bar for each vertex in the induced subgraph G (recall that $bar[u] = sd(u, t)$). The expansion of \mathcal{P}' starts with the path only containing vertex s . Therefore, the correctness of PEPF holds before the loop starts. For each iteration of expansion, given path $\mathcal{P}'[i]$ and its one-hop successor nbr , there are three cases to check in total: (1) Whether vertex nbr

Algorithm 3: NextBatch($\mathcal{P}, \mathcal{P}_D$)

Input : \mathcal{P} : intermediate path set in BRAM
 \mathcal{P}_D : intermediate path set in DRAM
Output : \mathcal{P}' : a batch of intermediate paths

- 1 $\mathcal{P}' \leftarrow \emptyset$;
- 2 $\Theta_1 \leftarrow$ batch size threshold of \mathcal{P}_D ;
- 3 $\Theta_2 \leftarrow$ batch size threshold of \mathcal{P} ;
- 4 **if** $\mathcal{P} \neq \emptyset$ **then**
- 5 $\mathcal{P}' \leftarrow$ **Batch-DFS**(\mathcal{P}, Θ_2);
- 6 **else**
- 7 **if** $\mathcal{P}_D \neq \emptyset$ **then**
- 8 $\mathcal{P} \leftarrow$ fetch a batch of paths from \mathcal{P}_D with Θ_1 ;
- 9 $\mathcal{P}' \leftarrow$ **Batch-DFS**(\mathcal{P}, Θ_2);
- 10 **return** \mathcal{P}' ;

is the target vertex; (2) Whether the path $\mathcal{P}'[i]$ exceeds the hop constraint when concatenating nbr to $\mathcal{P}'[i]$; (3) Whether vertex nbr has already appeared in $\mathcal{P}'[i]$. Only when nbr passes all the three cases can we generate a new intermediate path $p = \mathcal{P}'[i].push(nbr)$. Therefore, we will not prune any valid paths during the verification and the correctness of each iteration holds. The algorithm terminates when \mathcal{P}' is empty, suggesting that all of the intermediate paths have been processed. Hence the correctness of PEFP holds.

B. DFS-based Batch Processing with Caching

Intuitively, BFS-based path enumeration needs to store all intermediate results, causing notorious memory overhead to our system. To solve this challenging issue, we adopt the *buffer-and-batch* technique. The general idea of buffer-and-batch aims to store huge intermediate paths in FPGA's external memory (DRAM), then read and process the data from DRAM by batch to avoid BRAM overflow.

Nevertheless, there exists another concern. Although DRAM capacity is much larger than BRAM, the read latency of DRAM takes 7-8 clock cycles while the read latency of BRAM is only 1 clock cycle. Based on that observation, we propose a caching-based technique to efficiently reduce the read/write operations from/to DRAM, thereby lowering the system latency.

(1) Caching Intermediate Paths. Targeting maximizing FPGA on-chip memory usage and minimizing the number of direct accesses to DRAM, we design two areas in BRAM, namely **buffer area** and **processing area**. As shown in Algorithm 3, the input \mathcal{P} denotes the intermediate path set in BRAM, which is the **buffer area**; the input \mathcal{P}_D denotes the intermediate path set in DRAM, which is the **external memory area**; the output \mathcal{P}' represents a batch of intermediate paths we need to process next, which is called **processing area**. We first check the buffer area \mathcal{P} . If \mathcal{P} is not empty, we fetch a batch of paths directly from \mathcal{P} into \mathcal{P}' (Line 4-5) using Algorithm 4. Note that we use Θ_2 to denote the batch size threshold of \mathcal{P} (Line 3), which is the capacity of \mathcal{P}' . Otherwise, we check \mathcal{P}_D . If \mathcal{P}_D is not empty, we first fetch a batch of paths from \mathcal{P}_D into \mathcal{P} with batch size Θ_1 (which is defined in Line 2), then fetch a batch of paths from \mathcal{P} into \mathcal{P}' using Algorithm 4, finally return \mathcal{P}' (Line 6-10). Note that when we fetch a batch of paths from \mathcal{P}_D , we simply fetch from its tail with size Θ_1 to avoid memory fragmentation; we

do the same for the write operation. Thanks to the buffer area, we only need to read/write intermediate paths from/to DRAM when the buffer area is empty/full. By caching intermediate paths in BRAM, we can significantly reduce the data transfer between BRAM and DRAM, hence the overall performance is improved.

(2) Caching Data Graph and Barrier. From Algorithm 1 we know that we need to frequently access barrier data and get one-hop successors from data graph G for a given path p . Learning from the merits by caching, we also cache the data graph and barrier information in BRAM. More specifically, we have pre-allocated three fixed-size arrays *vertex_arr*, *edge_arr* and *bar_arr* to store vertex data, edge data and barrier data, respectively. When initializing the three arrays, we put as much data as possible into them from DRAM. When we access vertex, edge or barrier data, we always check the local BRAM array first instead of directly fetching it from DRAM. Thanks to the preprocessing to extract induced subgraph, we find that in most cases, we can fit the whole subgraph and barrier data in BRAM.

Algorithm 4: Batch-DFS(\mathcal{P}, Θ)

Input : \mathcal{P} : intermediate path set
 Θ : batch size threshold
Output : \mathcal{P}' : a batch of intermediate paths

- 1 $\mathcal{P}' \leftarrow \emptyset$;
- 2 $cnt \leftarrow 0$;
- 3 $i \leftarrow$ index of the last path in \mathcal{P} ;
- 4 **while** $i \neq 0$ **do**
- 5 $ptr_1, ptr_2 \leftarrow$ the end neighbor pointer of $\mathcal{P}[i]$;
- 6 $ptr_{last} \leftarrow$ the last neighbor pointer of $\mathcal{P}[i]$;
- 7 **if** $ptr_1 + \Theta - cnt < ptr_{last}$ **then**
- 8 $ptr_2 \leftarrow ptr_1 + \Theta - cnt$;
- 9 **else**
- 10 $ptr_2 \leftarrow ptr_{last}$;
- 11 $\mathcal{P}'.push(\mathcal{P}[i])$ with ptr_1 and ptr_2 ;
- 12 update start and end neighbor pointer of $\mathcal{P}[i]$ with ptr_1 and ptr_2 ;
- 13 $cnt \leftarrow cnt + ptr_2 - ptr_1$;
- 14 **if** $cnt < \Theta$ **then**
- 15 $i \leftarrow i - 1$;
- 16 **else**
- 17 **break**;
- 18 **return** \mathcal{P}' ;

(3) Batch-DFS. As mentioned before, only when the buffer area \mathcal{P} is full will it do write operations to DRAM. Therefore, it is essential to design an efficient batching technique to save the memory in buffer area. One alternative is to change the batch size dynamically. For instance, one can reduce the batch size according to the free space in \mathcal{P} . Nevertheless, when there is only little space left in \mathcal{P} , the batch size will be set to a rather small value. In this case, most space in the processing area is wasted, which leads to a low level parallelism of PEFP. Thus this naive technique is inefficient.

It is challenging to design an efficient batching algorithm that both fully utilizes the space in **processing area** and saves the memory in **buffer area**. To overcome this challenge, we propose a novel DFS-based batching algorithm **Batch-DFS**, which is shown in Algorithm 4. The motivation of this

algorithm comes from the following observation.

Observation 1: Given two paths p_1 and p_2 with $len(p_1) < len(p_2)$, suppose p_1 and p_2 have same number of successors, then p_2 will have a greater chance generating fewer intermediate paths than p_1 during one-hop expansion.

The observation is illustrated in Fig. 5. Suppose the hop constraint k is 6, $p_1 = s \rightsquigarrow u_1$, $p_2 = s \rightsquigarrow u_2$, $len(p_1) = 3$, $len(p_2) = 4$, and path p_1 and p_2 have a same successor u_3 , where $bar[u_3] = 2$. Clearly, u_3 will be pruned by p_2 because $len(p_2) + 1 + bar[u_3] > 6$, while it will not be pruned by p_1 . Accordingly, when we process p_2 prior to p_1 , it tends to produce fewer intermediate paths for p_2 's pruning power is stronger than p_1 in the barrier check stage. Specifically, when we process a path p with $len(p) = k - 1$, it will generate 0 intermediate results. Fewer intermediate results indicate \mathcal{P} will have a smaller chance to be full and flushed to DRAM, which can improve the overall performance.

Based on the above observation, Batch-DFS follows the idea of DFS. In DFS, the intermediate results are stored in a stack, and we always process its top element first. Similarly, we regard the buffer area \mathcal{P} as a stack, and we always fetch a batch of paths from its top.

The details of Batch-DFS are shown in Algorithm 4. The inputs of the algorithm include the buffer area \mathcal{P} and batch size threshold Θ , and its output is a batch of paths \mathcal{P}' that are going to be put into the processing area. We first initialize cnt with 0 (Line 2), where cnt denotes the number of intermediate paths that will be processed next. Hence we must ensure $cnt \leq \Theta$. Treating \mathcal{P} as a stack, we use i to trace \mathcal{P} from its top (Line 3). We continuously fetch paths from \mathcal{P} into \mathcal{P}' until cnt reaches the threshold Θ (Line 16-17). Due to the fact that there might exist a “**super node**” whose degree is larger than Θ , it is necessary to process its neighbors by batch, or it will blow the processing area. We achieve this by maintaining two pointers for each path's successors (or out-going neighbors), namely **start neighbor** and **end neighbor** pointer. The two pointers are initialized as pointing to the path's first neighbor. In Line 5, we declare two pointers ptr_1, ptr_2 and initialize them as the end neighbor pointer of $\mathcal{P}[i]$. Then we assign the last neighbor pointer of $\mathcal{P}[i]$ to ptr_{last} (Line 6). If $ptr_1 + \Theta - cnt < ptr_{last}$ holds, then we set ptr_2 to position $ptr_1 + \Theta - cnt$, which indicates that the remaining space in the processing area is not enough to hold all successors of $\mathcal{P}[i]$. Thereby we can only load a batch of its successors (Line 7-8). If processing area has enough space, we just set ptr_2 to ptr_{last} (Line 9-10). Then we put $\mathcal{P}[i]$ into \mathcal{P}' and update the start and end neighbor pointer of $\mathcal{P}[i]$ with ptr_1 and ptr_2 , respectively (Line 11-12). When we fetch $\mathcal{P}[i]$'s successors (Algorithm 1, Line 5), we will perform this operation according to ptr_1 and ptr_2 .

Overall, PEFP is a “hybrid” algorithm that combines the merits of BFS and DFS. In other words, PEFP exerts the parallel ability of FPGA through BFS and saves on-chip memory through DFS-based batch processing. Consequently, PEFP successfully tames both computational hardness and FPGA on-chip memory bottleneck.

C. Basic Pipeline of Verification

The read/write path operation can be easily pipelined on FPGA. The bottleneck remains in how to pipeline the ver-

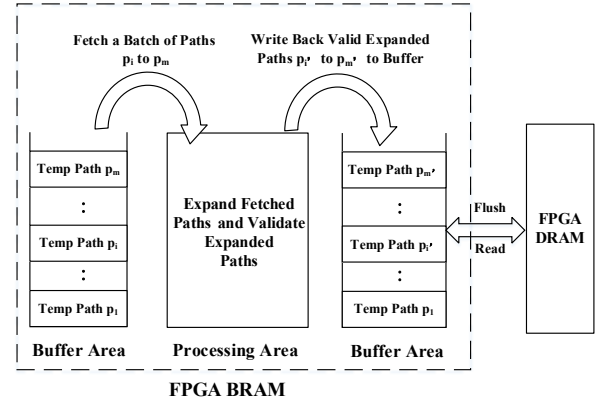


Fig. 4. Overview of FPGA Batch Processing

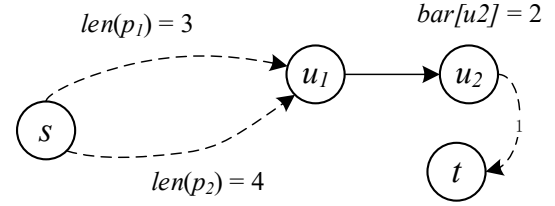


Fig. 5. An Example for Processing Longer Path First with $k = 6$

ification of each expanded path. In this subsection, we will demonstrate a basic pipeline technique for path verification. Note that we call path verification and path validity check interchangeably in this paper.

As illustrated in Fig. 6, given an intermediate path $\mathcal{P}'[i]$, its one-hop successor nbr and barrier $bar[nbr]$ (we call them input data i in Fig. 6), the basic verification module consists of three consecutively executed stages, namely (1) target check stage, (2) barrier check stage and (3) visited check stage. The input data of this module must include all the information required by the three stages according to Algorithm 2. The target check and barrier check can be finished in $O(1)$ time, while the visited check can be finished in $O(k)$ time without using hash set. We can unroll the visited check loop that has constant loop bound k , thus the time cost of visited check on FPGA can be reduced from $O(k)$ to $O(1)$.

In this design, the verification for each input data is pipelined, while the three stages inside the module cannot be executed in parallel, because only when the input data passes the current stage can it move to the next stage.

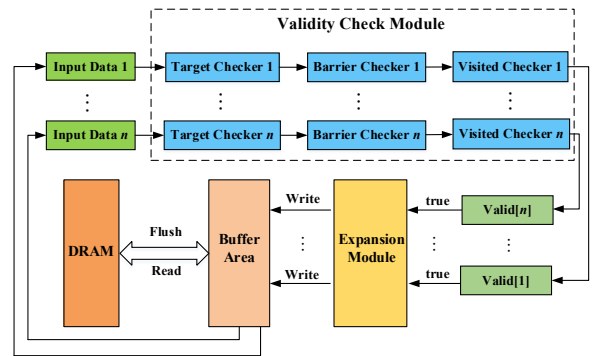


Fig. 6. Basic Pipeline of Path Verification on FPGA

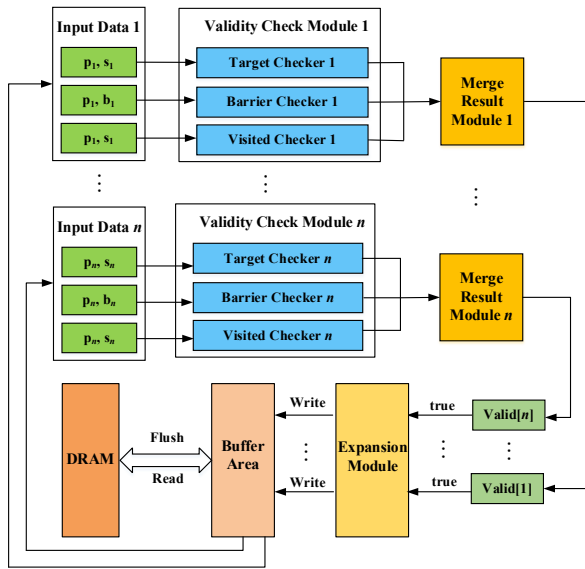


Fig. 7. Optimized Pipeline of Path Verification with Data Separation on FPGA

D. Optimized Pipeline of Verification by Data Separation

For the basic design, although it can pipeline the input data verification, the inner stages of the verification module are executed one by one, which cannot exert the parallel ability of FPGA. We observe that the bottleneck is caused by data dependencies among the stages; that is, the current stage cannot be executed until the previous stage is finished. Motivated by this, we separate the input data according to the stages so that each stage can do its own computation independently. Then we merge the outputs of the three stages to get the final verification result for each expansion.

More specifically, the input data of the path validity check module is separated into path p_i , successor s_i , and barrier b_i , as illustrated in Fig. 7. In this design, we send p_i and s_i to the target check and visited check stage, and send p_i and b_i to the barrier check stage. Consequently, there are no data dependencies among the stages. We also apply dataflow optimization to the stages, suggesting that each stage can start its computation once it receives input data without waiting for the previous stage to finish. As a result, the three stages can be executed in parallel. All we need to do is merge the validity check results of the three stages, which improves the overall performance of PEFP.

VII. EXPERIMENT

In this section, we conduct extensive experiments to evaluate the effectiveness and efficiency of our proposed algorithm PEFP. As discussed in Section II, none of the related FPGA works can be directly adapted to solve $s-t$ k -path enumeration problem. Moreover, JOIN is the state-of-the-art algorithm based on DFS paradigm, and it is non-trivial to implement a parallel version of JOIN either on multi-core CPUs or on FPGA. Therefore, in this paper, we address the original JOIN algorithm as the baseline solution, and we compare the performance of PEFP with JOIN on a wide range of datasets.

Dataset	Name	$ V $	$ E $	d_{avg}	D	D_{90}
Reactome	RT	6.3K	147K	46.64	24	5.39
soc-Epinions1	SE	75K	508K	13.42	14	5
Slashdot0902	SD	82K	948K	23.08	12	4.7
Amazon	AM	334K	925K	6.76	44	15
twitter-social	TS	465K	834K	3.86	8	4.96
Baidu	BD	425K	3M	15.8	32	8.54
BerkStan	BS	685K	7M	22.18	208	9.79
web-google	WG	875K	5M	11.6	24	7.95
Skitter	SK	1.6M	11M	13.08	31	5.85
WikiTalk	WT	2M	5M	4.2	9	4
LiveJournal	LJ	4M	68M	28.4	16	6.5
DBpedia	DP	18M	172M	18.85	12	4.98

TABLE II
STATISTICS OF DATASETS

A. Experiment Setup

Settings. All experiments are conducted on a Ubuntu 16.04 machine, with 250GB memory, 10TB disk and 2 Intel Xeon CPUs (E5-2620 v4 2.10GHz, 8 cores). The proposed FPGA-based algorithm PEFP is implemented on Xilinx Alveo U200 card² using Xilinx SDAccel³, where the FPGA card is equipped with 4×16 GB off-chip DRAMs and runs at 300MHz. The code of JOIN is obtained from the authors in [4], which is implemented in standard C++ and compiled with g++ 5.5.0⁴.

Datasets. All datasets are downloaded from two public websites: Konect⁵ and SNAP⁶. TABLE II demonstrates detailed data descriptions. Note that d_{avg} denotes the average degree, D denotes the diameter and D_{90} denotes the 90-percentile effective diameter of the graph.

Metrics. We randomly generate 1,000 query pairs $\{s, t\}$ for each dataset with hop constraint k , where the source vertex s could reach target vertex t in k hops. We then evaluate the average running time of the 1,000 queries, where each query's running time is obtained from an average of three runs. Note that for better presentation, we carefully set the range of k for each dataset based on its topology. For instance, k is set from 8 for Amazon, which is a rather sparse graph. Moreover, for each dataset, we have evaluated the time it takes to transfer the 1,000 queries and their corresponding data graphs (after preprocessing) from the host to FPGA DRAM at once, which is around 100ms~300ms. Hence, the average transfer time for each query is around 0.1ms~0.3ms, which can be ignored as the preprocessing time in host and query processing time on FPGA would dominate. We denote query preprocessing time as T_1 , query processing time as T_2 , and total time as $T = T_1 + T_2$. We evaluate T_1, T_2 , and T for both PEFP and JOIN, where the preprocessing of JOIN is introduced in Section V.

B. Evaluate Query Processing Time

In this experiment, we evaluate the query processing time of PEFP and JOIN on all 12 datasets by varying the hop constraint k , which is illustrated in Fig. 8. The blue dotted line in that figure represents the speedup of PEFP over JOIN,

²<https://www.xilinx.com/products/boards-and-kits/alveo/u200.html>

³<https://www.xilinx.com/products/design-tools/software-zone/sdaccel.html>

⁴JOIN's source code: <https://github.com/zhengminlai/JOIN>

⁵<http://konect.uni-koblenz.de/networks/>

⁶<http://snap.stanford.edu/data/>

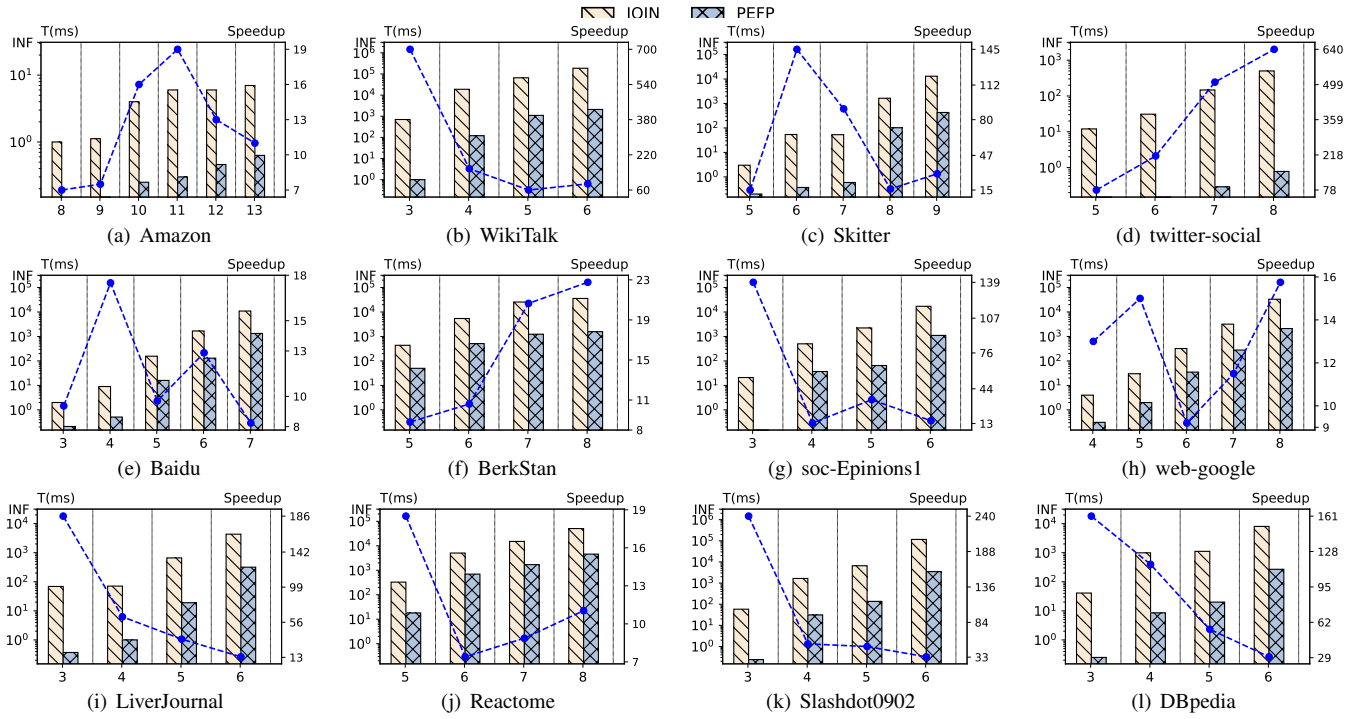


Fig. 8. Query Processing Time of Tuning k for All Datasets

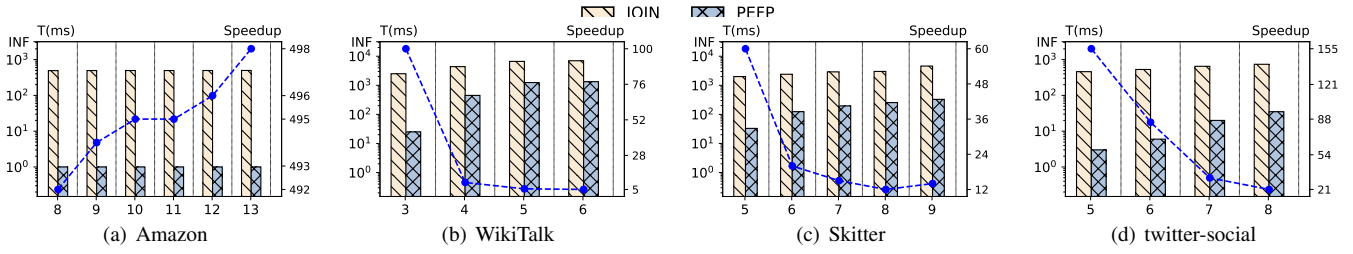


Fig. 9. Preprocessing Time of Tuning k for Different Datasets

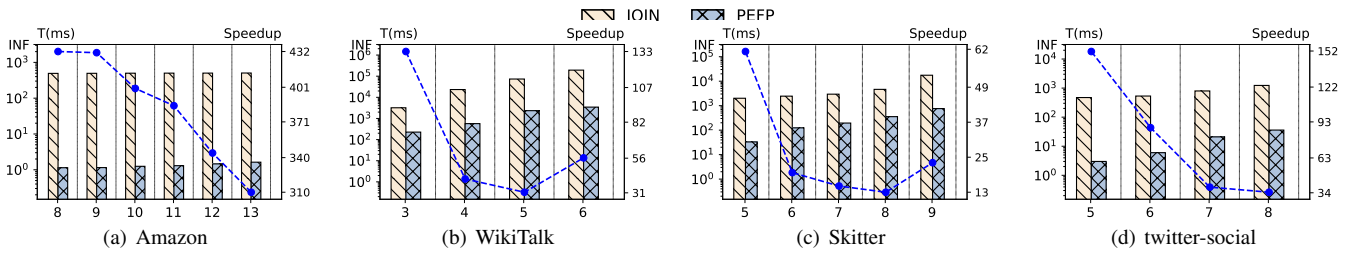


Fig. 10. Total Time of Tuning k for Different Datasets

which is same as the remaining experiments. We set the query time of an algorithm to INF if it cannot finish in 10,000 seconds.

(1) Effect of k . The results shown in Fig. 8 indicate that PEFP’s query processing time outperforms JOIN on all datasets for fixed k . It is not surprising that the time grows exponentially w.r.t k as s - t k -path number grows exponentially w.r.t k [4]. However, this does not hold for Amazon (Fig. 8(a)) – the time only grows marginally w.r.t k . An explanation would be that Amazon is an extremely small and sparse graph, and hence the number of reported results would be too small to see significant changes of query time when tuning k . Note that in BerkStan (Fig. 8(f)), the query time of $k = 7$ is almost the

same as the one of $k = 8$. This makes sense as we find their reported number of paths are on the same order of magnitude, which is 10^6 . The same explanation can be applied to WikiTalk (Fig. 8(b)) with $k = 5$ and $k = 6$.

From the perspective of the acceleration ratio (or speedup) w.r.t k , there are some interesting findings from inspecting Fig. 8. For most graphs like Amazon, Baidu, BerkStan and Reactome, the acceleration ratio remains rather stable, which is around $10\times$ to $20\times$ speedup. Note that the greatest difference between JOIN and PEFP is that JOIN is a DFS-based algorithm with carefully designed pruning technique BC-DFS, while PEFP is a BFS-based parallel algorithm on FPGA with a less delicate pruning technique (e.g., barrier check shown

in VI). When k is small, query processing is dominated by the expansion rather than the verification procedure, where the expansion can be fully pipelined in PEPF. Therefore, a substantial speedup can be observed when k is small in most graphs (e.g., $> 600\times$ speedup in WikiTalk with $k = 3$).

Another intriguing fact, as illustrated in Fig. 8(d), is the speedup of twitter-social tends to increase when k ranges from 5 to 8. This is because twitter-social is a graph with a very low diameter, which is 4.96 for 90% of the graph as demonstrated in TABLE II. Nevertheless, the minimal k set in twitter-social is 5, thus the pruning power of both JOIN’s BC-DFS and PEPF’s barrier check is almost zero. Under such condition, the query time is dominated by expansion; hence PEPF shows its considerable superiority over JOIN. We can explain the dramatic upsurge of speedup in Skitter from $k = 5$ to $k = 6$ in similar way; that is, as the D_{90} of Skitter is 5.85, the pruning power of BC-DFS becomes rather weak when k changes from 5 to 6.

(2) Effect of Dataset. It is apparent that for a given k , the query processing time varies in datasets with different graph topologies. What stands out in Fig. 8 is that twitter-social’s query time is much more than Amazon’s (e.g., $k = 8$). Although their numbers of vertices and edges are similar according to TABLE II, the diameter of Amazon is 44 while the diameter of twitter-social is only 8. This implies that twitter-social is a graph with considerable local density. Consequently, for a given k , the query time of twitter-social is much more than that of Amazon. However, the speedup in Amazon is significantly less than that in twitter-social. The reason is that the number of intermediate results in Amazon is too low to observe a substantial acceleration ratio. The same explanation can be applied to Skitter with $k = 5$.

Baidu is a smaller dataset with similar average degree compared to Skitter. Nevertheless, for a given k (e.g., $k = 6$), the query time of Baidu is much more than Skitter’s. This is because there exist some extremely dense subgraphs in Baidu. In addition, the acceleration ratio of Baidu is less competitive than Skitter’s, suggesting that PEPF tends to have a greater speedup in sparse graphs than in dense graphs. A possible reason is that the pruning power of JOIN is stronger in dense graphs, which tames the acceleration ratio brought by the parallelism of PEPF.

Overall, benefited from the huge parallelism offered by FPGA and the reduced search space by induced subgraph, PEPF outperforms JOIN by more than 1 order of magnitude by average, and up to 2 orders of magnitude in query processing time.

C. Evaluate Query Preprocessing Time

In Fig. 9, we evaluate the query preprocessing time of PEPF and JOIN by varying the hop constraint k on four datasets with different topologies, namely Amazon, WikiTalk, Skitter and twitter-social.

Fig. 9 shows that PEPF outperforms JOIN in all datasets w.r.t k . Particularly, in Fig. 9(a), PEPF is $495\times$ faster than JOIN by average, and the acceleration ratio does not change dramatically as k increases. The main reason is that Amazon is a very small and sparse graph, and minor tuning of k does not affect the preprocessing time of both JOIN and PEPF

in such graphs. In addition, it is reported in Fig. 9(a) that JOIN’s complicated preprocessing procedures are rather costly in small and sparse graphs compared with PEPF.

As shown in Fig. 9(b), Fig. 9(c), and Fig. 9(d), we can expect more than $10\times$ acceleration ratio on average. Specifically, PEPF can achieve more than $100\times$ speedup when k is small (e.g., $k = 5$ in Fig. 9(d)), since JOIN’s preprocessing cost is much more expensive than PEPF’s in this case. Furthermore, the acceleration ratio of the three datasets tends to decrease w.r.t k , for JOIN’s preprocessing time w.r.t k is more stable than PEPF in these datasets. Nevertheless, JOIN fails to outperform PEPF as its preprocessing needs to perform k -hop BFS and expensive set intersections in computing middle vertices cut [4], while PEPF only needs to perform $(k - 1)$ -hop BFS as introduced in Section V. As a result, PEPF outperforms JOIN by more than 1 order of magnitude by average, and up to 2 orders of magnitude in preprocessing time.

D. Evaluate Total Time

In this subsection, we evaluate the total running time of a given query, where the total time is the sum of query preprocessing and query processing time. As shown in Fig. 10, we investigate the total time of PEPF and JOIN by varying the hop constraint k on four datasets, namely Amazon, WikiTalk, Skitter and twitter-social. Then we report the total time of all datasets with $k = 5$ in Fig. 11, where the white part represents query processing time, and the grey part denotes preprocessing time.

(1) Effect of k . In Fig. 10, we report the total time of JOIN and PEPF on four datasets by varying k . The acceleration ratio of Amazon tends to decrease when k ranges from 10 to 13. This makes sense as PEPF’s total time w.r.t k grows faster than JOIN’s in an extremely sparse graph. For the other three datasets, a similar trend of speedup is observed. Particularly, the speedup is substantial with a small k . Nevertheless, when k increases, the speedup tends to first decrease, and then remain stable. This is because when k is small, the total time of JOIN is dominated by preprocessing time, and hence we can expect a considerable speedup as discussed in Section VII-C. However, this significant advantage brought by preprocessing will be paid off by query processing when increasing k .

(2) Effect of Dataset. The total time of all datasets is illustrated in Fig. 11. We set $k = 8$ for *Amazon* and *twitter-social* to achieve similar performance with other graphs while $k = 5$ for the remaining graphs. What stands out in Fig. 11 is that both JOIN and PEPF’s total time are dominated by preprocessing time in sparse graphs like Amazon and Skitter, while the total time of JOIN in twitter-social is dominated by query processing time because of the dataset’s local density topology. It is worth mentioning that the graph density is a key factor influencing total time – when the graph is sparse, the total time is dominated by preprocessing time, and vice versa.

In short, the results in this experiment show that PEPF outperforms JOIN by more than 1 order of magnitude by average, and up to 2 orders of magnitude in total time.

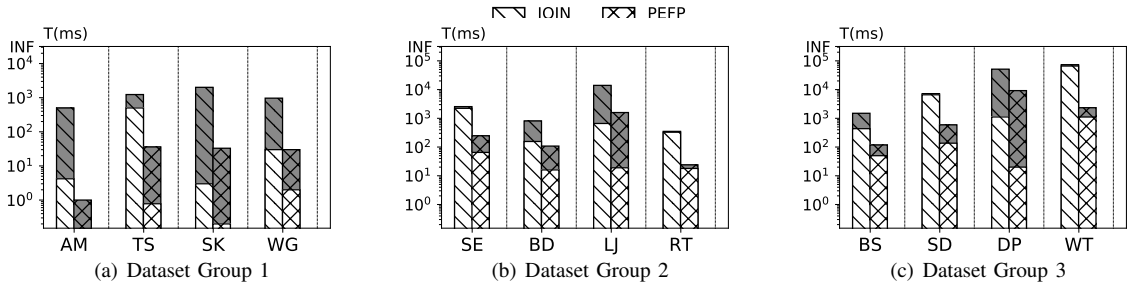


Fig. 11. Average Total Time of All Datasets with $k = 5$

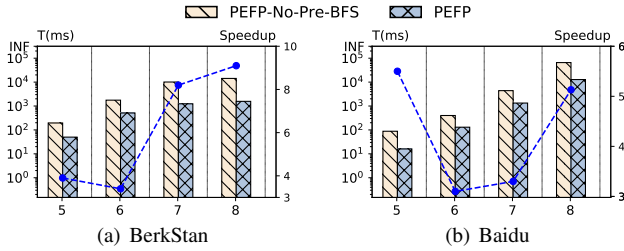


Fig. 12. Evaluation of Pre-BFS Technique Tuning k

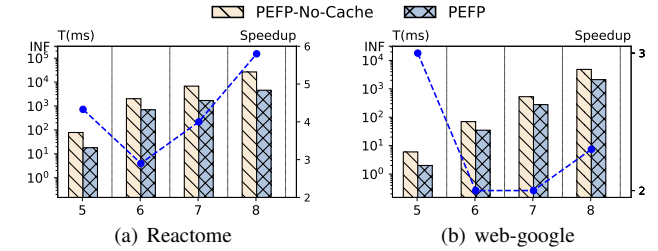


Fig. 14. Evaluation of Caching Technique Tuning k

Dataset	$l = 2$	$l = 3$	$l = 4$	$l = 5$	$l = 6$	$l = 7$
Baidu	3117	17346	10033	4522	1064	0
BerkStan	9374	14376	10678	7991	5114	0
WikiTalk	52498	103544	63935	13207	1198	0
LiveJournal	276802	351396	299003	165018	11027	0

TABLE III

NUMBER OF NEWLY GENERATED INTERMEDIATE PATHS WHEN DOING ONE-HOP EXPANSION WITH 1,000 PATHS FOR DIFFERENT PATH LENGTH l WITH $k = 8$

E. Evaluate Efficiency of Pre-BFS

As demonstrated in Fig. 12, we evaluate the efficiency of our proposed preprocessing algorithm Pre-BFS on BerkStan and Baidu, where **PEFP-No-Pre-BFS** denotes the PEFP algorithm without Pre-BFS. It is shown that Pre-BFS can achieve $3\times$ to $9\times$ speedup in the two datasets. As we mentioned in Section V and Section VI, Pre-BFS can improve the performance of PEFP in two ways. First, it significantly reduces the search space by removing invalid nodes that will not be contained in any $s-t$ k -path. Second, the subgraph it extracts is much smaller than the original graph, making it possible for FPGA to cache the whole subgraph on BRAM; thus, it is necessary to apply Pre-BFS optimization for $s-t$ k -path enumeration.

F. Evaluate Efficiency of Batch-DFS

(1) Number of Intermediate Paths. To better illustrate the intuition of Batch-DFS, for each path length $l \in [2, k - 1]$ (we set k to 8 in this experiment), we randomly pick 1,000

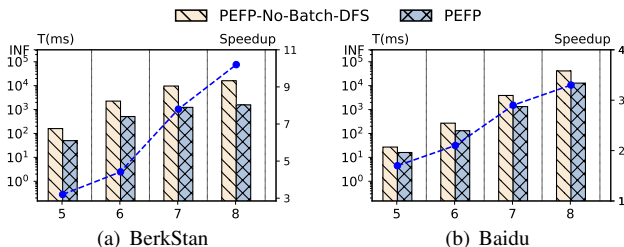


Fig. 13. Evaluation of Batch-DFS Technique Tuning k

paths to do one-hop expansion and evaluate the number of newly generated intermediate paths on four datasets – Baidu, BerkStan, WikiTalk and LiveJournal. The experimental results are presented in TABLE III, which shows that given $k = 8$, for two small path lengths $l_1 = 2, l_2 = 3$, the number of newly produced paths tends to increase. We attribute this to the fact that, when l is small, the pruning power of path length is rather weak, while the chance of touching the high degree nodes tends to increase w.r.t l . Nevertheless, the pruning power of hop constraint is getting stronger when l becomes large – the number of newly generated paths tends to decrease when $l > 3$. Specifically, it will generate 0 intermediate paths when $l = k - 1 = 7$. Therefore, the experimental results demonstrate the effectiveness of Batch-DFS which follows the art of “*always process a batch of the longest paths first*” to save memory.

(2) Query Time. The efficiency evaluation of our proposed Batch-DFS technique on BerkStan and Baidu is shown in Fig. 13, where **PEFP-No-Batch-DFS** denotes the PEFP algorithm without Batch-DFS. Instead, we use First-In-First-Out (FIFO) batching order to replace Batch-DFS, which is “*always process a batch of the shortest paths first*”. The results in that figure show that Batch-DFS can achieve $2\times$ to $10\times$ speedup. Moreover, we can see that the speedup for BerkStan is higher than Baidu’s. This is reasonable as the number of intermediate results of BerkStan is larger than Baidu’s, which brings more I/O cost without Batch-DFS.

G. Evaluate Efficiency of Caching

In Fig. 14, we evaluate the efficiency of our proposed caching techniques on Reactome and web-google, where we use **PEFP-No-Cache** to denote the PEFP algorithm without caching techniques. It is shown that caching can achieve more than $2\times$ speedup by average, and up to $6\times$ speedup for PEFP-No-Cache. It is worth mentioning that caching results in better speedup in Reactome than in web-google. This makes sense as Reactome is a much denser graph than web-google, which incurs more vertex and edge data accesses to DRAM; hence its performance is significantly affected.

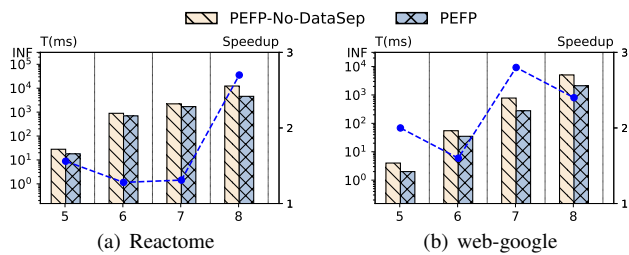


Fig. 15. Evaluation of Data Separation Technique Tuning k

H. Evaluate Efficiency of Data Separation

As illustrated in Fig. 15, we evaluate the efficiency of our proposed data separation technique on Reactome and web-google, where **PEFP-No-DataSep** denotes the PEFP algorithm without data separation technique. The results in that figure show that data separation can achieve up to $3\times$ speedup. This is because data separation enables dataflow optimization for the path verification module such that its inner stages can be executed in parallel, which improves the overall performance.

VIII. CONCLUSION

In this paper, we propose the first FPGA-based algorithm PEFP to efficiently solve the s - t k -path enumeration problem. On the host side, we develop the preprocessing algorithm Pre-BFS to reduce the search space. On the FPGA side, we first propose a novel DFS-based batching and caching technique to improve the system latency by reducing read/write operations from/to FPGA DRAM. Then, a data separation technique for the path verification module is developed, which enables its inner stages to be executed in parallel. We conduct extensive experiments on 12 real-world datasets, whose results show that PEFP outperforms the state-of-the-art algorithm JOIN by more than 1 order of magnitude by average, and up to 2 orders of magnitude in terms of preprocessing time, query processing time and total time, respectively.

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REFERENCES

- [1] Y. Peng, Y. Zhang, W. Zhang, X. Lin, and L. Qin, "Efficient probabilistic k -core computation on uncertain graphs," in *2018 IEEE 34th International Conference on Data Engineering (ICDE)*. IEEE, 2018, pp. 1192–1203.
- [2] B. Liu, L. Yuan, X. Lin, L. Qin, W. Zhang, and J. Zhou, "Efficient (α, β) -core computation in bipartite graphs," *VLDB J.*, vol. 29, no. 5, pp. 1075–1099, 2020.
- [3] Y. Peng, Y. Zhang, X. Lin, L. Qin, and W. Zhang, "Answering billion-scale label-constrained reachability queries within microsecond," *Proceedings of the VLDB Endowment*, vol. 13, no. 6, pp. 812–825, 2020.
- [4] Y. Peng, Y. Zhang, X. Lin, W. Zhang, L. Qin, and J. Zhou, "Towards bridging theory and practice: hop-constrained st simple path enumeration," in *International Conference on Very Large Data Bases*. VLDB Endowment, 2019.
- [5] X. Qiu, W. Cen, Z. Qian, Y. Peng, Y. Zhang, X. Lin, and J. Zhou, "Real-time constrained cycle detection in large dynamic graphs," *PVLDB*, vol. 11, no. 12, pp. 1876–1888, 2018.

- [6] F. Chung, L. Lu, and V. Vu, "Eigenvalues of random power law graphs," *Annals of Combinatorics*, vol. 7, no. 1, pp. 21–33, 2003.
- [7] M. Besta, D. Stanojevic, J. D. F. Licht, T. Ben-Nun, and T. Hoefler, "Graph processing on fpgas: Taxonomy, survey, challenges," *arXiv preprint arXiv:1903.06697*, 2019.
- [8] Xilinx, "https://www.xilinx.com/products/boards-and-kits/alveo.html."
- [9] D. Yue, X. Wu, Y. Wang, Y. Li, and C. Chu, "A review of data mining-based financial fraud detection research," in *International Conference on Wireless Communications, Networking and Mobile Computing*, 10 2007, pp. 5519 – 5522.
- [10] M. Kimura and K. Saito, "Tractable models for information diffusion in social networks," in *European conference on principles of data mining and knowledge discovery*. Springer, 2006, pp. 259–271.
- [11] U. Leser, "A query language for biological networks," *Bioinformatics*, vol. 21, pp. ii33–9, 10 2005.
- [12] R. Rizzi, G. Sacomoto, and M. Sagot, "Efficiently listing bounded length st-paths," in *IWOCA*, 2014, pp. 318–329.
- [13] R. Grossi, A. Marino, and L. Versari, "Efficient algorithms for listing k disjoint st-paths in graphs," in *Latin American Symposium on Theoretical Informatics*. Springer, 2018, pp. 544–557.
- [14] K. Böhmová, L. Häfziger, M. Mihalák, T. Pröger, G. Sacomoto, and M.-F. Sagot, "Computing and listing st-paths in public transportation networks," *Theory of Computing Systems*, vol. 62, no. 3, pp. 600–621, 2018.
- [15] D. E. Knuth, *The Art of Computer Programming, Volume 4A: Combinatorial Algorithms*. Addison-Wesley Professional, 2011.
- [16] N. Yasuda, T. Sugaya, and S. Minato, "Fast compilation of s - t paths on a graph for counting and enumeration," in *Proceedings of the 3rd Workshop on Advanced Methodologies for Bayesian Networks, AMBN*, 2017, pp. 129–140.
- [17] E. Birmelé, R. A. Ferreira, R. Grossi, A. Marino, N. Pisanti, R. Rizzi, and G. Sacomoto, "Optimal listing of cycles and st-paths in undirected graphs," in *SODA*, 2013, pp. 1884–1896.
- [18] G. L. D. and K. N. P., "Identifying certain types of parts of a graph and computing their number," *Ukrainian Mathematical Journal*, vol. 24, no. 3, pp. 313–321, 1972.
- [19] P. Giscard, N. Kriege, and R. C. Wilson, "A general purpose algorithm for counting simple cycles and simple paths of any length," *CoRR*, vol. abs/1612.05531, 2016.
- [20] Z. Gotthilf and M. Lewenstein, "Improved algorithms for the k simple shortest paths and the replacement paths problems," *Information Processing Letters*, vol. 109, no. 7, pp. 352–355, 2009.
- [21] J. Y. Yen, "Finding the k shortest loopless paths in a network," *Management Science*, vol. 17, no. 11, pp. 712–716, 1971.
- [22] J. C. Rivera, H. M. Afsar, and C. Prins, "Mathematical formulations and exact algorithm for the multitrip cumulative capacitated single-vehicle routing problem," *European Journal of Operational Research*, vol. 249, no. 1, pp. 93–104, 2016.
- [23] N. Shi, S. Zhou, F. Wang, Y. Tao, and L. Liu, "The multi-criteria constrained shortest path problem," *Transportation Research Part E: Logistics and Transportation Review*, vol. 101, pp. 13–29, 2017.
- [24] H. Liu, C. Jin, B. Yang, and A. Zhou, "Finding top- k shortest paths with diversity," *IEEE Transactions on Knowledge and Data Engineering*, vol. 30, no. 3, pp. 488–502, 2017.
- [25] L. Talarico, K. Sørensen, and J. Springael, "The k -dissimilar vehicle routing problem," *European Journal of Operational Research*, vol. 244, no. 1, pp. 129–140, 2015.
- [26] M. Tommiska and J. Skyttä, "Dijkstra's shortest path routing algorithm in reconfigurable hardware," in *International Conference on Field Programmable Logic and Applications*. Springer, 2001, pp. 653–657.
- [27] S. Zhou, C. Chelmiss, and V. K. Prasanna, "Accelerating large-scale single-source shortest path on fpga," in *2015 IEEE International Parallel and Distributed Processing Symposium Workshop*. IEEE, 2015, pp. 129–136.
- [28] U. Bondhugula, A. Devulapalli, J. Fernando, P. Wyckoff, and P. Sadayappan, "Parallel fpga-based all-pairs shortest-paths in a directed graph," in *Proceedings 20th IEEE International Parallel & Distributed Processing Symposium*. IEEE, 2006, pp. 10–pp.
- [29] B. Betkaoui, Y. Wang, D. B. Thomas, and W. Luk, "Parallel fpga-based all pairs shortest paths for sparse networks: A human brain connectome case study," in *22nd International Conference on Field Programmable Logic and Applications (FPL)*. IEEE, 2012, pp. 99–104.
- [30] Compressed sparse row, "https://en.wikipedia.org/wiki/sparse_matrix."