Research Article

An Efficient Design of QCA Full-Adder-Subtractor with Low Power Dissipation

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The continuous market demands for high performance and energy-efficient computing systems have steered the computational paradigm and technologies towards nanoscale quantum-dot cellular automata (QCA). In this paper, novel energy- and area-efficient QCA-based adder/subtractor designs have been proposed. First, a QCA-based 3-input XOR gate is designed and then a full adder and a full subtractor are realized. The power consumption of the proposed design was tested via the QCAPro estimator tool with different kind of energy ($\gamma = 0.5\ Ek$, $\gamma = 1.0\ Ek$, and $\gamma = 1.5\ Ek$) at temperature T = 2 in Kelvin. QCADesigner 2.0.03 software was applied to evaluate the simulation results of the proposed designs. The proposed design has better complexity than the conventional designs in terms of cell count, area, and power dissipation.

1. Introduction

Over the past few decades, the microelectronics industry has been driven by increasing market demands for enhanced integration, energy efficiency, and speed of integrated circuits (ICs) [1–4]. On one side, traditional Complementary Metal Oxide Semiconductor (CMOS) based transistors cannot be reduced much smaller than their current size, due to current leakage problems arising from quantum mechanically tunneling, so the device cannot be switched off properly and increased heat dissipation, which threatens to melt the chip. This fact has pushed designers to search for new technologies to allow greater integration and lower power consumption for Digital Signal Processor (DSP) IC applications. On the other side, scalability of the classical technology is reaching the end that makes the development of nanomolecular instruments. International Technology Roadmap for Semiconductors (ITRS) summarizes several new nanodevices that can replace CMOS, such as single-electron transistor (SET), resonant tunneling diode (RTD), carbon nanotubes (CNT), and quantum-dot cellular automata (QCA) [5]. Quantum-dot cellular automata (QCA) is one of the most promising solutions to design

ultralow power and very-high-speed digital circuits, which can be scaled down to the molecular nanoscale device level [6]. It is an up-and-coming nanotechnology with strong prospects to supplement and possibly replace the current CMOS technology [7–9]. Unlike conventional CMOS structures, QCA-based structures represent binary values based on the positions of confined electrons in certain quantum dots. This ultimately allows the QCA-based structure to surpass CMOS-based counterparts in terms of switching speed, device density, and power consumption. Essentially, QCA offers potential advantages of ultralow power dissipation. QCA is expected to achieve very high device density of 1012 device/cm^2 and switching speeds of 10 ps and a power dissipation of 100 W/cm^2 [10]. In QCA technology, no voltage or current is used. It is based on Coulombic interactions of electrons in the quantum dots. Therefore, it will be the alternative candidate for CMOS technology currently used in integrated circuits (ICs). Several attempts are made towards the cost-effective realization of QCA circuit in [11–19]. QCA logic design circuit is stimulated by its applications in low-power electronic design. It has lately attracted significant attention. On the other hand, adder is one of the most important operations in many

digital applications. Moreover, other operations such as subtraction, multiplication, and division are usually performed by adders. There are a number of research papers in literature which deal with the design of adder using QCA technology. Most of these designs rely on a so-called gate-based design approach. In other words, this approach is based on the use of a majority voter, which when exploited in complex designs leads to an increase in time delay, size, and power consumption. So an efficient QCA-based adder design can be of great assistance in designing arithmetic circuits. The main contributions of this manuscript about the proposed structures are summarized as follows:

(i) A novel structure of 3-input XOR gate, based on the possibility of achieving the desired function using the electrostatic interactions between cells, has been proposed.

(ii) The proposed 3-input XOR circuit is further utilized for designing the smallest QCA full adder and subtractor efficiently which are containing 19 and 20 cells, respectively.

(iii) Comparison results show the remarkable improvement apropos of the complexity, occupied area, power dissipation, and latency.

The main concern of this paper is to present a new design of 1-bit full adder and 1-bit full subtractor based on QCA technology, which yields significant reduction in terms of cell count, area, and energy dissipation.

The organization of the paper is as follows: Section 2 discusses the basics of QCA technology. In Section 3, the design and the simulation of the proposed designs have been presented. In Section 4, the results obtained from the simulation of the circuits are discussed and a comparison has been done in terms of area, cell count, delay, and power dissipation. Conclusions are given in Section 5.

2. Background of QCA Technology

Typically, QCA devices are described on the basis of symmetric square cells, whereby all computational logic gates and memory structures can be correctly imitated. These structures can be implemented by assembling QCA cells in a specific geometric pattern to achieve the desired logic function. The QCA cell has four quantum dots and two electrons [7]. Two electrons tend to occupy diagonal quantum dots owing to the Coulomb force, forming two configurations for encoding binary logical "0" and "1" as depicted in Figure 1(b). The majority and the inverter gates are two fundamental gates of QCA technology used for the circuit design as shown in Figures 1(d) and 1(e), respectively. The inverter can inverse the polarization state of an input cell by arranging two cells diagonally. The three-input majority gate is a core logic device of QCA [6–10]. In addition, the QCA majority voter gate contains five cells forming a cross with a cell in the center as a device cell, three cells as its inputs, and one cell as its output. The device cell polarity is determined based on Coulomb repulsion of the three inputs and the polarity is transferred to the output. Unlike

traditional CMOS circuits, which rely on currents to process information, the calculation of QCA circuits relies entirely on the Coulomb force between electrons, which is fast and disordered. In this area, the clocking mechanism provides energy for QCA circuits to make up for the loss in dissipative processes due to switching the state of polarization. In this context, energy is provided by an external electric or magnetic field. Generally, clocking has four phases, which are Switching, Hold, Release, and Relax, as illustrated in Figure 1(a). In QCA, four clock signals are used, where a clock has a phase difference of 90 degrees rather than the next and the previous signals. For example, when Clock0 is in the Hold phase, Clock1 is in the Switching phase and data transmission is performed from Clock0 cells to Clock1 cells [9, 10].

3. Proposed Designs

In this section, a novel 3-input XOR gate with excellent performance indicators has been proposed. Thereafter, an optimum full adder and a full subtractor are provided via the proposed gate.

3.1. The Proposed Three-Input QCA XOR Gate. The XOR gate is the essential component of many digital circuits, such as parity bit generator circuit and arithmetic circuits. Up to date, various models of XOR gates have been reported in the literature [20–24]. Figure 2 shows some previously designed exclusive-OR gates. In 2014, Angizi et al. [20] presented an XOR gate based on QCA technology. This circuit consists of 94 cells and occupied $0.073\,\mu\text{m}^2$ area with a delay of 1.5 clock cycles. In 2016, another three-input XOR gate was introduced by Ahmad et al. [21]. As can be seen, this design consists of 14 cells with an area of $0.022\,\mu\text{m}^2$. So, output appears after 0.5 clock cycle. In 2017, Bahar et al. [22] presented another XOR gate whose layout realization is shown in Figure 2(e). As shown in Figure 2(e), this design consists of 12 cells with an area of $0.012\,\mu\text{m}^2$. In this work, we first designed a novel 3-input XOR gate; then a new QCA full subtractor and a full adder are suggested using this circuit. The proposed QCA layout of 3-input XOR gate is depicted in Figure 3 which contains 8 cells with occupied area of $0.006\,\mu\text{m}^2$ and requires two clock phases. Besides, it is achieved without using any majority gate, which leads to planning with lower energy consumption and fewer space. Here, the desired function of the proposed 3-input XOR gate is based on electrostatic interactions between cells.

3.2. Proposed Full Adder and Full Subtractor Designs. Previous related investigations about full adder and subtractor have been implemented widely on QCA technology [25–31]. These performance indicators about full adder and full subtractor are considered: excellent power consumption, smaller delay, and lower complexity. Here, the proposed 3-input XOR gate is used to obtain both an efficient design of full adder and full subtractor in terms of latency, area, delay, and power consumption. The proposed designs are verified by simulating them with QCADesigner software and the
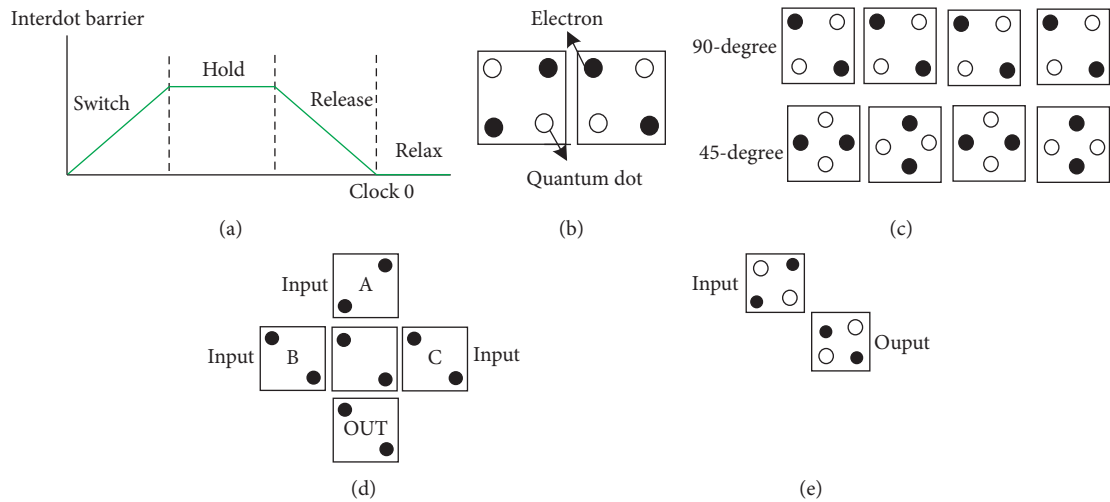
FIGURE 1: (a) The four-phase clocking scheme. (b) The logical states defined by the electron configuration for the QCA cell consisting of four quantum dots, (c) A binary wire that can be achieved by two cell layouts. (d) The majority gate with three inputs and the single output with a binary state decided by majority voting behaviour, (e) The Inverter that is achieved by placing the two cells diagonally.
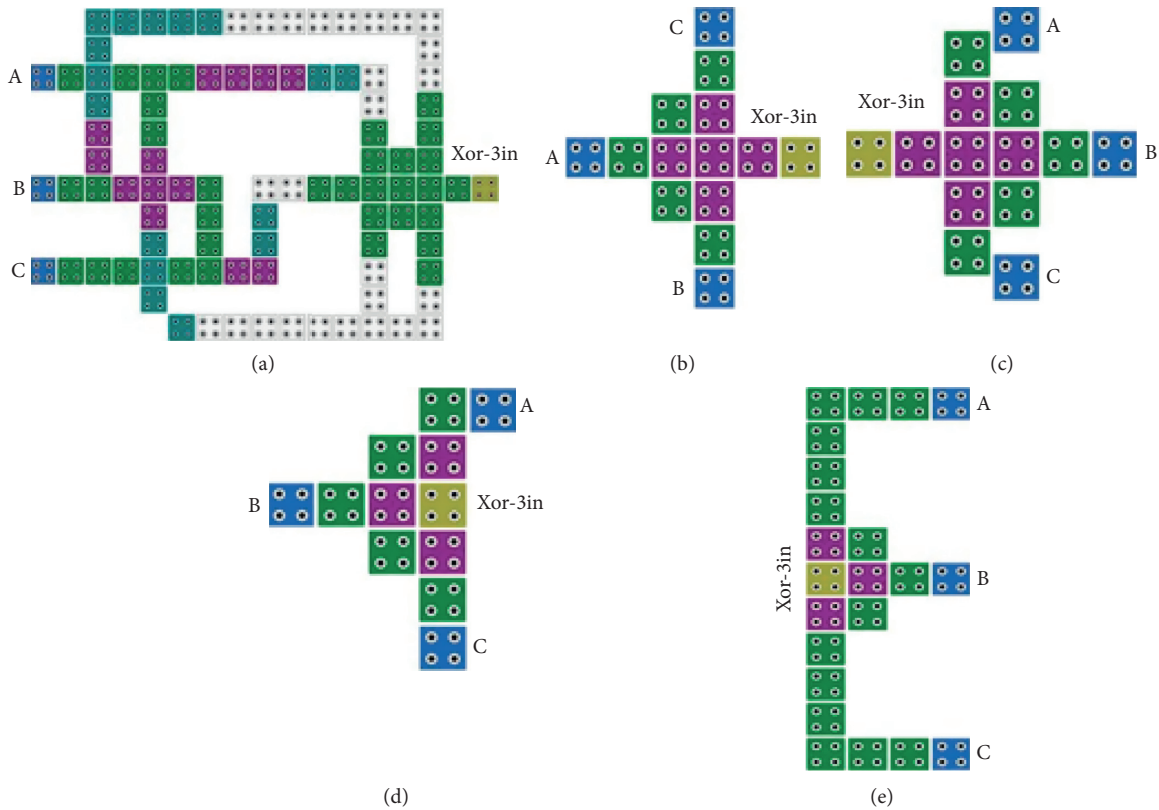

FIGURE 2: Previous three-input XOR gate based on QCA technology. (a) [20], (b) [21], (c) [22], (d) [23], and (e) [24].

results are given in Figures 4 and 5, respectively. The adder proposed here requires only 19 QCA cells with two clock phases. The area required for the proposed full adder is about $0.01\,\mu m^2$. In addition, an optimal full subtractor based on the suggested 3-input XOR gate is proposed. It includes 20 QCA cells and occupies an area of $0.01\,\mu m^2$. Here, the output generation of the proposed full subtractor occurs in two

phases of the clock. Consequently, the most prominent feature of the proposed designs compared to all previous traditional QCA circuits is performing computations with the least circuit complexity and least energy dissipation compared to existing traditional QCA schemes. Various costs such as cell count, area occupation, and latency for full adder and full subtractor are shown in Tables 1 and 2.
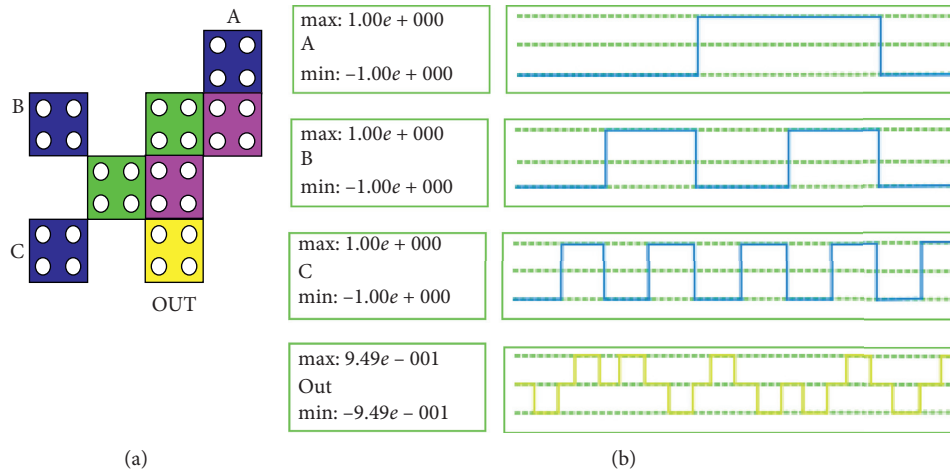
(a)

| max: 1.00e + 000 |
| A |
| min: −1.00e + 000 |

| max: 1.00e + 000 |
| B |
| min: −1.00e + 000 |

| max: 1.00e + 000 |
| C |
| min: −1.00e + 000 |

| max: 9.49e − 001 |
| Out |
| min: −9.49e − 001 |

(b)

FIGURE 3: (a) The QCA layout of the proposed three-input XOR gate; (b) its simulation results.

(a)

| max: 1.00e + 000 |
| A |
| min: −1.00e + 000 |

| max: 1.00e + 000 |
| B |
| min: −1.00e + 000 |

| max: 1.00e + 000 |
| C |
| min: −1.00e + 000 |

| max: 9.49e − 001 |
| Sum |
| min: −9.49e − 001 |

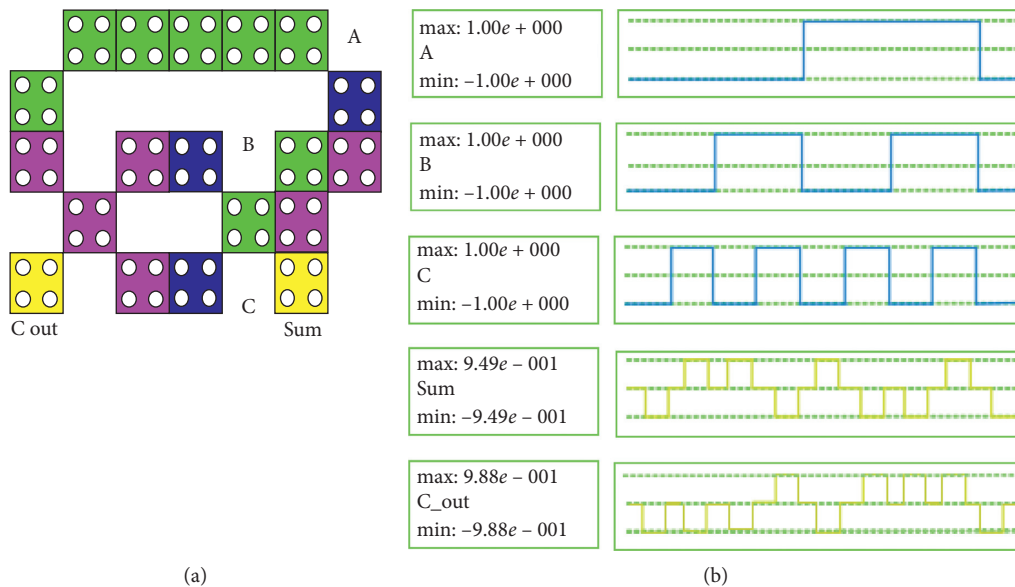| max: 9.88e − 001 |
| C_out |
| min: −9.88e − 001 |

(b)

FIGURE 4: (a) The layout of the proposed full adder and (b) its simulation results.

4. Results and Discussions

Reduction in the adder/subtractor size will lead to a subsequent reduction of the scaled-up systems. In this section, a comparison is made between the proposed QCA 3-input XOR gate and the previous ones. Besides, a comparison is made between the proposed QCA full subtractor and previous works, and, finally, we present a comparison between the proposed QCA full adder and similar previous schemes. Here, the advantage of the QCA circuits implemented in this manuscript is evident. As can be seen from Table 3, the suggested XOR gate has a significant advantage over all

previous designs. In fact, the area has improved at least 45.4% and cell count at least 42.8%. On the other hand, the proposed full adder and full subtractor have already been designed and simulated using QCADesigner; compared with conventional schemes, the numbers of cells consumed are reduced by 58.69% and 37.5%, respectively. The designs reported in this paper are superior in terms of important parameters. Specific parameters are shown in Tables 1 and 2. Figure 6 depicts the considerable optimization of the proposed design with regard to cell count and used space. It can be observed from Figure 5 that the proposed design performs better as compared to previously reported works in
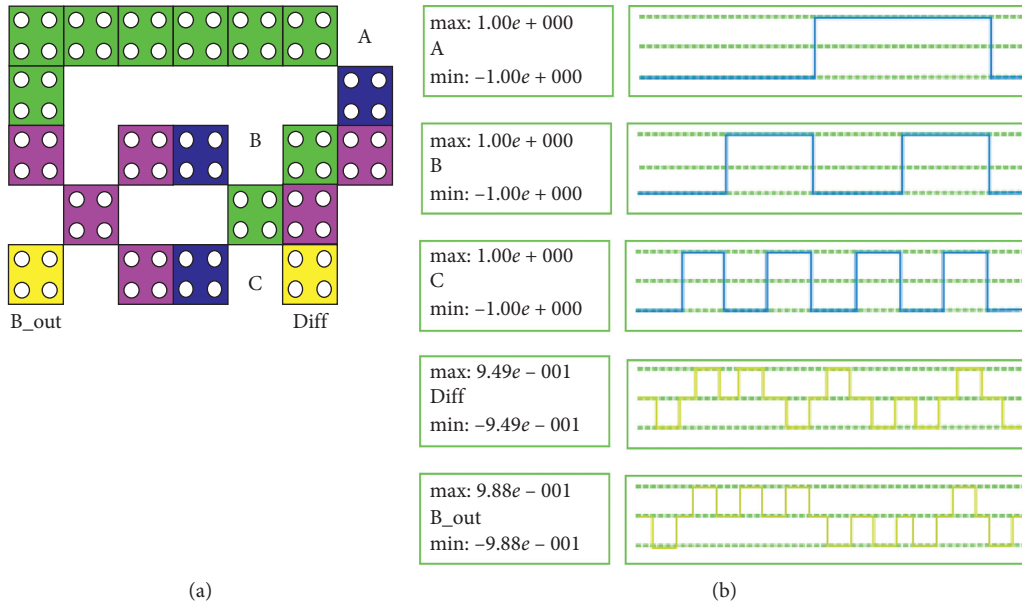
(a)   (b)

FIGURE 5: (a) The layout of the proposed full adder and (b) its simulation results.

TABLE 1: Full subtractor comparison.

Subtractor circuit	Area (μm^2)	Cell count	Latency
Ref [32]	0.205	178	8
Ref [33]	0.168	136	7
Ref [34]	0.1043	104	7
Ref [22]	0.0287	32	2
Proposed full subtractor	0.01	20	2

TABLE 2: Full adder comparison.

Adder circuit	Area (μm^2)	Cell count	Latency
Ref [35]	0.206	198	N
Ref [36]	0.144	135	1.5
Ref [37]	0.146	105	0.75
Ref [38]	0.0875	95	2.25
Ref [39]	0.0876	93	1.25
Ref [40]	0.0801	73	0.75
Ref [41]	0.044	73	0.75
Ref [42]	0.0434	59	1
Ref [43]	0.034	51	0.75
Ref [44]	0.042	49	1
Ref [45]	0.035	46	1
Proposed full adder	0.01	19	0.5

TABLE 3: Three-input QCA XOR gates comparison.

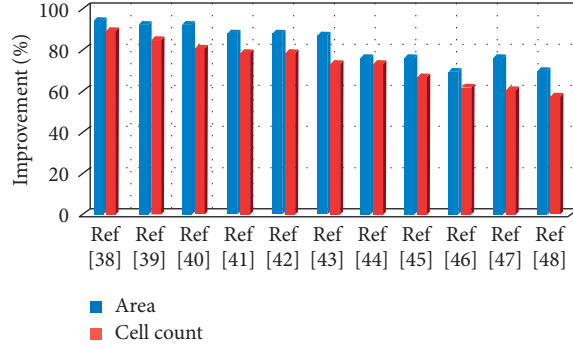| Three-input XOR	Area (μm^2)	Cell count	Latency
Ref [22]	0.012	12	1
Ref [24]	0.017	22	1
Ref [20]	0.073	94	1.5
Ref [21]	0.022	14	0.5
Ref [23]	0.011	14	0.5
Proposed design	0.006	8	0.5

FIGURE 6: Improvements of proposed adder over others.

TABLE 4: Power analysis results of the proposed 3-input XOR gate and previously reported designs.

| Three-input XOR gate	Leakage energy dissipation			Switching energy dissipation			Total energy dissipation		
	$0.5\ E_K$	$1\ E_K$	$1.5\ E_K$	$0.5\ E_K$	$1\ E_K$	$1.5\ E_K$	$0.5\ E_K$	$1\ E_K$	$1.5\ E_K$
Ref [47]	11.51	31.91	54.69	35.78	30.48	25.66	47.29	62.39	80.34
Ref [20]	19.65	59.28	106.51	126.79	112.29	97.95	146.44	171.57	204.47
Ref [48]	10.78	28.57	48.15	25.43	21.71	18.4	36.20	50.28	66.58
|Ref [48]	9.73	29.7	52.78	40.08	33.73	28.05	49.81	63.49	80.83
Ref [22]	1.54	4.85	8.27	10.58	9.32	8.02	12.11	14.17	16.28
Proposed XOR	1.32	3.76	7.15	9.11	8.49	7.17	10.43	12.25	14.32
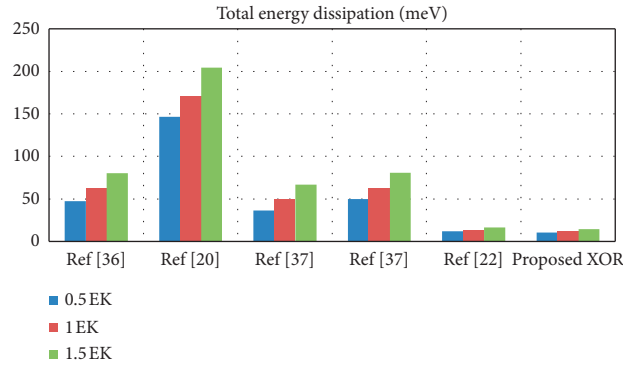
FIGURE 7: The total energy dissipation of the adders at three different tunneling energy levels.

terms of cell count, hence improving total area. As shown, the proposed design optimizes the QCA circuit complexity (cell count) by 58.69% compared to the best circuit reported in [45]. Besides, it improves the QCA occupied area by 71.72% over the best circuit reported in [45].

In this work, QCAPro software has been applied for energy depletion study, which estimates the polarization error and nonadiabatic switching power loss in QCA circuits. This tool uses a fast approximation-based technique to estimate highly erroneous cells in QCA circuit design [46]. Therefore, the power estimation of the proposed circuits is analyzed with the Hartree-Fock mean-field method approximation, where the Hamiltonian is given in the two-state model as [46]

$$H = \begin{bmatrix} \dfrac{-E_k}{2}\sum_i C_i f_{i,j} & -\gamma \\[2em] -\gamma & \dfrac{E_k}{2}\sum_i C_i f_{i,j} \end{bmatrix} = \begin{bmatrix} \dfrac{-E_k}{2}\left(C_{j-1}+C_{j+1}\right) & -\gamma \\[2em] -\gamma & \dfrac{E_k}{2}\left(C_{j-1}+C_{j+1}\right) \end{bmatrix}. \tag{1}$$
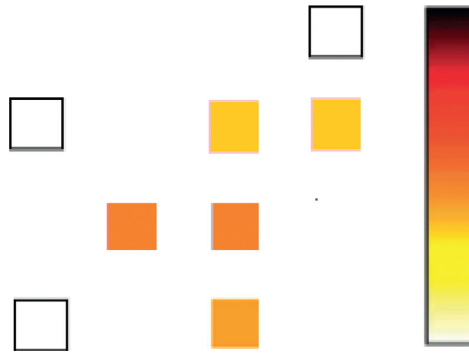
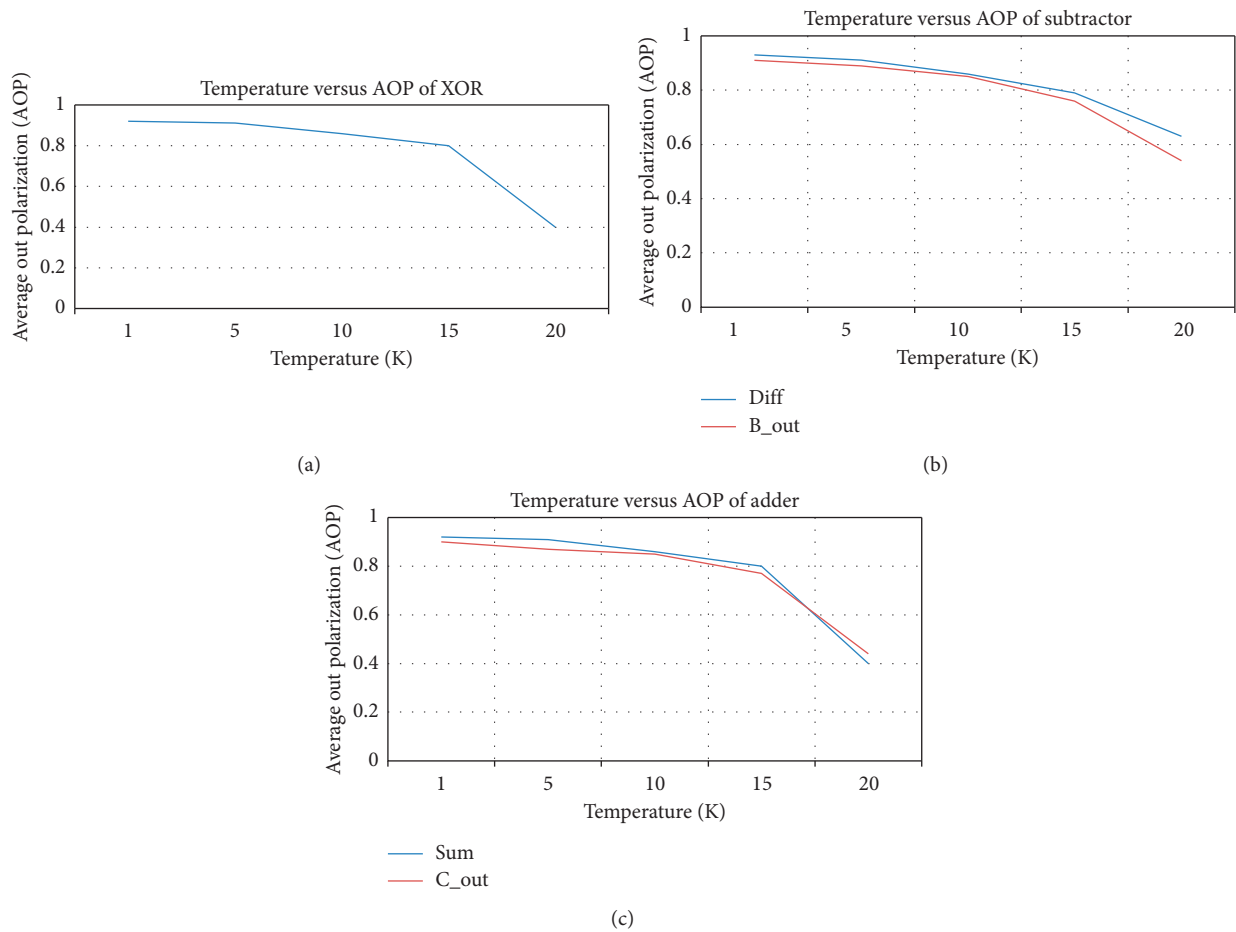FIGURE 8: The thermal layouts of proposed Feynman.

(a)

(b)

(c)

FIGURE 9: The calculated average output polarization (AOP) of the proposed designs against temperature T in Kelvin. (a) Three-input XOR gate, (b) subtractor for outputs "B_out" and "Diff," and (c) adder for outputs "Sum" and "C_out."

As per the upper constrained power estimation model [35], the power dissipation of a QCA cell is analyzed as

$$P_{diss} = \frac{E_{diss}}{T_{cc}} \frac{\hbar}{2T_{cc}} \overrightarrow{\Gamma}_+ \times \left[-\frac{\overrightarrow{\Gamma}_+}{|\overrightarrow{\Gamma}_+|} \tanh\left(\frac{\hbar|\overrightarrow{\Gamma}_+|}{k_B T}\right) + \frac{\overrightarrow{\Gamma}_-}{|\overrightarrow{\Gamma}_-|} \tanh\left(\frac{\hbar|\overrightarrow{\Gamma}_-|}{k_B T}\right) \right]. \tag{2}$$

The results associated with the power consumption analysis of the proposed XOR gate and the previously reported designs are depicted in Table 4. The energy dissipation comparisons of the XOR gates listed in Table 4 are depicted in bar-graph forms as shown in Figure 7. It can be seen from Figure 7 that the proposed gate consumes the lowest amount of energy over previous designs, and therefore it is very appropriate for ultralow power devices. The thermal layout of proposed 3-input XOR gate is shown in Figure 8.

The temperature impact on the average output polarization (AOP) of the proposed QCA circuits is carried out by performing different temperature runs with the QCADesigner software and the effect is depicted in Figure 9.

5. Conclusion

Design of low-power high-speed adder/subtractor is always a challenge for DSP applications. In this article, a novel design of 3-input XOR gate, 1-bit full adder, and 1-bit full subtractor in the QCA technology has been presented. The QCADesigner 2.0.3 simulation tool was used to verify the functional correctness of the proposed structures and assess their structural cost in terms of the occupied area. By comparison of previous designs and the proposed designs, it could be concluded that the proposed design has appropriate features and performance. In the future, we will strive to explore and construct more excellent full adder/full subtractor unit architecture in order to provide basic module for the larger-scale arithmetic operation circuits on QCA platform.

Data Availability

The data used to support the findings of this study are available from the corresponding author upon request.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

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