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New transformer-less DC–DC converter topologies with reduced voltage stress on capacitors and increased voltage conversion ratio

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Abstract

This article proposes new transformer-less step-up/down and step-up DC–DC topologies providing numerous merits such as less voltage stress on capacitors, lower duty-cycle, and higher voltage conversion ratio compared to other DC–DC converters. The proposed converters are extendible by benefiting from several switched-capacitors, making it possible to transfer more power from the converter. The proposed structures are more suitable for modern applications in which it is desirable to achieve high voltage gains by using non-extreme duty-cycles. For proving the analysis and claims, the detailed comparison and experimental results are presented. In the experiments, the dynamic performance of the proposed converters is also validated.

1 | INTRODUCTION

Among various types of DC–DC converters, structures with step-up/down capability are of the most popular ones in many industrial applications like renewable energy source (RES) applications [1]. Step-up/down converters like Zeta, Cuk, and Sepic are suitable for power applications since they can generate a high voltage at the output even in the existence of a small input voltage [2]. However, these structures also have some serious drawbacks. These days, numerous modern applications are needing a steep voltage step-down/up at the converter output which cannot be achieved by the mentioned converters. Additionally, these converters use an extreme value of duty-cycle to generate a high voltage conversion ratio, but this can cause many problems like decreased efficiency, increased cost for the control system, malfunctions at high frequencies, and also hindrances for transient response [3]. For overcoming these problems, there are three major solutions:

- Using a transformer along with these converters
- Cascading these converters with each other
- Developing modified/new converter structures

As mentioned, converters can be used along with a transformer. However, it is not a desirable solution due to the increased volume, cost, losses, and voltage stress on primary side elements. Besides, cascading the conventional converters is also an unfavourable solution since it drastically decreases the total efficiency. As the third solution, researchers have presented many modified versions of these conventional converters. In [3], embedding some simple step-up/-down blocks in conventional converters makes it possible to produce more desirable voltage gains with smaller conduction losses and decreased size of the inductors. In [4], a modified step-up/down structure is presented for renewable applications with advantages such as increased voltage gain and efficiency as well as reduced input current ripple compared to the Sepic converter. In [5], a single-switch buck-boost topology is introduced with a high step-up voltage conversion ratio and low voltage stress on switches. In [6, 7], two switched-capacitor based extendible converters are developed which are capable of providing higher voltage gain in comparison to the conventional topologies. However, in these converters, the more the voltage gain increases, the more the number of passive components increases, which is undesirable. In [8], a modified high gain structure is presented, providing high efficiency and low switching voltage stress. In [9], the Cuk converter is modified in a way that mitigates the parasitic effect and voltage drop of its components. Also, in [10], a modified Sepic-based converter topology is developed, capable of providing higher voltage gain and less voltage stress on its power components as compared with conventional topologies. Switched-capacitor (SC) topologies are also one of the most popular types

of DC–DC converters used in a wide range of applications [11, 12]. These converters have the same operating principles including two modes of charging and discharging for a group of interconnected capacitors. Up to now, many SC topologies have been developed and presented for various industrial applications [13]. Generally, the most popular conventional SC converters are charge pump type multilevel modular, Marx generator type voltage multiplier, and generalized multilevel type structures [14]. These topologies suffer from serious drawbacks such as remarkable switching losses and large size [15]. So far, several switching methods have been developed like the switching method [14] which can significantly mitigate the switching losses by using very small stray inductors. Also, some studies have tried to overcome the mentioned problems by developing new topologies. For instance, in [16], a new step-up SC structure is developed, providing many merits such as decreased cost, reduced control complexity, fewer components, less voltage stress on components, and smaller size over conventional structures. A new type of step-up/down DC–DC converters is introduced in [17–19] that can provide high voltage gains by low duty-cycles. These converters impose lower voltage stresses on capacitors as compared with other topologies. In [20], a bidirectional SC-based DC–DC structure with high voltage gains is introduced, benefiting from low component power rating, fewer switching devices, and low output capacitance requirement. In [21], a multilevel DC–DC power conversion system with multiple DC sources is presented, which enables changing the output voltage continuously and is suitable for high-temperature operations. In [22], a new high step-up non-isolated DC–DC converter is developed based on diode–capacitor cells, providing some merits such as lower voltage stress on switches and also having modularity. Moreover, in [23], a step-up SC-based converter with a high conversion ratio is introduced for RES applications like photovoltaic (PV) systems. This converter has advantages like high voltage gain, low voltage stress, and continuous input current. In [24], a high step-up DC–DC converter with high power density for RES applications is presented. This converter also benefits from lower voltage stress on switches, recycled energy of the leakage inductor, and eliminated inrush current. In [25], a high gain switched-inductor/capacitor-based DC–DC converter is presented for PV applications that can recycle the energy in its loss-less passive components, achieving a high voltage gain and improved efficiency. Having fewer ripples, lower power loss, and smooth continuous current are other advantages of the converter of [25]. In [26], a step-up DC–DC converter is presented to provide a higher gain with smaller turn ratios. This converter has a smaller size and also higher efficiency compared to other converters.

Since one of the applications of the proposed converters can be RES applications, in the following, some of the DC–DC converters developed for these applications are presented. In [27], a new topology of DC–DC converter is introduced for renewable system applications. In [28], a step-up pulse width modulation DC–DC converter is introduced which has some advantages such as providing a continuous input current and also generating high voltage gain using a low duty ratio. In [29], a new non-isolated DC–DC converter with high voltage gain is developed for RES applications. The converter has a higher efficiency and a lower switching voltage stress than the conventional converters models which were analysed. In [30], a new single switch converter with high step-up convention ratio and less voltage strain on the switch is introduced that consists of a voltage tripler and a sepic boost converter. In [31], a study is conducted on the modelling, dynamic analysis, and simulation of the bidirectional DC–DC boost-buck power converter used for RES applications. The switching sequence applies diverse duty-ratios in both input and output stages that leads to obtaining fully regulated system variables. In [32], a new high-gain step-up converter is developed for solar applications based on PSOL topology. This structure can provide higher voltage gains and impose lower voltage stress on its switches and diodes.

In this article, new SC DC–DC converter topologies with expansion ability are proposed. The proposed converters can provide higher voltage gain, reduced value of duty-cycle, and lower voltage stress on the components in comparison to previously mentioned topologies in the same operating class. These converters employ multiple SC cells in their structures, which makes it possible to transfer more energy from the converter input to its output. This leads to obtaining very high voltage gains with non-extreme duty-cycles and low voltage stress on the SCs. Consequently, compared to other topologies, the proposed topologies are more appropriate for modern applications with high power and voltage ratings. They can be utilized for regulating (increasing/decreasing) the output voltage of RES generation units such as solar and wind generation units. Besides, the proposed Cuk-based converters can also extract the maximum power from RESs like solar panels since their input current is continuous. To prove the analysis and claims, thorough comparisons and experiments are presented.

This article is organized as follows. In Section 2, the proposed converter topologies are introduced and analysed. Then, Section 3 compares the proposed and previously introduced converters. The experimental results are given in Section 4. In Section 5, the conclusion is presented.

2 | PROPOSED SC CONVERTER TOPOLOGIES

Here, the proposed converters are presented and discussed. These converters have two operational modes. In Table 1, the operational characteristics of the proposed converters, including charging/discharging modes of the components and switching states of the switches and diodes, are listed.

2.1 | Proposed SC Cuk-based topology

Figure 1(a) presents the proposed SC step-up Cuk-based DC–DC converter which is composed of one constant DC voltage (V_{in}), one filtering capacitors (C_O), n SCs (C_1,…,C_n), two coupled inductors (L_1 and L_2), one pure-resistive load (R), ($2n$-1) power switches (T_1,…, T_n, and S_1,…, S_{n-1}) and (n+2) diodes (D_1, D_2, … D_{n+2}), where n is the number of SC cells. Like

TABLE 1 Operational characteristics of the proposed converters

			Proposed non-hybrid converters	Proposed hybrid converters
Mode 1	Switching states	ON	(T_1,…, T_n) and D_{n+2}	(T_1,…, T_n), D_{n+2}, D'_1 and D'_3
		OFF	(S_1,…, S_{n-1}), (D_1,…, D_n) and D_{n+1}	(S_1,…, S_{n-1}), (D_1,…, D_n), D_{n+1} and D'_2
	Charging modes	Charge	L_1 and L_2	L_{11}, L_{12} and L_2
		Discharge	C_1,…, C_n	C_1,…, C_n
Mode 2	Switching states	ON	(S_1,…, S_{n-1}), (D_1,…, D_n) and D_{n+1}	(S_1,…, S_{n-1}), (D_1,…, D_n), D_{n+1} and D'_2
		OFF	(T_1,…, T_n) and D_{n+2}	(T_1,…, T_n), D_{n+2}, D'_1 and D'_3
	Charging modes	Charge	C_1,…, C_n	C_1,…, C_n
		Discharge	L_1 and L_2	L_{11}, L_{12} and L_2

conventional step-up/down converters such as Zeta, Cuk, and SEPIC, the proposed converter also has two operation modes. In Figure 1, these operation modes are presented. Figure 1(b) shows the first mode where the T switches and the diode D_{n+2} are ON while the rest of the switches and diodes are OFF. In this mode, the inductors are in charging mode, and all the SCs are discharged. Figure 1(c) shows the mode 2 where the T switches and the diode D_{n+2} are not closed. Here, the diodes D_1, D_2, … D_{n+1} and the S switches are conducting. Also, the inductors and the SCs are charged. As a matter of fact, in ideal-state, the average voltage of an inductor in one full cycle is zero. Thus, in the proposed converter, the voltage balances on the inductors give:

$$DV_{in} - (1-D)\left[V_{in} - V_{Ck}\right] = 0 \tag{1}$$

$$D(nV_{Ck} - V_{out}) - (1-D)\left[V_{Ck} - V_{out}\right] = 0 \tag{2}$$

In the above equations, D, V_{Ck}, V_{in} and V_{out} respectively represent the duty-cycle, voltage across the SC cell (k), and input and output voltages of the converter. Note that the voltages of SCs are similar ($V_{C1}=V_{C2}=\ldots=V_{Cn}$) since they have similar sizes and charging currents. By solving Equations (1) and (2), the voltage gain of the converter is attained as follows:

$$G_1 = \left|\frac{V_{out}}{V_{in}}\right| = \frac{(n-1)D+1}{1-D} \quad for\ 0 < D < 1 \tag{3}$$

Also, the voltage of SCs can be gained by Equation (4).

$$V_{Ck} = \frac{1}{1-D}V_{in} \quad for \quad k = 1, 2, .., n \tag{4}$$

In the following, the components of the converter are sized. Generally, the current of the inductor L_1 can be expressed below:

$$i_{L1}(t) = \frac{1}{L_1}\int_0^t V_{L1}dt + i_{L1}(0) \tag{5}$$

Considering $t = DT$ where T is the periodic time of switching pulses, Equation (5) can be transformed as follows:

$$\Delta i_{L1} = i_{L1-\max} - i_{L1-\min} = \frac{1}{L_1}\int_0^{DT} V_i dt = \frac{DTV_i}{L_1} \tag{6}$$

in which $i_{L1-\min}$ and $i_{L1-\max}$ denote the minimum and maximum values of the inductor current. Also, $\Delta i_{L1}$is the inductor current ripple. The periodic time is obtained by $T = (1/f_s)$where f_s is the switching frequency. Thus, the inductor size can be obtained as:

$$L_1 = \frac{D}{f_s \Delta i_{L1}}V_{in} \tag{7}$$

By doing the same process, the size of L_2 is obtained as:

$$L_2 = \frac{(n-1)D}{f_s \Delta i_{L2}}V_{in} \tag{8}$$

In Equation (8), the inductor current ripple is denoted byΔi_2. Since the SCs are the same, their charging and discharging currents are also similar, resulting in the identical voltages that can be expressed as:

$$V_{Ck}(t) = \frac{1}{C_k}\int_0^t i_{Cn}dt + V_{Ck}(0) \tag{9}$$

By regarding $t = TD$, Equation (9) can be rewritten as:

$$V_{Ck}(DT) = \frac{1}{C_k}\int_0^{DT} (-I_o)dt + V_{Ck-\max} \tag{10}$$

By solving Equation (10) and considering $I_o = (V_{out}/R)$and $\Delta V_{Ck} = V_{Ck-\max} - V_{Ck-\min}$, the size of SCs can be obtained

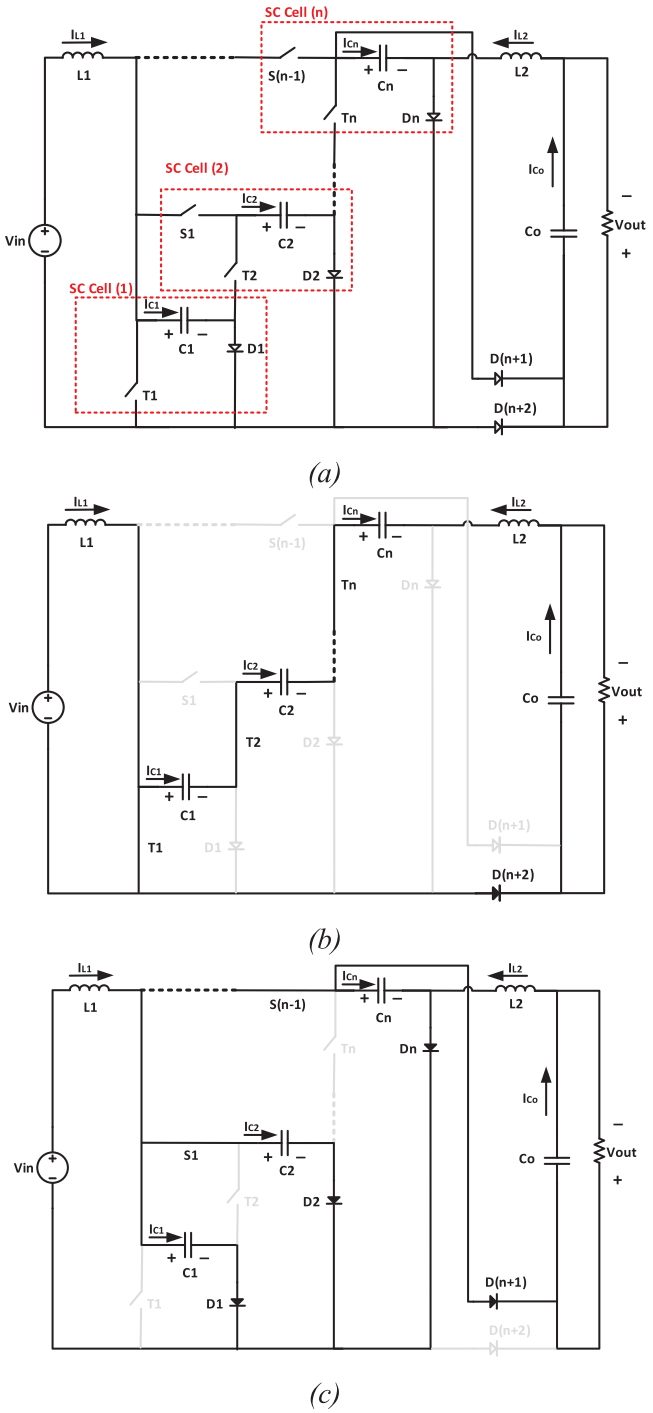

FIGURE 1 (a) Proposed SC Cuk-based topology; and its (b) operational mode 1 (c) operational mode 2

as:

$$C_k = \frac{\left[1 + (n-1)D\right] D}{(1-D)\,\Delta V_{Ck} f_s R} V_{in} \tag{11}$$

According to Figure 1 and Table 1, the capacitor C_O is charged for $T/2$ with average current of $\Delta i_{L2}/4$. Thus, by doing the same procedure done for sizing C_k, the size of the filtering

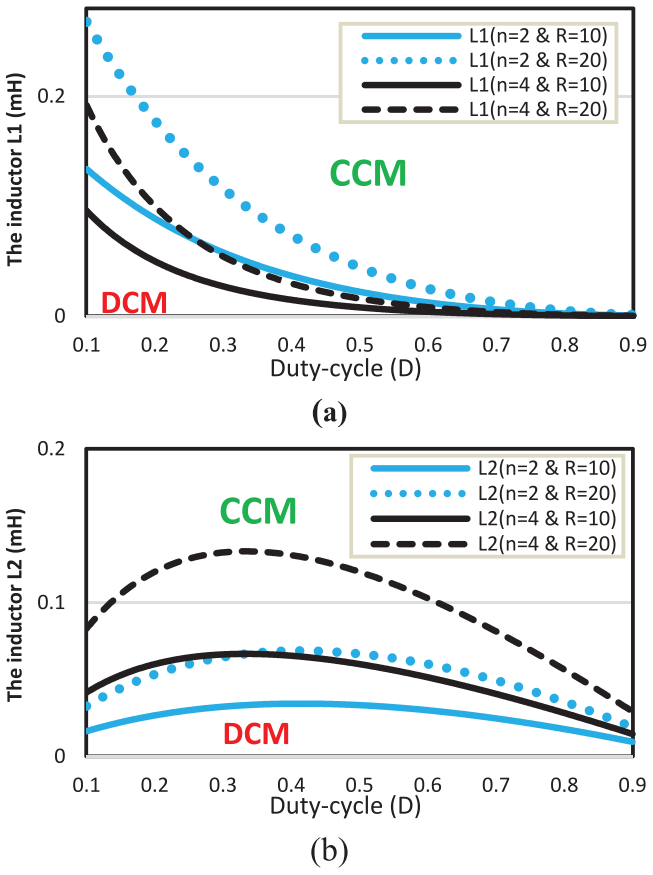

FIGURE 2 CCM and DCM boundaries of the proposed Cuk converter when f_s = 25kHz and D = [0.1–0.9] for the inductor (a) L_1 and (b) L_2

capacitor is obtained below:

$$C_o = \frac{(n-1)D}{8\Delta V_{Co} L_2 f_s^2} V_{in} \tag{12}$$

Generally, the proposed Cuk-based SC converter should operate in continuous condition mode (CCM). To this end, each of the inductors L_1 and L_2 must be sized with consideration of the following conditions:

$$L_1 \geq \frac{(1-D)^2 V_{in} R}{2 f_s (1 + (n-1)D)^2 V_o} \tag{13}$$

$$L_2 \geq \frac{D(n-1) V_{in} R}{2 f_s V_o} \tag{14}$$

where, R denotes the load resistance. By using the above equations, CCM and DCM (discontinuous condition mode) boundaries of the proposed SC converter for both of the inductors are calculated and presented in Figure 2.

In the following, the power losses of components are calculated. Generally, the total power loss of a switching device includes two parts: conduction losses and switching losses.

Thus, the total power losses of the switch T_1 can be written as:

$$P_{T1(total)} = P_{T1(c)} + P_{T1(s)} \tag{15}$$

in which $P_{T1(c)}$ and $P_{T1(s)}$ respectively represent the conduction and switching losses. Also, its current is given as:

$$i_{T1}(t) = \begin{cases} \left[\dfrac{(n-1)D+1}{1-D}+1\right] I_o & t \in (0, DT] \\ 0 & t \in [DT, T) \end{cases} \tag{16}$$

By (16), the switch conduction power loss is obtained as:

$$P_{T1(c)} = r_T \left(\sqrt{\frac{1}{T}\int_0^T \left[i_{T1}(t)\right]^2 dt} \right)^2 = r_T \sqrt{D} \left[\frac{(n-2)D+2}{1-D}\right] I_o \tag{17}$$

where, r_T is the internal equivalent resistance of the switches. Since the voltage stress on the switch T_1 in OFF state is equal to V_{Ck}, its switching power loss is expressed as:

$$P_{T1(s)} = \frac{V_{Ck} I_o f_s}{6} \left(\frac{(n-1)D+1}{1-D}+1\right)\left(t_{on}+t_{off}\right) \tag{18}$$

where, t_{on} and t_{off} respectively denote the on- and off-transients of the switch.

According to Figure 1 and Table 1, the switches T_2, T_3, … and T_n are in series and only conducting in mode 2 where their currents are equal to the average output current (I_O). Thus, similar to Equations (15)–(18), by considering that their voltage stress is V_{Ck} in OFF state, their total power loss can be expressed as:

$$P_{In(total)} = r_T \left(D I_o^2\right) + \frac{V_{Ck} I_o f_s}{6}\left(t_{on}+t_{off}\right) \tag{19}$$

Generally, the S switches in conducting mode have similar currents ($i_S(t)=i_{S1}=\ldots=i_{S(n-1)}$) that is equal to $\frac{I_{in}}{n} = \left(\frac{(n-1)D+1}{n(1-D)}\right) I_o$. But, their OFF-state voltage stresses are unequal as follows:

$$V_{Sj} = jV_{Cn} \quad for \quad j = 1, 2, \ldots, (n-1) \tag{20}$$

Accordingly, their total power loss is obtained as follows:

$$P_{Sj(total)} = \frac{r_T D^2 I_o^2}{1-D} + \frac{jV_{Ck} I_o f_s}{6n(1-D)}\left((n-1)D+1\right)\left(t_{on}+t_{off}\right) \tag{21}$$

The current and voltage of the diodes D_1, D_2, … and D_{n-1} are similar to the S switch located in the same SC cell. Thus, the conduction power loss of these diodes is gained by Equation (22).

$$P_{D(c)} = r_D \left[\frac{1}{T}\int_0^T (i_S)^2 d\right] + V_D \left[\frac{1}{T}\int_0^T i_S dt\right] \tag{22}$$

where, V_D and r_D respectively denote the equivalent voltage drop and equivalent resistance of the diodes. Besides, the switching power loss of these diodes can be obtained by Equation (21).

$$P_{Dj(s)} = \frac{jV_{Ck} I_o f_s}{6n(1-D)}\left((n-1)D+1\right)\left(t_{on}+t_{off}\right) \tag{23}$$

where, t_{on} and t_{off} are the diodes on- and off-transients. So, the total power loss of each diode can be acquired as:

$$P_{Dj} = P_{D(ct)} + P_{Dj(s)} \tag{24}$$

Similarly, the total power loss of the diodes D_n, D_{n+1}, and D_{n+2} are respectively obtained by Equations (25)–(27).

$$P_{Dn} = \left(\frac{1+\mathrm{n}+\mathrm{D}}{n}\right)\left[\frac{r_D I_o^2}{1-D}\left(\frac{1+\mathrm{n}+\mathrm{D}}{n}\right) + V_D I_o + \frac{nV_{Ck} I_o f_s}{6(1-D)}\left(t_{on}+t_{off}\right)\right] \tag{25}$$

$$P_{D(n+1)} = (1-D)\left[r_D I_o^2 + V_D I_o\right] + \frac{(n-1)V_{Ck} I_o f_s}{6}\left(t_{on}+t_{off}\right) \tag{26}$$

$$P_{D(n+2)} = r_D I_o^2 D + V_D I_o D + \frac{V_{Ck} I_o f_s}{6}\left(t_{on}+t_{off}\right) \tag{27}$$

Also, the inductors power losses can be obtained as:

$$P_{L1} = R_{L1}\left(\frac{(n-1)D+1}{1-D} I_o\right)^2 \tag{28}$$

$$P_{L2} = R_{L2} I_o^2 \tag{29}$$

where, (P_{L1}, R_{L1}) and (P_{L2}, R_{L2}) are respectively the power loss and equivalent internal resistance of the inductors L_1 and L_2. The SCs current can be expressed below:

$$i_{Ck}(t) = \begin{cases} -I_o & t \in (0, DT] \\ \left[\dfrac{(n-1)D+1}{n(1-D)}\right] I_o & t \in [DT, T) \end{cases} \tag{30}$$

By using Equation (30), the RMS value of the SCs' current is obtained, and then the power loss is obtained below:

$$P_{Ck} = \frac{R_{Ck}}{T}\int_0^T \left[i_{Ck}(t)\right]^2 dt \tag{31}$$

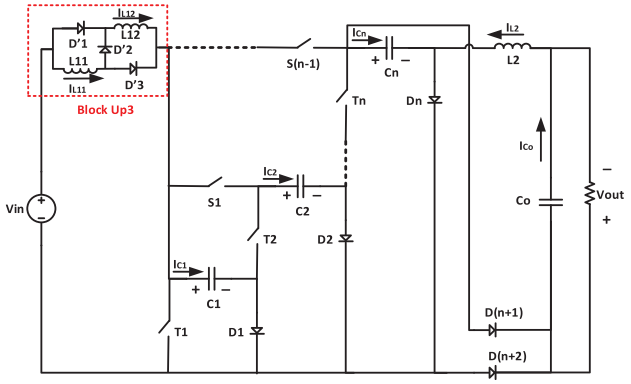

FIGURE 3 Proposed hybrid SC Cuk-based converter

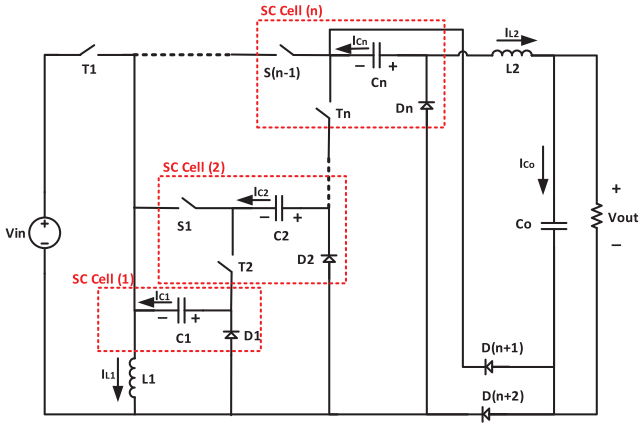

FIGURE 4 Proposed SC Zeta-based converter

in which $R_{Ck}$is the equivalent resistance of SCs. As already mentioned, the average current of C_O is equal to $\Delta i_{L2}/4$. Thus, by using (8), its power loss is obtained as follows:

$$P_{Co} = R_{Co}\left(\frac{\Delta i_{L2}}{4}\right)^2 = \frac{R_{Co(}}{16}\left(\frac{(n-1)D}{f_s L_2}V_{in}\right)^2 \tag{32}$$

where, R_{Co} denotes the equivalent internal resistance of this capacitor. As a result, the total power loss can be acquired as:

$$P_{Tot} = P_{Co} + nP_{Ck} + \sum_{1}^{2} P_{T(i)} + \sum_{1}^{n+2} P_{D(i)} + \sum_{1}^{n-1} P_{S(i)} + \sum_{1}^{n} P_{T(i)} \tag{33}$$

So, the efficiency of the proposed converter can be calculated as:

$$\%\eta = \frac{P_o}{P_o + P_{Tot}} \times 100 \tag{34}$$

where, P_o is the converter output power.

2.2 | Proposed hybrid SC Cuk-based topology

Figure 3 shows the proposed hybrid step-up Cuk-based SC structure. As seen, this converter is developed by adding the block Up3 of [3] to the proposed Cuk-based structure in Figure 1. The voltage gain of this hybrid topology is obtained as follows:

$$G_2 = \left|\frac{V_{out}}{V_{in}}\right| = \frac{(1+D)\left[1+(n-1)D\right]}{1-D} \tag{35}$$

Moreover, the SCs voltage is expressed by Equation (35).

$$V_{Ck} = \frac{1+D}{1-D}V_{in} \tag{36}$$

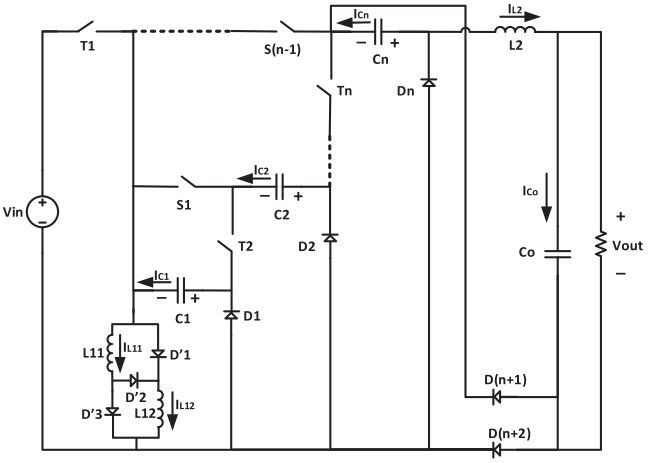

FIGURE 5 Proposed hybrid SC Zeta-based converter

2.3 | Proposed SC Zeta-based topology

In Figure 4, the proposed step-up/down SC Zeta-based structure is presented. Its voltage gain can be given as:

$$G_3 = \frac{V_{out}}{V_{in}} = \frac{2D + (n-2)D^2}{1-D} \tag{37}$$

Furthermore, the voltage across SCs is calculated by Equation (38).

$$V_{Ck} = \frac{D}{1-D}V_{in} \tag{38}$$

2.4 | Proposed hybrid SC Zeta-based topology

In Figure 5, the proposed hybrid step-up/down Zeta-based SC topology is presented. As shown, this converter is acquired by using the block Up3 of [3] in the proposed Zeta-based structure presented in Figure 4. It in turn gives a higher voltage

conversion ratio which can be calculated by Equation (39).

$$G_4 = \frac{V_{out}}{V_{in}} = \frac{3D + (2n-3)D^2}{1-D} \tag{39}$$

Moreover, the voltage across SCs of this converter is expressed as:

$$V_{Ck} = \frac{2D}{1-D} V_{in} \tag{40}$$

3 | COMPARISONS

Here, the proposed converters are thoroughly compared with previously introduced ones. In Table 2, the major specifications of the converters are listed. As seen, there are two types of topologies: extendible and non-extendible. In some cases, the proposed converters with $n = 1$ are compared with conventional converters without expansion ability.

3.1 | Number of power components

Here, all of the topologies are compared in terms of the number of passive components and the total number of components.

Initially, the topologies without expansion capability are checked. As seen in Table 2, among non-extendible topologies, along with conventional Zeta, Sepic, and Cuk converters and the converter of [28], the proposed Cuk- and Zeta-based SC converters ($n = 1$) employ the fewest number of passive components. Besides, the proposed hybrid SC Zeta- and Cuk-based converters ($n = 1$) share the second place in the fewest number of passive components along with hybrid converters of [3] and the converter of [8, 9, 29]. In the case of the total number of the components, after the conventional converters and the converters of [9, 28], the proposed SC Zeta- and Cuk-based converter ($n = 1$) employ the fewest number of total components in step up/down and step up converters respectively. Generally, the proposed topologies for $n = 1$ use a less or similar number of total components in comparison to others. It should be noted that the converters of and [30, 32] employ the highest total numbers of components, 17 and 15, respectively.

It should be noted here that the non-extendible converters need to be cascaded to provide a high voltage gain in contrast to the proposed converters. This means that these converters need more components compared with the proposed ones. For instance, to obtain the voltage gain of 40 with a non-extreme duty-cycle (about 0.9), the proposed SC Cuk-based converter with $n = 4$ needs seven passive components and total components of 20. However, to generate the same voltage gain, four 3rd order boost converter with $D = 0.89$ should be cascaded, increasing the needed passive components to 12 and total number of components to 24. Similarly, it is needed to cascade four conventional Cuk converter to generate $G = 40$ with $D = 0.91$, leading to employ 16 passive components where the total number of components is 24. Thus, for generating very high voltage gains with non-extreme duty-cycles, the proposed converters can be considered one of the best options.

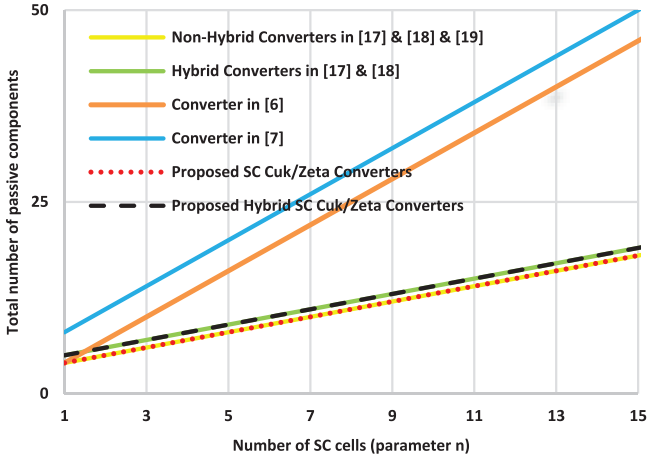

FIGURE 6 Number of passive components of extendible converters

In the following, a thorough comparison between the proposed converters and other extendible structures is presented. In Figure 6, the topologies with expansion ability including the proposed ones are compared in terms of the number of passive components. As seen, the proposed non-hybrid converters and the non-hybrid step-up/down converters presented in [17–19] have the minimum number of passive components. The proposed hybrid converters and the hybrid topologies of [17–19] employ a similar number of passive components and share the second place. Moreover, compared to the converters of [6, 7], the proposed topologies have excessively fewer passive components, making them much more cost-, weight- and size-effective.

Additionally, it is seen in Table 2 that the proposed converters with expansion capability have an equal or similar number of total components in comparison with the other extendible structures.

3.2 | Voltage conversion ratio (voltage gain)

In Figure 7(a), voltage conversion ratios of various structures without expansion ability, and the proposed ones with $n = 1$ are compared. As seen, the proposed SC hybrid Cuk-based structure ($n = 1$), hybrid Cuk topology with Up2 block, and converters of and [8, 29] can produce the highest voltage gain for all duty-cycles. Besides, for $D < 0.4$, the proposed Cuk-based converter ($n = 1$) along with the converters of [4, 9] have the second place in providing the highest voltage gain; for $D > 0.4$, the proposed hybrid Zeta-based converter ($n = 1$) is placed in the second place. It should be noted that the proposed Cuk-/Zeta-based converters generate higher voltage gains than the conventional Sepic, Cuk, and Zeta converters.

The voltage gains of the extendible topologies are compared in Figure 7(b) by considering $n = 5$. As seen, the proposed hybrid SC Cuk-based converter shows a close or similar performance at the start compared with the converter of [6]. But, for $D > 0.45$, the proposed converter surpasses the converter of

TABLE 2 Specifications of different DC-DC converter topologies

Structure name	Voltage conversion ratio	Maximum voltage stress		Number of components						Type
		Capacitors	T switches	Cap.	Induct.	Passive	Sw.	Diode	Total	
Zeta & Cuk & Sepic	$D/(1-D)$	–	$V_i(1/(1-D))$	2	2	4	1	1	6	NON-EXTENDIBLE
Hybrid Zeta with Up2 [3]	$2D/(1-D)$	$V_i(D/(1-D))$	$V_i(1/(1-D))$	3	2	5	1	2	8	
Hybrid Zeta with Up3 [3]	$D(1+D)/(1-D)$	$V_i(2D/(1-D))$	$V_i((1+D)/(1-D))$	2	3	5	1	4	10	
Hybrid Cuk with Up3 [3]	$D(1+D)/(1-D)$	$V_i((1+D)/(1-D))$	$V_i((1+D)/(1-D))$	2	3	5	1	4	10	
2x multiplier [10]	$(2+D)/(1-D)$	$V_i((1+D)/(1-D))$	–	5	*2*	7	1	4	12	
Converter in [8]	$(1+D)/(1-D)$	$V_i(1/(1-D))$	–	3	*2*	5	1	2	8	
Modified converter [9]	$1/(1-D)$	$V_i(\|2D-1\|/(1-D))$	–	2	*3*	5	1	1	7	
Hybrid Cuk with Up2 [3]	$(1+D)/(1-D)$	$V_i(1/(1-D))$	$V_i(1/(1-D))$	3	2	5	1	2	8	
Converter [4]	$1/(1-D)$	V_i	–	3	3	6	1	1	8	
Converter of [28]	$(1-D)/(1-2D)$	–	$V_i(1/(1-D))$	2	2	4	1	2	7	
Converter of [29]	$(1+D)/(1-D)$	$V_i(1/(1-D))$	–	2	3	5	1	2	8	
Converter of [30]	$3(1+D)/(1-D)$	$3V_i(1/(1-D))$	–	6	2	8	1	6	15	
Converter of [32]	$3(1+D)/(1-D)$	–	$V_i((1+2D)/(3+3D))$	3	3	6	1	10	17	
Proposed SC Zeta converter ($n=1$)	$D(2-D)/(1-D)$	$V_i(D/(1-D))$	$V_i(1/(1-D))$	2	2	4	1	3	8	
Proposed SC Hybrid Zeta converter ($n=1$)	$D(3-D)/(1-D)$	$V_i(2D/(1-D))$	$V_i((1+D)/(1-D))$	2	3	5	1	6	12	
Proposed SC Cuk converter ($n=1$)	$1/(1-D)$	$V_i(1/(1-D))$	$V_i(1/(1-D))$	2	2	4	1	3	8	
Proposed SC Hybrid Cuk converter ($n=1$)	$(1+D)/(1-D)$	$V_i((1+D)/(1-D))$	$V_i((1+D)/(1-D))$	2	3	5	1	6	12	
Zeta Converter [17]	$[D+(n-1)D^2]/(1-D)$	$V_i(D/(1-D))$	$V_i(1/(1-D))$	n+1	2	n+3	*2n-1*	*n*	4n+2	
Zeta-derived Hybrid converter [17]	$[D+(2n-1)D^2]/(1-D)$	$V_i(2D/(1-D))$	$V_i((1+D)/(1-D))$	n+1	3	n+4	*2n-1*	*n+3*	4n+6	EXTENDIBLE
Cuk converter [17]	$nD/(1-D)$	$V_i(1/(1-D))$	$V_i(1/(1-D))$	n+1	2	n+3	*2n-1*	*n*	4n+2	
Cuk-derived Hybrid converter [17]	$nD(1+D)/(1-D)$	$V_i((1+D)/(1-D))$	$V_i((1+D)/(1-D))$	n+1	3	n+4	*2n-1*	*n+3*	4n+6	
Zeta converter [18]	$[D+(n-1)D^2]/(1-D)$	$V_i(D/(1-D))$	$V_i(1/(1-D))$	n+1	2	n+3	*n+1*	*2n-1*	4n+3	
Zeta-based Hybrid converter [18]	$[D+(2n-1)D^2]/(1-D)$	$V_i(2D/(1-D))$	$V_i((1+D)/(1-D))$	n+1	3	n+4	*n+1*	*2n+2*	4n+7	
Cuk converter [18]	$nD/(1-D)$	$V_i(1/(1-D))$	$V_i(1/(1-D))$	n+1	2	n+3	*n+1*	*2n-1*	4n+3	
Cuk-based Hybrid converter [18]	$nD(1+D)/(1-D)$	$V_i((1+D)/(1-D))$	$V_i((1+D)/(1-D))$	n+1	3	n+4	*n+1*	*2n+2*	4n+7	

(Continues)

TABLE 2 (Continued)

Structure name	Voltage conversion ratio	Maximum voltage stress		Number of components						Type
		Capacitors	T switches	Cap.	Induct.	Passive	Sw.	Diode	Total	
converter in [19]	$(1+(n-1)D)D/1-D$	$V_i(D/(1-D))$	$V_i(1/(1-D))$	n+1	2	n+3	*3n-2*	1	4n+2	
converter in [16]	n	V_i	NA	n	n	*2n*	n	*2n-1*	5n-1	
converter in [20]	n	V_i	NA	n	2n	*3n*	*2*	0	5n	
GMSCC [21]	n	V_i	NA	$\frac{(n+1)n}{2}-1$	$n(n+1)-2$	$\frac{3(n+1)n}{2}-3$	$\frac{(n+1)n}{2}-1$	0	$\frac{5(n+1)n}{2}-5$	
converter in [6]	$[2+(n-1)D]/(1-D)$	–	–	2n+1	n	3n+1	1	n+2	4n+4	
converter in [7]	$[1+(n-1)D]/(1-D)$	–	–	2n+3	*n+1*	3n+4	1	n+3	4n+8	
Proposed Zeta-based SC converter	$[2D+(n-2)D^2]/(1-D)$	$V_i(D/(1-D))$	$V_i(1/(1-D))$	n+1	2	n+3	2n-1	n+2	4n+4	
Proposed Zeta-based Hybrid SC converter	$[3D+(2n-3)D^2]/(1-D)$	$V_i(2D/(1-D))$	$V_i((1+D)/(1-D))$	n+1	3	n+4	2n-1	n+5	4n+8	
Proposed SC Cuk-based converter	$[1+(n-1)D]/(1-D)$	$V_i(1/(1-D))$	$V_i(1/(1-D))$	n+1	2	n+3	2n-1	n+2	4n+4	
Proposed SC Cuk Hybrid converter	$\frac{(1+D)[1+(n-1)D]}{(1-D)}$	$V_i((1+D)/(1-D))$	$V_i((1+D)/(1-D))$	n+1	3	n+4	2n-1	n+5	4n+8	

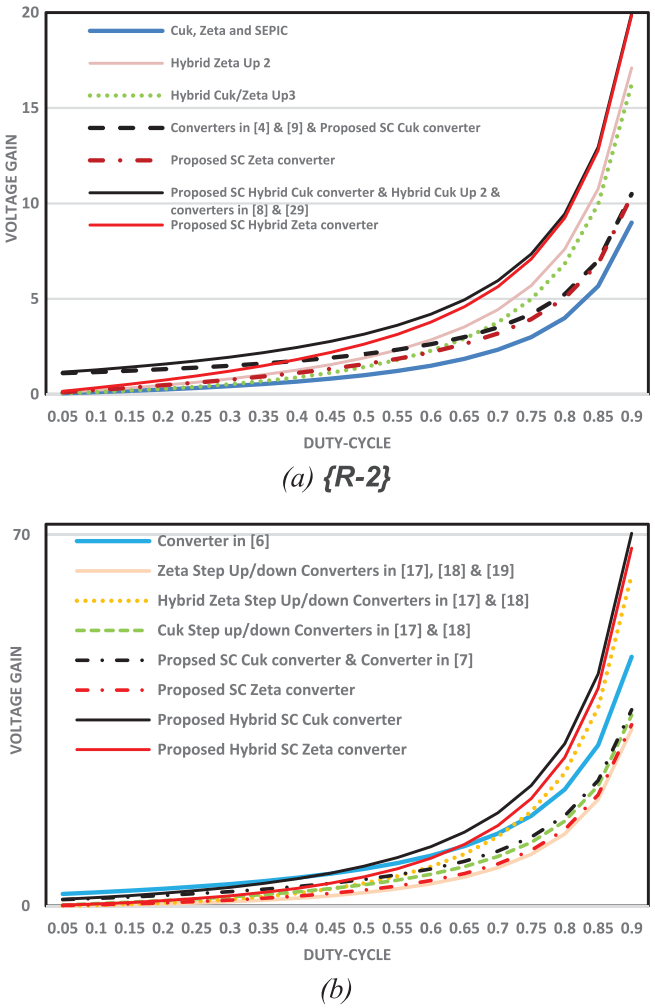

FIGURE 7 Comparing voltage gains between proposed converters and others (a) without expansion ability ($n = 1$) (b) with expansion ability ($n = 5$)

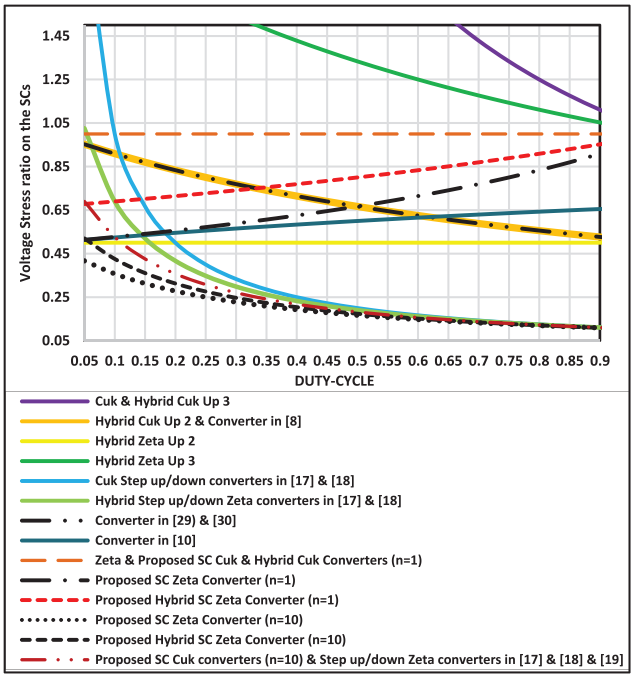

FIGURE 8 Comparing voltage stress on SCs of converters

[6] and provides the highest voltage gain. Besides, for D > 0.6, the proposed hybrid SC Zeta converter possesses the second-highest voltage gain. Also, as clearly seen, the non-hybrid proposed SC Cuk-based converter shows a more desirable performance as compared to other extendible topologies presented in [17–19].

By considering Figure 7(a,b), it is evidently seen that the voltage conversion ratios of the previously introduced converters without expansion ability are much lower than those of proposed extendible ones. Besides, this difference in their voltage gains will get larger by increasing n.

Consequently, the proposed topologies are suitable for modern industrial applications requiring high voltage gains.

3.3 | Voltage stress on capacitors

Here, the maximum voltage stresses on the SCs of diverse structures are compared. To this end, the parameter VR_C (ratio of the maximum voltage stress on SCs to the converter output voltage) is described as follows [19]:

$$VR_C = \frac{V_{Ck[\max]}}{V_{out}} \tag{41}$$

where, $V_{Ck[\max]}$ and V_{out} respectively present the maximum voltage of the SCs and the converter output voltage. Since the compared converters generate different voltage gains at the same duty-cycles, the intended comparison only can be done just by calculating VR_C for different duty-cycles [19]. Figure 8 shows the obtained VR_C values of different structures for $D \in [0.05,\ 0.09]$, and $n = 1$ and $n = 10$. As seen, the proposed non-hybrid and hybrid SC Zeta-based topologies respectively have the lowest voltage stress on their SCs. Then, the proposed SC Cuk-based converters share the second place with the step-up/down Zeta-derived converters presented in [17–19]. Moreover, the voltage stress on the SCs of the proposed converters with $n = 1$ is lower than that of the conventional non-extendible converters. Also, note that by boosting the parameter n from 1 to 10, the voltage stress of SCs remarkably decreases for the proposed SC converters. In other words, for providing high voltage gains, the proposed structures are the most desirable ones.

3.4 | Voltage stress on power switches

In the following, a thorough comparison is presented for the voltage stress on the power switches of diverse structures. To this end, according to [19], the ratio of the maximum voltage stress of the switches to the converter output voltage is

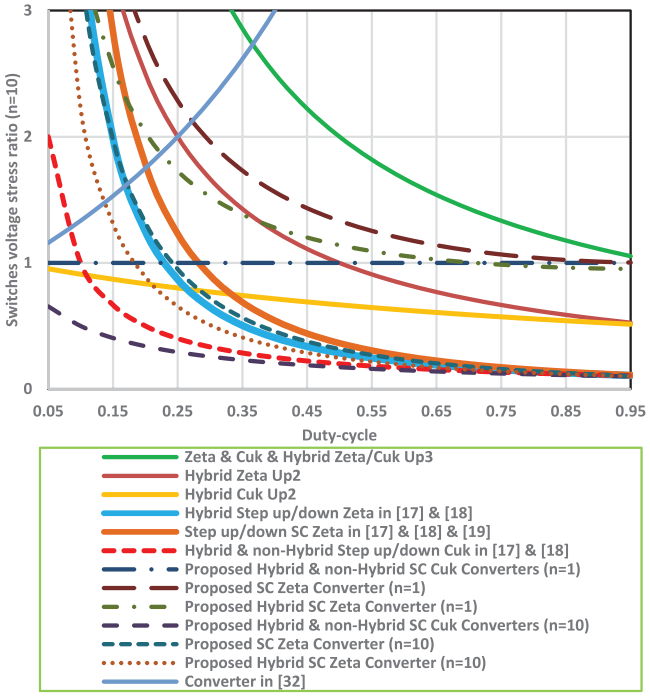

FIGURE 9 Comparing voltage stress on switches of proposed converters and other structures

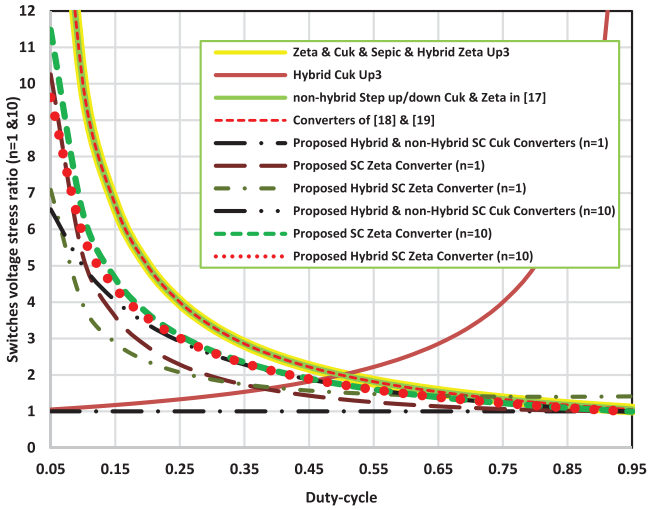

FIGURE 10 Comparing voltage stress on diodes of converters

described below:

$$VR_{sw} = \frac{V_{sw[max]}}{V_{out}} \tag{42}$$

where, $V_{sw[\max]}$ denotes the maximum voltage stress of the power switches. Figure 9 shows the curve of VR_{sw} for different converters by regarding the number of SC cell (n) and duty-cycle (D) as the variables. It should be noted that the maximum voltage stress of the switch T_1 is presented in this section since the average current of this switch is higher current compared to that of other switches. As seen, among all the converters, the proposed hybrid and non-hybrid SC Cuk-based converters ($n = 10$) can impose the lowest voltage stress on their switches. The proposed hybrid SC Zeta-based converter is placed in the third place after the Cuk converters of [17, 18]. As seen, the proposed converters are capable of providing lower voltage stress than other non-extendible topologies. In other words, the more the parameter n increases, the more the switches voltage stress decreases. Note that, even by considering $n = 1$, the proposed converters provide lower voltage stress on switches as compared with conventional structures like Cuk, Zeta, and hybrid Zeta/Cuk Up3.

3.5 | Voltage stress on diodes

Here, the voltage stresses of the diodes in different structures including the proposed ones are compared. Similar to Sections 3.3 and 3.4, the ratio of the maximum voltage stress of the diodes to the output voltage is defined below:

$$VR_d = \frac{V_{d[max]}}{V_{out}} \tag{43}$$

where, $V_{d[\max]}$ denotes the maximum voltage stress of the diodes. In Figure 10, the parameter VR_d for different converters are calculated and shown. As seen, among all the compared converters, the proposed hybrid and non-hybrid SC Cuk-based converters ($n = 1$) provide the lowest voltage stress on their diodes. Among the expandable converters, the proposed hybrid and non-hybrid SC Cuk-based converters have the least voltage stresses on their diodes. Moreover, the proposed hybrid and non-hybrid SC Zeta-based converters are placed in the second and third places among the expandable ones. As seen, the proposed converters provide lower voltage stress on their diodes compared to other extendible and non-extendible topologies. As a rule, the larger parameter n would lead to the more voltage stress reduction on diodes. Note that, even by considering $n = 1$, the proposed converters can provide lower voltage stress on switches.

3.6 | Efficiency

Figure 11 presents the efficiencies of different topologies for various output powers. Here, the number of SCs (n) is equal to 2. The proposed structures can provide close or better efficiencies as compared with the others. As seen, among the proposed converters, the proposed SC Cuk-/Zeta-based converters provide the highest efficiencies after the conventional Zeta, conventional Cuk and the step up/down Zeta- and Cuk-based converters of [17–19].

As mentioned previously, the conventional topologies need an extreme duty-cycle to produce very high voltage conversion ratios, which in turn imposes very high voltage stress on the components and thus increases the costs. To provide such

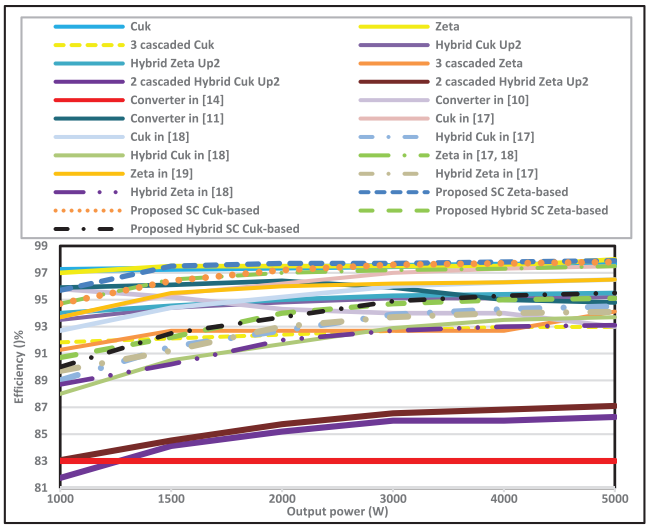

FIGURE 11 Comparing efficiencies of different converters

TABLE 3 Maximum current stress on the components of the SC cells in different converters including the proposed SC converters

	Maximum current stress on the components			
Structure	**SCs**	**Diodes**	***T* switches**	***S* switches**
SC step-up/down Zeta converter of [17]	8.6A	6.7A	1.94A	6.7A
SC step-up/down Cuk converter of [17]	9.2A	6.2A	1.97A	6.2A
SC step-up/down Zeta converter of [18]	8.62A	7A	1.98A	5.7A
SC step-up/down Cuk converter of [18]	9.3A	6.7A	2.08A	4.91A
SC converter of [19]	8.7A	–	2.1A	6.5A
Proposed Cuk-based SC converters	6.86A	7.03A	2.1A	7.03A
Proposed Zeta-based converters	8.6A	7.2A	2.05A	7.2A

a voltage gain with desirable duty-cycles, these converters can be used in cascaded structures. However, this can apply heavy penalties on the total efficiency of the cascaded converter since the total efficiency is acquired by multiplying the efficiencies of all the m converters used in cascaded structures ($\eta_{total} = \eta_1 \times \ldots . \times \eta_m$). As seen in Figure 11, cascading the converters with each other significantly reduces the total efficiency, which is not desirable.

3.7 | Current stress on SCs, diodes and switches

In this section, the maximum current stress on the components of different SC-based step-up/down and step-up structures including the proposed converters are compared. To have a precise and fair comparison, this comparison is performed for all converters under the same operating conditions, that is, similar input voltage (100 V) and output voltage (356 V) and load (251Ω). Table 3 lists the maximum current stress on different components of SC cells of the compared converters. It should be noted that in this table, T and S switches respectively are responsible for discharging and charging the SCs of these SC-based converters. Based on the results, it is evident that the lowest maximum current stress on the SCs belongs to the proposed Cuk-based SC converter. Besides, the proposed Zeta-based SC converter takes the second place along with the Zeta-based step-up/down converters of [17–19]. In addition, in terms of the maximum current stress on the T switches, all of the converters have a very close performance. Besides, in the rest of the results, the performances of the proposed converters are acceptable as compared to other circuits.

In summary, compared to other SC-based converters, the proposed converters are able to show desirable performances and impose an acceptable current stress on their components.

To gain a better understanding of the comparisons, all the results are summarized and listed in Table 4. In all the comparison categories, the proposed topologies are the best structures or among the best ones. In summary, the proposed topologies are the superior ones in comparison to the other converters. The proposed SC converters have a fewer number of passive components and can provide higher voltage conversion ratios in low duty-cycles. This means that there is no need for a very fast and costly control system. Besides, the proposed structures impose lower voltage stress on their components and also offer close or higher efficiencies as compared with others. Besides, the proposed converters impose desirable current stress on their components used in their SC-cells. Therefore, the proposed converter topologies have a clear and strong superiority over other topologies, especially in modern high power rated applications requiring high voltage gains.

4 | EXPERIMENTAL RESULTS

Here, thorough experimental results of the proposed SC Zeta-based and Cuk-based converters are presented to validate their performance. Several experiments have been performed for each converter. First, the performances of the proposed converters are evaluated for two different duty-cycles. Then, their dynamic performance is validated by applying a step-change in their input voltage while they are equipped with open-loop and closed-loop control systems.

In all the experiments, the number of SCs (n) and switching frequency (f_s) are respectively considered to be 2 and 25 kHz. In Figure 12, the experimental set-ups of the converters are shown. In these circuits, MOSFETs (47N60C), TLP250 drivers, and ultra-fast diodes (UG12) are employed. In the following sub-sections, before the experimental results, the components of the converters are calculated and sized. Note that the proposed hybrid converters are obtained by adding the block Up3 to the non-hybrid ones. Thus, by validating the performances of the proposed non-hybrid converters with the experiments, the

TABLE 4 The qualitative results of the comparison

Comparison parameters	Structure type	Qualitative	Best converters
Total number of passive components	Non-extendible	Proposed SC Cuk converter (n=1)> Proposed SC Zeta converter (n=1)= Cuk=Zeta=Sepic < Proposed SC Hybrid Cuk/Zeta converters (n=1)= Hybrid Zeta/Cuk with Up2/Up3 < [4] < [10]	Proposed SC Cuk-based converter
	Extendible	Proposed SC Zeta-/Cuk-based converters= [19]= non-hybrid step-up/down converters of [18, 17] <Proposed SC hybrid Cuk/Zeta converters=non-hybrid step-up/down converters of [17, 18] < [6] < [7]	Proposed SC Zeta- and Cuk-based converters, [19], non-hybrid step-up/down converters of [18, 17]
Voltage conversion ratio (Voltage gain)	Non-extendible	For D<0.45: Proposed SC Hybrid Cuk converter (n=1)= Cuk Up2= [8]=[29] > Proposed SC Cuk-based converter (n=1)= [4]= [9] > Proposed Hybrid SC Zeta converter(n=1) > Proposed SC Zeta converter (n=1)= Zeta Up2 > Cuk/Zeta Up3 > Cuk= Zeta= Sepic	Proposed hybrid SC Cuk-based converter, Hybrid Cuk Up2, [8], [29]
		For D>0.45: Proposed Hybrid SC Cuk converter (n=1)= Cuk Up2= [8]=[29] > Proposed Hybrid SC Zeta converter (n=1) > Cuk Up2 > Cuk/Zeta Up3 > Proposed SC Cuk-/Zeta converters > Cuk=Zeta=Sepic	Proposed hybrid SC Cuk-based converter, Hybrid Cuk Up2, [8], [29]
	Extendible	For D<0.45: Proposed SC hybrid Cuk converter (n=5), [6] > Proposed SC Cuk converter (n=5)= [7] > Proposed SC hybrid Zeta converter (n=5) > Proposed SC Zeta converter (n=5)= Step-up/down Cuk of [17] & [18] > Step-up/down Zeta converters of [17, 18, 19]	Proposed hybrid SC Cuk-based converter, [6]
		For D>0.45: Proposed SC hybrid Cuk converter (n=10) > Proposed SC hybrid Zeta converter (n=10) > Hybrid Zeta converters of [17,18] > [6] > Proposed SC Cuk converter (n=10)=[7] > non-hybrid up/down Cuk of [17,18]> Proposed SC Zeta converter (n=10) > [19]= Non-hybrid step-up/down Zeta of [17, 18]	Proposed hybrid SC Cuk-based converter
Maximum voltage stress on diodes	Non-extendible	For D<0.4: Proposed SC Hybrid & non-hybrid Cuk converter (n=1)< Cuk Up3 < Proposed Hybrid SC Zeta converter(n=1) < Proposed SC Zeta-based converter (n=1) < Cuk= Zeta= Sepic = Zeta Up3	Proposed SC Hybrid & non-hybrid Cuk converter
		For 0.4<D<0.5: Proposed SC Hybrid & non-hybrid Cuk converter (n=1)< Proposed Hybrid SC Zeta converter(n=1) < Proposed SC Zeta-based converter (n=1) < Cuk Up3 < Cuk= Zeta= Sepic = Zeta Up3	Proposed SC Hybrid & non-hybrid Cuk converter
		For D>0.5: Proposed SC Hybrid & non-hybrid Cuk converter (n=1)< Proposed Hybrid SC Zeta converter(n=1) < Proposed SC Zeta-based converter (n=1) < Cuk= Zeta= Sepic = Zeta Up3 < Cuk Up3	Proposed SC Hybrid & non-hybrid Cuk converter
	Extendible	Proposed SC Hybrid & non-hybrid Cuk converter (n=10)< Proposed Hybrid SC Zeta converter(n=10) < Proposed SC Zeta-based converter (n=10) < converters of [18] & [19] < non-hybrid step-up/down Zeta- & Cuk-based converters of [17]	Proposed SC Hybrid & non-hybrid Cuk converter
Maximum voltage stress on switches	Extendible & Non-extendible	Proposed hybrid & non-hybrid SC Cuk converters (n=10) < Step-up/down Cuk converters of [17, 18] < Proposed hybrid SC Zeta converter (n=10) < Hybrid Zeta of [17, 18] < Proposed SC Zeta converter (n=10) < [19]= Step-up/down Zeta of [17, 18] < Cuk Up2 < Proposed hybrid and non-hybrid Cuk converters (n=1), Zeta Up2 < Proposed hybrid Zeta converter(n=1) < Proposed Zeta converter(n=1) < Zeta= Cuk= Sepic= Zeta/Cuk Up3> [32]	Proposed hybrid & non-hybrid SC Cuk-based converters
Maximum voltage stress on capacitors	Extendible & Non-extendible	Proposed SC Zeta converter (n=10) < Proposed hybrid SC Zeta converter (n=10) < Proposed hybrid & non-hybrid SC Cuk converters (n=10)= [19]= Step-up/down Zeta converters of [17, 18] < Hybrid step-up/down Zeta of [17, 18] < Step-up/down Cuk converters of [17, 18] < Zeta Up2 < [10] < Proposed Zeta converter (n=1) < Cuk up 2=[30]=[8]=[29] <Proposed hybrid Zeta converter(n=1) < Proposed hybrid/non-hybrid Cuk converters(n=1) =Zeta < Zeta Up 3 < Cuk= Cuk Up3	Proposed SC Zeta-based converter
Efficiency	Extendible & Non-extendible	Cuk≃Zeta≃Step-up/down Zeta converters of [17, 18] ≃Proposed SC Zeta/Cuk converters > [19]≃ Step-up/down Cuk converter of [18]> Proposed hybrid SC Cuk/Zeta converters > Hybrid step-up/down Zeta/Cuk converters of [17] > Hybrid step-up/down Zeta/Cuk converters of [18]> 3 cascaded Zeta≃3 cascaded Cuk > 2 Cascaded Zeta Up2 > 2 Cascaded Zeta Up2 > 2 Cascaded Cuk Up2 > [14]	Cuk, Zeta, Step-up/down Zeta converters of [17, 18], Proposed SC Zeta- and Cuk-based converters

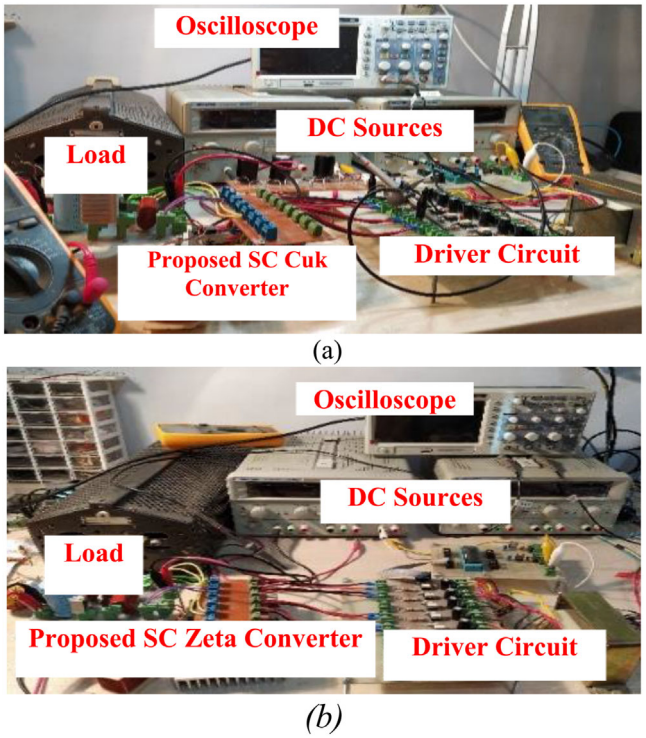

FIGURE 12 Experimental circuits of the proposed SC (a) Zeta-based topology (b) Cuk-based topology

performances of the proposed hybrid ones will be automatically proved. So, the experiments of the proposed hybrid converters will be omitted here.

4.1 | Results of the proposed SC Cuk topology

In the first experiment, the input and output voltages are considered to be 25 and 225 V. Thus, the voltage gain is equal to 9. By using Equation (3), the duty-cycle is calculated ($D = 80\%$). Based on Equations (7) and (8) and considering $\Delta i_{L1,2} \leq 30\%$, L_1 and L_2 should be respectively sized as more than 189 μH and 1.7 mH. Hence, their sizes are selected as:$L_1 = 200\,\mu H$ and$L_2 = 2\,mH$. For sizing the capacitors, the maximum voltage ripple is assumed to be 10%. Under this condition and based on Equation (11), the SCs should be more than 3.5μF. Thus, 5μFcapacitors are used in the experiment. Moreover, according to Equation (12), the size of the filtering capacitor is chosen as 1μF. The parameters used for this experiment are listed in Table 5.

In Figure 13, the results of the first experiment of the proposed SC Cuk converter are presented. As seen, there are two pulses (V_{GT} and V_{GS}) to control the switches. By applying V_{in} =25 V when D =0.8, the proposed converter can generate V_O=224 V which is desirable. Besides, both of the SCs (C_1 and C_2) are successfully charged to 124 V with acceptable voltage ripples. Furthermore, in this figure, voltages of the switches and diodes are presented. The voltages across the switches T_1 and T_2 (V_{T1} and V_{T2}) are the same, with the maximum value of 131 V. In addition, the maximum voltage of switch S_1 (V_{S1}) is about 130 V. The diodes also have desirable voltages (V_{D1}, V_{D2}, V_{D3}, and V_{D4}). The voltages of the diodes D_1 and D_3 are the same (V_{D1}=V_{D3}). It is obvious that, based on the results, all switching devices follow the switching pattern defined for them. In the end, the currents of the inductors L_1 and L_2 (I_{L1} and I_{L2}) are presented which are plausible in terms of both continuity and value.

In the second experiment, the input and output voltages are considered to be 80 and 320 V (voltage gain=4). So, the duty-cycle is obtained equal to 60% according to Equation (3). Similar to the calculations done for the first experiment, by considering maximum allowable ripples of the voltages of the capacitors and the inductors current equal to 10% and 30%, the sizes of L_1, L_2, C_k, C_o should be respectively sized as more than 800 μH, 3 mH, 1.9μFand0.2 μF. Under these conditions, the parameters listed in Table 6 were selected and used for the second experiment of the proposed Cuk-based converter.

In Figure 14, the results of the second experiment of the proposed SC Cuk converter are presented. As seen, there are two pulses (V_{GT} and V_{GS}). By applying V_{in} = 80 V when D = 0.6, the proposed converter can successfully generate V_O = 318.1 V. Besides, the capacitors C_1 and C_2 are successfully charged to about 199 V. Moreover, the voltage waveform of the switches

TABLE 5 Specifications used for first experiment of proposed Cuk converter

Parameters	Symbol	Values
Input voltage	V_{in}	25 V
Output voltage	V_{out}	225 V
Output power	P_{out}	301 W
Switched capacitors	$C_{1,2}$	5μF
Filtering capacitor	C_O	1μF
First inductor	L_1	200μH
Second inductor	L_2	2 mH
Load	R	168Ω
Duty cycle	D	80%

TABLE 6 Specifications of the second experiment of proposed Cuk converter

Parameters	Symbol	Values
Input voltage	V_{in}	80 V
Output voltage	V_{out}	320 V
Output power	P_{out}	512 W
Switched capacitors	$C_{1,2}$	5μF
Filtering capacitor	C_O	1μF
First inductor	L_1	850μH
Second inductor	L_2	3 mH
Load	R	200Ω
Duty cycle	D	60%

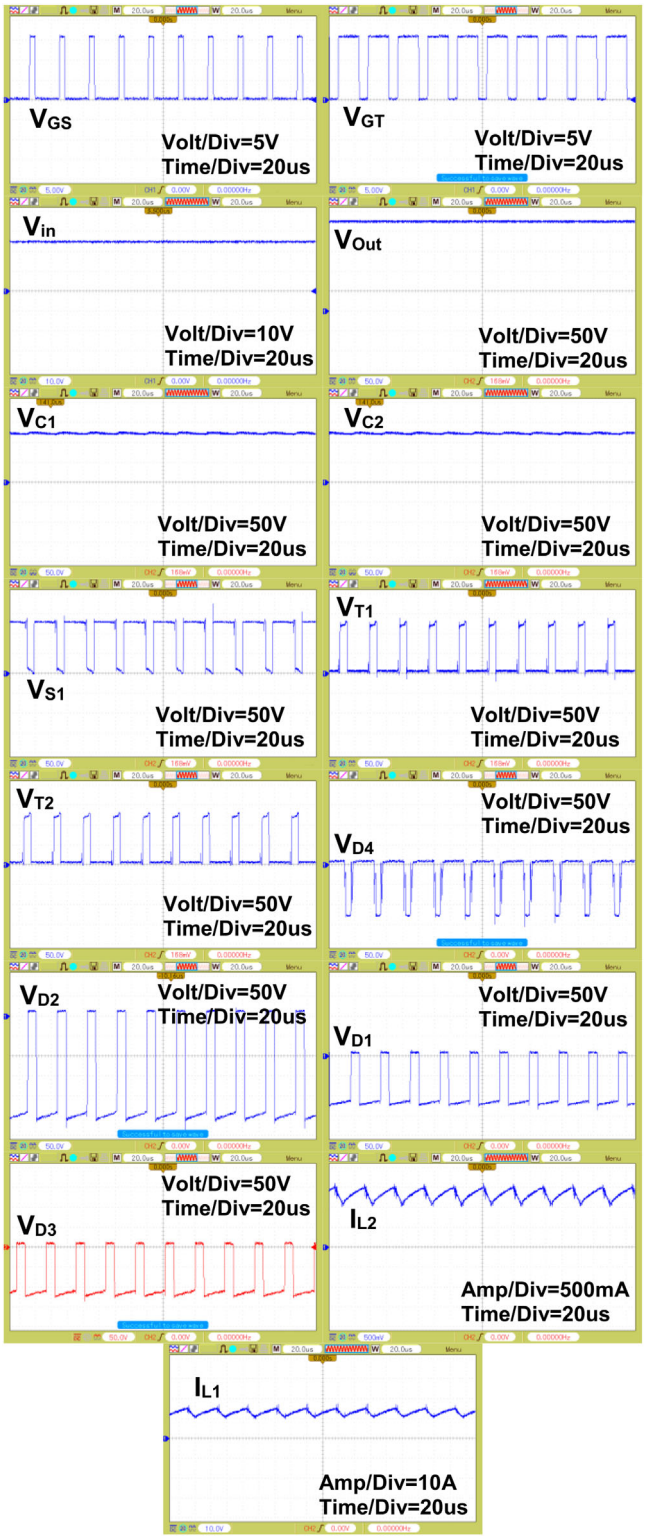

FIGURE 13 Experimental results of the proposed SC Cuk-based converter for $D = 80\%$

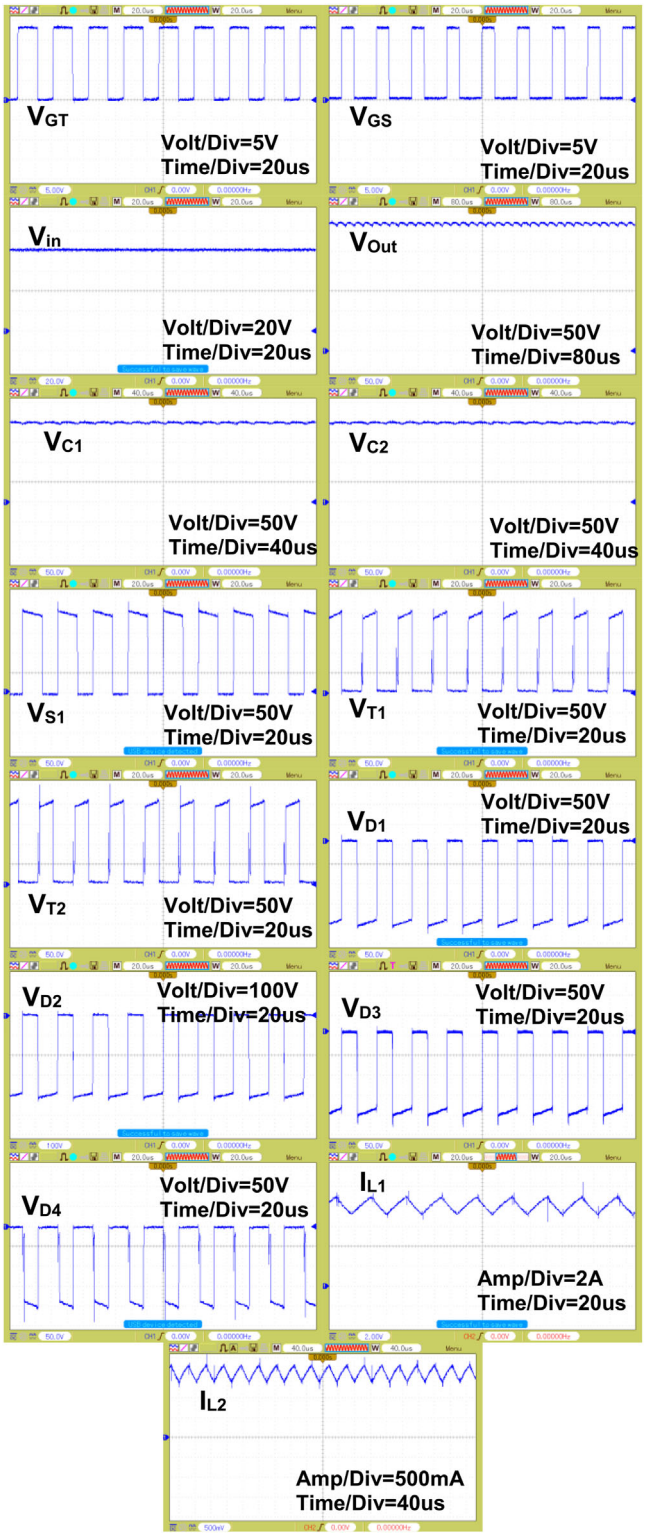

FIGURE 14 Experimental results of the proposed SC Cuk-based converter for $D = 60\%$

S_1, T_1 and T_2 and the diodes D_1, D_2, D_3 and D_4 are presented which are all desirable. As seen, the switches T_1 and T_2 and the diodes D_1 and D_3 have similar voltages ($V_{T1}=V_{T3}$ and $V_{D1}=V_{D3}$) which their maximum values are approximately equal to those of the voltages of the switch S_1 and the diode D_4 (about |212 V|). Also, as seen, the voltage stress on the diode D_2 is also desirable (about −423 V). Finally, in Figure 14, the current waveform of the inductors (I_{L1} and I_{L2}) are shown. As seen, they are completely acceptable in terms of both continuity and value.

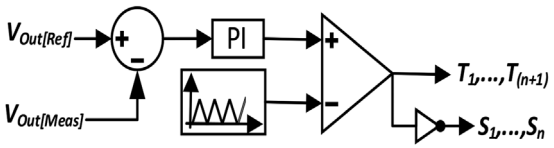

FIGURE 15 Simple block diagram of the closed-loop control system designed for regulating the output voltage of the proposed converters

In the following, the performance of the proposed SC Cuk-based converter equipped with open-loop and closed-loop controllers is studied by step changing the input voltage from 80 to 60 V. Figure 15 shows the simple closed-loop control system used in this section. This control system can regulate the output voltage of the converter under the input voltage changes. As seen, the output voltage is measured and compared with its reference value, and new switching pulses are generated if there is any difference between the measured and reference values. The parameters employed in this experiment are given in Table 6. Please note that the initial duty-cycle for the following experiments is considered as 0.63.

In Figure 16, the experimental results of the converter with and without the closed-loop controller are presented under the pre-defined step-change in the input voltage. As seen in Figure 16(b), even by changing the input voltage (from 80 to 60 V) shown in Figure 16(a), the converter with an open-loop controller maintains its stability, and its output voltage is decreased from 352 to 264 V. Besides, the voltages across the capacitor C_1 is also shown which is desirable. As expected, this voltage changes from 215 to 162 V by applying the step change.

In Figure 16(c), the experimental results of the converter equipped with the closed-loop controller are presented under the mentioned step change. As seen, the converter can generate the desired output voltage (352 V) without losing its stability. The voltages of the SC (C_1) is favourable since it decreases from 215 to 205 V.

Consequently, the proposed SC Cuk-based converter with and without the closed-loop control system has a desirable dynamic performance since it maintains stable operation and provides the desired output voltage successfully under the defined step change.

4.2 | Results of the proposed SC Zeta topology

For the first experiment of this converter, 25 and 200 V are considered as the input and output voltages, giving the voltage gain of 8. According to Equation (15), the duty-cycle is obtained as 80%. Similar to Equations (5)–(12), sizes of the capacitors and inductors of this converter can be obtained as:

$$L_1 = \frac{D}{\Delta i_{L1} f_s} V_{in} \tag{44}$$

$$L_2 = \frac{D\left[(n-3)D - (n-2)D^2 + 1\right]}{(1-D)\Delta i_{L1} f_s} V_{in} \tag{45}$$

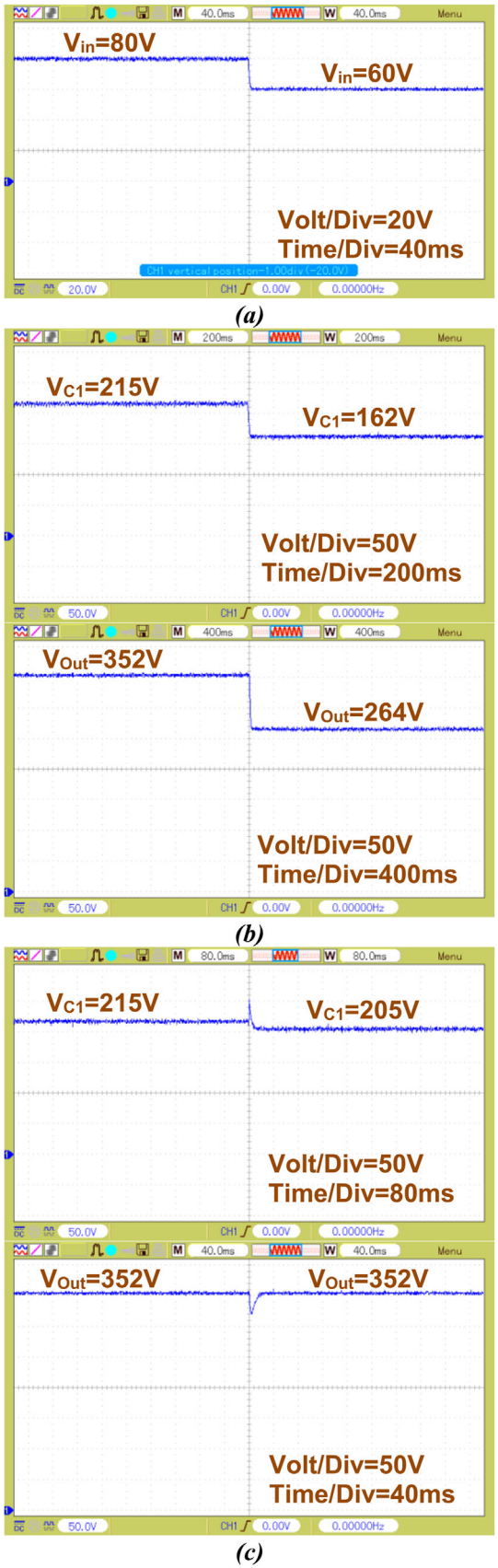

FIGURE 16 Experimental results of the proposed SC Cuk converter with step change in input voltage (a) input voltage (b) the results with open-loop control system (c) the results with close-loop control system

TABLE 7 Specifications of the first experiment of proposed Zeta converter

Parameters	Symbol	Values
Input voltage	V_{in}	25 V
Output voltage	V_{out}	200 V
Output power	P_{out}	300 W
Switched capacitors	$C_{1,2}$	$5\mu F$
Filtering capacitor	C_O	$1\mu F$
First inductor	L_1	$200\mu H$
Second inductor	L_2	1.5 mH
Load	R	133Ω
Duty cycle	D	80%

$$C_k = \frac{D^2(2+(n-2)D)}{(1-D)Rf_s\Delta V_{Ck}}V_{in} \tag{46}$$

$$C_o = \frac{\left[1+(n-3)D-(n-2)D^2\right]}{8f_s^2\Delta V_{Co}L_2(1-D)}V_{in} \tag{47}$$

For sizing the inductors, the maximum current ripple is assumed to be 30%. Thus, based on Equations (43) and (45), the allowed ranges for the inductor sizes are $L_1 \geq 190\ \mu H$ and $L_2 \geq 1.5\ mH$. Under these conditions, their sizes are considered as$L_1 = 200\ \mu H$and$L_2 = 1.5\ mH$. Besides, based on Equations (46) and (47) and by considering $\Delta V_C \leq 10\%$, the sizes of SCs and filtering capacitor are selected as $C_k = 5\,\mu F$ and $C_o = 1\,\mu F$, respectively. The parameters used for this experiment are given in Table 7.

The results of the first experiment of the proposed SC Zeta-based converter are presented in Figure 17. Two switching pulses (V_{GT} and V_{GS}) are employed to control the power switches. The DC input voltage (V_{in}) is equal to 25 V. As clearly seen, the proposed converter can successfully charge the SCs (C_1 and C_2) to the desired voltage (V_{C1}=V_{C2} =99.5 V), with the desired output voltage (V_O =198V). In this figure, the voltages across all of the switches ($V_{S1,}$ $V_{T1,}$ and V_{T2}) and the diodes ($V_{D1,}$ $V_{D2,}$ $V_{D3,}$ and V_{D4}) are presented. The maximum voltage stress on the switches T_1, T_2, and S_1 are respectively equal to 130, 104, and 104 V. The voltages across the diodes D_1 and D_3 are similar to each other (V_{D1}=V_{D3}). Note that among the diodes, the maximum and minimum voltage stress respectively belong to the diodes D_2 and D_4. Based on the results, all the switching devices follow the switching pattern defined for them. Additionally, the first and second inductors currents (I_{L1} and I_{L2}) are shown in Figure 17.

In the second experiment of this converter, 100 and 355.6 V are considered as the input and output voltages, giving the voltage gain of 3.56. Based on Equation (15), the duty-cycle is calculated as 64%. For sizing the passive components, the maximum ripples of their voltages and currents are assumed to be similar to the first experiment. Thus, based on Equations (44)–(47), the allowed ranges for the components are obtained as $L_1 \geq 1\ mH$ and $L_2 \geq 4\ mH$, $C_k \geq 2.1\ \mu F$ and$C_o \geq 0.4\mu F$. The parameters used for this experiment are given in Table 8.

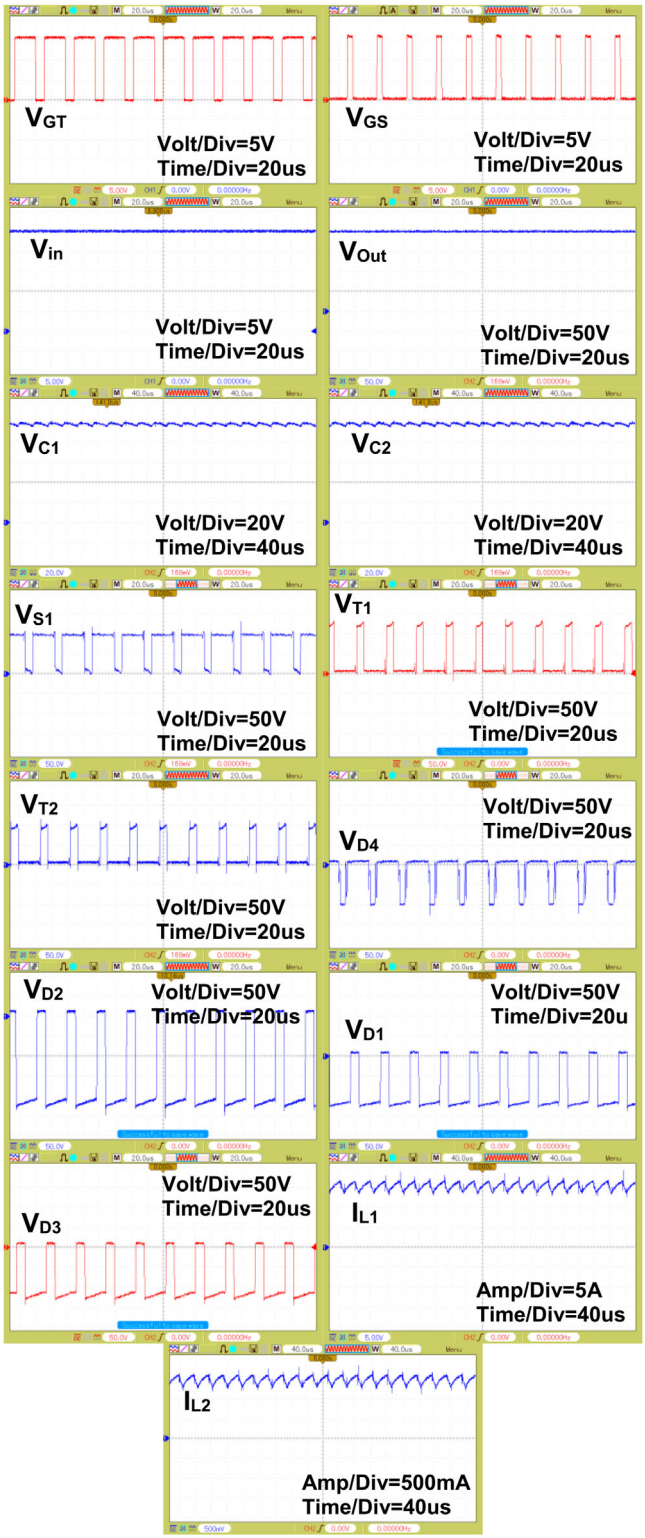

FIGURE 17 Experimental results of the proposed SC Zeta-based converter for $D = 80\%$

The results of the second experiment of the proposed SC Zeta-based converter are presented in Figure 18. As seen, two switching pulses (V_{GT} and V_{GS}) employed to control the

TABLE 8 Specifications of the second experiment of proposed Zeta converter

Parameters	Symbol	Values
Input voltage	V_{in}	100 V
Output voltage	V_{out}	355.6 V
Output power	P_{out}	503 W
Switched capacitors	$C_{1,2}$	5 μF
Filtering capacitor	C_O	1 μF
First inductor	L_1	1 mH
Second inductor	L_2	4 mH
Load	R	251 Ω
Duty cycle	D	64%

switches are presented. Also, the input voltage (V_{in} = 100 V) is shown. As evidently seen, the SCs are charged to a favourable value (about 177 V), and the desired output voltage is generated successfully (V_O =353.5 V). As seen in this figure, the voltages waveform of all switches and the diodes are also presented. As seen, the maximum voltage stress on the switches T_2 and S_1 and the diode D_4 are approximately similar (|189 V|). Also, the diodes D_1 and D_3 have similar voltage waveform ($V_{D1} = V_{D3}$). Besides, the diode $D2$ has the highest voltage stress among the diodes.

Based on the results, all of the switching devices properly follow the switching pattern defined for them. Additionally, the currents of inductors (I_{L1} and I_{L2}) are presented in this figure. Clearly, these current waveforms are desirable.

Consequently, the experimental results are completely in agreement with the analysis, validating the desirable performances of the proposed converter topologies.

In this step, the performance of the proposed Zeta-based converter with and without a closed-loop control system is studied while the input voltage experiences a step change from 90 to 75 V. The closed-loop control system used in this experiment is the one that is shown in Figure 15. As already explained, this controller enables the converter to generate a fixed voltage at its output despite any changes in the input voltage. The parameters employed in this experiment are given in Table 7. The initial duty-cycle for the following experiments is considered as 0.69.

In Figure 19, the experimental results of the proposed SC Zeta-based converter with and without the feed-back controller are presented under the given step-change in the input voltage. In Figure 19(b), the experimental results of the converter with the open-loop controller are shown where after applying the step change, that is, changing the input voltage from 90 to 75 V presented in Figure 19(a), the output voltage is decreased from 399 to 332 V. Moreover, the voltage of the capacitor C_1 is also shown in this figure. As seen, this SC's voltage is 199 and 165 V before and after the step change, respectively. It is evident that the converter with an open-loop controller has a desirable and stable performance.

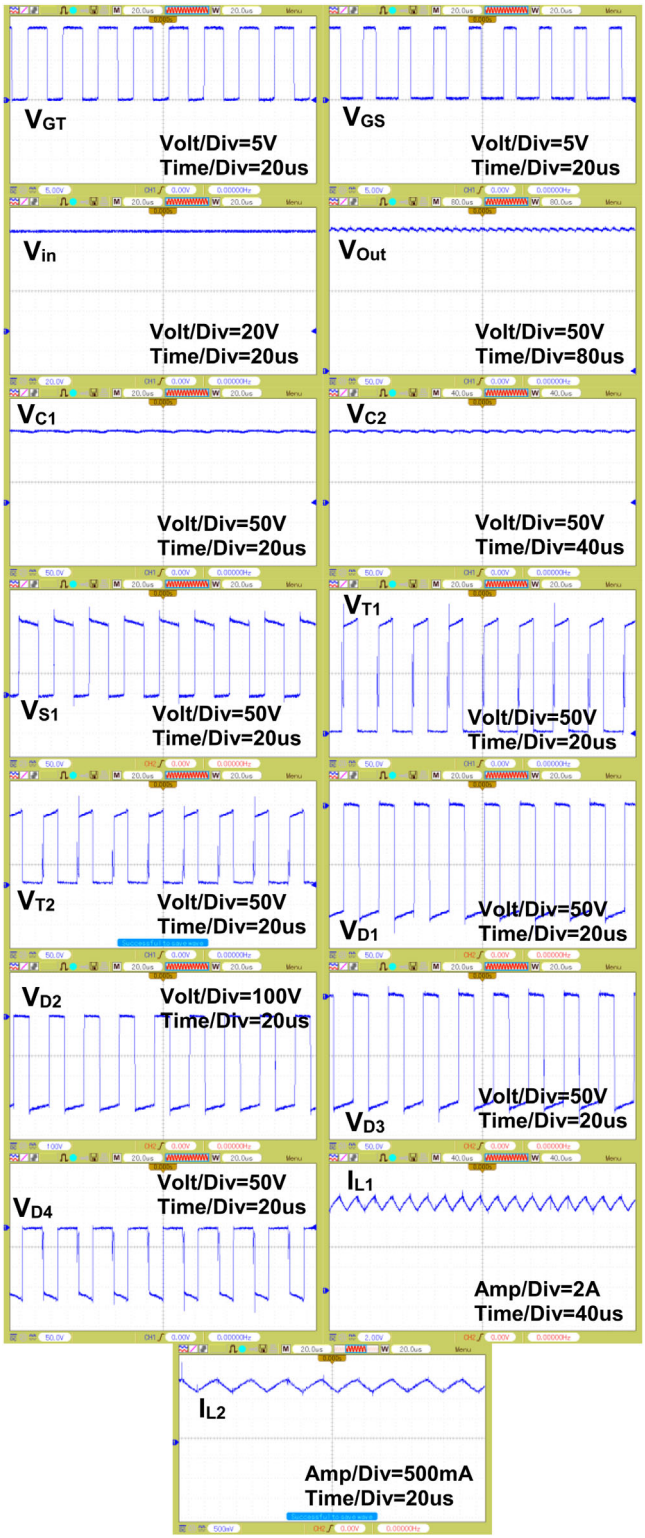

FIGURE 18 Experimental results of the proposed SC Zeta-based converter for D = 64%

In Figure 19(c), the experimental results of this converter are presented under the step change while it is equipped with the closed-loop controller shown in Figure 15. As seen, the converter can generate a constant output voltage (about 399 V) without losing its stability. The voltages across the SC (C_1) is

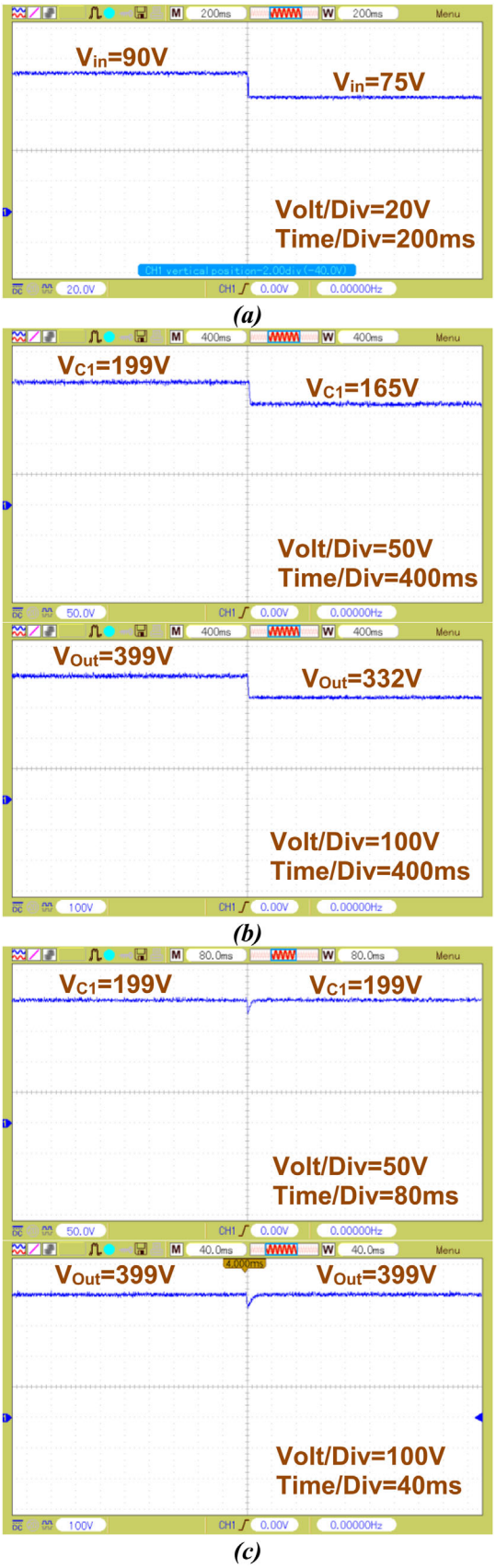

FIGURE 19 Experimental results of the proposed SC Zeta converter with step change in input voltage (a) input voltage (b) the results with open-loop control system (c) the results with close-loop control system

also desirable since it has a constant value (about 200 V) before and after applying the step change. Consequently, the proposed SC Zeta-based converter with and without the closed-loop control system has a desirable dynamic performance since it maintains stable operation and provides the desired output voltage successfully under the defined step change.

In summary, the proposed hybrid and non-hybrid SC Zeta- and Cuk-based converters have desirable performances based on the presented experimental results. This means that the proposed converter topologies can be widely used in modern industrial applications.

5 | CONCLUSION

This article proposes new step-up and step-up/down DC–DC converters with several advantages compared to other converter structures. Based on the results, the proposed topologies can provide very higher voltage gains by employing lower and non-extreme duty-cycles. Also, they impose lower voltage stress on their components like switches and SCs. The proposed converters can provide these benefits by employing a fewer or similar number of components, making them more cost-, size- and weight-effective in comparison with previously introduced converters, especially the conventional ones. Moreover, the desirable performances of the proposed converters are proved by comprehensive experimental results. Thus, among the compared structures, the proposed structures are the superior choices for industrial applications that need high voltage gains. It should be noted that, based on the experimental results, the proposed converters have desirable dynamic performances since they can maintain their stability even under applying a step-change in input voltage.

It is worth mentioning that the proposed converter family includes two Cuk-based SC converters and two Zeta-based SC converters. If an application only needs the step up capability, the proposed Cuk-based ones, which are step up converters, are the best options. In contrast, in applications requiring high voltage gain along with both step-up and step-down capabilities, the proposed Zeta-based converters can be used. To avoid extreme duty-cycles and high voltage stresses on the components, the conventional converters need to be cascaded to achieve high voltage gains, which in turn causes some serious problems such as reduced efficiency and increased number of components. Thus, the proposed converters are better options for such applications due to their modular structures.

Note that the source-load grounds are different in the proposed topologies. Having a common-grounded structure is a merit for the converters used in some special applications such as PV systems. Please note that for some applications, this feature, that is, being common-ground, is a merit; but it is not required for all applications. For instance, since in the PV panels, there are leakage currents causing current harmonics, using a common-ground converter can eliminate these harmonics. In the proposed topologies, this problem can be also solved by other solutions such as considering this problem in designing the control system and also filters.

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