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Initial investigations into the MOS interface of freestanding 3C-SiC layers for device applications

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Abstract

This letter reports on initial investigation results on the material quality and device suitability of a homo-epitaxial 3C-SiC growth process. Atomic force microscopy surface investigations revealed root-mean square surface roughness levels of 163.21 nm, which was shown to be caused by pits (35 μm width and 450 nm depth) with a density of 1.09×10^5 cm^{-2} which had formed during material growth. On wider scan areas, the formation of these were seen to be caused by step bunching, revealing the need for further epitaxial process improvement. X-ray diffraction showed good average crystalline qualities with a full width of half-maximum of 160 arcseconds for the 3C-SiC (002) being lower than for the 3C-on-Si material (210 arcseconds). The analysis of C–V curves then revealed similar interface-trapped charge levels for freestanding 3C-SiC, 3C-SiC on Si and 4H-SiC, with forming gas post-deposition annealed freestanding 3C-SiC devices showing D_{IT} levels of 3.3×10^{11} cm^{-2} eV^{-1} at $E_C - E_T = 0.2$ eV. The homo-epitaxially grown 3C-SiC material's suitability for MOS applications could also be confirmed by leakage current measurements.

Keywords: 3C-SiC, homo-epitaxial growth, CVD, AFM, XRD, MOSCAP, D_{IT}, leakage

(Some figures may appear in colour only in the online journal)

1. Introduction

Silicon carbide (SiC) is an excellent material for power electronics, outperforming silicon (Si) under ambient and extreme device operation conditions (high frequency, high temperature, high power) because of its material properties [1]. Due to its relatively low defect concentration, electronic quality and commercial availability, 4H-SiC is the most common SiC polytype for power electronics applications. Hence, mature unipolar 4H-SiC device structures such as Schottky barrier diodes and metal-oxide-semiconductor field-effect transistors (MOSFETs) are commercially available and highly competitive in power converter applications (600–1700 V blocking voltage), potentially replacing Si PiN diodes and Si insulated-gate bipolar transistors (IGBTs).

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Furthermore, SiC has the advantage over other wide bandgap semiconductors, whereby silicon dioxide (SiO_2) can be directly thermally grown on the epilayer for the use as a gate oxide in metal-oxide-semiconductor (MOS) devices, offering compatibility with mature Si processing technology. However, the quality of reported 4H-SiC/SiO_2 interfaces has suffered from a higher density of interface traps (D_{IT}), as well as higher leakage current levels as a result of a smaller conduction band offset (2.7 eV) compared to the Si/SiO_2 interface (3.2 eV) [2].

In contrast to the hexagonal polytype 4H, SIC's cubic polytype 3C offers the opportunity to be grown hetero-epitaxially on Si substrates, largely reducing material costs. Furthermore, the larger conduction band offset (3.7 eV) at the 3C-SiC/SiO_2 interface theoretically enables MOS devices to have considerably lower leakage currents and D_{IT} levels than unipolar MOS devices fabricated on 4H-SiC.

However, the large mismatch in physical, thermal and crystallographic properties between 3C-SiC and the underlying Si substrate hampers the development of this material [3]. Even though high mobility (up to 228 cm^2 V^{-1} s) 3C-SiC MOSFETs have been reported in the past decade [4, 5], in-depth studies of 3C-SiC MOS capacitors (MOSCAPs) still show high quantities of positive charge at, or near, the 3C-SiC/SiO_2 interface [6].

Homo-epitaxial growth of freestanding 3C-SiC will eliminate the lattice mismatch and the thermal expansion coefficient difference caused by heteroepitaxy of 3C-SiC on Si, which limits the epitaxial thickness and causes in built material stress, causing wafer bow and warp [7]. Other works to grow freestanding 3C-SiC [8] used sublimation growth on a chemical vapor deposition (CVD) grown 3C-SiC on Si template, with the Si template then melted *in-situ*. There, high quality free-standing (001), 20–90 μm thick layers with diameters of >10 mm were achieved, verified with x-ray diffraction (XRD) analysis. Other reports [9] demonstrated fabrication of free standing substrates of 300 μm thickness by growth of 3C-SiC grown on undulant Si templates, where the Si template was then chemically removed as the last step. In later works, these were then subsequently used to grow a 40 μm thick epitaxial layer [10] by means of the sublimation epitaxy where layers showed local accumulation of stacking faults, resulting in the formation of different polytypes. Since CVD growth is more ubiquitous for active device formation a 3C-SiC homo-epitaxial CVD process with standard Si substrates would have more potential in a commercial process. Recently, a process using CVD epitaxy on standard large (100 mm) wafer diameter wafers has been reported [11], with high polytype uniformity and low defect densities.

In this study, we present the results of an initial investigation into homo-epitaxially grown 3C-SiC. The materials physical properties are evaluated using atomic force microscopy (AFM) to extract the surface roughness and using high-resolution XRD to analyse the crystal quality. In addition, the electrical properties of MOSCAPs, utilising SiO_2 as a gate oxide, wherein the results of conventional, thermally formed oxides are compared to those formed via atomic layer deposition (ALD). D_{IT}, flatband voltages and hysteresis voltages are extracted to test the suitability of this material for device applications.

2. Methodology

Homo-epitaxial 3C-SiC layers (on-axis) were grown using CVD on Si (100) substrates in a LPE ACiS M-10 hot-wall reactor. Initially, growth was carried out a temperature close to the melting point of Si (1400 °C) to form a 90 μm highly doped 3C layer. By increasing the temperature further, the Si substrate melted and was removed, leaving the remaining freestanding SiC layer. This was used as a seed layer to homo-epitaxially grow at a temperature of 1640 °C a further 150 μm of highly nitrogen-doped 3C. A final 10 μm n-type drift layer of doping (2×10^{16} cm^{-3}) was epitaxially grown. The exact process has been reported by Anzalone *et al* [3].

For benchmarking, 4H-SiC epitaxial layers were grown on four degrees off (0001) substrates using an LPE ACiS M8 reactor. The growth temperature was 1650 °C, using a trichlorosilane (TCS) and ethylene (C_2H_4) mix in an H_2 ambient at a nominal growth rate of 30 μm h^{-1}. A 10 μm thick epilayer was intentionally doped during growth at 4×10^{15} cm^{-3} with nitrogen on a 1×10^{19} cm^{-3} highly N-doped substrate. Furthermore, 3C-on-Si material was provided by NOVASIC, which had an unintentionally doped (2×10^{16} cm^{-3}) n-type 3C-SiC (100) 10 μm thick epitaxial layer which was grown on-axis on a 4 inch Si (100) substrate. MOS-devices, made with a thermal oxide have recently been reported, demonstrating the high quality of this material [12].

For roughness analysis, a Bruker Icon AFM was used in PeakForce Tapping mode to investigate the surface of the freestanding 3C-SiC material. The probe tip was made of Si on a nitride lever, with scan areas ranging from 1 μm × 1 μm to 80 μm × 80 μm. Extracted data were analysed using the Gwyddion software package. Here, the root-mean square (RMS) surface roughness is computed as square sum of absolute values of height data differences from the mean height over the entire scan area.

The crystal quality of two 3C-SiC wafers was analysed using XRD in a high resolution x-ray facility, consisting of two Panalytical X'Pert Pro MRDs, both equipped with a Cu Kα 1 hybrid monochromator as the incident beam optics and a receiving slit/analyser crystal in the diffracted beam optics.

3. Results and discussion

3.1. Surface roughness investigation using atomic force microscopy

RMS roughness values for the freestanding 3C-samples increase exponentially with scan size from 1.62 nm (1 μm × 1 μm) in figure 1(a) to 163 nm (80 μm × 80 μm) in figure 1(b), as figure 1(c) reveals. Whereas the RMS roughness value for the smallest size demonstrates a reasonable range for device performance, the RMS values of bigger scan sizes will lead to a severe impact on key electrical parameters such as leakage current and reduce effective field mobility, hence increasing any specific on-resistance ($R_{SP,ON}$) values made from as-grown materials. The reason for the worsening of surface roughness can be seen in figure 1(b),

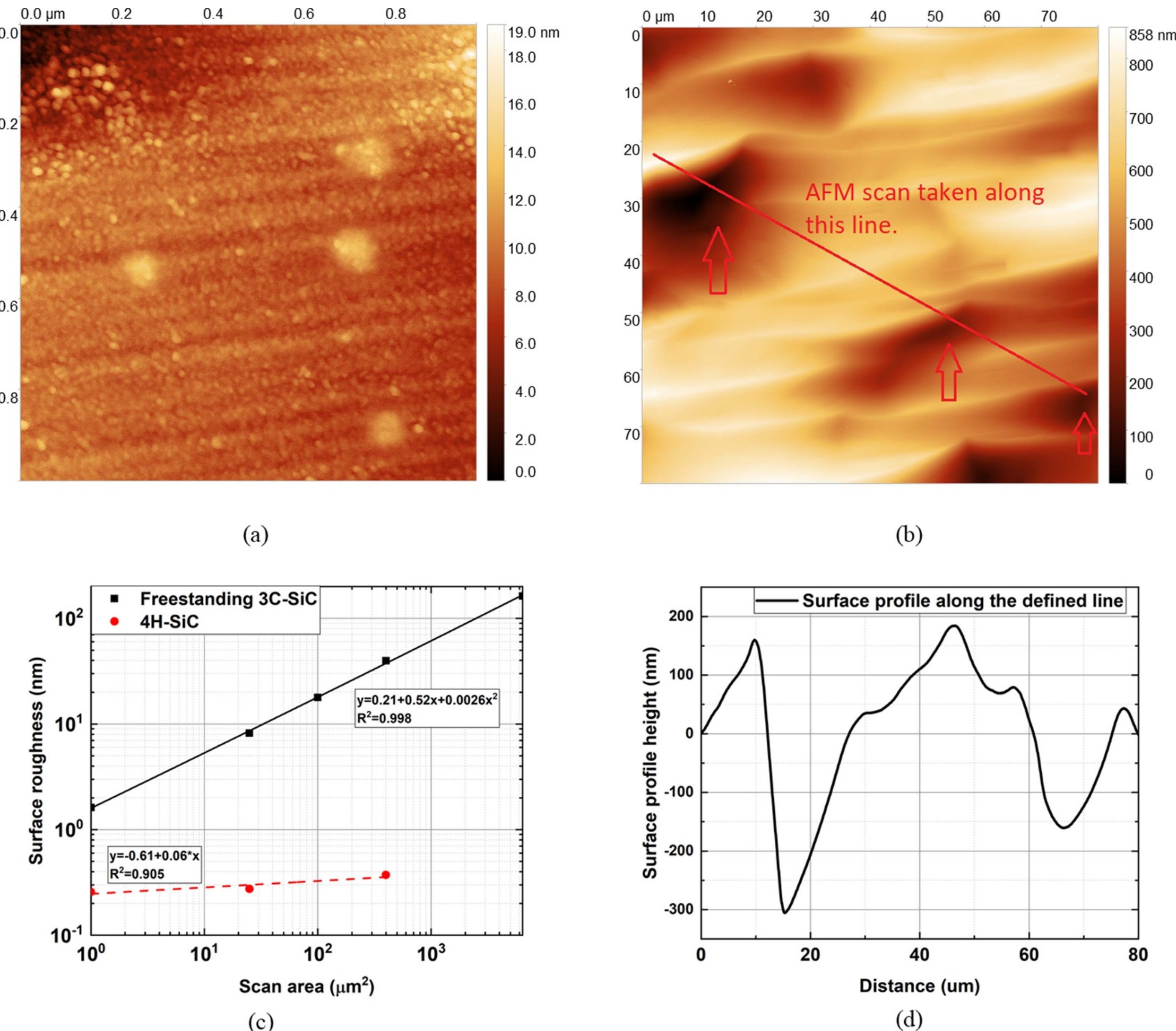


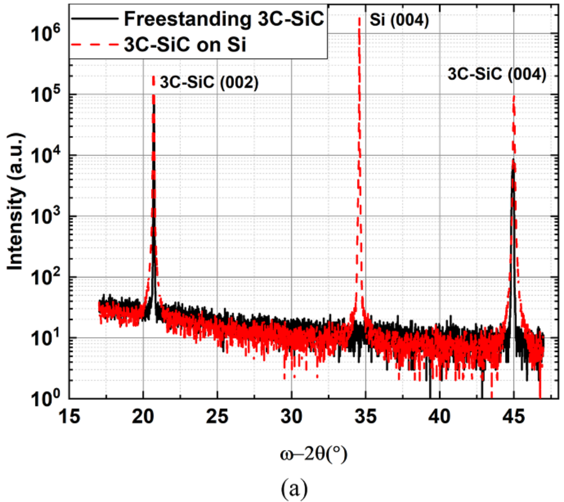
Figure 1. Atomic force microscopy images of freestanding 3C-SiC samples with 1 μm × 1 μm (a) and 80 μm × 80 μm (b) scan sizes as well as a plot of surface roughness over scan area (c) which includes a 4H-SiC sample as well. The surface profile in image (d) was extracted across the line in figure (b), starting from the top left corner down to the bottom right corner.

where the presence of large pits (35 μm width and and 100–450 nm depth), with a density of 1.09 × 10^5 cm^{-2} is the cause of a sharp increase in surface roughness. The structural location of these pits resembles step bunching, a phenomenon widely reported for 4H-SiC with fewer reports for 3C-SiC [13]. They could also be phase boundary artifacts from protrusions during deposition of the initial 3C-SiC/seed. This can usually be reduced by process optimisation of the epitaxial growth or polishing. In comparison, the investigated 4H-SiC sample shows a smoother surface with no visible surface features and only marginal increase in surface roughness and RMS values below 1 nm for all measured scan areas, revealing a significant difference in terms of surface quality when compared to the freestanding 3C-SiC sample.

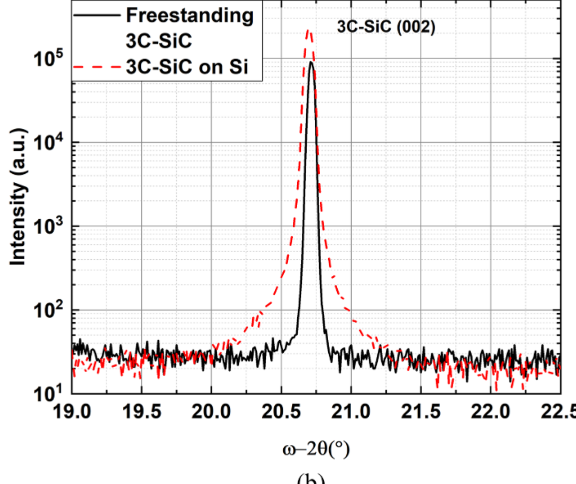
3.2. Crystal quality investigation using XRD

In figure 2(a), a $\omega-2\theta$ curve is shown depicting a 3C-SiC (002) peak at 21° and a 3C-SiC (004) peak at 45° for both samples. A third Si (004) peak could be detected at 35° for the 3C-SiC on Si sample only.

Furthermore, the full width of half-maximum (FWHM) of the 3C-SiC (002) peak was extracted from the rocking curve in figure 2(b) for both samples. A high FWHM in the rocking curve of the 3C-SiC (002) peak has been shown [14] to be directly related to a high density of well-reported defects in 3C-SiC, such as stacking faults and micro-twins; a low FWHM generally demonstrates a good average material quality [15]. The FWHM of the freestanding 3C-SiC is approximately 160 arcseconds, lower than the FWHM of 210 arcseonds



(a)



(b)

Figure 2. $\omega - 2\theta$ XRD scans (rocking curves) depicting (a) the full XRD spectrum and the (b) 3C-SiC (002) region for a freestanding 3C-SiC and a 3C-SiC on Si samples.

extracted for the 3C-SiC on Si sample. This is in good agreement with previous reports [3] and suggests promising material quality when compared to 3C-SiC on Si material.

3.3. Electrical results

For further investigations into the suitability of the previously described materials for device processing, electrical characteristics were extracted from MOS-devices. Oxides formed using ALD and thermal oxidation were considered. A FG post-deposition anneal was carried out on ALD-deposited samples since this process has recently shown a big improvement in terms of electrical parameters and interface quality when compared to as-deposited ALD silicon dioxide and thermal oxide [16, 17].

All samples were cleaned with a solvent clean, followed by a HF(10%)/RCA1/HF(10%)/RCA2/HF(10%) process. SiO_2 was deposited on the ALD samples in an Ultratech Fiji G2 plasma-enhanced ALD system, with a substrate temperature of 200 °C, bis(diethylamino)silane (BDEAS) as the Si precursor and O_2 plasma as a co-reagent. The deposited layer thickness was ≈30 nm (500 cycles). Again, 4H-SiC samples were used for benchmarking.

Following deposition, one set of samples (freestanding 3C-SiC, 3C-SiC on Si and 4H-SiC) was left as-deposited, and a second set of samples was loaded into a high-temperature anneal furnace, where they were annealed in forming gas (FG, 5% H_2 in 95% N_2) for 1 h with a gas flow of 5 slm and a temperature of 1100 °C, as this process has been reported to improve the interface on 4H-SiC/SiO_2 MOSCAPs [16].

A third set of samples underwent thermal oxidation processes. The SiO_2 for the 4H-SiC samples were formed using a direct N_2O thermal growth in a HiTech furnace at 1300 °C for 4 h in an Ar:N_2O (4 slm: 1 slm) ambient [18].

The freestanding 3C-SiC samples underwent a dry oxidation process in the same furnace at 1200 °C for 10 min in an Ar:O_2 (4 slm: 1 slm) ambient followed by a post oxidation anneal at 1200 °C in an Ar:N_2O (4 slm: 1 slm) ambient since this process has been proven to be highly reliable for 3C-on Si SiC MOSCAPs [12]. A dataset for thermal oxides on 3C-on Si was not included in this study but can be found in a study carried out by Li *et al* [12]. Aluminium (Al) contacts were formed on top of the oxide layers using an Al wet etch and a 1 μm thick Al ohmic contact was deposited on the backside using electron beam evaporation.

Afterwards, room temperature vertical capacitance–voltage (C–V) measurements were recorded using an Agilent E4980A LCR meter and the D_{IT} was calculated using the high-low method (1 MHz and 1 kHz).

Key electric parameters such as flatband voltage (V_{FB}), hysteresis voltage and frequency dispersion in accumulation were then extracted and averaged from at least 16 devices per sample. Results are shown in table 1 whereas

Table 1. Summary of measured flatband voltage, hysteresis and frequency dispersion of 16 samples per category, with a device area of 8.04×10^{-4} cm^2. For thermal and 4H-SiC oxides, the device area was 3.14×10^{-4} cm^2.

Sample	Flatband voltage (V)	Hysteresis voltage (V)	Frequency dispersion (% × dec^{-1})
Freest. 3C-SiC as-dep.	−0.72 ± 1.14	1.49 ± 0.58	0.08 ± 0.05
Freest. 3C-SiC FG-anneal	−3.71 ± 0.42	2.26 ± 1.37	0.20 ± 0.09
Freest. 3C-SiC thermal	−4.06 ± 0.23	0.15 ± 0.07	0.47 ± 0.40
3C-SiC/Si as-dep.	0.54 ± 0.13	1.02 ± 0.33	0.07 ± 0.04
3C-SiC/Si FG-anneal	−2.73 ± 0.18	0.16 ± 0.07	0.37 ± 1.14
4H-SiC as-dep.	8.39 ± 1.02	0.16 ± 0.13	2.58 ± 1.54
4H-SiC FG-anneal	−0.29 ± 0.13	0.10 ± 0.08	0.33 ± 0.29
4H-SiC thermal	0.61 ± 0.12	0.15 ± 0.01	0.40 ± 0.19

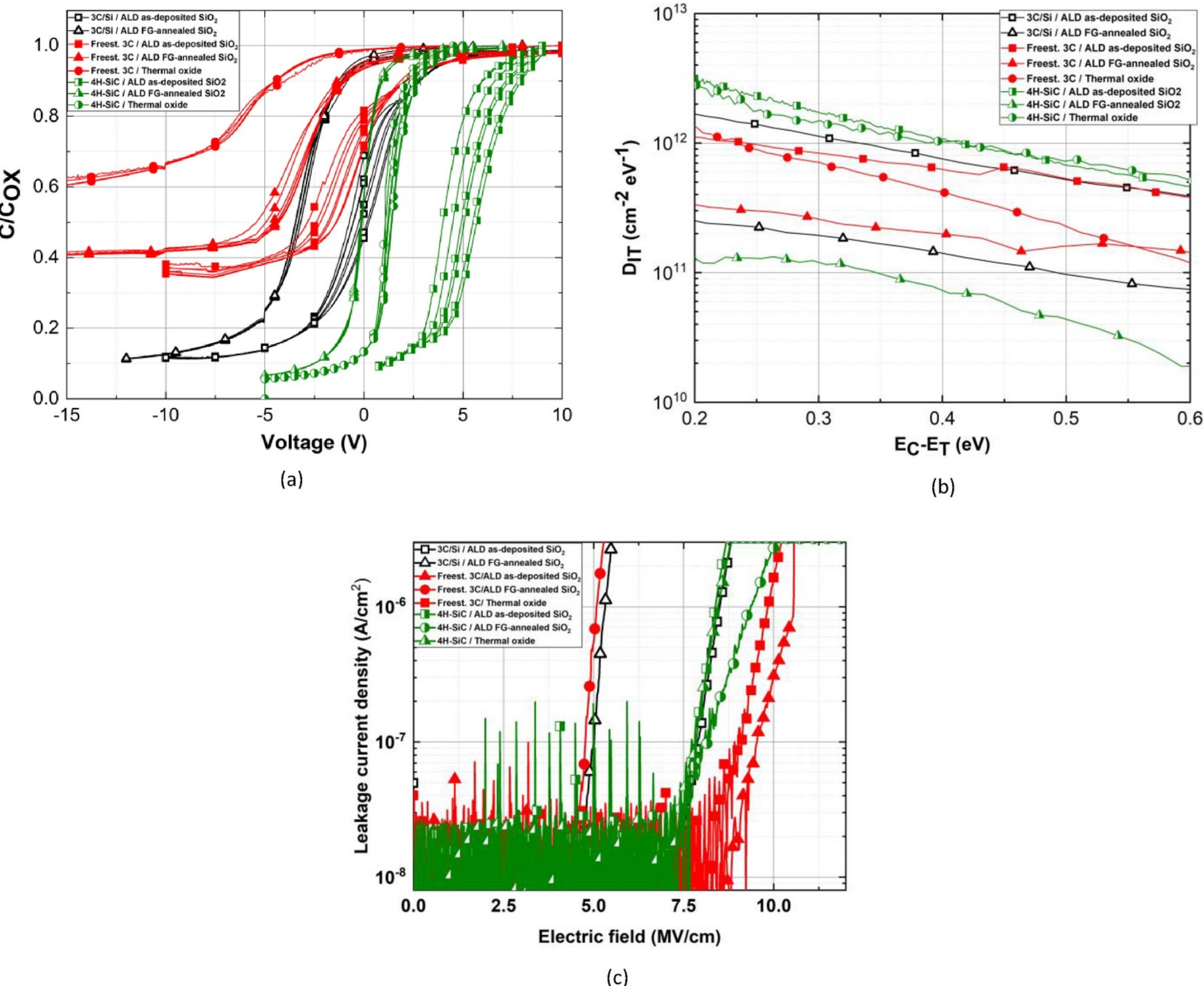


Figure 3. Normalised capacitance–voltage curves for each dataset (a) and the respective D_{IT} curves (b). Leakage current is shown in (c). The device area is 8.04×10^{-4} cm^2. For thermal and 4H-SiC oxides, the device area is 3.14×10^{-4} cm^2.

characteristic C–V responses of the dataset are shown in figure 3(a) and their D_{IT} levels relative to the conduction band edge are represented in figure 3(b). For leakage current measurements, I–V measurements were carried out on the same MOSCAPs, with representative results being shown in figure 3(c).

Generally, the as-deposited and FG-annealed devices which were fabricated on 3C-SiC on Si are very repeatable, with all electrical parameters having tight distributions. Here, flatband voltages and frequency dispersions of the as- deposited sample (3C-SiC on Si) show an excellent performance, averaging 0.54 V and 0.07% $\times$ dec^{-1}, respectively. This is already a significant improvement compared to reported 4H-SiC/ALD-deposited SiO_2 (as-deposited) interfaces utilising the same process, in which flatband voltages averaged at 8.63 V and accumulation was not fully accomplished [17]. This suggests that positively charged (donorlike) states near or at the 3C-SiC/SiO_2 interface [19] neutralised a significant quantity of negative charge, which is created during the ALD-deposition of SiO_2, leading to a low flatband voltage.

In comparison, the FG-anneal on 3C-SiC on Si samples reduced hysteresis voltage values, averaging 0.16 V, whilst shifting the C–V curve further away from the ideal response, with flatband voltages averaging −2.73 V. It also reduced the D_{IT} by roughly one order of magnitude to 2.8×10^{11} cm^{-2} eV^{-1} at $E_C - E_T = 0.2$ eV. As a side note, this is further confirmation that, on 3C-SiC on Si, MOSCAPs utilising deposited oxides can achieve similar D_{IT} levels as those using thermally grown oxides, as seen previously [12, 20]. The flatband voltage of thermal oxides on 4H-SiC averaged 0.61 V, with D_{IT} levels at 2×10^{12} cm^{-2} eV^{-1} at $E_C - E_T = 0.2$ eV. The best interface quality was shown in the FG-annealed 4H-SiC sample, with a D_{IT} levels at 1.5×10^{11} cm^{-2} eV^{-1} at $E_C - E_T = 0.2$ eV.

The most significant outcome of this investigation is the performance of both as-deposited and FG-annealed

MOSCAPs on freestanding 3C-SiC. The as-deposited samples show good flatband voltage and frequency dispersion distributions, averaging −0.72 V and 0.07 × dec^{-1}. D_{IT} levels of the devices are in the same range as for devices fabricated on 3C-SiC on Si, with a trap level of 2.8×10^{11} cm^{-2} eV^{-1} at $E_C - E_T = 0.2$ eV. Although the average hysteresis voltage value of 1.49 V indicates a high quantity of charge in the oxide and near the interface [21], this is a promising result which is confirmed by the excellent leakage current performance with samples reaching a current level of 1×10^{-9} A at an electric field higher than 10 MV cm^{-1} . The forming gas annealed samples on freestanding 3 C-SiC follow a similar trend as for the 3 C-SiC on Si dataset, with D_{IT} levels being significantly reduced to 3.3×10^{11} cm^{-2} eV^{-1} at $E_C - E_T = 0.2$ eV, with trap levels being about an order of magnitude lower than for the thermal oxide on freestanding 3C-SiC. However, the hysteresis response is poor for the FG-annealed samples on freestanding 3C-SiC, averaging at 2.36 V, which warrants further investigation, though this is likely related to the presence of slow traps in the semiconductor due to the step bunching. Leakage levels reveal that the FG-annealed samples on both 3C-on-Si as well as well as the freestanding 3C-SiC suffer from a relatively poor leakage performance, with tunneling beginning before an electric field of 5 MV cm^{-1}. The leakage current of the FG-annealed device on 4H-SiC shows lower leakage current levels (1×10^{-9} A at an electric field of about 10 MV cm^{-1}) than for the as-deposited and thermal oxides on 4H-SiC. This indicates that a high quality/chemical-mechanical polished surface might be able to lower the leakage current levels of the other two FG-annealed 3C-SiC samples.

4. Conclusion

In conclusion, a homo-epitaxial (freestanding) 3C-SiC growth process has been investigated in terms of its surface properties and crystalline quality and its suitability for device application has been established. AFM surface investigations show that the surface quality of the freestanding 3C material, without having undergone a polishing process, is promising at 163 nm RMS roughness for a scan size of 80 μm × 80 μm, but is not directly comparable to an optimised 4H-SiC homoepitaxy process on chemical-mechanical polished surface, measured at roughly 2 nm. It was shown this was caused by pits (35 μm width and 450 nm depth) with a density of 1.09×10^5 cm^{-2} which had formed during material growth. This undermined the generally good material uniformity seen at smaller scan sizes. XRD analysis revealed that freestanding 3C-SiC, with a FWHM for the 3C-SiC (002) peak of 160 arcseconds, has a superior crystal quality with potentially lower densities than for 3C-on-Si material (210 arcseconds). *C–V* analysis then revealed similar trap levels for both 3C-SiC materials as well as 4H-SiC. The ALD deposited, FG annealed MOS capacitors on freestanding devices having a D_{IT} level of 3.3×10^{11} cm^{-2} eV^{-1} at $E_C - E_T = 0.2$ eV. Also, both the thermally oxidised and ALD as-deposited samples on freestanding 3C-SiC showed the lowest leakage current levels of the entire dataset, with both devices reaching still low leakage current levels of 1×10^{-9} A at electric fields above 10 MV cm^{-1}. Hence, the general competitiveness of homo-epitaxially grown 3C-SiC with 3C-on-Si as well as 4H-SiC material in terms of device quality was demonstrated, particularly given the scope for improving surface morphology and proving the suitability of the material thickness for wafer-scale processing.

Data availability statement

The data that support the findings of this study are available upon reasonable request from the authors.

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