Research Article

Design of New High Step-Up DC-DC Converter Topology for Solar PV Applications

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A new topology for high step-up nonisolated DC-DC converter for solar PV applications is presented in this paper. The proposed high-voltage gain converter topology has many advantages like low-voltage stress on the switches, high gain with low duty ratio, and a continuous input current. The analytical waveforms of the proposed converter are presented in continuous and discontinuous modes of operation. Voltage stress analysis is conducted. The voltage gain and efficiency of the converter in presence of parasitic elements are also derived. Performance comparison of the proposed high-gain converter topology with the recently reported high-gain converter topologies is presented. Validation of theoretical analysis is done through the test results obtained from the simulation of the proposed converter. For the maximum duty ratio of 80%, the output voltage of 670 V is observed, and the voltage gain obtained is 14. Comparison of theoretical and simulation results is presented which validates the performance of the proposed converter.

1. Introduction

The application of renewable energy sources for day-to-day life is increasing widely. This is due to clean and green nature of energy produced by renewable energy sources. Among the renewable energy sources, solar energy is most promising because of its pollution-free nature. But the output voltage obtained from the solar photovoltaic (PV) panels is very low, and therefore, it cannot be connected to high-voltage load or grid directly. Therefore, a dc-dc conversion stage with high gain is required to interface the solar PV with high-voltage load or grid. Many high-gain DC-DC converters were reported in the last one decade. But the design improvement of these high-gain DC-DC converters with respect to increased voltage gain, component reduction, increased efficiency, and reduced losses is still being reported by many researchers. These high-gain DC-DC converters also find their applications in fuel cells, electric vehicles, battery energy storage, automotive industries, and uninterrupted power supplies [1–4].

Basically, there are two types of DC-DC converters, namely, nonisolated and isolated DC-DC converters. Isolated DC-DC converters mainly used in high power applications. But the presence of transformers increased the converter size. The conventional boost converters are used in the earlier stages for stepping up the voltage, but the limitation is the high-voltage stress on the switch, and hence, high-rating switch is needed.

An interleaved high step-up boost converter was proposed in [5] for PV applications. This converter provides a high efficiency and high step-up gain, but this converter uses more number of components which leads to increase in losses at higher loads due to the effect of parasitic elements. Converters reported in [6, 7] employed a switched capacitor structures to achieve a high step-up conversion ratio. Even though this technique provides a high conversion ratio, the stability of the converter reduces due to the presence of impulse current.

A nonisolated high step-up DC-DC converter with single-inductor energy storage cell based switched capacitor

configuration was proposed in [8]. This configuration was derived from the basic boost-, buck-boost-, and type II boost/buck-boost-based converters. This converter integrates the merits of high gain of switched capacitor (SC) converter and high output voltage regulation of switching mode DC-DC converter.

A high-gain nonisolated DC-DC converter for DC microgrids was proposed in [9]. This converter used voltage multiplier cell and hybrid switched-capacitor technique. Here, the switches are operated with a combined duty ratio of maximum 95% to achieve the gain. Clamping circuits used increase the circuit complexity. A nonisolated converter with automatic output voltage balancing was reported in [10]. High step-up DC-DC converter with active switched LC-network was proposed in [11]. This converter uses an active switched capacitor and inductor network. Input-parallel output-series dc-dc boost converter was reported in [12]. Here, the input current ripple is reduced by adopting interleaved structure. Though the gain and efficiency are more, the number of components used are more which increases the size and cost.

A dc-dc multilevel boost converter which combines the boost converter and a switched capacitor was reported in [13]. This converter operates with a continuous input current and high switching frequency. Cascaded structure for n-stage conversion is also discussed. A nonisolated boost DC-DC converter based on voltage-lift technique with a single switch was reported in [14]. This technique is based on energy storage elements inductor and capacitor. But the increase in number of components makes the system complex. A new family of single-switch three-diode dc-dc pulse width-modulated (PWM) converters operating at constant frequency and constant duty cycle was discussed in [15]. There is a less-voltage stress on the diodes and decreased switch and conduction losses. Voltage multipliers can be integrated to increase the voltage gain.

A transformerless inverter with active power decoupling was reported in [16]. An extended duty ratio (EDR) boost is implemented as the high-gain dc-dc stage. A high step-up DC-DC converter with active switched inductor and passive switched capacitor networks was proposed in [17]. Here, voltage stresses are minimal. Extendable nonisolated high-gain DC-DC converter based on active-passive inductor cells was proposed in [18]. The principle of operation is based on parallel charging and series discharging of the inductors. This uses more number of components; hence, more complex is the system. Recently, coupled inductors find their applications in DC-DC converters to obtain a high-voltage gain. This leads to a compact system because of only one inductor [19–23]. A single-switch buck-boost DC/DC converter [24], SEPIC-based single switch buck/boost DC/DC converter with continuous input current [25], and a single-switch quadratic buck/boost DC/DC converter with continuous input and output current [26] were also reported. In all these single-switch converters, the number of capacitors, inductors, and diodes are more. The converter reported in [27] used switched inductor concept and uses two switches. [29] reports the quasiswitched converter which produces high gain with the low duty ratio. An interleaved converter

with inverting capability is reported in [28]; even though the gain is high, the total components required is more. Therefore, the need for a high-gain transformerless DC-DC converter with less number of components arises to enhance the dc-link voltage.

Figure 1 shows the application of high-gain DC-DC converter in grid-connected solar PV system. In this paper, a new topology for a high-gain DC-DC converter is introduced. The proposed high-gain DC-DC converter uses three switches. The operating principle of the proposed converter in continuous conduction mode (CCM) and discontinuous conduction mode (DCM) are explained, and the boundary conditions are derived. Performance comparison of the proposed high-gain converter topology and the other recent high-gain topologies is made and analyzed. Simulink model of the proposed converter is developed, and the results were presented and discussed in detail.

2. Principle of Operation of Proposed Converter

A high-gain DC-DC converter with crossconnected capacitors is proposed in this paper. Figure 2 shows the circuit configuration of the proposed converter. The proposed converter consists of three switches S_1, S_2, and S_3, two inductors L_1 and L_2, four diodes D_1, D_2, D_3, and D_4, and three capacitors C_1, C_2, and C_o. The duty ratio of S_1 and S_3 is d_1 and that of S_2 is d_2. The crossconnected capacitor structure used at the end of the converter circuit will double the output voltage; hence, increase in voltage gain is achieved in the proposed converter circuit. Depending on the switching operations of the switches S_1, S_2, and S_3, there are three modes of operations present in the proposed converter during continuous conduction mode (CCM).

Mode 1: in this mode, all the three switches S_1, S_2, and S_3 are simultaneously turned on at t_0. The equivalent circuit shown in Figure 3(a) for this mode shows the current path clearly. Here, the inductors L_1 and L_2 are parallelly charged from the input source V_i. The diodes D_1, D_2, and D_3 are reverse biased. Diode D_4 is forward biased. The load current is supplied by the capacitors C_1 and C_2. The voltage across both the inductors L_1 and L_2 is equal to the input source voltage.

Mode 2: when the switches S_1 and S_3 are turned off at t_1, this mode of operation is established. Switch S_2 still conducts. Figure 3(b) shows the equivalent circuit for this mode. Here, the diodes D_1 and D_4 are forward biased, and other diodes are reverse biased. Both the inductors will get connected in series and are charged from the input source. The voltage across each inductor is $V_i/2$. The output voltage V_o is equal to the sum of V_{C1} and V_{C2}.

Mode 3: this mode of operation is established when the switch S_2 is turned off at t_2. Equivalent circuit for this mode is shown in Figure 3(c). Diode D_4 is reverse biased, and the other diodes are forward biased. The inductors will discharge the stored energy to the load with a voltage of $(2V_i - V_o)/4$.

From the analytical waveforms in Figure 4(a), the expression for voltage gain of the proposed converter in
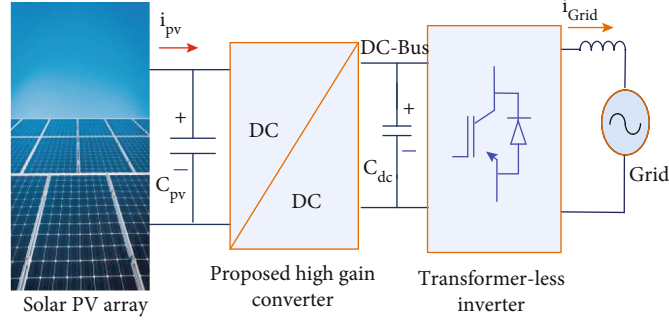
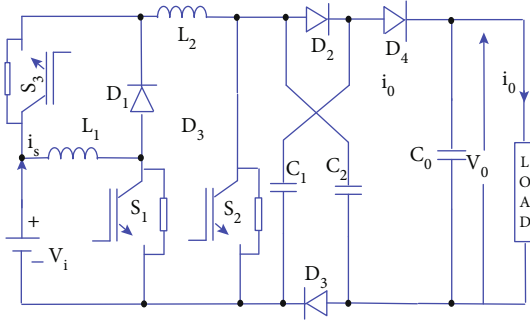FIGURE 1: A high-voltage gain DC-DC converter in grid tied solar PV application.

FIGURE 2: Circuit diagram of proposed high-gain DC-DC converter.

CCM is obtained. By applying the volt-second balance principle for the inductor L_1, the voltage gain expression is derived as

$$M_{\mathrm{CCM}} = \frac{V_o}{V_i} = 2\frac{1+d_1}{1-d_2}. \tag{1}$$

3. Performance Analysis of Proposed Converter

3.1. DCM Operation. The proposed converter operates in four modes for the DCM. Mode 1: all the switches S_1, S_2, and S_3 are turned on at t_0. The current through the inductors L_1 and L_2 increases from zero and reaches I_{L1} at t_1. Hence, this operating mode in DCM and CCM is identical. The peak value of inductor current is expressed as

$$I_{L1pk} = \frac{V_i}{L}d_1T_s. \tag{2}$$

Mode 2: here, switches S_1 and S_3 are turned off. From the instant t_1, the current of the inductors further increases and reaches the peak value I_{L2} at t_2. The magnitude of the inductor current during mode 2 operation is expressed as

$$I_{L2pk} = \frac{V_i}{2L}(d_2 - d_1)T_s + I_{L1pk}. \tag{3}$$

Mode 3: when S_2 is also turned off at t_2, the inductor current starts decreasing and reaches zero at the instant d_xT_s.

The magnitude of the inductor current in mode 3 operation is expressed as

$$I_{L2pk} = \frac{2V_i - V_o}{4L}d_xT_s. \tag{4}$$

Mode 4: the equivalent circuit of the proposed converter in this mode is shown in Figure 3(d). Since the inductor current reached zero state, the load current is supplied by the capacitor C_o.

From (9) and (10), dx can be calculated as

$$d_x = \frac{2V_i(d_1 + d_2)}{2V_i - V_o}. \tag{5}$$

The average current of capacitor C_o is expressed as

$$I_{\mathrm{Co}} = \frac{1}{2}d_x I_{L2} - I_o. \tag{6}$$

From Equations (4), (5), and (6) the expression for I_{Co} can be found as

$$I_{\mathrm{Co}} = \frac{V_i^2(d_1 + d_2)^2}{2V_i - V_C}\frac{T_s}{2L} - \frac{V_{\mathrm{Co}}}{R}. \tag{7}$$

Solving Equation (7), the DCM gain of the proposed converter is derived as

$$M_{\mathrm{DCM}} = 1 + \sqrt{1 + \frac{(d_1 + d_2)^2}{2\tau_L}}, \tag{8}$$

where $\tau_L = L/RT_s$ is the inductor time constant.

3.2. Boundary Condition Operation. The boundary condition for the proposed converter is determined by considering the CCM and DCM voltage gains are equal.

Therefore,

$$M_{\mathrm{DCM}} = M_{\mathrm{CCM}}. \tag{9}$$

By substituting Equations (1) and (8) in (9), the time constant of the inductor current at the boundary for the proposed converter is obtained
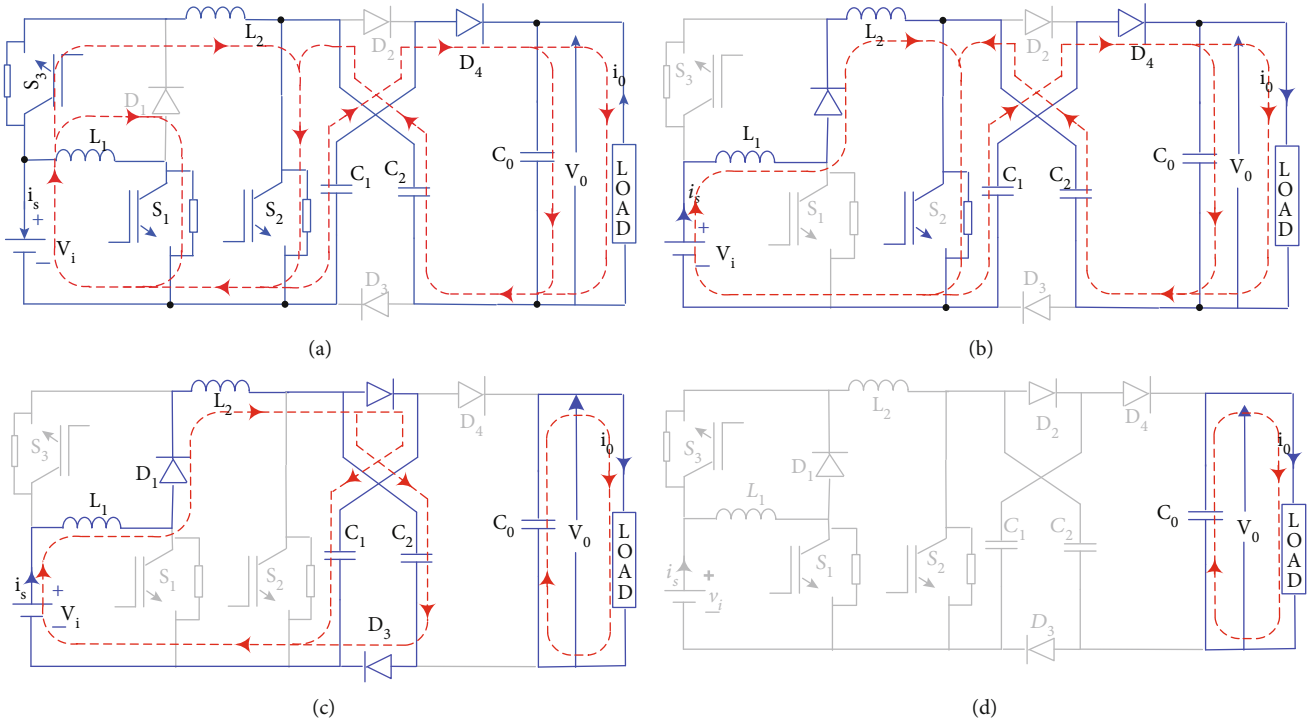
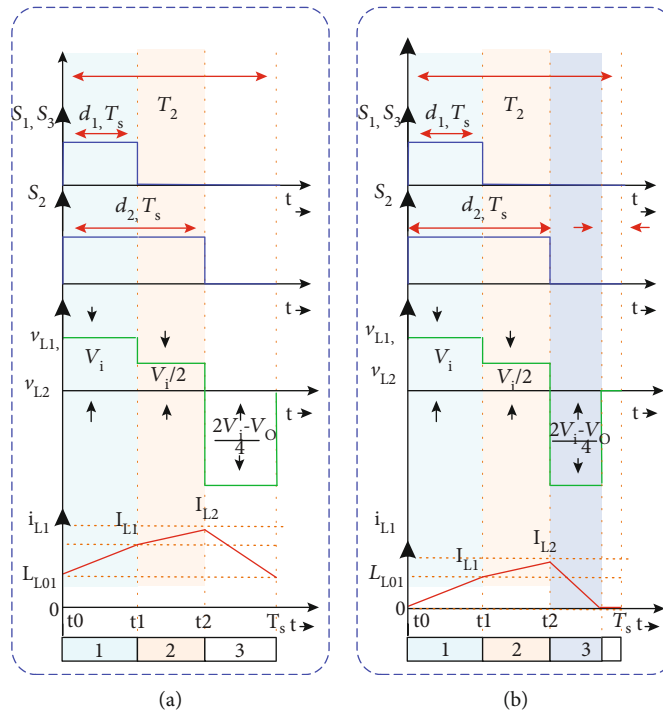FIGURE 3: Equivalent circuit of the proposed converter: (a) mode 1, (b) mode 2, (c) mode 3, and (d) mode 4.

FIGURE 4: Analytical waveforms of the proposed converter. (a) CCM and (b) DCM.

$$\tau_{\text{LB}} = \frac{(d_1 + d_2)(1 - d_2)^2}{8(1 + d_1)}. \tag{10}$$

The variation of the time constant of the inductor τ_{LB} with respect to the duty cycle variation is depicted in

Figure 5. The margins of CCM and DCM operation for the proposed converter are clearly shown.

3.3. Analysis of Dc-Voltage Gain and Converter Efficiency with Parasitic Elements.
In this section, the effect of parasitic elements on the voltage gain and the efficiency of the
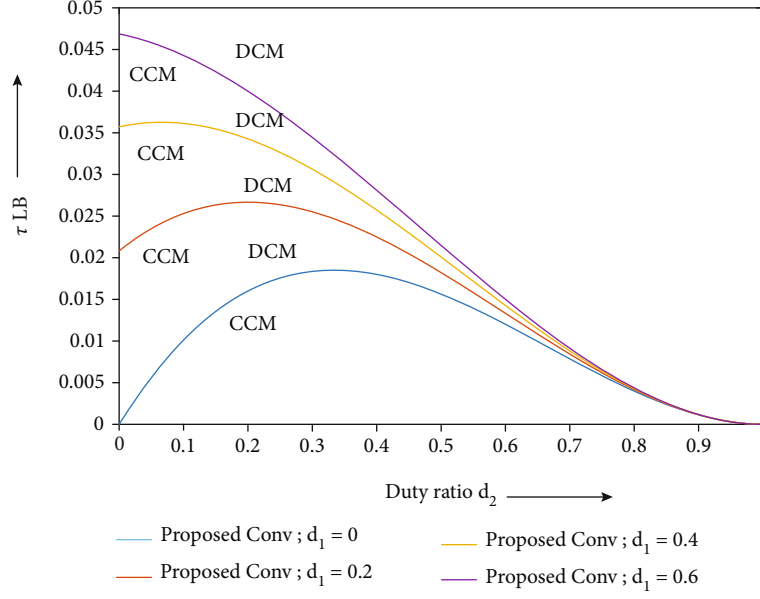
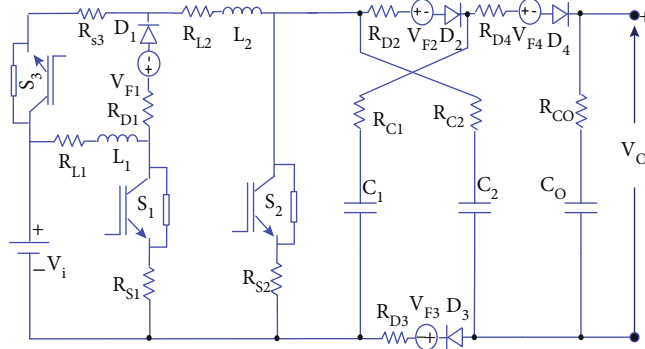FIGURE 5: Boundaries of the proposed high-gain DC-DC converter.

FIGURE 6: Equivalent circuit of the proposed converter with parasitic elements.

proposed converter is discussed. Figure 6 shows the equivalent circuit of the proposed converter configuration with the presence of parasitic elements. The internal resistances of the inductors L_1 and L_2 are represented by R_{L1} and R_{L2}, respectively. The on-state resistances of the switches S_1, S_2, and S_3 are represented by R_{S1}, R_{S2}, and R_{S3}, respectively. The internal resistances and the forward voltages of the diodes D_1, D_2, D_3, and D_4 are represented as R_{D1}, R_{D2}, R_{D3}, and R_{D4} and V_{F1}, V_{F2}, V_{F3}, and V_{F4}, respectively. Series equivalent resistances of the capacitors C_1, C_2, and C_o are shown as R_{C1}, R_{C2}, and R_{Co}, respectively.

Assuming that the internal resistances of all the diodes are equal to R_D, series equivalent resistance of all the capacitors are equal to R_C, forward voltages of all the diodes are equal to V_F, on-state resistances of all the switches are equal to R_S, and the internal resistances of both the inductors are equal to R_L the output voltage expression of the proposed converter with parasitic elements is derived as

$$V_o = \frac{2(1+d_1)V_i + 2V_F(d_1+d_2-2)}{(1-d_2) - A(R_L/R_o) - B(R_S/R_o) - C(R_D/R_o)}, \quad (11)$$

where

$$A = \frac{4(2d_1^2 - d_1 d_2 + d_1 - 2d_2)}{1-d_2}, B = 4d_1, \text{ and } C$$
$$= \frac{4(d_1^2 + d_1 d_2 + d_1 - d_2)}{1-d_2}. \quad (12)$$

The efficiency of the proposed converter in presence of parasitic elements is expressed as given in

$$\eta = \eta' - \frac{P_S}{P_i}, \quad (13)$$

where

$$\eta' = \frac{1 + (V_F/V_i)((d_1 + d_2 - 2)/(1+d_1))}{1 - A(R_L/R_o)(1/(1-d_2)) - B(R_S/R_o)(1/(1-d_2)) - C(R_D/R_o)(1/(1-d_2))}. \quad (14)$$

Efficiency of the converter in presence of parasitic elements is plotted and is given in Figure 7. The values of
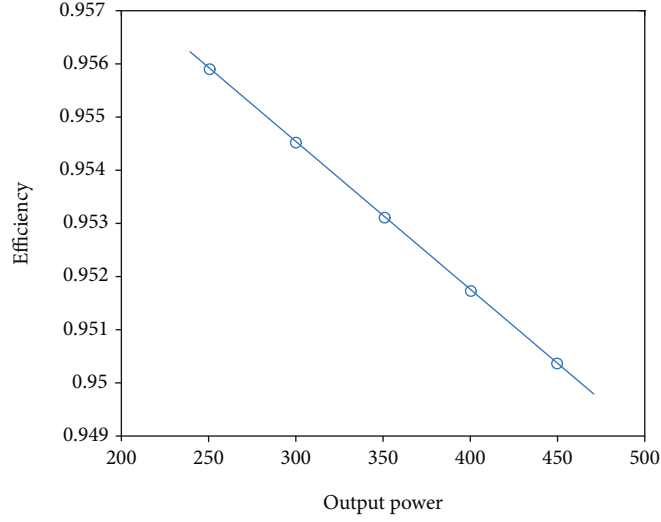
FIGURE 7: Efficiency vs. output power with parasitic elements.

TABLE 1: Performance comparison of proposed and other existing converter topologies.

Topology	Proposed converter	Conventional boost converter	SEPIC converter	SC-boost [13]	Converter [12]	Converter [25]	Converter [24]	Converter [26]
Voltage gain	$2(1 + d_1/1 - d_2)$	$1/1 - d$	$d/1 - d$	$2/1 - d$	$2/1 - d$	$3d/1 - d$	$2d/1 - d$	$(d/1 - d)^2$
Switches	3	1	1	1	2	1	1	1
Diodes	4	1	1	3	3	3	2	5
Capacitors	3	1	2	3	3	6	3	3
Inductors	2	1	2	1	2	4	2	3
Total device count	12	4	6	8	10	14	8	12
Voltage stress on switches	$V_o/2$	V_o	V_o/d	$V_o/2$	$V_o/2$	$V_o/3d$	$V_o/2d$	V_o/d^2
Continuous input current	Yes	Yes	Yes	Yes	Yes	Yes	No	Yes

various parameters are taken as follows: $V_F = 0.74\,V$; $R_L = 0.01\,\Omega$; $R_S = 0.027\,\Omega$; $R_D = 0.0177\,\Omega$. From the graph, it can be observed that the efficiency of the converter in presence of parasitic elements is varying between 95% and 95.65%.

The switching loss is given in

$$P_S = V_i I_S (t_r + t_f) f_s. \tag{15}$$

The input power is given in

$$P_i = \frac{M_{\text{IDEAL}} V_i V_o}{R_o}. \tag{16}$$

The constants A, B, C, and D are same as described above in Equation (11).

4. Analysis of Voltage Stress and Current Stress

4.1. Voltage Stress Analysis. The voltage stress across the three switches S_1, S_2, and S_3 during off state are given in Equations (17), (18), and (19), respectively.

$$V_{\text{SW1}} = \frac{2V_i + V_o}{4}, \tag{17}$$

$$V_{\text{SW2}} = \frac{V_o}{2}, \tag{18}$$

$$V_{\text{SW3}} = \frac{2V_i - V_o}{4}. \tag{19}$$

The voltage stress across the various diodes during reverse biased condition are given as follows:

$$V_{D1} = -V_i,$$
$$V_{D2} = V_{D3} = V_{D4} = \frac{-V_o}{2}, \tag{20}$$

where V_{D1}, V_{D2}, V_{D3}, and V_{D4} are the voltages across the diodes D_1, D_2, D_3, and D_4, respectively, during the reverse biased condition.

4.2. Current Stress Analysis. The maximum current flowing through the various components of the proposed converter

is determined by applying Kirchoff's Current Law (KCL) during various modes of operation. From Figures 3(a)–3(c), the current through the inductors L_1 and L_2 is derived as

$$I_{L1} = I_{L2} = I_o \frac{2 + d_1 - d_1^2}{1 - d_2}. \tag{21}$$

In the same way, the current through the switches S_1, S_2, and S_3 are derived as

$$I_{SW1} = I_{SW3} = I_o \frac{1 + d_1}{1 - d_2}, I_{SW2} = 2I_o \frac{1 + d_1}{1 - d_2}. \tag{22}$$

Similarly, the current through the diodes D_1, D_2, D_3, and D_4 are derived as

$$I_{D1} = 2I_o \frac{1 - d_1^2}{1 - d_2},$$
$$I_{D2} = I_{D3} = I_o \frac{1 + d_1}{1 - d_2}, \tag{23}$$
$$I_{D4} = I_o \frac{1 + d_1}{1 - d_2}.$$

5. Design and Selection of Components

5.1. Inductor Design. The minimum value of inductance for both the inductors L_1 and L_2 are determined using

$$L_1 = L_2 = \frac{V_i d}{\Delta i_L f_S}, \tag{24}$$

where Δi_L is the ripple current and is generally taken as 10% of the load current and f_S is the switching frequency equal to 50 KHz.

5.2. Capacitor Design. The value of capacitors C_1, C_2, and C_o are determined using

$$C_1 = C_2 = C_o = \frac{P_o}{V_o \Delta V_C f_S}, \tag{25}$$

where ΔV_C is the ripple voltage and is usually assumed as 2% of the load voltage and P_o is the load power.

6. Performance Comparison

This section analyses the comparative performance of the proposed converter and the other recent converters reported in the references, i.e., [12, 13, 24–26], and the conventional boost and SEPIC converters. Detailed comparison of the proposed converter and the above converters is presented in Table 1. The plot of duty ratio versus the voltage gain of these converters is shown in Figure 8. A fixed duty ratio of 0.4 is assumed as d_1 for the proposed converter. This plot clearly illustrates that the voltage gain attained by the proposed converter is higher compared to the other seven con-
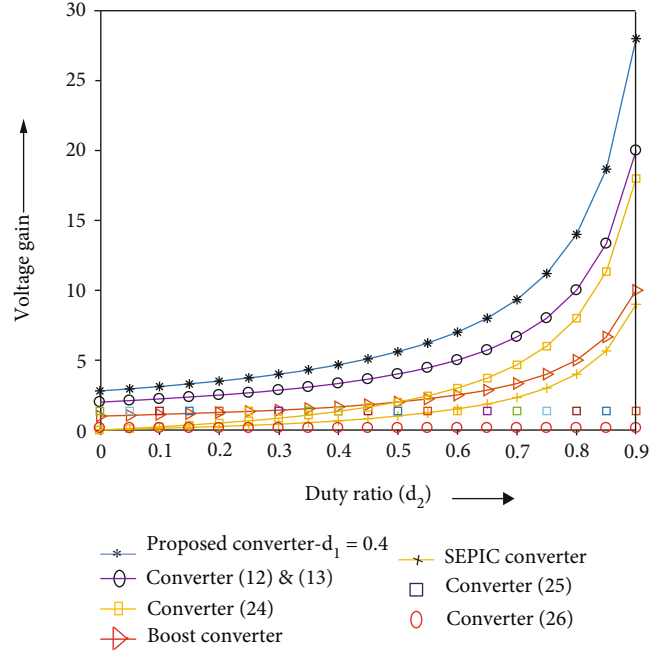

FIGURE 8: DC-voltage gain vs. duty ratio of the proposed converter and the compared converters.

TABLE 2: Simulation parameters.

Parameter	Value
Input voltage	48 V
Resistance of load	75 ohms
Frequency	50 kHz
Inductors L_1 and L_2	0.5 mH
Capacitors C_1, C_2, C_o	250 μF
Duty cycle for S_1 and S_3	40%
Duty cycle for S_2	80%

verters. It can be observed that the proposed converter attains a gain of higher value at the lowest duty ratio d_2, whereas the other reported converters achieves the similar gain with higher duty ratio.

From Table 1, it is clearly noted that the switches in the proposed converter are subjected to a minimum voltage stress compared to the other converters reported. In conventional boost converter, the voltage stress across the switch is equal to the output voltage. So higher rating switch is needed. Even though the number of components used in the proposed converter seems to be slightly higher, it is of comparable value with the total component count in the recently reported converters. The increase in component count in the proposed converter is due to the use of cross-connected capacitor structure in the circuit for doubling the output voltage. The proposed converter shows a continuous input current which is most preferable for solar PV applications. Therefore, the proposed converter shows better performance than the reported converters.
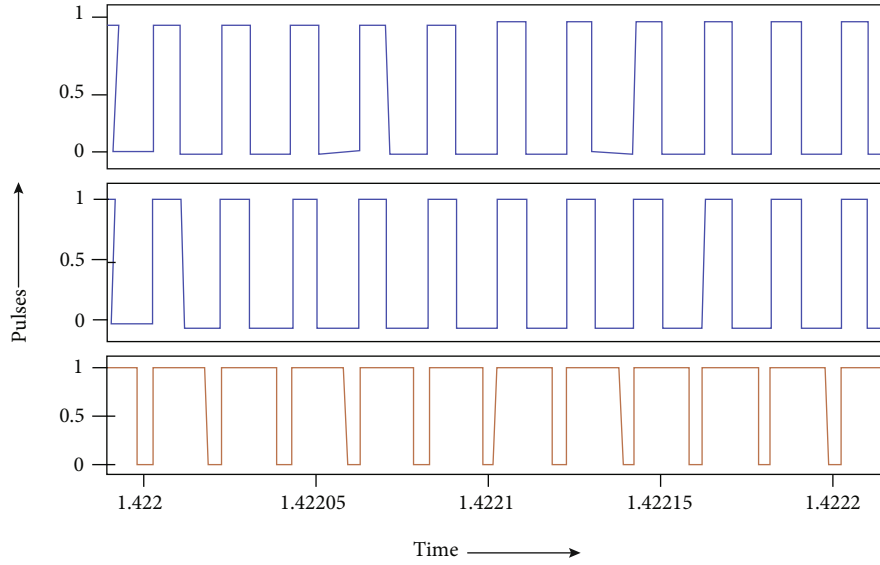
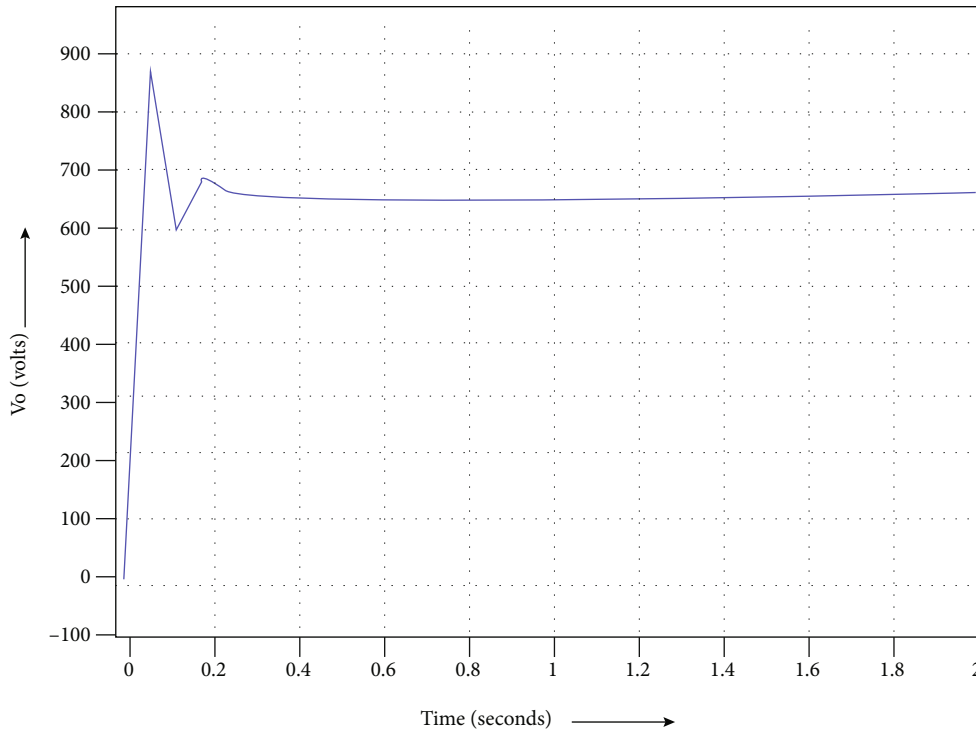FIGURE 9: Switching pulses for S_1, S_3, and S_2.

FIGURE 10: Output voltage of the proposed converter.

7. Results and Discussion

Simulation of the proposed converter has been carried out using MATLAB/Simulink platform. Converter parameter values taken for simulation are given in Table 2. Input voltage is taken as 48 V and the load resistance is 75 ohms. Various parameters of the proposed converter are measured, and the results are produced in this section. Waveforms of various parameters were observed and presented. Figure 9 shows the pulses applied to the switches. Duty ratio is taken

as 40% (d_1) for switches S_1 and S_3 and is 80% (d_2) for S_2. Figure 10 shows the output voltage and is observed as 670.5 V. Therefore, the gain of the proposed converter is 13.97 and is closely matches with its theoretical value.

Figure 11 shows the voltage stress appearing across the switches in the proposed converter. Figure 12 shows the voltage across the inductors L_1 and L_2. Both the inductors are charged to a voltage equal to input voltage of 48 V during mode 1. In mode 2, the voltage across the inductors is equal to half of the input voltage 24 V. During mode 3, when the
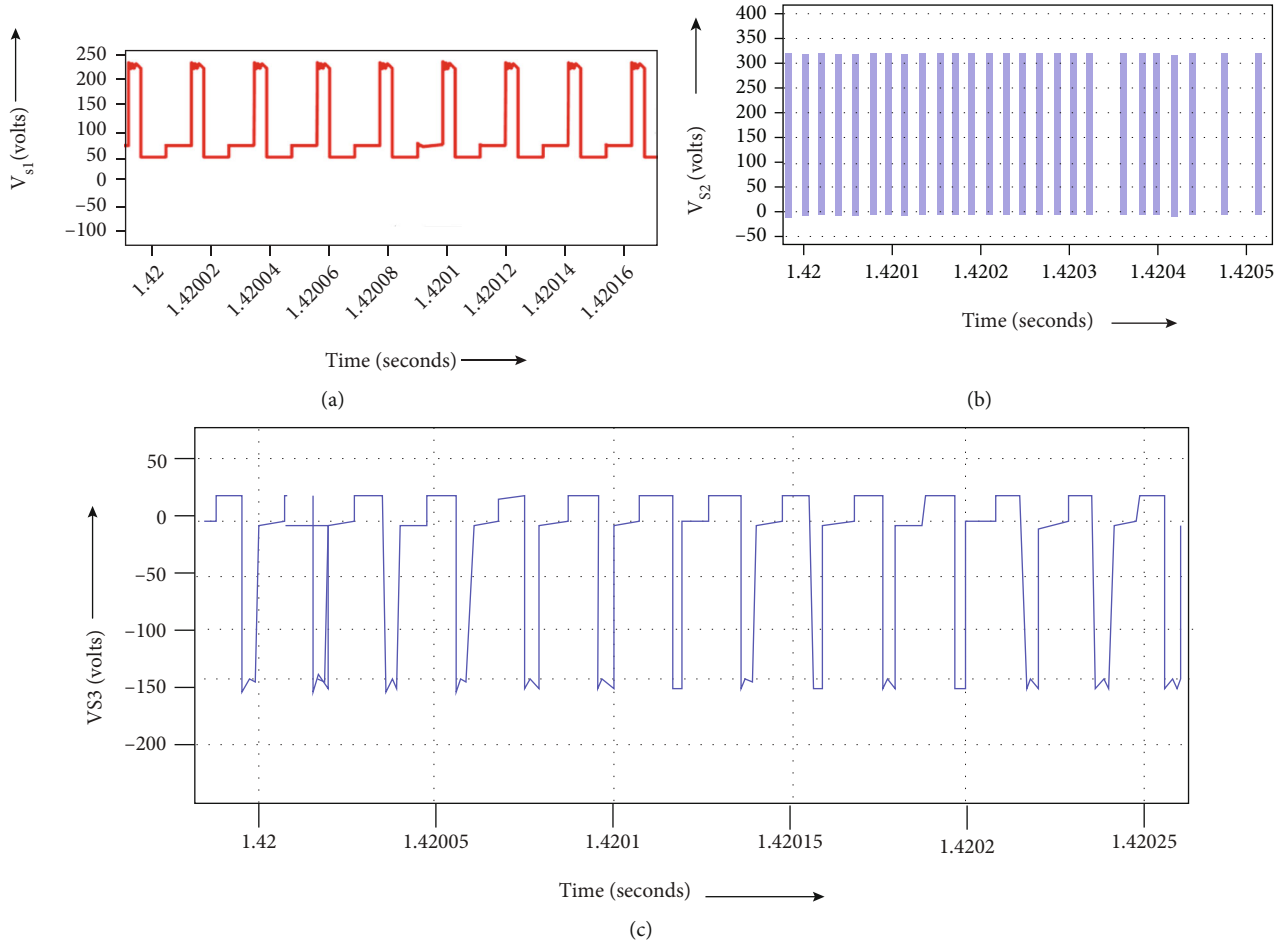
(a)

(b)

(c)

FIGURE 11: Voltage stress across the switches (a) S_1, (b) S_2, and (c) S_3.
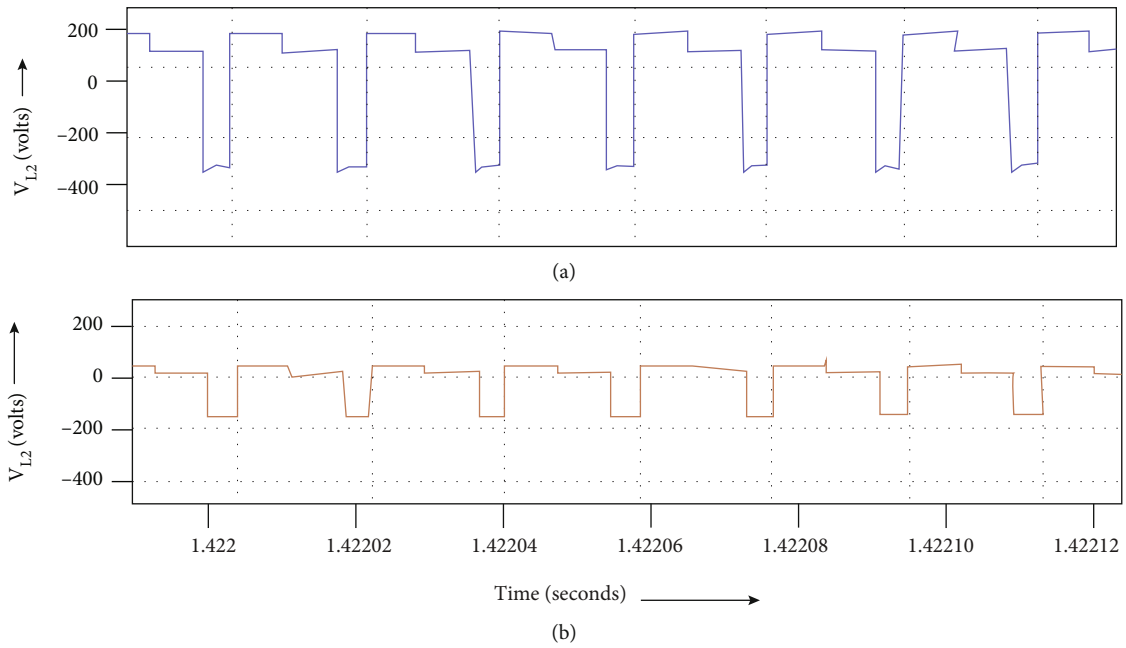

(a)

(b)

FIGURE 12: Voltage across the inductors (a) L_1 and (b) L_2.

TABLE 3: Comparison of theoretical and simulation results.

Parameters	Theoretical value	Simulated value
Voltage gain	14	13.97
Output voltage	670 V	670 V
Voltage stress across switch S_1	191.5 V	191.7 V
Voltage stress across switch S_2	335 V	335.4 V
Voltage stress across switch S_3	-143.5 V	-143.6 V

switch S_2 is turned off, the inductor discharges the stored energy, and the voltage across each inductor is observed as -143.5 V. Voltage stress across the switch S_2 is measured as 335.4 V which is half of the output voltage ($V_o/2$). Voltage stress across the switch S_1 is measured as 191.7 V. Voltage stress across the switch S_3 is measured as -143.6 V. This validates the theoretical performance calculations.

Comparison of the simulated results and theoretical analysis with respect to various parameters is done and given in Table 3. From this, it is observed that both the results closely match which validate the performance of the proposed converter.

8. Conclusions

In this paper, a high step-up nonisolated DC-DC converter was proposed, analyzed, and validated through the simulation results. The proposed converter used a crossconnected capacitor structure which doubled the output voltage of the converter, and hence, the voltage gain is also doubled. The proposed converter was operated with $d_1 = 0.4$ and $d_2 = 0.8$, and the voltage conversion ratio was theoretically calculated as 14. Also, the highest value of voltage across the switch is half of the output voltage, and therefore, the switching losses are reduced. Theoretical analysis was done in CCM, DCM, and BCM using the analytical waveforms. Comparative performance analysis was made with the recently reported converters and presented in the paper. Comparison of the voltage gain is done through the gain plot also. Comparative analysis shows that the proposed converter has a better performance than the other reported converters. The performance of the proposed converter was analyzed in presence of parasitic elements, and the expressions for output voltage and efficiency were derived. Finally, the simulation results and waveforms were presented to validate the proposed converter. Comparison of theoretical and simulation results is executed which validates the working of the proposed converter. Therefore, the proposed converter is best suitable for grid connected as well as for standalone solar PV applications.

Data Availability

Data will be provided on request.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

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