

Weighted Random Pattern Generator by Using BIST

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Abstract: In Built-In Self-Test (BIST), test patterns are generated and applied to the circuit-under-test (CUT) by on-chip hardware; minimizing hardware overhead is a major concern of BIST implementation. In pseudorandom BIST architectures, the test patterns are generated in random nature by Linear Feedback Shift Registers (LFSR). A System-on-Chip (SoC) is the integration of all components of an electronic/computing system on a single integrated circuit. This paper presents a novel test pattern generation technique called BIST. As the complexity grows, testing is becoming one of the most significant factors that contribute to the final product cost. The established low-level methods for hardware testing are not any more sufficient and more work has to be done at abstraction levels higher than the classical gate and register-transfer levels. This thesis deals with testing and design for testability of modern digital systems. This process is performed BY Pseudo-random testing is an attractive approach for BIST. A linear feedback shift register (LFSR) can be used to apply pseudo-random patterns to the CUT. An LFSR has a simple structure requiring small area overhead. Moreover, an LFSR can also be used as an output response analyzer thereby serving a dual purpose. BIST techniques such as circular BIST and BILBO registers make use of this advantage to reduce overhead. **Results and Discussions:** Simulation results prove that this technique has reduction in power consumption and high fault coverage with minimum ***** of test patterns. The results also show that it reducing the testing effort for modern SoC designs.

Keywords: ATPG -Automatic Test Pattern Generation, BIST-Built In Self-Test, CUT -Circuit Under Test, LFSR –Linear Feedback Shift Register, MISR (Multiple Input Signature Register).

1. Introduction

A System-on-Chip (SoC) increasing capacity of system integration in modern semi-conductor processes, reduced time-to-market requirements, and decreasing system costs make multi core systems and systems-on-chip implementations as new design paradigms in integrated circuit design. A typical SoC includes components such as volatile memory systems, non-volatile memory systems, digital signal processors, microprocessors, mixed signal circuits, logic circuits and buses. Testing is checking the quality, performance, reliability and functionality of the system before actually using it. Once the designed circuit is manufactured, the circuit needs to be tested to check if it is functioning properly and if it meets the specifications. Test vectors are used to ensure the circuit functions properly. The main issues in testing of cores are the design and development of core-level test, core test access and core test wrapper. The below figure shows how the cores are tested in a system

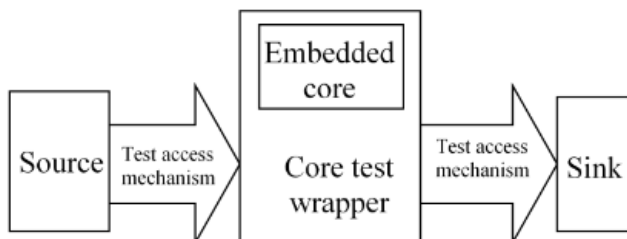


Figure: Testing of Embedded Cores

The persistent growth of mobile computing is driving an increasing need to manage power consumption within semiconductor devices. This has significant implications on the design and test of these devices. Low-power requirements affect test in two separate ways. First, it's

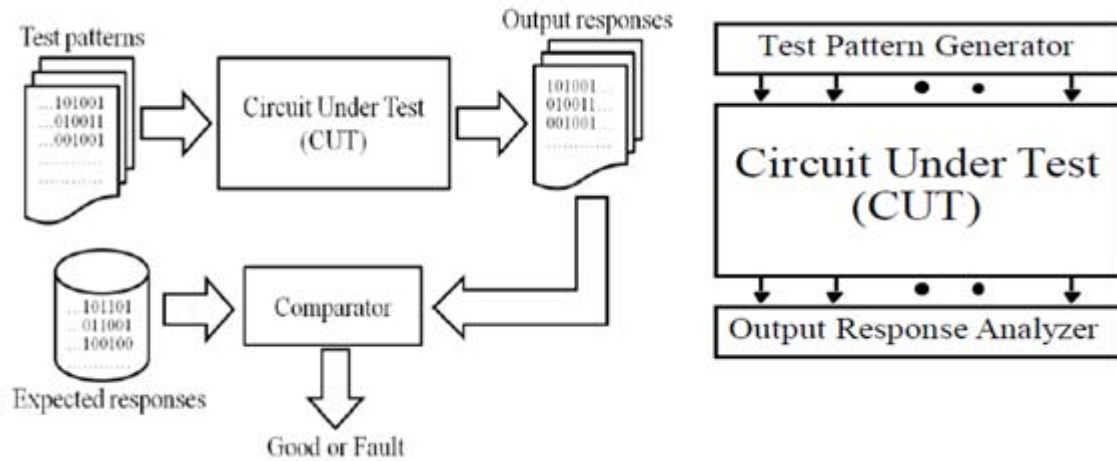
important to ensure that any functional power constraints are met (or at least adequately managed) during test execution. Second, it's necessary to ensure that a test solution is compatible with whatever low-power design techniques are being used. This is accomplished by generating the scan test patterns in such a way as to control the ***** of 1 to 0 and 0 to 1 transitions within each pattern. The transition frequency corresponds directly to circuit toggle activity and thus to average power. Each PRPG output produces a stream of pseudo-random bits. These bit streams are fed into a phase shifter to produce a much larger ***** of pseudo-random bit streams to feed each of the individual scan chains within the circuit under test.

2. Literature Review

what is bist

BIST-based (Built-In Self Test) field test is a promising way in guaranteeing the reliability of the circuit because it can detect the aging-induced faults during circuit operation. In the manufacturing process of VLSI, process variations such as impurities in wafer material and chemicals, dust particles or in the projection system, etc., can produce physical defects on the chip. Typical defects are broken conductors, missing contacts, bridging between conductors and many other phenomena that can make the chip fail. Since defects produced during manufacturing process are unavoidable, as a result, a fabricated chip may be non-conformance to the specification decided by the designer that is faulty and cannot be shipped to the market. In order to find the defect-free chip, test is required. The below figure illustrates the basic principle of VLSI testing. A set of binary stimuli (test patterns) is applied to the inputs of circuit under test (CUT), and compares the output responses with the expected

responses decided by the designer. The circuit is considered to be good if the responses match.



The above figure is a block diagram showing the architecture for BIST. The circuit that is being tested is called the *circuit-under-test (CUT)*. There is a *test pattern generator* which applies test patterns to the CUT and an *output response analyzer* which checks the outputs. The test pattern generator must generate a set of test patterns that provides a techniques such as circular BIST and BILBO registers make use of this advantage to reduce overhead. high fault coverage in order to thoroughly test the CUT.

Pseudo-random testing is an attractive approach for BIST. A linear feedback shift register (LFSR) can be used to apply pseudo-random patterns to the CUT. An LFSR has a simple structure requiring small area overhead. Moreover, an LFSR can also be used as an output response analyzer thereby serving a dual purpose. BIST .

There are limits on the *test length*, which is the ***** of pseudo-random patterns that can be applied during BIST. One limit is simply the amount of time that is required to apply the patterns. Another limit is the fault simulation time required to determine the fault coverage. A third limit is heat dissipation for an unpackaged die. Thus, in order for pseudo-random pattern testing to be effective, high fault coverage must be obtained for an “acceptable” test length. What is considered acceptable depends on the particular test environment.

This paper presents architecture of a low power pseudo random test pattern generator with programmable features that allow selection of wide range of user-defined toggling rates. An *n*-bit PRPG connected with a phase shifter feeding scan chains forms a kernel of the generator producing the actual pseudorandom test pattern. A linear feedback shift register or a ring generator can implement a PRPG. More importantly, however, *n* hold latches are placed between the PRPG and the phase shifter. Each hold latch is individually controlled via a corresponding stage of an *n*-bit toggle control register.

As the BIST power consumption can easily exceed the maximum ratings when test-ing at speed, scan patterns must be shifted at a programmable low speed, and only the last few cycles and the capture cycle are applied at the maximum frequency. In the burst-mode approach typically five

consecutive clock cycles are used. The first four cycles serve shifting purposes, whereas the last one is designated for capture. The objective is to stabilize the power supply before the last shift and capture pulses are applied, which are critical for at-speed tests.

Why Test?

Microelectronics is synonymous with making products smaller, faster, and denser. Functionality that 10 to 20 years ago now literally fits in the palm of your hand. Today's designers using Design Automation (DA) with the latest semiconductor technology are accelerating this

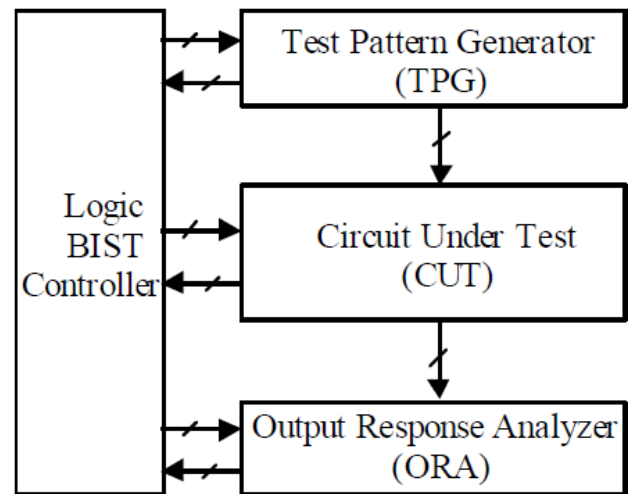


Figure 1: Typical BIST system

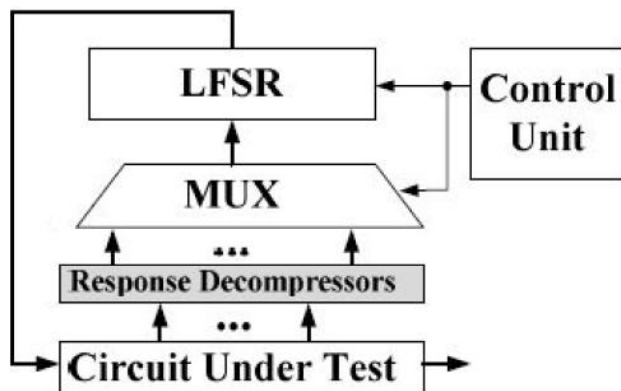
rate of integration even more. This combination of increased functionality with the faster, denser, and smaller packaging brings up a dilemma: it is becoming more difficult to access, test, and verify chip and system functionality using traditional external equipment and instruments.

3. Proposed Design

In this paper have to developed a routing-efficient implementation of an internal-response-based BIST. A net sharing algorithm and a response decompression method are together employed to significantly reduce the total ***** of internal nets required for the BIST scheme. The net

sharing algorithm determines a minimal set of internal nets that can be shared by the BIST input ports. For those input ports that cannot share internal nets, the required input values can be provided by employing a (set of) response decompressor(s) to manipulate a subset of the internal nets. Experimental results show that our methods require only a small fraction of internal nets and small area overhead to achieve complete testing.

A full toggle pattern may consume more power at every pattern it generated and trends to rise in power dissipation. Apart from these high switching activity can result in failure of chips functionality during test phase. Intermediate test vectors that increase the correlation between adjacent bits loaded in the scan chains of LOS schemes but the toggling result in high power consumption.



Though the result show improvement in reducing power consumption but the test pattern generated are repeated since there is knowledge of the chains. In the author presents bit swapping in LFSR which reduce power consumption and cost of testing. But during swapping the problems comes when the n is even the swap chain resets to zero and start again. In the testing Power-Aware At-Speed Scan Test Methodology for Circuits with Synchronous Clocks is presented with modifying the previous works. A low transition in LFSR to reduce the power consumption is presented in by minimizing the test patterns which increases the cost of testing. In a review on existing power testing is presented in which low-power testing scheme is divided into the following two categories. Low - Power Testing Techniques for External Testing (B) Low - Power Testing Techniques for Internal Testing. A new dual speed LFSR is presented in which works on either in slow or fast mode based upon the requirement. In a cost effective PRNG is presented, Generation of pseudo-random numbers using Cellular Automata (CA) for Built-In-Self-Test (BIST) applications has been emphasized. From the work and research BIST strongly emphasizing a low power and low cost BIST architecture while generation. The solution in [1] modifies the internal structure of traditional LBIST LFSRs to generate intermediate test vectors that increase the correlation between adjacent bits loaded in the scan chains of LOS schemes but the toggling result in high power consumption.

Application of Deterministic Logic BIST on Industrial Circuits:

Modern IC design technologies and the introduction of systems-on-chip (SOC) using embedded cores allow integrating more and more gates on a single IC. To test such large ICs, a huge amount of test patterns is required. In addition, these large ICs show a sharp increase in the ratio of number of gates per pin. Transporting lots of test data over a limited amount of IC pins is causing a bandwidth problem, which leads to increasing test time and the use of expensive test equipment. Built-in self-test (BIST) is becoming an attractive alternative, since it solves the bandwidth problem by eliminating the need for external testing.

For industrial applications, logic BIST synthesis is currently supported by a few commercially available CAD tools [MNBB98, HETH99] based on the STUMPS architecture [BaMc84] for pseudo-random testing. Test patterns are generated and responses are compressed using linear feedback shift registers (LFSRs).

4. Conclusion

This paper has proposed a low-power test pattern generation method that could be easily implemented by hardware. It also developed a theory to express a sequence generated by linear sequential architectures, and extracted a class of SoC sequences named MSIC. Shift power is test coverage effects in CUT controller and tester cover a negligible portion of chip area, the burden of area overhead can be avoided.

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