Pulse Power Supply With Faster Response and Low Ripple Current Using Inductive Storage and Interleaving Technology

Zhibao Yuan and Haiping Xu

***Abstract*—Switched mode pulse power supply is a promising technique for high-power quasi-continuous laser driver. Contrast to lossy linear laser drivers, switched mode laser drivers can achieve higher efficiency. However, many challenges have been proposed, such as fast pulse edge, low current ripple. This paper proposes a multiphase interleaved pulse power supply with energy recovery and inductive storage (MIEF-PPS). The basic concept of the topology is the inclusion of a multiphase converter with pulse forming circuits to the converter system, which decouples the current slew rate and current ripple. Using an inductive storage technology and pulse forming circuits, a shorter pulse current rising time is obtained. The inductor energy is fed back to the input source not discharged to the load, resulting in a fast pulse trailing edge and energy saving. Thus the pulse current response observed when using this proposed technique is found to be much faster when compared to the conventional interleaved buck driver. Moreover, a pre-charge method is proposed to overcome the challenge of digitally controlling the inductive storage. The proposed topology was simulated in MATLAB/Simulink and validated against the experimental results of a laboratory prototype, 360 W dual-interleaved pulsed power supply.**

***Index Terms*—Energy recovery, fast response, multiphase interleaved, precharge control, pulse power supply.**

I. Introduction

HIGH-POWER semiconductor laser arrays are vital in many fields, such as medical, industrial, and military fields, because of their advantages such as having a small volume, low weight, high efficiency, good beam quality, high reliability, and long lifespan [1]–[4]. A laser diode (LD) is a current-driven device and has similar characteristics to a light-emitting diode. From the voltage-current (V-I) characteristic and the characteristic curve of the optical power and injection current (P-I) of a laser diode [5], [6], it is sensitive to current variation, and small changes in the current lead to significant changes in the output optical power, resulting in the expansion of the spectral linewidth of the output wavelength; therefore, a small injection current ripple is required. In general, LD can function in continuous wave and pulse modes. In the pulse mode, the forward peak current of a high-power laser diode can reach over 100 amperes with a pulse duty cycle of less than 0.1 in most cases, which are generally used in peak power ranging and all solid state laser pump source [1]. As the optical output power and the conversion efficiency are increased along with injection current, by the same output optical power, the smaller the duty cycle of the pulse laser, the higher efficiency will be achieved [7]. Another characteristic is that pulse lasers produce minimal heat; as a result, the threshold current of the P-I characteristic curve reduces and the slope efficiency increases [8]. Thus, operating LD in a pulse mode is recommended and offers a chance to exploit its performance. Generally, the output pulse current rising edge of high-power quasi-continuous pulse power supply is steep and a short time within 20 μs is always required [9], [10]. The development of laser power [11], has enhanced the demand for pulse power supply (PPS). Being one of the critical technologies of a laser system, the stability, pulse rise time, efficiency, and power density of the PPS affect the overall performance of a laser system. Therefore, the PPS has to be carefully considered.

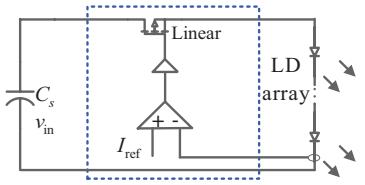

Fig. 1. Typical linear laser driver circuit.

In general, semiconductor laser PPS drivers are classified into two types: linear drivers and switched mode drivers. Drivers with linear regulators [12]–[14] have simple structures and a low cost and generate fast enough rising and falling times, as shown in Fig. 1. However, they suffer from lower electrical efficiency owing to power loss at the linear stage, especially in high power applications. In contrast, switched mode drivers achieve higher electrical efficiency; however, they suffer from longer rising and falling times and overshoot owing to LC filters and control bandwidth [15]. Some efforts

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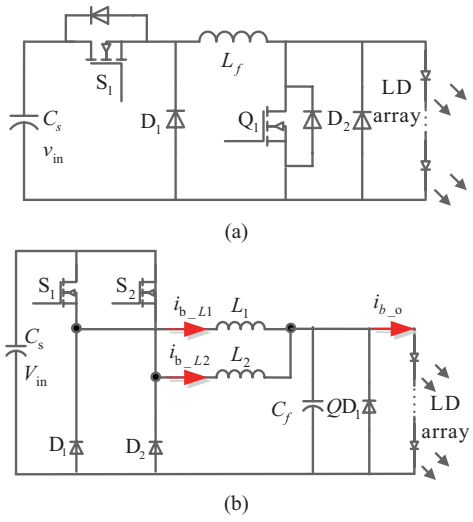


Fig. 2. Switched mode laser driver circuits. (a) Inductive storage driver circuit [16]–[18]. (b) Multiphase interleaved buck type circuit [9], [19].

to improve switched mode power supply have been undertaken in [9], [16]–[19]. Typically, a buck current source is simple and easy to implement [20], [21], but the current rising edge is limited by the circuit parameters, and the current ripple and pulse edge response speed are compromised. To improve the rising edge whilst maintaining a low current ripple, a switch shunt concept with higher inductance was adopted named inductive storage topology and present in [16]–[18], as shown in Fig. 2(a). The semiconductor switch is connected to a load in parallel to realize fast switching of the load and obtain a short duration of the pulse waveform. However, due to the low energy storage density of the inductor and a single-stage converter, a lower power density is achieved in high-power applications. To generate a low current ripple, basic buck type converters with a high-order passive filter at the output are studied in literature [15]. However, this approach is constrained because it offers a bulky solution and leads to a worse dynamic current response. Some active ripple filter topologies have been presented in [22], [23]. In [22], the current ripple is measured from the inductor and flows opposite to the current into the load. In [23], the shunt switch conducts a low current ripple. However, the power sent to the shunt switch operating in a linear state is sacrifice. In [18], [24], a bidirectional converter replaces the shunt switch in [23] to compensate for the output current ripple, which increases the complexity of the circuit implementation. Another attractive option is to employ a typical multiphase interleaved buck type converter (Fig. 2(b)), with the advantages of a low current ripple, high power density and fast rising time (owing to a lower inductance value) [9], [19]. However, it is equivalent to the buck current source, thus the rising and falling current time are affected by the circuit parameters (inductor value, input/output voltage), making it difficult to achieve a faster rising and falling current edge. Moreover, at the end of the pulse command, the energy stored in the inductors is discharged through the load, which not only increases the pulse falling edge time, but also wastes energy and reduces the efficiency.

Herein, switched mode drivers are studied to overcome rising and falling edge limitations, increase efficiency and maintain a low current ripple [19] for high-power semiconductor laser array drivers. This paper proposes a multiphase interleaved PPS with energy recovery and inductive storage topology (MIEF-PPS). The MIEF-PPS operates in an interleaved pulse-width modulation (PWM) current-loop control under steady-state conditions and its operation changes to the fixed duty cycle control during transient of inductor current. This proposed topology improves the transient response of the multiphase interleaved converter without relying on the low inductance value and the high voltage across the inductors. Further, a digital pre-charge control for the inductor energy storage is also proposed to obtain a fast rising time. Moreover, this topology with energy recovery, improves fast falling time and saves energy. Section II describes the configuration and operation principle of the proposed topology in detail, and a multiphase inductor design process is also briefly presented. The control approach is discussed in Section III. In this section, a digitally pre-charge control and average current sharing method are also presented. Finally, in Section IV, the simulation and implementation of a prototype are described, and some experimentally obtained results are presented, to demonstrate the operation and performance of the proposed topology. Section V presents the conclusions.

II. Circuit Configuration of MIEF-PPS

A. Circuit Configuration

A switched mode driver circuit topology has been evolved, which is depicted in Fig. 3. The proposed topology is derived from interleaved buck converter and the pulse forming concept from the topology of Fig. 2. As shown in Fig. 3, the proposed MIEF-PPS topology consists of N phases of interleaved buck circuits ($D_1 \ldots D_N$, $L_1 \ldots L_N$, $S_1 \ldots S_N$) and pulse forming circuits for inductor storage energy feedback and pulse forming (Q_1, Q_2, D_{q3}, D_{q4}). The three-terminating devices (D_j, S_j, L_j, $j = 1,\ldots,N$) are composed of a basic buck converter and are connected in parallel to meet the requirements of high current and low ripple. In Fig. 3, v_{in} indicates the voltage of storage capacitor C_s and D_{q4} denotes a freewheeling diode to protect the load.

The Q_1 provides a path for the inductive (L_1–L_N) storage, preparing for the pulse current discharge to the load. When the inductors energy storage are filled, it means that the inductor current reaches a given value, which generates a fast rising current edge by turning off Q_1 and turning on Q_2. This means that even with a larger inductance of L_1–L_N, the MIEF-PPS can also has a fast rising current slew. At the end of the pulse, the switch Q_2 is turned off quickly, and the inductor energy is fed back to the input power through the continuation diode D_{q3}, to obtain a fast falling edge. In the flat-top pulse interval, phase shift control maintains a low current ripple. The pulse width and period are determined by the ON and OFF states of Q_1 and Q_2. Small circuit parameter differences (e.g., inductance difference) lead to final inductor branch current differences,

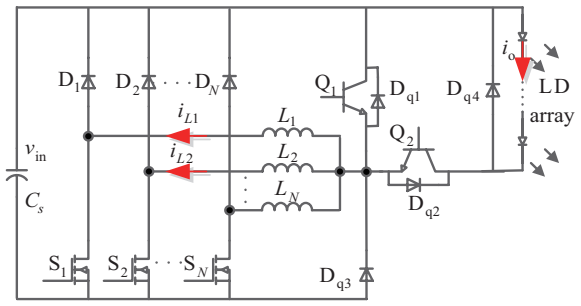


Fig. 3. Proposed MIEF-PPS topology.

but they do not affect the stability of the system for their minor differences. Notably, although the MIEF-PPS can be extended to any phase, parallel multiphase leads to increased circuit complexity and difficulty in control. Moreover, from the perspective of circuit theory, the proposed topology is not limited to the buck circuit, any DC/DC topology operates as a current source can form the proposed MIEF-PPS topology type.

B. Operation Principle

In order to simplify the analysis, this paper adopts the general dual-interleaved energy feedback pulse power supply topology, which analysis results are also applicable to the proposed MIEF-PPS topology. The proposed MIEF-PPS topology is based on the interleaved buck topology; therefore, the gate signals are driven following the buck mode in the flat-top time. In terms of pulse forming, the pulse operation can be strictly divided into two mechanisms, a high switching frequency of S_j and a low switching frequency of switch Q_1 and Q_2. The equivalent operation circuits are shown in Fig. 4. Fig. 5 depicts the key waveforms of the proposed topology during a pulse period. In Fig. 5, the gate signals v_{gS1}, v_{gS2}, v_{gQ1}, and v_{gQ2} correspond to the switches of S_1, S_2, Q_1, and Q_2 respectively, i_{L1} and i_{L2} are the currents of inductors L_1 and L_2, i_o is the pulse load current. Therefore, the overall operation of the proposed MIEF-PPS topology can be summarized as follows:

Stage 1 [t_0–t_1] Inductive Storage In this stage, switches S_1, S_2, and Q_1 are turned on, Q_2 is turned off, and the corresponding equivalent circuit in this mode is shown in Fig 5(a). The inductors L_1 and L_2 are energized by the input voltage source v_{in}, and their currents rise linearly. As Q_2 is in the OFF state, and therefore, there is no current flowing through the load. Considering the inductive parasitic resistance and ignoring other parasitic parameters of the circuit, the inductors charging time of each phase is determined by the following equation:

$$\begin{cases} \dfrac{\mathrm{d}i_{Lj}}{\mathrm{d}t} = \dfrac{v_{in}}{L_j} - i_{L_j} \cdot \dfrac{R_{ej}}{L_j} \\ i_{L_j}\big|_{t=0} = 0 \end{cases} \tag{1}$$

where R_{ej} is the resistance of the inductor L_j (j = 1, 2…). It will enter the next state until the current value of inductor L_j reaches its reference value i_{Lj_ref} at t_1.

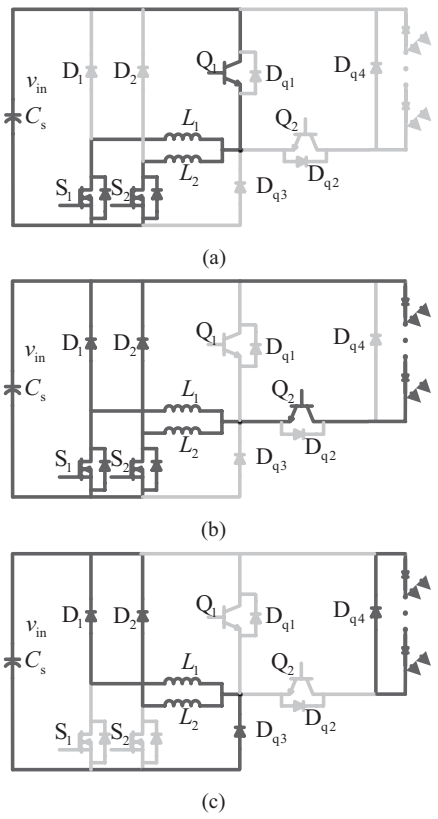


Fig. 4. Equivalent circuits for each stage. (a) Stage 1: inductive storage. (b) Stage 2: pulse forming. (c) Stage 3: energy recovery.

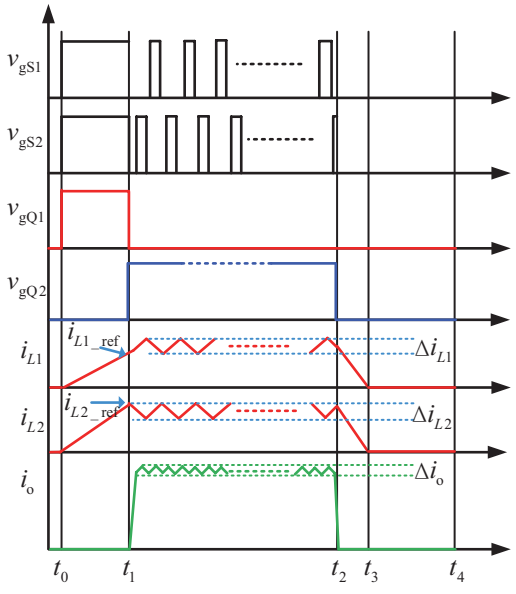


Fig. 5. Key wavefroms during pulse period.

Stage 2 [t_1–t_2] Pulse Forming In this stage, the switch Q_1 is turned off, while switch Q_2 is turned on. At this moment, in the whole stage, the circuit is equivalent to two-phase interleaved buck circuits in parallel, as shown in Fig. 4(b). Switches S_1 and S_2 operate in a high frequency buck mode to maintain

constant inductance current. The two paralleled buck circuits are controlled by the interleaving technology to obtain a low current ripple [25], [26]. The inductor currents are expounded as follows:

$$\begin{cases} \dfrac{\mathrm{d}i_{Lj}}{\mathrm{d}t} = \dfrac{v_{\mathrm{in}} - v_{\mathrm{o}}}{L_j} - i_{Lj} \cdot \dfrac{R_{ej}}{L_j}, \ \mathrm{S}_j \text{ on} \\ \dfrac{\mathrm{d}i_{Lj}}{\mathrm{d}t} = \dfrac{-v_{\mathrm{o}}}{L_j} - i_{Lj} \cdot \dfrac{R_{ej}}{L_j}, \ \mathrm{S}_j \text{ off} \\ i_{Lj}\big|_{t=0} = i_{Lj\_\mathrm{ref}} \end{cases} \tag{2}$$

where v_{o} is the voltage of the load. The load obtains a fast rising current slope with the initial inductor currents and a quick turn on of switch Q_2.

Stage 3 [t_2–t_3] Energy Recovery In this state, all switches are turned off. The remaining energy stored in L_1 and L_2 returns to the capacitor C_{s} through D_1, D_2, and D_{q3}. The residual load energy continues to flow through the freewheeling diode D_{q4}. A fast falling slope is obtained while the switch Q_2 is turned off. The inductor currents are expounded as follows:

$$\begin{cases} \dfrac{\mathrm{d}i_{Lj}}{\mathrm{d}t} = \dfrac{-v_{\mathrm{in}}}{L_j} - i_{Lj} \cdot \dfrac{R_{ej}}{L_j} \\ \dfrac{\mathrm{d}v_{\mathrm{in}}}{\mathrm{d}t} = \dfrac{i_{Lj}}{C_{\mathrm{s}}} \\ i_{Lj}\big|_{t=t_2} \approx i_{Lj\_\mathrm{ref}} \end{cases} \tag{3}$$

Stage 4 [t_3–t_4] Idle State In this state, all switches are turned off and there is no energy in inductors and load, waiting for the next pulse current discharge.

C. Inductor Design

As shown in Fig. 5, the inductor current waveforms are of the pulse current during a pulse period. In stage 2, the phase inductor currents are in continuous conduction mode (CCM). In order to prevent the maximum DC current from causing the core to saturate, this paper mainly considers the flat-top current as the design basis of the inductor. At this stage, the symmetrical phase shift control is used to keep the output pulse current ripple small, and the phase shift duration is calculated from the following equation:

$$\theta = \frac{2\pi}{N} \tag{4}$$

To conduct the analysis, the followings assumptions are made:

1) Every phase is operating in CCM during stage 2;

2) Every phase has the same duty cycle D, inductance L and current ripple Δi_L, $D_j = D_k = D$, $L_j = L_k = L$, $\Delta i_{Lj} = \Delta i_{Lk} = \Delta i_L$, $k = 1, \ldots, N\ (k \neq j)$.

Under the above assumptions, the peak-to-peak value of inductor current Δi_L, is governed by the following:

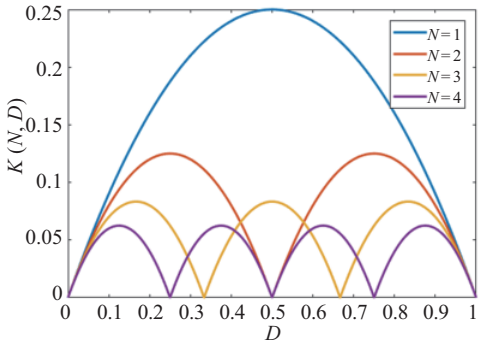


Fig. 6. Normalized coefficient of total current ripple.

$$\Delta i_{Lj} = \Delta i_L = \frac{v_{\mathrm{in}} D\ (1 - D)}{L f_{\mathrm{s}}} \tag{5}$$

It can be seen from (5) that the current ripple is inversely proportional to the inductance. Generally, the larger the inductance, the smaller the current ripple. For interleaved parallel converters, the inductance affects not only the output current ripple but also the power density, so it is especially important to design the inductor practically.

With the above analysis, the inductor design is analyzed in accordance with the multiphase buck converter. For an interleaved buck converter, a simple analytic expression of the total current ripple under CCM is expressed as [27]:

$$\Delta i_{\mathrm{o}} = \Delta i_L \cdot \left(D - \frac{m}{N} \right) \cdot \frac{1 + m - ND}{D(1 - D)} \tag{6}$$

where m = floor (ND), which returns the greatest integer value less than the argument; Δi_{o} is total current ripple. The total current ripple can be further expressed by combining (5) and (6):

$$\Delta i_{\mathrm{o}} = \frac{v_{\mathrm{in}}}{L f_{\mathrm{s}}} \cdot \left(D - \frac{m}{N} \right) \cdot (1 + m - ND) = \frac{v_{\mathrm{in}}}{L f_{\mathrm{s}}} \cdot K\ (D, N) \tag{7}$$

$$K\ (D, N) = \left(D - \frac{m}{N} \right) \cdot (1 + m - ND) \tag{8}$$

$K\ (N, D)$ is defined as the normalized coefficient of Δi_{o} and illustrated in Fig. 6 according to the number of phases N and the duty cycle D.

It shows that $K\ (D, N)$ satisfies the following equation:

$$0 \leqslant K\ (D, N) \leqslant K_{\max}(D, N) \tag{9}$$

where $K_{\max}\ (D, N)$ is the maximum value of $K\ (D, N)$. Moreover, due to the symmetric distribution of the waveform, the number of solutions satisfying the duty ratio at which $K\ (D, N)$ takes the maximum value is equal to the number N of parallel phases. When $K\ (D, N)$ takes the maximum value $K_{\max}\ (D, N)$, the corresponding duty ratio is:

$$D_q = \frac{q - 1}{N} + \frac{1}{2N} \quad q = 1, \ldots, N \tag{10}$$

An expression for the range of inductance values can be obtained from (7)–(10):

$$0 \leqslant L \leqslant \frac{v_{\text{in}} K_{\max}(D_q, N)}{\Delta i_{\text{o}} f_{\text{s}}} \tag{11}$$

Equation (10) gives the range of inductance values that satisfy the symmetric phase shift to eliminate the current ripple. When the parameters such as the number of parallel phases is determined, the inductance value under the working conditions can be found.

Taking the dual-phase interleaved circuit inductor design as an example, the parameters are: $v_{\text{in}} = 50$ V, $f_{\text{s}} = 50$ kHz, $\Delta i_{\text{o}} = 2$ A, and the coefficient $K_{\max}(D_q, N)$ can be obtained by equations (8) and (10), $K_{\max}(D_q, N) = 0.125$. From the (11), the range of inductance under the previous assumptions can be obtained: $0 \leqslant L \leqslant 62.5\ \mu$H. Considering the margin and the actual winding process, the final inductance applied to the subsequent parallel verification experiment is approximately 80 μH.

III. Current Control Schemes

A. Inductive Storage Control

Interleaved circuit design will reduce the inductor's value and its size [25], [26]. Therefore, the inductance of L_1 and L_2 are typically designed to range from tens to hundreds of microhenry which leads to inductive storage control difficulties in stage 1 by adopting digital control, such as average current control and peak current control. For example, if the MIEF-PPS total input voltage was set to a value of $v_{\text{in}} = 50$ V with an inductance $L = 80\ \mu$H, the minimum time required to reach inductor current of $I_{\text{ref}} = 15$ A, is obtained from (1):

$$i_{Lj} = \frac{v_{\text{in}}}{R_{ej}}\left(1 - e^{-\frac{R_{ej}}{L_j}t}\right) \tag{12}$$

By using the first-order Taylor series expansion, the inductor current can be approximately expressed as:

$$i_{Lj} \approx \frac{v_{\text{in}}}{R_{ej}}\left(1 - 1 + \frac{R_{ej}}{L_j}t\right) = \frac{v_{\text{in}}}{L_j}t \tag{13}$$

Using (13), the current rising time would be 24 μs. Thus, the MIEF-PPS would have an inductor charging rate of 0.625 A/μs. This means that if a digital pulse width modulation (PWM) controller is adopted, the switching frequency must be greater than 625 kHz to control the current accurately in one ampere, leading to implementation difficulties. Another consideration is the accuracy of the sampling in the A/D converters of the MCU. Because of the limitation of A/D sampling speed and accuracy, it is difficult for A/D to accurately sample the slope function. Therefore, it is not easy to use the closed-loop controller to control current in State 1 accurately.

To solve the above-mentioned problem, a precharge control called a fixed duty ratio digital PWM control method is proposed to control the inductor charging current approximately accurately. The waveforms of inductor charging current and corresponding PWM gate signal are shown in Fig. 7. The basic concept of the method is to control the inductor current to a reference value I_{ref} by M fixed duty cycles. In Fig. 7, there are two modes in a switching interval.

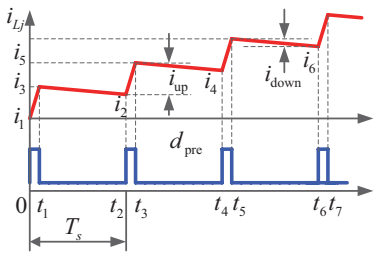


Fig. 7. Ideal inductor current of each phase by pre-charge control.

In mode 1 [0, t_1], switches S_1, S_2, and Q_1 are turned on and inductor currents start to rise with the applied voltage v_{in}.

In mode 2 [t_1, t_2], switches S_1, S_2, are turned off and inductor currents flow through the freewheeling diode D_1 and D_2, respectively.

The duty ratio d_{pre} of S_j gate signal has a relationship with inductor current i_{Lj}, (1) is solved and using a Taylor first-order approximation, (14) can be derived.

$$\begin{cases} \Delta i_{\text{up}} \approx \dfrac{v_{\text{in}}}{L_j} \cdot d_{\text{pre}} \cdot T_{\text{s}} \\ \Delta i_{\text{down}} \approx \dfrac{v_{\text{in}}}{L_j^2} \cdot R_{ej} \cdot d_{\text{pre}} \cdot (1 - d_{\text{pre}}) \cdot T_{\text{s}}^2 \end{cases} \tag{14}$$

where Δi_{up} and Δi_{down} are inductor current increments and decrease respectively in a switching interval. After M switching cycles, the final inductor current can be expounded as:

$$\begin{aligned} i_{Lj\_M} &= M \cdot (\Delta i_{\text{up}} - \Delta i_{\text{down}}) \\ &= M \cdot \frac{v_{\text{in}}}{L_j} \cdot d_{\text{pre}} \cdot T_{\text{s}} \cdot \left(1 - \frac{R_{ej}}{L_j} \cdot (1 - d_{\text{pre}}) \cdot T_{\text{s}}\right) \end{aligned} \tag{15}$$

From (15), Δi_{Lj_M} is always the reference value of inductor current I_{ref}, so we can easily control the inductor charging current by M fixed duty cycle.

B. Interleaved Buck Converter Control

A stable current should be maintained during the flat-top pulse current time (stage 2), so a closed-loop control algorithm is needed to control the current stability. In stage 2, according to the analysis of operating mode, the topology is equivalent to a dual-interleaved buck circuit, which functions in a constant current mode. The conventional buck interleaved control is the output voltage control based on a small signal model [28]–[30]. This paper adopts the average current control method to achieve the output current control.

The control block diagram of the proposed topology is shown in Figs. 7 and 8. It is composed by an open loop control

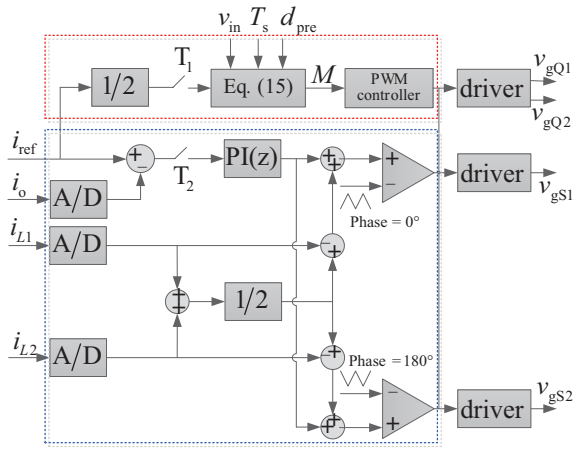


Fig. 8. Diagram of the proposed current control block.

of stage 1 and closed-loop average current control of stage 2. In Stage 1 control, T_1 is turned on and the number of fixed duty cycles M is calculated by (15). Inductors are charged by the gate signals from the PWM controller. As in stage 2 control, it is composed of a single outer loop that deals with the output current control and current sharing loop control, which is responsible for the current control of each phase. The output current is measured to obtain high accuracy of the current control.

IV. Simulation and Experiment Verification

A. Simulation Verification

To verify the operation of the proposed topology, a simulation was performed using MATLAB/Simulink and compared to a conventional diver topology in Fig. 2(b). Table I gives the parameters of the simulation. Figs. 9 and 10 show the simulation results of the proposed and conventional topologies, respectively. Fig. 9(a) and (b) shows the overall waveforms of currents and gate signals, respectively, that correspond to the analysis waveforms of Fig. 5. It also shows that the output current ripple is reduced by the interleaved technology in Fig. 9(a). Fig. 10(a) shows the overall waveforms of currents of conventional topology, where i_{b_o} represents the load current, i_{b_L1} and i_{b_L2} represent the inductor current respectively. Fig. 10(b) and (c) show that the conventional topology pulse rising and falling times are 120.8 μs and 119.4 μs respectively. Comparing with Fig. 10, it is shown that the proposed topology greatly improves the response speed of the pulse edge.

In order to simplify the calculation of parameter M, only the first term in (15) is adopted, and the influence of parasitic parameters in the second term is ignored. This makes the calculated value of M relatively small, resulting in the final value of the pre-charge inductor current being slightly less than the given value, but it does not affect the control process. As shown in Fig. 9(a), the inductor currents of L_1 and L_2 are charged to the $i_{ref}/2$ by the proposed pre-charge control method. The fixed duty ratio $d_{pre} = 0.1$, according to (15), M is approximately 8, which means that 8 fixed duty cycles are

TABLE I
Parameters for the Circuit

Parameter	Symbol	Value
SiC MOSFET Switching frequency	f_s	50 kHz
Input DC voltage	v_{in}	50 V
BUCK inductor	L_j	80 μH
Output current	i_o	20 A
Load	R_L	0.9 Ω
Pulse frequency	f_{period}	160 Hz
Pulse width	P_{width}	0.5 ms
Rise time	t_r	<20 μs

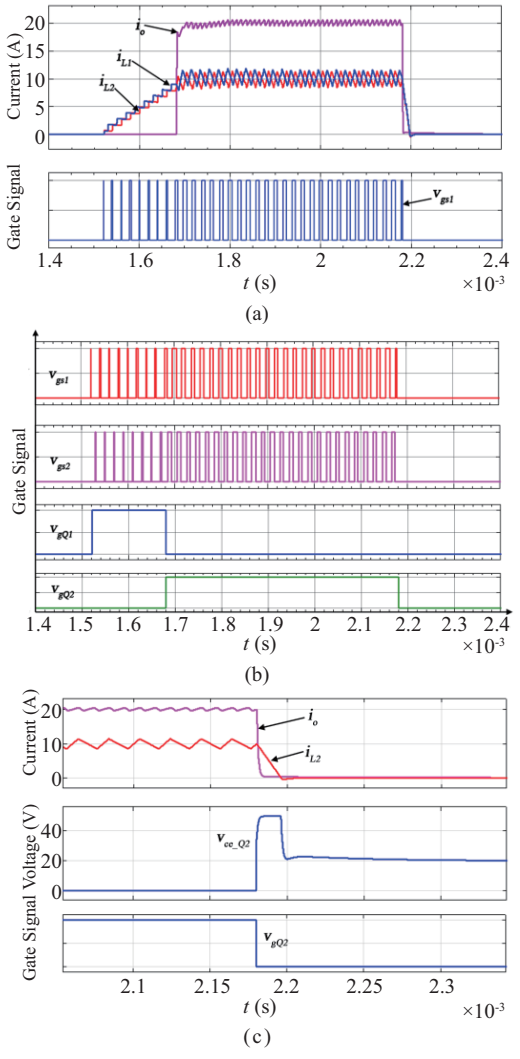


Fig. 9. Simulation results for the proposed topology at one pulse cycle. (a) Overall waveforms of currents. (b) Gate signals for switches. (c) Falling edge with voltage stress of Q_2.

needed to charge the inductors corresponding to the simulation results. From Fig. 9(a), we can see that a fast rising and falling slope are obtained by switch Q_1, Q_2 and the inductor currents pre-charge control method. Fig. 9(c) shows that the inductor currents decrease linearly and the voltage v_{ce_Q2} across Q_2 is approximately v_{in} until the inductor current is zero which

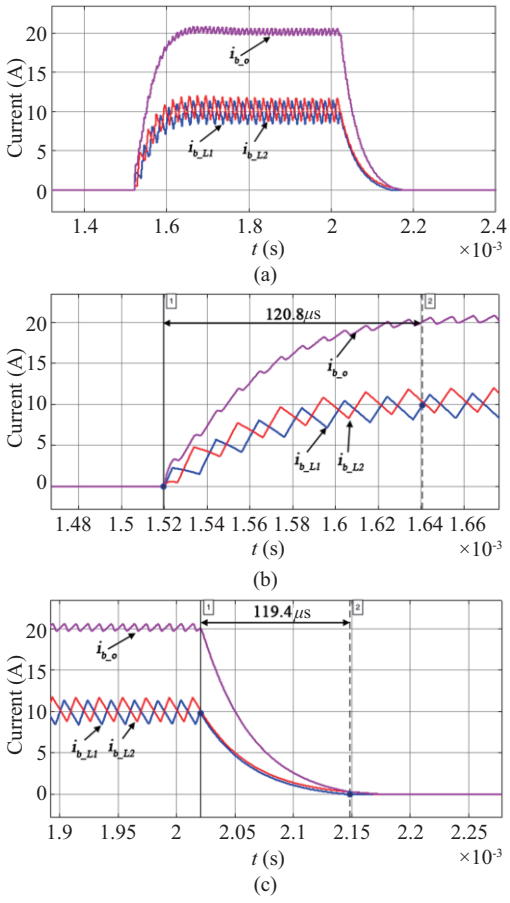


Fig. 10. Simulation results for the conventional topology at one pulse cycle. (a) Overall waveforms of currents. (b) Rising edge partial enlargement. (c) Falling edge partial enlarfement.

means that the energy stored in the inductors is fed back to the input source. Moreover, since the inductance energy is not discharged through the load (unlike the conventional topology pulse falling edge in Fig. 10(c)), the falling edge time of the pulse current is reduced. Fig. 10(c) shows that there is no inductor energy feedback, the inductor energy is discharged through the load, and with time constant $\tau = L/R_L$, the simulation falling time is approximately 119.4 μs which is much larger than the time of current falling edge when energy feedback occurs.

B. Experiment Verification

To evaluate the performance of the proposed MIEF-PPS and the control method, an experiment was performed using a laboratory prototype based on the specifications listed in Table I and a compared a conventional topology. The controller was digitally implemented with a TMS320F28377D from Texas Instruments. The interleaved circuit was designed by a high-frequency SiC MOSFET and pulse forming circuit with low switching frequency used in IGBT modules. Only dual-interleaved topology was used to verify the correctness of the proposed topology and the control algorithm. For the

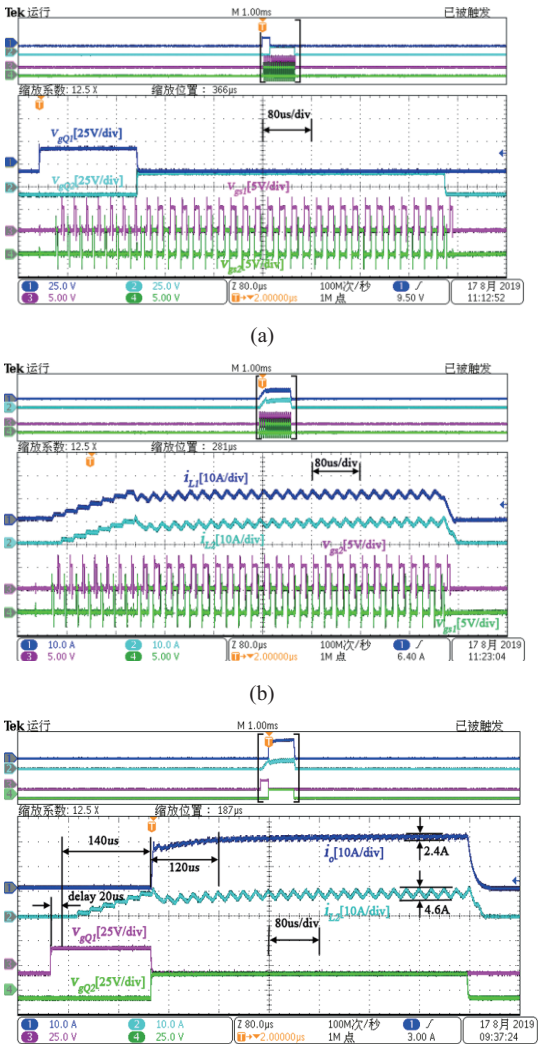
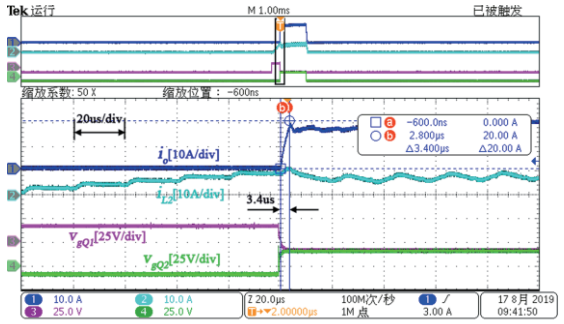


Fig. 11. Experiment results for the proposed topology at one pulse cycle. (a) Gate signals for switches. (b) Inductor currents and drive waveforms under interleaving control. (c) Waveform of pulse output current related to inductor current and impulse control.

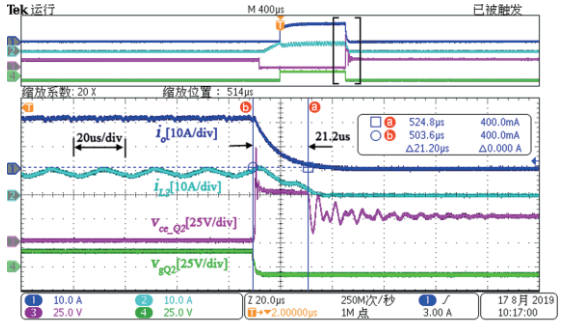
future consideration of high-power designs, the parameter redundancy of the prototype design is high, but has a negligible effect on the verification of the principle.

To verify the operation of the proposed topology, the main waveforms in a pulse period were measured, as shown in Fig. 11. The activation gate signals of MIEF-PPS, which correspond to Fig. 5, as shown in Fig. 11(a). The inductor is charged while v_{gQ1} is at a high level, and v_{gQ2} is low. The proposed pre-charge PWM control and interleaving control results in the final waveforms shown in Fig. 11(b). i_{L1} and i_{L2} are the branch inductor currents of MIEF-PPS, respectively. It is shown that inductors are charged by fixed duty rate gate signals. Fig. 11(c) shows the waveform of a pulse output current related to the inductor current and low-frequency pulse control gate signals.

Pre-charge stage waveforms were measured and amplified, as shown in Fig. 11(c). The proposed pre-charge PWM control was applied, and M equals to 7 as calculated by (15). From

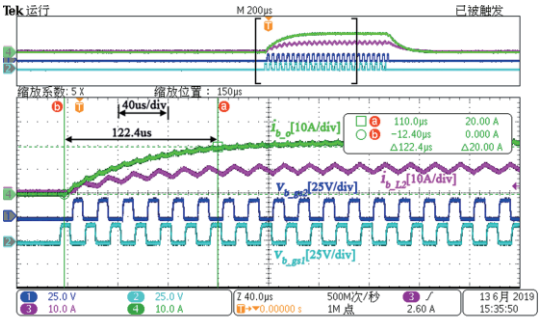


(a)

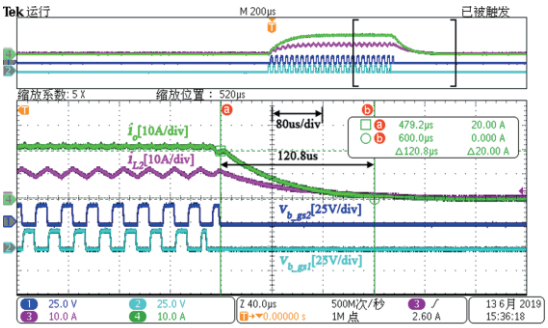


(b)

Fig. 12. Pulse leading and fall edge waveforms of MIEF-PPS. (a) Pulse leading edge with inductor storage. (b) Pulse fall edge with energy feedback.



(a)



(b)

Fig. 13. Pulse leading and falling edge waveforms of conventional topology. (a) Pulse leading edge. (b) Pulse fall edge.

Fig. 11(c), the inductor current of each phase is approximately charged to its reference current by using pre-charge control and the feasibility and availability of this method are illustrated. It also shows that there is an interruption in the cycle delay (20 μs) between gate signal v_{gQ1} and inductor current due to digital loop control, but a negligible effect on pre-charge control. Fig. 11(c) shows current in a steady state of the pulse flat-top interval. As shown, the inductor current ripple and the output current ripple are approximately 4.6 A and 2.4 A, respectively, showing a better performance of current reduction by using interleaving technology. It also shows transient waveforms at the start of pulse discharge, showing that the output current needs some control period to reach its given current, which is related to the digital control design and compensator parameters. This paper highly focuses more on topology innovation, impulse response speed and steady-state current, and will also study transient problems in the future.

Fig. 12 shows the proposed topology output current rising time and pulse-end stage waveforms in detail. From the simulation results in Fig. 9 and experiment results in Figs. 11 and 12, it is seen, that the performance of the proposed topology for both results almost equals. Fig. 12(a) shows the zoomed-in sections of Fig. 11(c) at the pulse leading edge. As shown, the rising time of output pulse current i_o is approximately 3.4 μs less than 20 μs, illustrating a better performance in the current respond speed. Fig. 12(b) shows the key waveform of the inductor energy feedback at the end of the pulse. The symbol v_{ce_Q2} is the voltage across switch Q_2. As shown, the voltage v_{ce_Q2} is changed to v_{in} at the pulse end, which indicates that the inductor's energy is feed back to C_s from the diode D_{q3}. When the inductor energy discharged is completed, the voltage v_{ce_Q2} of Q_2 approximately stabilizes to half of the input voltage v_{in} due to the series connection of diode D_{q1} and D_{q3}.

Fig. 13 shows the conventional topology (Fig. 2(b)) output current rising time and falling time waveforms in detail. Compared with simulation results in Fig. 10, it is shown that the rising and falling time are almost equal. Fig. 13(a) shows zoomed-in sections of the waveform at the pulse leading edge. As shown, the rising time of output pulse current is approximately 122.4 μs which is much longer than the proposed topology pulse rising time of 3.4 μs. Fig. 13(b) shows zoomed-in sections of the waveform at the pulse falling edge. As shown, the falling time of output pulse current i_{b_o} is approximately 120.8 μs that is much longer than the proposed topology. Comparing Figs. 12 and 13, indicates that the proposed topology has improved the transient response of the pulse current. Moreover, the short falling time means that extra energy is saved.

V. Conclusion

This paper proposed a switched mode multiphase interleaved pulsed power supply topology with energy recovery and inductive storage based on the interleaved buck converter and pulse forming concept. The proposed topology was configured as a hybrid combination of interleaved buck topology and multiple switches, which connected to the load. The proposed topology improves the pulse current response speed and reduces the output current ripple with the pre-charge control method and interleaved technology. In addition, it showed

an energy recovery capability and achieved a fast falling edge when in the pulse end state. The features and operation principles of the proposed topology have been described in detail. The overall schematic was presented, and its control method was briefly discussed. A 360 W prototype driver was implemented and tested. The obtained experimental results verified the operation and performance levels of the proposed topology.

References

[1] A. Geng, Chapter 1, in *Solid State Laser and Its Application*. Beijing: National defense industry press, 2014.

[2] M. Wölz, A. Pietrzak, A. Kindsvater, J. Meusel,K. Stolberg, R. Hülsewede, J. Sebastian, and V. Loyo. (2016). *Laser diode stacks: Pulsed Light Power for Nuclear Fusion*. High Power Laser Science and Engineering. 4, 2016.

[3] R. Platz, B. Eppich, J. Rieprich, W. Pittroff, G. Erbert, and P. Crump, "High duty cycle, highly efficient fiber coupled 940-nm pump module for high-energy solid-state lasers," *High Power Laser Science and Engineering*, 4, 2016.

[4] R. Platz, C. Frevert, B. Eppich, J. Rieprich, A. Ginolas, S. Kreutzmann, S. Knigge, G. Erbert, and P. Crump, "Progress in high duty cycle, highly efficient fiber coupled 940-nm pump modules for high-energy class solid-state lasers," in *Components and Packaging for Laser Systems IV*, 2018.

[5] Z. Huang, Chapter 3, in *Optical Fiber Communication Optoelectronic Devices and Components*, Beijing university of posts and telecommunications press, 2001.

[6] H. Y. Du, "New semiconductor laser drive power supply," in *Applied Laser*, vol. 30, no. 3, pp. 214–218, 2010.

[7] W. Zhou and K. Jin, "Efficiency evaluation of laser diode in different driving modes for wireless power transmission," in *IEEE Transactions on Power Electronics*, vol. 30, no. 11, pp. 6237–6244, 2015.

[8] D. Hodgson, K.Noonan, B. Olsen, and T. Orosz, "Pulsing a Laser Diode," in *Application note 11*, ILX lightwave Corporation.

[9] C. Dong and H. Huang, "Analysis and design of high-current constant-current driver for laser diode bar," in *2011 International Conference on Electronics, Communications and Control (ICECC)*, 2011, pp. 1321–1324.

[10] K. Liu, R. Fu, Y. Gao, Y. Sun, and P. Yan, "High-voltage repetition-frequency charging power supply for pulsed laser," in *IEEE Transactions on Plasma Science*, vol. 43, no. 5, pp. 1387–1392, 2015.

[11] V. V. Bezotosnyiet al., "Quasi-cw 808-nm 300-W laser diode arrays," in *Quantum Electronics*, vol. 47, no. 1, pp. 5–6, 2017.

[12] E. S. Fulkerson et al., "Pulsed power system for the HAPLS Diode Pumped Laser System," in *2015 IEEE Pulsed Power Conference (PPC)*, 2015, pp. 1–6.

[13] E. Fulkerson, R. K. Lanning, and S. Telford, "Compact high current, high efficiency laser diode driver," Ed: Google Patents, 2018.

[14] M. Wang, K. Yang, Z. Wang, and Z. Fan, "Design of laser diode driver with constant current and temperature control system," in *AOPC 2017: Laser Components, Systems, and Applications*, 2017.

[15] A. Sharma, C. Panwar, and R. Arya, "High power pulsed current laser diode driver," in *2016 International Conference on Electrical Power and Energy Systems (ICEPES)*, 2016, pp. 120–126.

[16] S. Tsuda, T. Tamida, T. Hashimoto, and T. Morimoto, "Power supply apparatus for driving laser diode provided with power supply for supplying power to laser oscillator," Ed: Google Patents, 2018.

[17] W. Yao and Y. Ji, "Design of high-performance driving power supply for high-power DPSSL," in *Machinery & electronics*, vol. 5, pp. 15–18, 2010.

[18] E. Penovi, R. G. Retegui, S. Maestri, G. Uicich, and M. Benedetti, "Multistructure power converter with h-bridge series regulator suitable for high-current high-precision-pulsed current source," in *IEEE Transactions on Power Electronics*, vol. 30, no. 12, pp. 6534–6542, 2014.

[19] Z. Wang, X. Ma, C. Wang, and F. Guo, "Study on the power supply of semiconductor laser with two-phase double chopper transformation," in *Laser technology*, vol. 39, no. 3, pp. 386–390, 2015.

[20] S. M. Granat, "Switched mode current source for pulsed loads," Ed: Google Patents, 2010.

[21] F. Z. Chen, J. Y. Wang, Y. C. Song, and F. S. Ho, "High efficiency synchronous pulse laser driver system," in *2017 IEEE 3rd International Future Energy Electronics Conference and ECCE Asia (IFEEC 2017-ECCE Asia)*, 2017, pp. 1878-1881.

[22] M. T. Thompson and M. F. Schlecht, "High power laser diode driver based on power converter technology," in *IEEE Transactions on Power Electronics*, vol. 12, no. 1, pp. 46–52, 1997.

[23] I. D. Crawford, "Low-noise current source driver for laser diodes," Ed: Google Patents, 2003.

[24] W. Zhou and K. Jin, "Efficiency Evaluation of Laser Diode in Different Driving Modes for Wireless Power Transmission," in *IEEE Transactions on Power Electronics*, vol. 30, no. 11, pp. 6237–6244, 2015.

[25] I. O. Lee, S. Y. Cho, and G. W. Moon, "Interleaved buck converter having low switching losses and improved step-down conversion ratio," in *IEEE Transactions on Power Electronics*, vol. 27, no. 8, pp. 3664–3675, 2012.

[26] O. Garcia, P. Zumel, A. de Castro, and J. A. Cobo, "Automotive DC-DC bidirectional converter made with many interleaved buck stages," in *IEEE Transactions on Power Electronics*, vol. 21, no. 3, pp. 578–586, 2006.

[27] S. Wu, G. Luo, and S. Guo, "Mathematical Analysis of Output Current Ripple in Switched Power Supply Interleaved Topology," in *Automation Information*, vol. 1, pp. 289–292, 2003.

[28] R. W. Erickson and D. Maksimovic, Fundamentals of power electronics, 2 ed. Springer Science & Business Media, 2007.

[29] G. Gkizas et al., "Digital state-feedback control of an interleaved DC–DC boost converter with bifurcation analysis," in *Control Engineering Practice*, vol. 73, pp. 100–111, 2018.

[30] G. Guo and B. Shi, "Design of multi-phase DC-DC converter with master-slave current sharing control," in *2002 IEEE Region 10 Conference on Computers, Communications, Control and Power Engineering. TENCOM'02. Proceedings*, 2002, vol. 3, pp. 1990–1993.

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