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# Suppression of charge trapping in ON-state operation of AlGaIn/GaN HEMTs by Si-rich passivation

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## Abstract

In this paper, we investigate the charge trapping in power AlGaIn/GaN high electron mobility transistors which occurs in ON-state operation ( $V_{DS} = 40$  V,  $V_{GS} = 0$  V,  $I_{DS} = 0.18$  A mm<sup>-1</sup>). By analysing the dynamic ON-resistance ( $R_{ON}$ ) after OFF-state and ON-state stress in devices with different SiN<sub>x</sub> passivation stoichiometries, we find that this charge trapping can be largely suppressed by a high Si concentration passivation. Both potential probe and electroluminescence (EL) measurements further confirm that the stress can induce negative charge trapping in the gate–drain access region. It is shown that EL is generated as expected under the field plates at the gate edge, but is obscured by the field plates and is actually emitted from the device near the drain edge; hence care is required when using EL alone as a guide to the location of the high field region in the device. From temperature-dependent dynamic  $R_{ON}$  transient measurements, we determine that the apparent activation energy of the measured ‘trap’ response is around 0.48 eV, and infer that they are located in the heavily carbon-doped GaN layer. Using the leaky dielectric model, we explain the response in terms of the hopping transport from the same substitutional carbon acceptor buffer dopants.

Keywords: GaN HEMTs, ON-state operation, charge trapping, electroluminescence, silicon nitride passivation

(Some figures may appear in colour only in the online journal)

## 1. Introduction

Power AlGaIn/GaN high electron mobility transistors (HEMTs) have attracted wide attention for their outstanding performance with high breakdown voltage and low ON-resistance [1]. However, charge trapping remains a major issue, resulting in current collapse and efficiency losses.

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Charge trapping exists either on the surface [2] or in the GaN buffer [3]. Typically, in power GaN transistors where a carbon-doped buffer layer is used to prevent the punch through effect [4] and to suppress breakdown, the C<sub>N</sub> carbon acceptor ( $E_a = 0.8 \pm 0.2$  eV) is reported as the major buffer trap. Several measures have been adopted to minimize current collapse, i.e. field plates [5], epitaxy [6] and SiN<sub>x</sub> passivation layers [7].

Simultaneous applied voltage and current operation is an important regime for power transistor application when the transistor is switched from OFF-state to ON-state, resulting in a high electrical field and a high current during switching [8]. Hot electrons and high temperature will be involved during this regime and the consequently induced charge trapping can be a reliability issue for GaN HEMTs [9]. The ON-state

is sometimes referred to as semi-ON or hard-switching [10]. Meneghini *et al* [11] investigated the device degradation after the semi-ON-state stress ( $V_{DS} = 30$  V) in GaN HEMTs, and found it was only partially recoverable with UV light illumination. Meneghini *et al* [9] also determined that an additional charge trapping (with short detrapping time constant  $< 1$  s) can be induced during semi-ON-state compared to the OFF-state in GaN HEMTs. In our recent study [12] on hard-switching, we found that hot electrons could induce surface trapping causing an increase of  $R_{ON}$ .

Several studies have shown how  $\text{SiN}_x$  low-pressure chemical vapour deposition (LPCVD) passivation layers with different stoichiometries can affect charge trapping in the GaN HEMTs during OFF-state. In [13], using transient dynamic  $R_{ON}$  and substrate bias measurements, it is shown that negative charge trapping can occur due to the high vertical electrical fields in the devices; but it is suppressed by a Si-rich passivation. In [14], charge trapping distributions following OFF-state stress on the same wafers were measured by  $C$ - $V$  using Schottky gate sensing probes to the channel and it was found that negative charges either accumulate locally at the field plate edge or spread along the gate-drain access region. Hard- and soft-switching operation ( $V_{DS} = 150$  V for a maximum duration of 130 ns) showed that Si-rich passivation suppressed both surface and bulk induced dynamic  $R_{ON}$  [12].

In this paper, in contrast to these previous studies [12–14], we consider the long-period ON-state stress ( $V_{DS} = 40$  V,  $V_{GS} = 0$  V for 10 s) in power AlGaIn/GaN HEMTs, a stress which is sometimes used in reliability tests, and show that long time constant charge trapping recovery can be induced, and that it can be strongly suppressed by the use of Si-rich passivation. In temperature-dependent measurements, ON-state stress and substrate stress induce buffer trap responses with an activation energy of 0.44–0.48 eV. By analysing the Schottky gate probe data, we show that the negative charges are distributed along the top of carbon-doped GaN layer, but especially accumulate under the gate in ON-state. We discuss the charge accumulation and relaxation in terms of the leaky dielectric model of the buffer [15, 16]. We show that the recovery time constants are all consistent with rate limiting hopping transport from the carbon doped layer rather than trap emission, and explain the presence of two different time constants from just one trap state [17]. This data provides strong support for the leaky-dielectric model.

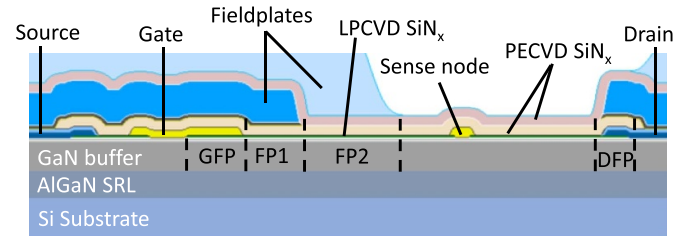
Electroluminescence (EL) measurements show apparent light emission from the drain edge, however using sense probe measurements it is shown that in fact the EL occurs under the gate with refraction/reflection of the light at the drain edge. This potentially important result suggests that care should be used when using EL to identify the location of high fields in GaN HEMTs.

## 2. Experimental results

The devices under test are AlGaIn/GaN HEMTs fabricated on 150 mm diameter GaN-on-Si wafers. Schottky gated HEMTs with a gate fieldplate and two source fieldplates

**Table 1.** LPCVD  $\text{SiN}_x$  properties by wafers.

Wafer	A	B	D
DCS/ $\text{NH}_3$	0.33	2.49	4.38
Refractive index	2.01	2.10	2.21



**Figure 1.** Schematic of GaN HEMTs with Schottky sense node structures. GFP is the gate connected field plate, and FP1 and FP2 are two source field plates.

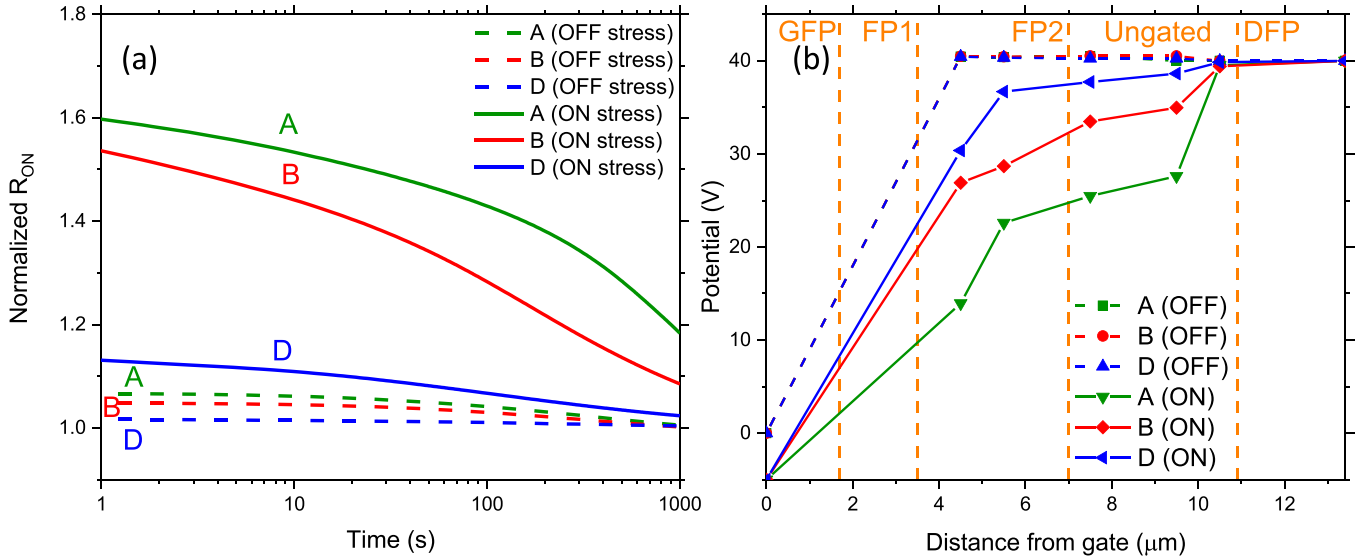
are used in this paper ( $L_{SG} = 3.5$   $\mu\text{m}$ ,  $L_G = 1$   $\mu\text{m}$ ,  $L_{GD} = 13.4$   $\mu\text{m}$  and  $W_G = 100$   $\mu\text{m}$ ). The epitaxy contains an AlGaIn based strain relief layer (SRL), a carbon-doped GaN layer ( $N_C \sim 10^{19}$   $\text{cm}^{-3}$ ), an unintentionally doped (UID) GaN channel layer, a 20 nm AlGaIn barrier and a 3 nm GaN cap layer. A 70 nm LPCVD  $\text{SiN}_x$  passivation is placed above the GaN cap and two 300 nm plasma-enhanced chemical vapour deposition (PECVD)  $\text{SiN}_x$  layers are deposited between the source fieldplates. The LPCVD  $\text{SiN}_x$  contains less hydrogen impurities than the PECVD  $\text{SiN}_x$  and thus works better to suppress any diffusion or trapping. In addition, the PECVD technique needs a lower temperature (200  $^\circ\text{C}$ –400  $^\circ\text{C}$ ) to deposit  $\text{SiN}_x$  than the LPCVD (700  $^\circ\text{C}$ –800  $^\circ\text{C}$ ), so it is suitable for deposition after the gate metal [18].

Wafer A, B and D with different LPCVD  $\text{SiN}_x$  stoichiometry are used and span the full range of device behaviour seen in previous studies of these wafers. Table 1 displays the LPCVD  $\text{SiN}_x$  properties (DCS/ $\text{NH}_3$  refers to dichlorosilane/ $\text{NH}_3$  ratio in fabrication and ranges from 0.33 to 4.38). Wafer A corresponds to stoichiometric  $\text{Si}_3\text{N}_4$ . More detailed device information can be found in [12–14, 19].

To characterize the potential distribution in the devices, HEMTs with an additional Schottky contact (sense node) at different positions between gate and drain were used. A cross-section is shown in figure 1. The positions of the sense nodes are 4.5, 5.5, 7.5, 9.5, 10.5  $\mu\text{m}$  away from the gate edge [14].

Figure 2(a) presents measurements of time-dependent dynamic  $R_{ON}$  of GaN HEMTs after 10 s OFF-state and ON-state stress for wafers A, B and D, measured at  $V_{DS} = 1$  V,  $V_{GS} = 0$  V. In the OFF- and ON-state stress,  $V_{DS}$  is always kept at 40 V while  $V_{GS} = 0$  V for ON-state and  $V_{GS} = -5$  V for OFF-state ( $V_{th} = -2$  V). After OFF-state stress, less than 10% increase in  $R_{ON}$  can be observed in all three wafers. However, after ON-state stress increased dynamic  $R_{ON}$  is seen and especially in wafers A and B which are closer to  $\text{Si}_3\text{N}_4$  stoichiometry.

In figure 2(b), the potential distributions during OFF- and ON-state are characterized by using the HEMTs with sense nodes. In these measurements, the source is grounded and the



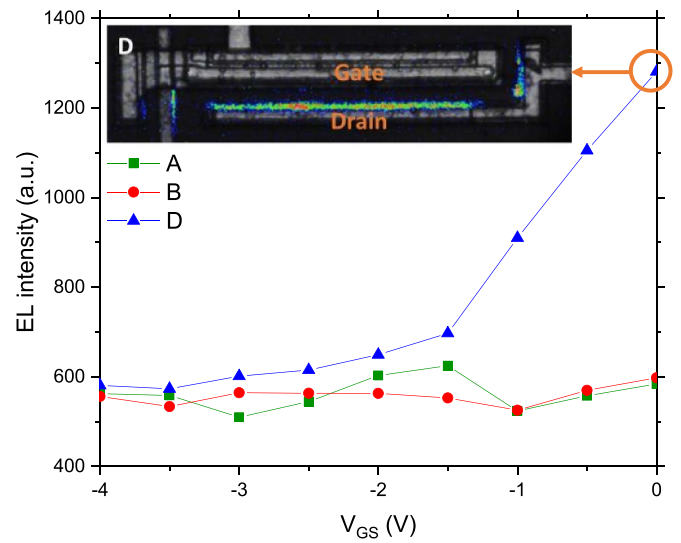
**Figure 2.** (a) Dynamic  $R_{ON}$  measured after the OFF-state stress ( $V_{DS} = 40$  V,  $V_{GS} = -5$  V for 10 s) and ON-state stress ( $V_{DS} = 40$  V,  $V_{GS} = 0$  V for 10 s) in wafer A, B and D. The average measured currents during ON-state stress are 0.179, 0.172 and 0.176 A  $\text{mm}^{-1}$  for wafer A, B and D respectively. (b) Potential distribution measured in the gate–drain access region during OFF-state ( $V_{DS} = 40$  V,  $V_{GS} = -5$  V) and ON-state ( $V_{DS} = 40$  V,  $V_{GS} = 0$  V) in wafer A, B and D. The OFF-state potential distributions of three samples are almost overlaid.

gate is biased at  $-5$  V for OFF-state and 0 V for ON-state. Meanwhile, the sense node is forced with 1 nA constant current while the drain is swept from 0 to 40 V slowly ( $\sim 0.83$  V  $\text{s}^{-1}$ ). Thus, we can obtain the potential of the sense node in nearly steady state when  $V_{DS} = 40$  V [13, 14].

During OFF-state, as expected all three samples show the same potential distribution with all the voltage drop occurring near the gate edge; there is no potential change in the gate–drain access region where the probes are located. However, during ON-state operation, a variation of potential distribution between the gate and the drain can be observed between the three wafers. From wafer D to A, the potentials in the ungated region start to drop, and eventually lead to a significant potential drop in the vicinity of the drain edge in wafer A.

EL measurements are carried out with a  $50\times$  objective and Opticstar charge-coupled device camera by biasing HEMTs in ON-state. Figure 3 shows the measured EL intensity against  $V_{GS}$  in wafer A, B and D. Wafer D shows visible EL emission, however, no significant EL emissions were recorded in wafers A and B for  $V_{DS}$  up to 40 V. As seen in the inset of figure 3, we were able to determine that in wafer D, the EL emission appears to come from the edge of the drain, and at the side contact to the gate and drain.

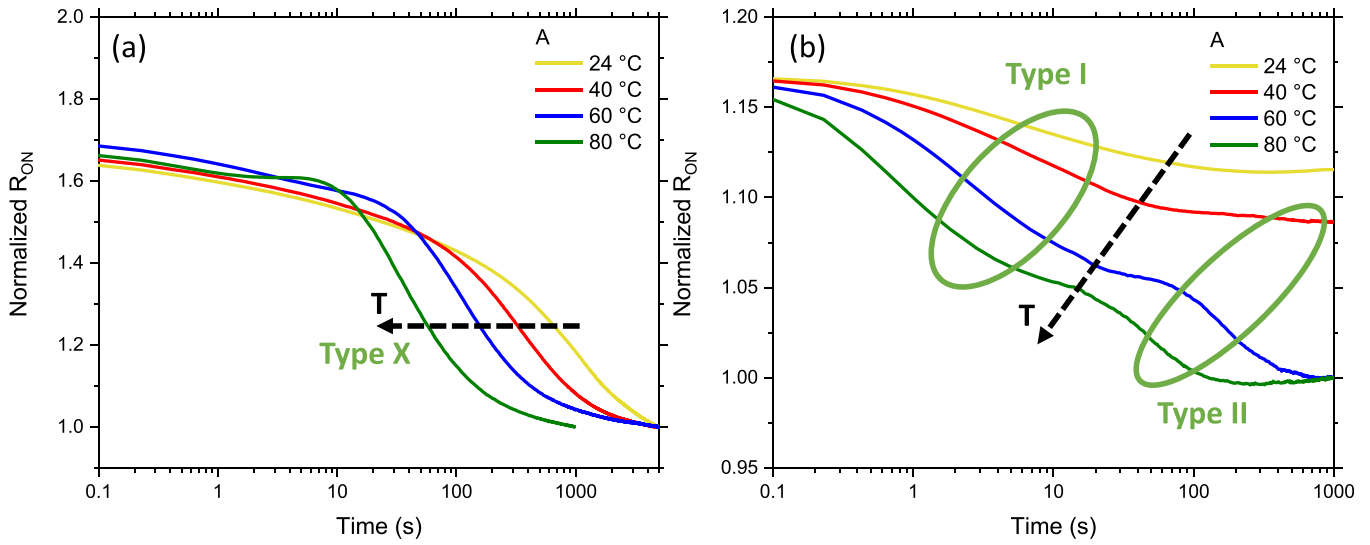
In figure 4, temperature-dependent drain current transient measurements following ON-state stress ( $V_{DS} = 40$  V,  $V_{GS} = 0$  V for 10 s) or Si substrate stress ( $V_{SUB} = -150$  V,  $V_{DS} = 1$  V and  $V_{GS} = 0$  V for 10 s) have been performed in order to extract the apparent activation energy of the possible trap responses in wafer A. This technique to characterize the charge trapping is also known as current mode deep-level transient spectroscopy [20]. The substrate bias stress, in contrast to the drain stress which has a high



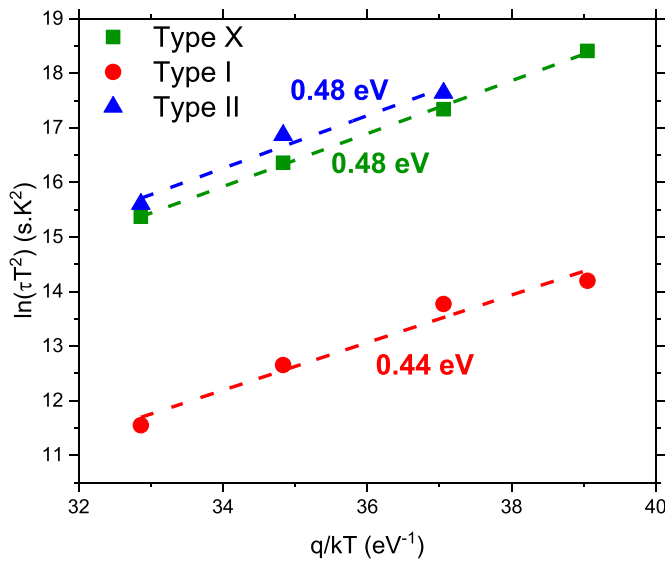
**Figure 3.** Measured EL intensity against  $V_{GS}$  in wafer A, B and D ( $V_{DS} = 40$  V, exposure time = 10 s). The inset shows the captured image in wafer D ( $V_{DS} = 40$  V,  $V_{GS} = 0$  V).

lateral field component, primarily applies a vertical electric field between the 2DEG and the Si substrate. Figure 4(a) shows the temperature-dependent recovery of dynamic  $R_{ON}$  after the ON-state stress; the S-shape curves suggest the existence of a dominant detrapping process (labelled as type X). In figure 4(b), after the substrate stress, the recovery curves show two quite distinct de-trapping processes (labelled as type I and II). Figure 5 shows conventional Arrhenius plots assuming that trap emission is the rate limiting step for the responses found in figure 4. The emission process can be described by the Arrhenius function  $\ln(\tau T^2) = \frac{E_a}{kT} + \ln\left(\frac{1}{\gamma\sigma}\right)$ ,



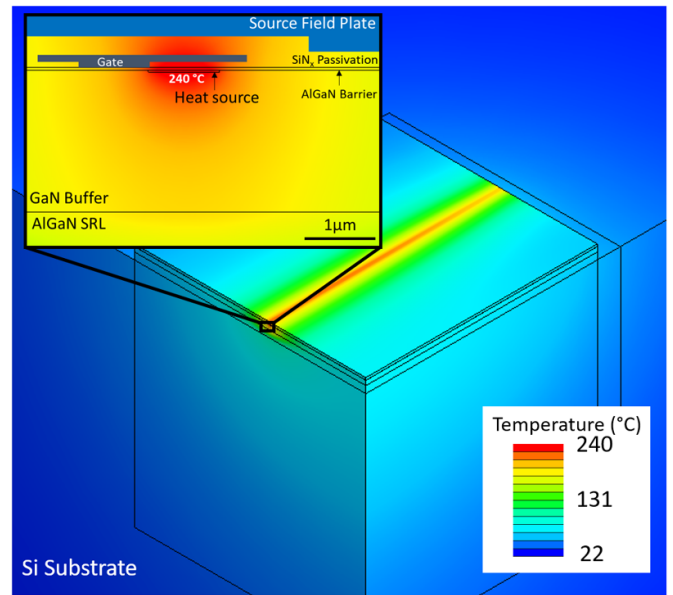


**Figure 4.** (a) Temperature-dependent dynamic  $R_{ON}$  measured after the ON-state stress ( $V_{DS} = 40$  V,  $V_{GS} = 0$  V for 10 s) in wafer A. (b) Temperature-dependent dynamic  $R_{ON}$  measured after the substrate stress ( $V_{SUB} = -150$  V,  $V_{DS} = 1$  V and  $V_{GS} = 0$  V for 10 s) in wafer A. Measurement conditions during transient are  $V_{DS} = 1$  V,  $V_{GS} = 0$  V. The apparent trap responses are highlighted as type X, I and II.



**Figure 5.** Arrhenius plot of the acceptor-like trap responses (type X, I and II) as identified in this paper.

where  $\gamma = 2\sqrt{3}(2\pi)^{\frac{3}{2}}k^2m^*h^{-3}$ . Here  $\tau$  is the emission time constant,  $T$  is the ambient temperature,  $E_a$  is the activation energy for the electron to emit from the trap to the band edge,  $k$  is the Boltzmann constant,  $\sigma$  is the capture cross-section,  $m^*$  is the effective electron mass, and  $h$  is the Planck constant [20]. All the responses, type I, II and X show a similar apparent activation energy with type I  $\sim 0.44$  eV, while type X and II have  $\sim 0.48$  eV and similar apparent capture cross-section. However we note that according to [21], in heavily carbon-doped devices, the measured time constant is dominated by the transport through a defect band and not activation to the band edge. Hence, the fitted activation energies would not represent trap energy levels but be related to the transport process.



**Figure 6.** The 3D finite element model shows the simulated temperature distribution during the ON-state. This structure includes the Si substrate, the AlGaIn SRL, the GaN buffer, the AlGaIn barrier and the SiN<sub>x</sub> passivation. The model assumes a constant heat input ( $2.4 \times 10^{17}$  W m<sup>-3</sup>) inside the heat source ( $30$  nm  $\times$   $1$   $\mu$ m  $\times$   $1$  mm) in vicinity of the gate edge. The inset shows the maximum equilibrium channel temperature of about  $240$  °C.

### 3. Simulation

In this study, we investigate the impact of ON-state stress on the dynamic  $R_{ON}$  and trapping, as shown in figure 6. To estimate the thermal effect from the measurement condition, we ran thermal simulations with a broadly similar structure (AlGaIn barrier thickness =  $20$  nm, GaN thickness =  $2$   $\mu$ m, AlGaIn SRL thickness =  $3$   $\mu$ m, Si thickness =  $1$  mm) in Ansys. The thermal parameters used in the simulation are given in table 2

**Table 2.** Thermal conductivities  $\kappa$  and their temperature-dependent coefficients  $\eta$  at room temperature.

	GaN	Si	SRL
$\kappa, \text{Wm}^{-1}\text{K}^{-1}$	160	148	12
$\kappa (T^{-\eta})$	$T^{-1.4}$	$T^{-1.28}$	—

[22, 23]. In this simulation, we use an equilibrium ON-state condition of  $V_{\text{DS}} = 40 \text{ V}$ ,  $V_{\text{GS}} = 0 \text{ V}$ ,  $I_{\text{DS}} = 0.18 \text{ A mm}^{-1}$ , which gives a power of  $7.2 \text{ W mm}^{-1}$ . This leads to a maximum channel temperature increase of about  $218 \text{ }^\circ\text{C}$  (from the ambient temperature  $22 \text{ }^\circ\text{C}$ ). A drain bias of  $40 \text{ V}$  was the highest bias that could be applied without permanent degradation, and the calculated temperature rise is quite consistent with this being thermally driven.

## 4. Discussion

### 4.1. Dynamic $R_{\text{ON}}$ and potential distribution

In figure 2(a), the relatively low  $40 \text{ V}$  OFF-state stress in a device designed for  $650 \text{ V}$  results in only a small change in  $R_{\text{ON}}$  at room temperature. In contrast, there is a much larger increase of  $R_{\text{ON}}$  after the ON-state stress which is dependent on LPCVD stoichiometry. The self-heating [24] is potentially a major reason for the dynamic  $R_{\text{ON}}$  as the thermal simulation reveals a relatively high channel temperature ( $240 \text{ }^\circ\text{C}$ ). However, during ON-state stress, wafers A, B and D show a similar current level ( $0.17\text{--}0.18 \text{ A mm}^{-1}$ ) suggesting that they are experiencing a similar temperature. Hence, the self-heating is not the major reason here.

In figure 2(b), there are no differences between the potential distribution between wafer A, B and D during OFF-state, since the potential is almost entirely dropped under the gate foot and the gate wing edge. Meanwhile during ON-state stress, as the Si content decreases in the LPCVD passivation from wafer D towards stoichiometry of wafer A, the potential drops in the ungated region, and the electric field peak near the gate edge partially moves to the drain edge. The presence of a current in the channel makes any reduction in 2DEG density in the gate–drain gap visible since the region under the gate is no longer necessarily the highest resistance part of the channel. It suggests that there are trapped negative charges accumulated not just under the gate edge (saturated HEMT operation always results in negative ionized acceptor charge near the gate edge to support the lateral field in this region [25]) but also in the entire gate–drain gap during ON-state, and the density of these negative charges increases from wafer D to A. Related effects have been observed previously such as in OFF-state in [14], and Meneghini *et al* [26] have reported in p-Gate HEMTs, the electrical field peak can gradually shift from the gate edge towards the drain edge as time goes by due to the negative charge trapping in the gate–drain access region. Optical measurements have also revealed a peak field at the drain [27].

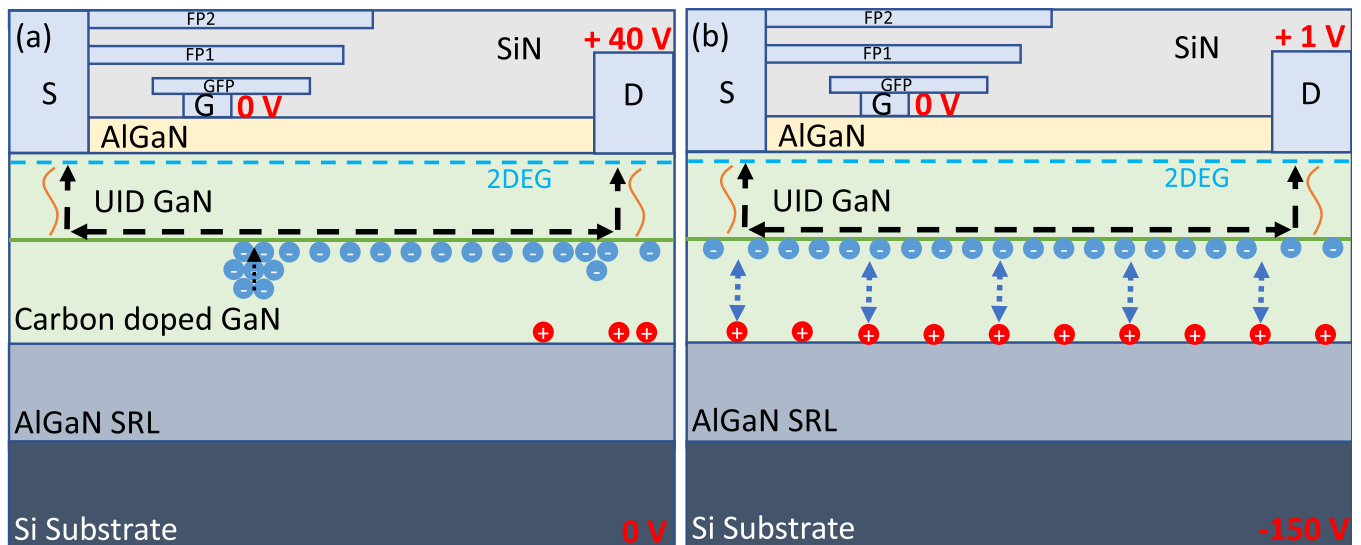
### 4.2. Electroluminescence

In figure 3, we observe the high EL emission largely from the edge of the drain in wafer D. EL is primarily originated from the Bremsstrahlung effect in GaN HEMTs, where the electron loses its energy and emits photons near scatterers in the high electric field [28]. However, the potential measurements indicate that the electric field peak in wafer D only appears near the gate edge, not the drain edge. The explanation is that the EL emission occurs under the field plates near the gate but is only visible where there are no field plates giving optical access, and light, guided along the GaN layer, is reflecting/refracting from the drain contact metal. That is also why we can observe EL emission near the drain and source contacts at the device sides where there is no current. Based on that explanation, the EL results are consistent with the potential measurements. This result suggests that care needs to be taken when interpreting the location of EL emission based purely on the EL images. From wafer D to A, the peak electric field near the gate edge is significantly reduced during the ON-state, thus no EL emission can be found in wafer A and B.

### 4.3. Charge trapping

In figures 4(a) and (b), we identify apparent negative charge trapping type X under the ON-state stress, and type I and II under the substrate bias in wafer A. In substrate bias measurements, any surface or upper barrier traps have been completely screened by the presence of the 2DEG during stress. Therefore, the type I and II trapping must be located in the buffer (most likely carbon doped-GaN layer where there is a high density of deep acceptors). Figure 5 shows the Arrhenius plots of all three types and in particular, the type X and II share similar activation energy and apparent capture cross-section, while the type I does not. Hence we suggest that the type X and II have the same origin in the buffer.

The potential measurements can help us to determine the location of the charge associated with the type X response. Negative charge trapping will partially deplete the 2DEG and increase the resistance through the backgating effect [29]. Thus, a higher resistance suggests a higher density of negative charge. In the ungated region, the derivative of the potential with respect to the distance from the gate ( $x$ ) is proportional to the local resistance of the 2DEG ( $R(x) = V(x)/I$  and  $I$  is a constant throughout 2DEG). Figure 7(a) shows a schematic of negative charge distribution in wafer A during the ON-state by applying this rule (consistent with the detailed simulations in [16]). Some negative charges are accumulated under the drain and gate edges leading to the peak lateral electrical fields, and uniform negative charges are distributed within the ungated region. In contrast, the wafer D shows little negative charge storage in the GaN buffer apart from below the gate edge. The basic difference between wafers A and D can be explained in the leaky dielectric model [15, 16], in terms of the relative vertical leakage through the UID GaN channel. For



**Figure 7.** Schematic of the charge distribution within the GaN buffer layer in wafer A. (a) During the ON-state stress, negative charges are distributed along the interface between the UID GaN and the carbon doped GaN layer, and localized under the gate edge, affecting the 2DEG through the back-gating effect. Some positive charges may be present on the bottom interface of the carbon doped GaN layer under the drain contact due to the vertical electric field. On the recovery stage, the localized negative charges under the gate spread laterally and then flow to the contacts (type X). (b) During the substrate stress, negative and positive charges accumulate on the top and bottom interfaces of the carbon doped GaN layer. On the recovery stage, vertical current flow first neutralizes the positive charges on the bottom interface (type I), while subsequently the remaining negative charges spread laterally and flow to the contacts (type II).

wafer A, the UID GaN is highly resistive, so under the influence of the drain bias, the less resistive buffer (p-type carbon doped layer) potential is mostly close to the source potential in the gate–drain gap, resulting in a high back-gate bias in the gate–drain gap. By contrast, for wafer D the leaky undoped channel layer allows the carbon doped buffer layer to follow the 2DEG potential in the gate–drain gap preventing the formation of a back-gate bias [16].

For wafer A, the charge distribution during the substrate bias is shown in figure 7(b), where the carbon doped layer is more conductive than the layers above and below it allows a negative charge to accumulate at its top surface and a positive charge at its bottom surface (Maxwell–Wagner effect [30]) under the influence of the vertical field. Previous substrate ramp measurements have shown that wafer A has a higher leakage to the buffer under the contacts than in the source–drain gap [13], and this results in the negative charge being partly suppressed under the contacts.

During the recovery following stress, the charges in the buffer must eventually leak away via the leakage paths under the contacts (presumably decorated threading dislocations). However the carbon doped layer has a lower resistivity than the layers above and below, so first charge redistribution and recombination will occur within this layer. Therefore, as shown in figure 7(a), after the ON-state stress, the localised negative charges at the gate edge will spread out first and then the negatively charged layer will ultimately flow to the Ohmic contact, corresponding to the type X response. Noticing that there is a small increase of  $R_{ON}$  at  $\sim 10$  s for  $80^\circ\text{C}$  in figure 4(a), as discussed in [16] it is very likely due to the initial transport of the localised negative charges at the gate edge as they move closer to the top of the carbon doped layer and then spread, resulting

in a transient increase of source resistance and thus the overall resistance.

After the substrate stress, there are two discharging paths as depicted in figure 7(b). The first path is vertical current flow leading to recombination between the positive and negative charges within the carbon doped GaN layer [16, 17]. The second path is the same as the mechanism discussed for ON-state stress, as the remaining negative charges spread laterally and flow to the contacts. Consequently, we can conclude that the type X/II is largely associated with the lateral charge flow to the Ohmic contacts, while the type I is due to the vertical charge flow within the carbon doped GaN layer. Since ON-state stress for wafer A results in only a small positive charge at the bottom of the carbon doped layer in the gate–drain gap, any vertical transport is insignificant and cannot be clearly distinguished in figure 4(a).

The charge trapping in the carbon-doped GaN buffer is expected to be due to the carbon atoms substituted for the N atoms and acting as a deep acceptor 0.8–0.9 eV above the valence band [31]. Despite this many publications report activation energies in the 0.5–0.6 eV range and attribute it to a deep level [20]. Here we find that all the responses are in the range 0.44–0.48 eV. Based on the results of Koller *et al* [21], an alternative and more likely explanation is that the rate limiting step determining the activation energy is hopping transport to the acceptor rather than capture/emission to the bandedge. They found that if the carbon density is  $\geq 10^{19}\text{ cm}^{-3}$ , charge transport occurred primarily in a defect band, instead of the valence band. The temperature dependence was non-Arrhenius but in the vicinity of room temperature, fitting an Arrhenius law over a limited temperature range gave an activation energy of  $\sim 0.5$  eV.



#### 4.4. The impact of passivation stoichiometry

In [12], we characterized the behavior of the same devices in ON-state conditions at 150 V during hard-switching ( $\leq 130$  ns stress). This resulted in hot electron stress leading to charge trapping with a small time constant ( $< 1$  ms) that was attributed primarily to surface trapping. That trapping was dramatically reduced for the non-stoichiometric  $\text{SiN}_x$  wafer D. In contrast, in this paper, we use a much more moderate ON-state bias condition but with significant self-heating and longer stress time of 10 s, and mainly characterize the charge trapping with long time constant ( $\sim 1000$  s at room temperature). The time constant here, as discussed before, relates to transport within a defect band through a hopping process rather than activation to the valence band edge. As for the hard switching stress in [12] we find that wafer D has much reduced sensitivity to dynamic  $R_{\text{ON}}$ . However, in this case the long time constant recovery is primarily consistent with buffer trapping. It suggests that, in hard-switching applications of GaN HEMTs, one will encounter dynamic  $R_{\text{ON}}$  due to surface and buffer trapping simultaneously, with the surface trapping only affecting the device properties for milliseconds while the buffer trapping can cause performance issues for hours.

An important finding in our study is that the Si-rich LPCVD passivation can suppress both surface and bulk trapping. Currently, no direct evidence has been found to show how the LPCVD layer changes the dispersive effect both at the surface and in the bulk of the device. However a plausible explanation for the suppression of surface trapping is based on the fact that the excess Si in the  $\text{SiN}_x$  results in a resistive passivation allowing lateral charge leakage leading to recovery of any surface charging [13]. The suppression of bulk trapping is less obvious, however we note that conduction along dislocations can occur in an impurity band whose conductivity is dependent on the charge state of the surrounding trap states [32]. Hydrogen incorporation in the bulk will be passivation recipe dependent, and it is quite reasonable that the Fermi level in the dislocation core can be shifted sufficiently to change the impurity band occupancy dramatically, changing the electrical properties of threading dislocations. The resulting change in leakage path from the 2DEG to the carbon doped GaN layer will in turn dramatically modify dynamic  $R_{\text{ON}}$  [16]. More work is required to obtain a more accurate physical model for the trap emission, charge transport process, and how the  $\text{SiN}_x$  affects this process.

## 5. Conclusion

A set of AlGaIn/GaN HEMTs with different  $\text{SiN}_x$  passivation layers have been tested for its impact on the ON-state-induced charge trapping. About 60% increase of  $R_{\text{ON}}$  after the ON-state stress has been found in the sample with the stoichiometric  $\text{Si}_3\text{N}_4$  LPCVD layer, while negligible increase of  $R_{\text{ON}}$  has been found after the OFF-state stress at room temperature, suggesting the presence of negative charge trapping in the device under test under the ON-state stress. The potential mapping on the devices with sense nodes shows significant drop

of potential in the gate–drain access region during ON-state rather than OFF-state, indicating that the negative charge is distributed within that region. The EL measurements show agreement with our analysis, and demonstrates that there is potential for misinterpretation of the location of EL emission. EL emission from the drain edge does not necessarily mean that the high field region is located at the drain, in this case it was actually located at the gate edge.

All features of the stress induced charge distributions and the recovery process can be explained using the leaky dielectric model. This includes the difference between substrate bias and ON-state bias recovery, and the presence of two different time constant responses with the same activation energy. The results are consistent with hopping transport in a defect band being the limiting step in determining trap responses, rather than the normally assumed emission to the band edge. Finally, we discuss how passivation of GaN HEMTs with Si-rich LPCVD passivation can dramatically suppress this charge trapping after ON-state stress.

## Data availability statement

The data generated and/or analysed during the current study are publicly available (<https://doi.org/10.6084/m9.figshare.15091062.v1>) for legal/ethical reasons but are available from the corresponding author on reasonable request.

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