

Designing, Modeling, and Optimizing Data-Intensive Computing Systems

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Abstract

The cost of moving data between the memory units and the compute units is a major contributor to the execution time and energy consumption of modern workloads in computing systems. At the same time, we are witnessing an enormous amount of data being generated across multiple application domains. Moreover, the end of Dennard scaling, the slowing of Moore’s law, and the emergence of dark silicon limit the attainable performance on current computing systems. These trends suggest a need for a paradigm shift towards a *data-centric* approach where computation is performed close to where the data resides. This approach allows us to overcome our current systems’ performance and energy limitations by minimizing the *data movement overhead* by ensuring that data does not overwhelm system components. Further, a data-centric approach can enable a *data-driven* view where we take advantage of vast amounts of available data to improve architectural decisions. Our current systems are designed to follow rigid and simple policies that lack adaptability. Therefore, current system policies fail to provide robust improvement across varying workloads and system conditions.

As a step towards modern computing architectures, this dissertation contributes to various aspects of the *data-centric* approach and further proposes several *data-driven* mechanisms.

First, we design NERO, a data-centric accelerator for a real-world weather prediction application. NERO overcomes the memory bottleneck of weather prediction stencil kernels by exploiting near-memory computation capability on specialized field-programmable gate array (FPGA) accelerators with high-bandwidth memory (HBM) that are attached through a cache-coherent interconnect to a host CPU system. Second, we explore the applicability of different number formats, including fixed-point, floating-point, and posit, for memory-bound stencil kernels. We search for the appropriate bit-width that reduces the memory footprint and improves the performance and energy efficiency with minimal loss in the accuracy.

Third, we propose NAPEL, an ML-based application performance and energy prediction framework for data-centric architectures. NAPEL uses ensemble learning to build a model that, once trained for a fraction of programs, can predict the performance and energy consumption of different applications. Fourth, we present LEAPER, the first use of few-shot learning to transfer FPGA-based computing models across different hardware platforms and applications. LEAPER provides the ability to reuse a prediction model built on an inexpensive low-end local system to a new, unknown, high-end FPGA-based system.

Fifth, we propose Sibyl, the first reinforcement learning-based mechanism for data placement in hybrid storage systems. Sibyl is a data-driven mechanism. It observes

different features of the running workload as well as the storage devices to make system-aware data placement decisions. For every decision it makes, Sibyl receives a reward from the system that it uses to evaluate the long-term performance impact of its decision and continuously optimizes its data placement policy online. Our extensive real-system evaluation demonstrates that Sibyl provides adaptivity and extensibility by continuously learning from and autonomously adapting to the workload characteristics, storage configuration and device characteristics, and system-level feedback to maximize the overall long-term performance of a hybrid storage system. We interpret Sibyl’s policy through our explainability analysis and conclude that Sibyl provides an effective and robust approach to data placement in current and future hybrid storage systems.

Overall, this thesis provides two key conclusions: (1) hardware acceleration on an FPGA+HBM fabric is a promising solution to overcome the data movement bottleneck of our current computing systems; (2) data should drive system and design decisions by leveraging inherent data characteristics to make our computing systems more efficient. Thus, we conclude that the mechanisms proposed by this dissertation provide promising solutions to handle data well by following a *data-centric* approach and further demonstrates the importance of leveraging data to devise *data-driven* policies.

We hope that the proposed architectural techniques and detailed experimental results presented in this dissertation will enable the development of energy-efficient data-intensive computing systems and drive the exploration of new mechanisms to improve the performance and energy efficiency of future computing systems.

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Chapter 1

Introduction

A wide range of application domains have emerged with the ubiquity of computing platforms in every aspect of our daily lives. These modern workloads (e.g., machine learning, graph processing, and bioinformatics) demand high compute capabilities within strict power constraints [147]. However, today’s computing systems are getting constrained by current technological capabilities, making them incapable of delivering the required performance. We highlight three major trends that call for a paradigm shift in the computing system landscape.

(1) The Memory Wall: Over the years, the improvements in memory access latency have not been able to keep up with the improvements in processor latency, which is referred to as the *memory wall* [509]. Earlier, system architects tried to bridge this gap by introducing multiple levels of the memory hierarchy that can cache data to avoid unnecessary off-chip data movement. Yet, the system remained *compute-centric*, where the data has to move a long distance from the memory subsystem over the power-hungry off-chip data bus through multiple levels of memory hierarchy to the compute units for processing. This compute-centric nature has led to a fundamental *data movement bottleneck*, which incurs a significant amount of energy and latency overhead in our current computing systems [331]. In addition, for a given application, there can be a strong mismatch between the nature of the data access patterns and the layout of the data in memory. Such a mismatch leads to limited spatial locality, which causes frequent data movement between the memory subsystem and the processing units.

(2) The Slowdown of Moore’s Law: The continuation of Moore’s law allowed more transistors per chip for each transistor node technology generation. This transistor scaling enabled us to have CPUs composed of a multi-core architecture with multiple levels of caches. In 1974, Dennard [109] postulated that the total chip power for a given chip area stayed constant from one process generation to another. This trend allowed CPU vendors to have higher clock frequencies without drastically impacting the

overall system power consumption. However, with the demise of Dennard scaling [109], we witness that with every process generation, total chip power does not remain constant due to the leakage effects. The leakage effects limit the shrinking of gate oxide in a transistor that forces higher voltage than required for Dennard scaling, which in turn increases the power density. As a result, the system-level performance gains are not enough to motivate a further increase in the single-core clock frequency compared to the significant increase in energy consumption. This increase in power consumption has led to the onset of dark silicon [123] in servers, whereby a large portion of transistors on a chip has to be switched off or run at a lower frequency to avoid the effects of high leakage [301]. While in system-on-a-chip (SoC)-based designs, specialized heterogeneous cores have emerged to overcome the disadvantages of dark silicon and slowdown of Moore’s law [173], where each core is optimized for a specific task. Therefore, in the Post-Dennard scaling era, the single-core CPU performance has stagnated because of its inability to operate within the given power budget.

Over the years, advancements in manufacturing technology have been slowing due to device physics limitations in transistor node scaling. On the other hand, the memory scaling is becoming even more challenging [138, 150, 326]. However, the demand for performance with high energy-efficiency has continued to grow. In the high-performance computing (HPC) domain, current scaling issues and high communication overheads limit HPC systems to realize exascale computers needed for modern and future data-intensive workloads [334].

Therefore, future architectural innovations are expected to come from optimizations across the entire hardware/software computing stack [327, 328].

(3) The Data Avalanche: At the same time, we are witnessing an enormous amount of data being generated across multiple application domains [334] like weather prediction modeling, radio astronomy, bioinformatics, material science, chemistry, health sciences, etc. In the domain of climate and weather modeling, for example, there is a data avalanche due to large atmospheric simulations [410]. Major efforts are currently underway towards refining the resolution grid of climate models that would generate *zettabytes* of data [410]. These high-resolution simulations are useful to predict and address events like severe storms. However, the sheer amount of generated data is one of the biggest challenges to overcome.

The Consortium for Small-Scale Modeling (COSMO) [116] built one such weather model to meet the high-resolution forecasting requirements of weather services. We use COSMO as a major case-study in this thesis. The main computational pipeline of COSMO consists of compound stencil kernels that operate on a three-dimensional grid [167]. The performance of these compound stencil kernels is dominated by memory-bound operations with irregular memory access patterns and low arithmetic intensity that often results in <10% sustained floating-point performance on current

CPU-based systems [290] that standard CPU-based optimization techniques cannot overcome (see Chapter 3).

We find another relevant example in radio astronomy. The first phase of the Square Kilometre Array (SKA) aims to process over 100 terabytes of raw data samples per second, yielding of the order of 300 petabytes of SKA data produced annually [209]. Recent biological disciplines such as genomics have also emerged as one of the most data-intensive workloads across all different sciences wherein just a single human genome sequence produces hundreds of gigabytes of raw data. With the rapid advancement in sequencing technology, the data volume in genomics is projected to surpass the data volume in all other application domains [337].

The above trends suggest that computer architects and system designers need to develop novel architectural solutions to overcome the aforementioned major technological challenges and effectively handle the overwhelming amount of data.

This chapter serves as an introduction to this dissertation. The chapter is structured as follows. Section 1.1 highlights the two guiding principles that we follow in this dissertation to overcome our current system challenges. Based on these guiding principles, we provide the thesis statement. Section 1.2 describes our approach to solve the thesis statement, while Section 1.3 lists the contributions of this dissertation. Finally, Section 1.4 provides the dissertation outline.

1.1 Problem and Thesis Statement

Future architectural innovations are expected to come from optimizations across the entire hardware/software computing stack [327]. We highlight two guiding principles that can be applied in complementary aspects of computer architecture to overcome the current system challenges and improve the overall performance: (1) *data-centric computing*, where we bring processing closer to the memory and use different techniques to reduce the data movement bottleneck (such as hardware specialization, data quantization, and domain specific-memory hierarchies); (2) *data-driven system optimization*, where we exploit the available data to perform architectural decisions or predictions.

1.1.1 Data-Centric Computing

Today's memory hierarchy usually consists of multiple levels of cache, the main memory, and the storage. The traditional approach is to move data up to caches from the storage and then process it. Figure 1-1 depicts the system evolution based on

the information referenced by a program during execution, which is referred to as a working set [172]. Prior systems were based on a *compute-centric* approach where data is moved to the core for processing (Figure 1 (a)-(c)). In contrast, the *data-centric* approach aims at processing close to where the data resides. This approach couples compute units close to the data and seek to minimize the expensive data movement. The system ensures that data does not overwhelm its components.

As shown in Figure 1 (d-e), near-memory computing (NMC) [11, 12, 68, 132, 145, 155, 182, 183, 225, 334, 434] and computation-in memory (CIM) [7, 77, 144, 264, 265, 399, 416, 417, 419, 429] are two data-centric paradigms. In near-memory computing (Figure 1 (d)), we place the processing cores closer to the memory units. On the other hand, the computation-in-memory (Figure 1 (e)) paradigm is more disruptive as it aims at reducing data movement completely by using memories with built-in compute capability (e.g., resistive random-access memory (ReRAM) and phase-change memory (PCM)). Processing right at the “home” of data can significantly diminish the data movement problem of data-intensive applications. Thus, data-centric architectures have the potential to overcome our current data movement bottleneck.

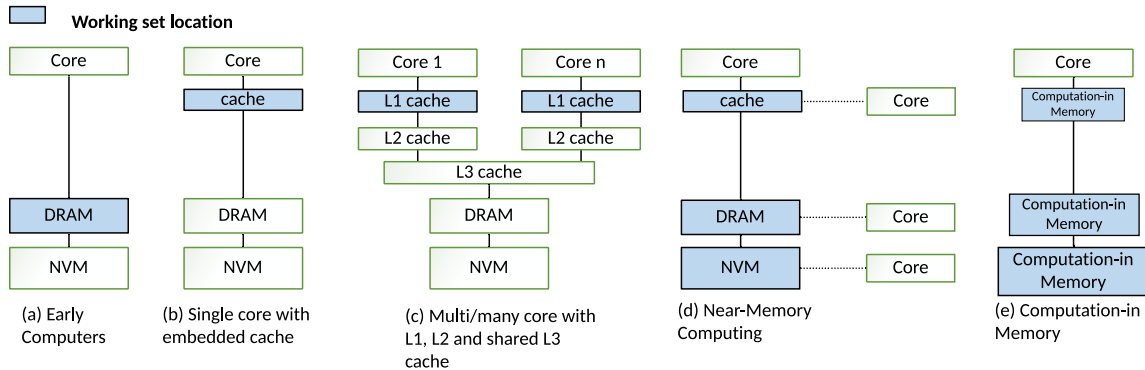


Figure 1-1: Classification of computing systems based on working set location [172]. Prior systems were based on a *compute-centric* approach where data is moved to the core for processing (Figure 1-1 (a)-(c)), whereas now, with *near-memory computing* (Figure 1-1 (d)), the processing cores are brought closer to the place where data resides. Therefore, in a *data-centric* approach, the data resides much closer to the processing units than in a *compute-centric* approach. *Computation-in-memory* (Figure 1-1 (e)) further reduces data movement by using memories with built-in compute capability (e.g., phase-change memory (PCM) [265])

Heterogeneous computing has emerged as an answer to continue to improve performance beyond the limits imposed by the slow down in Moore’s Law and the end of Dennard scaling [447]. Heterogeneous computing entails complementing processing elements with different compute capabilities, each to perform the tasks to which it is best suited. In the HPC domain, coupling specialized compute units with general-purpose cores while following a data-centric approach can meet the high-performance

computing demands and provides the ability to realize exascale systems needed to process data-intensive workloads [334].

The graphics processing unit (GPU) is one of the most popular acceleration platforms. GPUs have been used to accelerate workloads like computer graphics and linear algebra [485] because of their many-core architecture. However, GPUs are power-hungry due to high transistor density and, depending on the power constraints, may not always be the ideal platform for implementation. Recently, the use of field-programmable gate array (FPGA) in accelerating machine learning workloads with high energy-efficiency has inspired researchers to explore the use of FPGAs instead of GPUs for various high-performance computing applications [73, 119].

FPGAs provide a unique combination of flexibility and performance without the cost, complexity, and risk of developing custom application-specific integrated circuits (ASICs). The researchers at CERN, for example, are using FPGAs to accelerate physics workload in CERN’s exploration for dark matter [119]. Microsoft’s Project Catapult [73] is another example of how FPGAs can be used in the data center infrastructure. Driven by Catapult’s promising research results, Microsoft further deployed the architecture on the Azure cloud marketplace [316]. Such integration for certain workloads can even offer more energy efficiency than CPU or GPU-based systems. However, taking full advantage of FPGAs for accelerating a workload is not a trivial task. Compared to CPUs or GPUs, an FPGA must exploit an order of magnitude more parallelism in a target workload to compensate for the lower clock frequency.

The above trend raises a question: **how can we accelerate other scientific applications in an energy-efficient way on specialized hardware?**

Modern FPGAs show four key trends.

- The integration of high-bandwidth memory (HBM) [179] on the same package as an FPGA allows us to implement our accelerator logic much closer to the memory with an order of magnitude more bandwidth than the traditional DDR4-based FPGA boards. Thus, these modern FPGAs adopt a *data-centric* approach.
- The introduction of UltraRAM (URAM) [470] along with the BlockRAM (BRAM) that offers massive *scratchpad*-based on-chip memory next to the logic.
- New cache-coherent interconnects, such as IBM Coherent Accelerator Processor Interface (CAPI) [444], Cache Coherent Interconnect for Accelerators (CCIX) [49], and Compute Express Link (CXL) [421], allow tight integration of FPGAs with CPUs at high bidirectional bandwidth (on the order of tens of GB/s). This integration reduces programming effort and enables us to coherently access the host system’s memory through a pointer rather than having multiple copies of the data.

- FPGAs are being manufactured with an advanced technology node of 7-14nm FinFET technology [140] that offers higher performance.

These four trends suggest that **modern FPGA architectures deliver unprecedented levels of integration and compute capability due to new technological advances, which further provides an opportunity to overcome the *memory bottleneck* of real-world data-intensive applications.**

1.1.2 Data-Driven System Optimization

On a computing system, we generally run a diverse set of workloads that generate a large amount of data. However, our present systems do not take advantage of vast amounts of data available to them [327, 328, 331]. Current systems are built around rigid design rules that follow fixed heuristic-driven policies or perform an exhaustive exploration with a change in system scenario rather than leveraging previous knowledge. Moreover, these heuristic-driven approaches cannot fully capture complex relations present in various aspects of the computer architecture, such as data placement, memory management, and task scheduling. These approaches favor certain workloads and/or system configurations over others without considering an application’s inherent behavior or the underlying device characteristics. For example, the storage subsystem keeps executing the same data placement policy during the entire lifetime of a system regardless of the impact of the resulting decisions on the system. A storage subsystem sees a vast amount of data, yet it cannot learn from that data and adapt its policy because the policy is rigid and hard-coded by a human.

To overcome the inefficiency of our current computing system, we need to devise *data-driven* mechanisms that take advantage of the vast amount of available data by exploiting inherent data characteristics [52, 197, 205, 206, 207, 208, 217, 370, 371, 457, 521]. To this end, a data-driven approach can enable machine learning (ML) techniques in different aspects of computer architecture design and use. ML models are trained to make predictions or decisions without explicit programming by discovering inherent patterns or relationships in the data. Traditionally, computer architects have focused more on accelerating ML algorithms. In contrast, only in the past few years have we seen a growth in works using ML for architecture design and use [374].

Therefore, there is **an opportunity to develop novel mechanisms that allow computers to learn from experiences and reuse those experiences to make future decisions. In turn, closing a loop where computer architects enable ML and ML improves computer architectures. Moreover, we need to assess if these machine learning-driven approaches can outperform our current human-driven approaches.**

Data-driven techniques using ML can assist us in many aspects of computer

architecture, including architectural evaluation and design space exploration (DSE). In the early design stage, architects often use various evaluation techniques to navigate the design space of new architectures, avoiding the cost of chip fabrication. Usually, we employ analytic models or simulation techniques to provide performance and energy consumption estimates while using different workloads or architectural configurations. Analytic models are typically based on simple mathematical equations that provide fast estimates but at the cost of accuracy. Therefore, we often resort to simulation-based techniques that can model architectural interactions more accurately. However, simulation techniques can be extremely slow because a single simulation for a real-world application with a representative dataset can take hours or even days (see Chapter 5). This slow speed cannot meet the modern design productivity demands, despite the efforts of accelerating simulations with both hardware [372] and software-based [405] techniques.

In the later phase of the design cycle, architects often use FPGAs to prototype their design to get the accurate performance and power estimates. An FPGA is highly configurable and allows us to reconfigure its circuitry to implement any algorithm. However, an FPGA’s large configuration space and the complex interactions among configuration options lead many developers to explore individual optimization options in an ad hoc manner. Moreover, FPGAs have infamously low productivity due to the time-consuming FPGA mapping process [345].

Therefore, a common challenge that past works have also faced is **how to evaluate the performance of an application or a new architecture in a reasonable amount of time [346] such that a large design space can be covered?**

Thesis Statement

Based on the above-discussed aspects, the thesis problem statement is as follows: *Design system architectures to effectively handle data by: (1) overcoming the data movement bottleneck in data-intensive applications through a data-centric approach of bringing processing close to the memory and ensuring that data does not overwhelm system components; thus, enabling high performance in an energy-efficient way; and (2) further leverage the enormous amount of data to model and optimize computing systems by exploiting the inherent data characteristics to perform data-driven decisions.*

1.2 Overview of Our Approach

In line with the thesis statement, this dissertation provides five contributions based on nine methods (concepts) to handle and leverage data effectively. In Table 1.1, we discuss nine different methods that we use in this dissertation. Methods are

architectural concepts that we use in our contribution to reach a specific goal. We use six data-centric (DC) methods that put data and its processing at the center of the design. These methods minimize data movement and maximize efficiency while processing, accessing, and storing data. We also adopt three data-driven (DD) methods that take advantage of the vast amount of data that flow through the system. We briefly discuss these nine methods.

Table 1.1: We highlight across five contributions nine different methods (concepts) used in this dissertation to achieve the thesis statement of handling data well. We make use of two guiding principles: (1) *data-centric* (DC) is bringing processing closer to where data resides and ensuring that data does not overwhelm system components; (2) *data-driven* (DD) is leveraging data to perform architectural decisions or predictions

METHODS	CONTRIBUTIONS				
	NERO [434]	Low Precision [436]	NAPEL [437]	LEAPER [433]	Sibyl [438]
Specialization (DC)	FPGA-based accelerator	Implementation on an FPGA for fixed-point and floating-point representation		FPGA-based accelerator	
Revisit memory hierarchy (DC)	Scratchpad-based hybrid memory				Tiered hybrid storage system
Reducing copies between host and accelerator (DC)	Shared memory space	Quantize data			
Dataflow architecture (DC)	Task pipelining				
Near-memory computing (DC)	Processing near-high-bandwidth memory		Processing near-3D stacked memory		
Reducing memory footprint (DC)	Single and half floating-point precision	Different number representations—posit, fixed-point, and floating-point			
Static ML (DD)			Learns application performance and energy consumption	Learns resource utilization and performance models	
Speed up design space exploration (DD)	Auto-tuning for data transfer window size		Supervised ML, Design of experiment	Few-shot learning	Design of experiment
Dynamic ML (DD)					Reinforcement Learning
Goal	Overcome memory bottleneck of weather prediction application	Investigate computationally cheaper number representations	Quick performance and energy estimates of new applications	Quick area and performance estimates on new high-end FPGA-based platforms	Efficient and high performance data placement mechanism

1. **Specialization (DC):** Using specialized hardware platforms such as an FPGA to accelerate an application in an energy-efficient way.
2. **Revisit memory hierarchy (DC):** Design memory hierarchies to provide low latency access to data.
3. **Reducing copies between host and accelerator (DC):** Minimize the redundant amount of data copies between the host and the specialized hardware.

4. **Near-memory computing (DC):** Process data closer to the main memory to reduce the data movement overhead.
5. **Dataflow architecture (DC):** Enable task-level parallelism while exploiting data-level parallelism to maximize the utilization of compute resources.
6. **Reducing the memory footprint (DC):** Reduce an application’s required memory space to efficiently access and process data.
7. **Static machine learning (DD):** Leveraging ML during the design phase of architecture.
8. **Speedup design space exploration (DD):** Quick and accurate architectural evaluation and exploration.
9. **Dynamic machine learning (DD):** Leveraging reinforcement learning (RL) during the run-time of a system to continuously adapt system policies.

We demonstrate these above nine methods across the following five mechanisms.

First, we design NERO, a data-centric accelerator for a real-world weather prediction application. As mentioned above, the sheer amount of atmospheric simulation data generated is one of the biggest challenges in the domain of weather prediction. We use a heterogeneous system comprising of IBM[®] POWER9 CPU with field-programmable gate array (FPGA) as our target platform. An FPGA can provide both flexibility and energy efficiency, and moreover, is a cost-effective alternative to an application-specific integrated circuit (ASIC). We create a heterogeneous domain-specific memory hierarchy using on-chip URAMs and BRAMs on an FPGA. Unlike traditionally fixed CPU memory hierarchies, which perform poorly with irregular access patterns and suffer from cache pollution effects, application-specific memory hierarchies are shown to improve energy and latency by tailoring the cache levels and cache sizes to an application’s memory access patterns [465]. NERO overcomes the memory bottleneck of weather prediction stencil kernels by exploiting near-memory computation capabilities on specialized FPGA accelerators with high-bandwidth memory (HBM), which are attached to the host CPU.

Second, we explore the applicability of different number formats and exhaustively search for the appropriate bit-width for memory-bound stencil kernels to improve performance and energy-efficiency with minimal loss in the accuracy. Stencils are one of the most widely used kernels in real-world applications. Based on an exhaustive exploration of a broad range of number systems – fixed-point, floating-point, and posit [165] – we provide the precision and the corresponding accuracy deviation. Each number representation offers a different dynamic range, the usability of which depends upon the target workload.

Third, we propose NAPEL, a machine learning-based application performance and energy prediction framework for data-centric architectures. NAPEL uses ensemble learning to build a model that, once trained for a fraction of programs on a number of architecture configurations, can predict the performance and energy consumption of different applications.

Fourth, we present LEAPER, the first use of *few-shot learning* to transfer FPGA-based computing models across different hardware platforms and applications. Machine learning (ML)-based modeling has emerged as an alternative to traditional, slow simulation (or evaluation) techniques [346]. ML modeling provides the capability to both quickly evaluate various architectural design choices and perform suitability analysis for many workloads. Thus, quick exploration and large prediction time savings compared to simulation are possible. To this end, we develop NAPEL and LEAPER, which are ML-based model solutions.

However, ML needs a large amount of data to train models, which requires running time-consuming simulations. To alleviate this problem, we use a technique called the *design of experiments* (DoE) [321] to extract representative data with a small number of experimental runs. DoE is a set of statistical techniques meant to locate a small set of points in a parameter space with the goal of representing the whole parameter space. The traditional brute-force approach to collecting training data is time-consuming: the sheer number of experiments renders detailed simulations intractable.

Fifth, we propose Sibyl, the first technique that uses reinforcement learning (RL) for data placement in hybrid storage systems. Sibyl observes different features of the running workload as well as the storage devices to make system-aware data placement decisions. For every decision it makes, Sibyl receives a reward from the system that it uses to evaluate the long-term performance impact of its decision and continuously optimizes its data placement policy online. Compared to supervised learning, reinforcement learning provides the following three benefits. First, supervised learning requires large amounts of labeled data. In some scenarios, collecting labeled data can be difficult or even infeasible. Second, unlike supervised learning, which is purely driven by prediction accuracy, an RL-agent is objective-driven, making RL a great fit for objective-driven policies. Third, RL does not require separate training and testing phases. Instead, RL continuously learns and adapts based on the changes in the environment. We implement Sibyl on *real* systems with various HSS configurations, including dual- and tri-hybrid storage systems. Our in-depth evaluation of Sibyl shows that it outperforms four state-of-the-art techniques over a wide variety of applications with a low implementation overhead.

1.3 Contributions

This dissertation makes the following **key contributions**:

1. In **Chapter 3**, we propose NERO, the first near-HBM FPGA-based accelerator for representative kernels from a real-world weather prediction application. Weather prediction is one such high-performance computing application that generates a large amount of data. It consists of compound stencil kernels that operate on a three-dimensional grid. Such compound kernels are dominated by memory-bound operations with complex memory access patterns and low arithmetic intensity. This poses a fundamental challenge to acceleration.
 - (a) We perform a detailed roofline analysis to show that representative weather prediction kernels are constrained by memory bandwidth on state-of-the-art CPU systems.
 - (b) We optimize NERO with a data-centric caching scheme with precision-optimized tiling for a heterogeneous memory hierarchy (consisting of URAM, BRAM, and HBM).
 - (c) We evaluate the performance and energy consumption of our accelerator and perform a scalability analysis. We show that an FPGA+HBM-based design outperforms a complete 16-core POWER9 system (running 64 threads) by $4.2\times$ for the vertical advection (`vadv`) and $8.3\times$ for the horizontal diffusion (`hdiff`) kernels with energy reductions of $22\times$ and $29\times$, respectively.

2. In **Chapter 4**, we perform a precision exploration of the three-dimensional stencil kernels for future mixed-precision systems using a wide range of number systems, including fixed-point, floating-point, and posit.
 - (a) We provide the precision and the corresponding accuracy deviation for a broad range of number systems – fixed-point, floating-point, and posit.
 - (b) We tune stencil-based kernels on a state-of-the-art IBM POWER9 CPU and further evaluate them on an FPGA, which is coherently attached to the host memory. Thus, this chapter fills the gap between the current hardware capabilities and future hardware design.
 - (c) As an extension of this chapter, in Appendix B, we demonstrate our approach to automate the exploration for fixed-point configurations. We show our results for tuning the precision of weights for a neural network.

3. In **Chapter 5**, we propose NAPEL, a new, fast high-level performance and energy estimation framework for NMC architectures. NAPEL is the first such model to leverage ensemble learning techniques, specifically random forest, to quickly estimate the performance and energy consumption of previously-unseen applications in the early stages of design space exploration for NMC architectures.

- (a) We reduce the simulation time needed to gather training data for NAPEL by employing a DoE technique [300], which selects a small number of application input configurations that well represent the entire space of input configurations.
 - (b) We show that NAPEL can provide performance and energy estimates $220\times$ faster than a state-of-the-art microarchitecture simulator with an average error rate of 8.5% (performance) and 11.6% (energy) compared to the simulator.
 - (c) We show that we can use NAPEL to accurately determine if, and by how much, executing a certain workload on a specific NMC architecture can improve performance and reduce energy consumption versus execution on a CPU.
4. In **Chapter 6**, we present LEAPER, the first use of *few-shot learning* to transfer FPGA-based computing models across different hardware platforms and applications. This approach dramatically reduces (up to $10\times$) the training overhead by adapting a *base model* trained on a low-end edge FPGA platform to a new, unknown high-end environment (a cloud environment in our case) rather than building a new model from scratch).
- (a) We create an ensemble of transfer learning models to accurately transfer learning from multiple base learners to avoid a negative transfer, i.e., severe degradation of the predictive power of the transferred model.
 - (b) We demonstrate our approach across *five* state-of-the-art, high-end, on-premise cloud FPGA-based platforms with *three* different interconnect technologies, between host CPU and FPGA, on *six* real-world applications. For *5-shot* learning, we achieve an average performance and area prediction accuracy of 80–90%.
5. In **Chapter 7**, we propose Sibyl, a new self-optimizing mechanism that uses reinforcement learning to make data placement decisions in hybrid storage systems. Sibyl dynamically *learns*, using both multiple workload features and system-level feedback information, how to continuously adapt its policy to improve its long-term performance for a workload.
- (a) We show on real hybrid storage systems (HSSs) that prior state-of-the-art HSS data placement mechanisms fall short of the oracle placement due to: lack of (1) adaptivity to workload changes and storage device characteristics, and (2) extensibility.
 - (b) We conduct an in-depth evaluation of Sibyl on real systems with various HSS configurations, showing that it outperforms four state-of-the-art techniques over a wide variety of applications with a low implementation overhead.
 - (c) We provide an in-depth explanation of Sibyl’s actions that show that Sibyl performs dynamic data placement decisions by learning changes in the level of asymmetry in the read/write latencies and the number and types of storage

- devices.
- (d) We freely open-source Sibyl to aid future research in data placement for storage systems [95].
6. In addition to the above contributions, in **Chapter 2**, we analyze and organize the extensive body of literature on near-memory computing architectures across various dimensions: starting from the memory level where this paradigm is applied to the granularity of an application that could be executed on these architectures.
- (a) A survey of existing near-memory computing architectures. We review more than 30 architectures in detail and identify the strengths and weaknesses of the existing architectures in Appendix A.
 - (b) We highlight the opportunities and the challenges in the domain of near-memory computing.

Thesis Conclusion

Overall, we make the following two conclusions for this thesis.

1. *Hardware acceleration on an FPGA+HBM fabric is a promising solution to reduce the data movement bottleneck of our current computing systems in an energy-efficient way.*
2. *Data should drive system and design decisions by exploiting the inherent characteristics of data to perform efficient architectural decisions or predictions in various design aspects of the computer architecture.*

Therefore, we conclude that the mechanisms proposed by this dissertation provide promising solutions to handle data well by following a *data-centric* approach and further demonstrate the importance of leveraging data to devise *data-driven* policies.

1.4 Dissertation Structure

This thesis is organized into eight chapters. Chapter 2 provides background into near-memory computing, where we classify and evaluate various state-of-the-art *data-centric* architectures. In Appendix A, we describe in detail all the evaluated architectures. Additionally, Chapter 2 also highlights various challenges that need to be addressed. Chapter 3 presents NERO, a *data-centric* architecture of weather prediction application. Chapter 4 explores the applicability of different number systems for stencil kernels. As an extension to Chapter 4, Appendix B presents PreciseFPGA. It provides an automated exploration framework for fixed-point representation. Chapter 5 introduces NAPEL, a fast high-level performance, and energy estimation framework.

Chapter 6 presents LEAPER, our approach to quickly model different FPGA-based hardware platforms and applications. Chapter 7 introduces Sibyl, the first RL-based *data-driven* mechanism for data placement in a hybrid storage system. Chapter 8 concludes this dissertation and provides future directions that are enabled by its results – both in the domain of *data-centric computing* and *data-driven optimization* that can help us overcome present computing system challenges. In addition to the works presented in this thesis, Appendix C highlights several other contributions of the author.

Chapter 2

Near-Memory Computing

In the literature, data-centric computing has manifested with names such as *processing-in memory* (PIM), *near-data processing* (NDP), *near-memory processing* (NMP), or in the case of non-volatile memories as *in-storage processing* (ISP). However, all these terms fall under the same umbrella of *near-memory computing* (NMC), with the core principle of performing processing closer to the memory in contrast to the traditional *compute-centric* approach. In this dissertation, we focus on NMC rather than *in-situ* data-centric computing called *computation-in-memory* that performs logical operations using memory itself by exploiting physical properties of memory devices, such as phase-change memory.

This chapter deals with analyzing and organizing the extensive body of literature on NMC architectures across various dimensions: starting from the memory level where this paradigm is applied to the granularity of an application that could be executed on these architectures. We provide representative architectures in each category of our NMC taxonomy. The remainder of this chapter is structured as follows. Section 2.1 provides background on near-memory computing. Section 2.2 outlines the evaluation and classification scheme that we use. Section 2.3 highlights the present challenges with NMC-based systems, which include lack of evaluation tools, virtual memory, memory coherence, task scheduling, and data mapping. Finally, Section 2.4 concludes the chapter.

2.1 Background and Related Work

The idea of processing close to the memory dates back to the 1960s [442]. However, the first appearance of data-centric systems can be traced back to the early 1990s [108, 121, 153, 220, 240, 364]. As an example, *Vector IRAM* (VIRAM) [243], where the

The content of this chapter was published as “*Near-Memory Computing: Past, Present, and Future*” in MICPRO 2019.

researchers develop a vector processor with an on-chip embedded DRAM. They use VIRAM to exploit data parallelism in multimedia applications. Although such works obtained promising results, these earlier systems did not penetrate the market, and their adoption remained limited. One of the main reasons was attributed to the technological limitations because the amount of memory we could integrate with the processor was limited due to the difference in logic and memory technology processes.

Today, after almost two decades of dormancy, research in NMC architectures is regaining attention. We can largely attribute this resurgence to the following three reasons. First, technological advancements in the stacking technology – 3D (e.g., hybrid memory cube (HMC) [367] see Figure 2-1) and 2.5D (e.g., high-bandwidth memory (HBM) [179]) stacking that blends logic and memory in the same package. Second, moving the computation closer to where the data reside allows for sidestepping the performance and energy bottlenecks due to data movement by circumventing memory-package pin-count limitations. Third, the increase in data volumes produced in various application domains, such as weather prediction modeling, radio astronomy, and bioinformatics, calls for newer architectures designed to handle the overwhelming amount of data. As a result, in recent years, researchers have proposed various NMC designs and proved their potential in enhancing performance in many application domains [11, 12, 68, 132, 145, 155, 182, 183, 225, 334, 434]. For CIM-based architectures, prior works demonstrate that CIM can be achieved using various memory technologies such as static random-access memory (SRAM) [7, 120, 216, 429], dynamic random-access memory (DRAM) [77, 416, 417], PCM [265], and ReRAM [246, 262, 420].

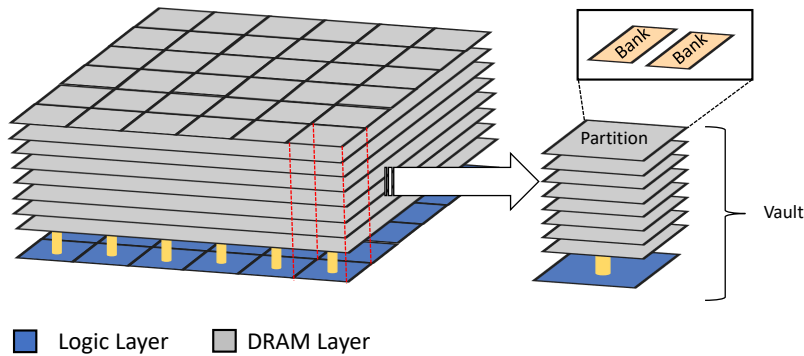


Figure 2-1: Micron’s Hybrid Memory Cube (HMC) [367] comprising of several DRAM layers stacked on top of a logic layer connected by through-silicon vias (TSVs). The memory organization is divided into vaults, with each vault consisting of multiple DRAM banks

Loh *et al.* [286], in their position paper, present an initial taxonomy for NMC. This taxonomy is based on the computing interface with software. Siegl *et al.* [425], in an overview paper, gave a historical evolution of NMC. Similar to the approach

of this thesis, Mutlu *et al.* [331], provide a thorough overview of the mechanisms and challenges in the field of near-memory computing. Unlike the survey of this thesis, the paper [331] does not focus on providing systematization to the literature. Our review characterizes near-memory computing literature in various dimensions starting from the memory level, where we apply the paradigm of near-memory computing to the type of near-memory processing unit, memory integration, and type of workloads/applications.

2.2 Classification and Evaluation

Figure 2-2 shows a high-level view of our classification based on the level in the memory hierarchy. We further split our classification into the type of processing unit (programmable, fixed-function, or reconfigurable). Conceptually the approach of near-memory computing can be applied to any level or type of memory to improve the overall system performance. Our taxonomy does not include magnetic disk-based systems because nowadays, it is only used as a long-term *cold data* storage medium, i.e., for long-term and rarely accessed data [139]. Nevertheless, there have been various research efforts towards providing processing capabilities in the disk. However, the industry did not adopt it widely due to the marginal performance improvement that could not justify the associated cost [226, 400]. Instead, we include emerging non-volatile memories termed storage class memory (SCM) [333], which are trying to fill the latency gap between DRAM and disk.

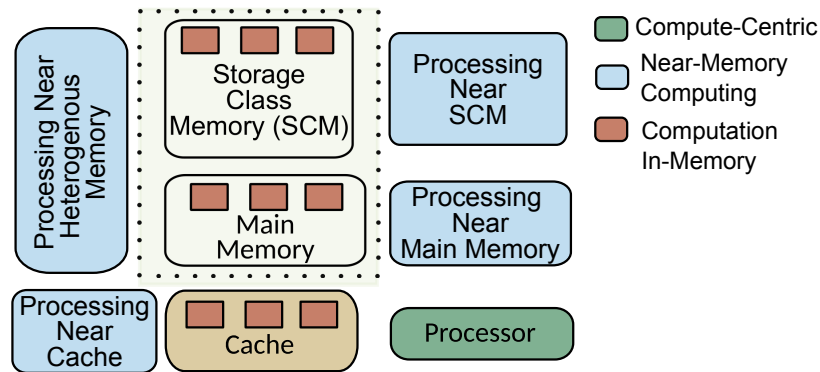


Figure 2-2: Processing options in the memory hierarchy highlighting three computation paradigms: (1) Compute-centric approach where data is moved through various levels of memory to the processor for computing; (2) Near-memory computing approach where the processing elements are placed closer to memory; and (3) Computation-in memory approach that uses inherent properties of memory to perform computation

This section introduces the classification and evaluation metrics (see Table 2.1) used to analyze various architectures in Appendix A.1 and Appendix A.2. We summarize

different architectures in Table 2.1.

For each architecture, we evaluate and classify across five main categories:

- **Memory** - The type of memory technology is one of the most fundamental questions on which the near-memory architecture depends.
- **Processing** - The type of processing unit and the granularity of processing it performs plays a critical role in our analysis.
- **Tool** - Any system’s success depends heavily on the available tool support. The effectiveness of the tool infrastructure indicates the maturity of the architecture.
- **Interoperability** - It is the integration of NMC processing units into the overall computer system architecture. Interoperability deals with aspects such as virtual memory support, memory coherence, efficient task scheduling, and data mapping. Interoperability is one of the key enablers for the adoption of any new system.
- **Application** - NMC follows a data-centric principle and is usually specialized for a particular workload or a set of workloads. Therefore, in our evaluation, we include the domain of the application.

Table 2.1: Classification metrics that we use to analyze some notable NMC architectures (see Table 2.2).

	Property	Abbreviation	Description
Memory	Hierarchy	MM	Main memory
		SCM	Storage class memory
		HM	Heterogenous memory
	Type	C3D	Commercial 3D memory
		PCM	Phase change memory
		DRAM	Dynamic random-access memory
		SSD	Solid-state drive
Integration		US	Conventional unstacked
		S	Stacked using 2.5D or 3D
Processing	NMC/Host Unit	CPU	Central processing unit
		GPU	Graphics processing unit
		FPGA	Field programmable gate array
		CGRA	Coarse-grained reconfigurable architecture
		ACC	Application-specific accelerator
Implementation		P	Programmable unit
		F	Fixed-function unit
		R	Reconfigurable unit
Granularity		I	Instruction
		K	Kernel
		A	Application
Host Unit			Type of the host unit
Tool	Evaluation Technique	A	Analytic
		S	Simulation
		P	Prototype/Hardware
Interoperability	Programming Model	-	Programming model for NMC unit
	Memory Coherence	Y/N	Mechanism for memory coherence
	Virtual Memory	Y/N	Virtual memory support
Application Domain	Workload	-	Target application domain for the architecture

Discussion

Based on the above classification, we highlight some of the notable architectures in the domain of near-memory computing. All solutions discussed in this section are summarized in Table 2.2 and described in Appendix A. From Table 2.2, we make the following five observations.

Table 2.2: Classification and evaluation of representative architectures in category of our NMC taxonomy, refer to Table 2.1 for the legend

NMC Architecture		Memory			Processing				Tool	Interoperability			App. Domain
Architecture	Year	Hierarchy	Type	Integration	NMC Unit	Implementation	Granularity	Host Unit	Evaluation	Programming Model	Cache Coherence	Virtual Memory	Workload
XSD [88]	2013	SCM	SSD	US	GPU	P	A	CPU	S	MapReduce	-	-	MapReduce
SmartSSD [219]	2013	SCM	SSD	US	CPU	P	A	CPU	P	MapReduce	Y	N	Database
WILLOW [415]	2014	SCM	SSD	US	CPU	P	K	CPU	P	API	Y	-	Generic
NDC [382]	2014	MM	C3D	S	CPU	P	K	CPU	S	MapReduce	R	N	MapReduce
TOP-PIM [527]	2014	MM	C3D	S	GPU	P	K	CPU	S	OpenCL	Y	-	Graph and HPC
AMC [334]	2015	MM	C3D	S	CPU	P	K	CPU	S	OpenMP	Y	Y	HPC
JAFAR [510]	2015	MM	DRAM	US	ACC	F	K	CPU	S	API	-	Y	Database
TESSERACT [11]	2015	MM	C3D	S	CPU	F	A	CPU	S	API	Y	N	Graph processing
Gokhale [154]	2015	MM	C3D	S	ACC	F	K	CPU	S	API	Y	Y	Generic
HRL [145]	2015	MM	C3D	S	CGRA+FPGA	R	A	CPU	S	MapReduce	Y	N	Data analytics
ProPRAM [494]	2015	SCM	PCM	US	CPU	P	I	-	S	ISA Extension	-	-	Data analytics
BlueDBM [212]	2015	SCM	SSD	US	FPGA	R	K	-	P	API	-	-	Data analytics
NDA [129]	2015	MM	DRAM	S	CGRA	R	K	CPU	S	OpenCL	Y	Y	MapReduce
PIM-enabled [12]	2015	MM	C3D	S	ACC	F	I	CPU	S	ISA extension	Y	Y	Generic
IMPICA [183]	2016	MM	C3D	S	ACC	F	K	CPU	S	API	Y	Y	Pointer chasing
TOM [182]	2016	MM	C3D	S	GPU	P	K	GPU	S	CUDA	Y	Y	Generic
BISCUIT [160]	2016	SCM	SSD	US	ACC	F	K	CPU	P	API	-	-	Database
Pattnaik [365]	2016	MM	C3D	S	GPU	P	K	GPU	S	CUDA	Y	-	Generic
CARIBOU [199]	2017	SCM	DRAM	US	FPGA	R	K	CPU	P	API	-	-	Database
Vermij [478]	2017	MM	C3D	S	ACC	F	A	CPU	S	API	Y	Y	Sorting
SUMMARIZER [241]	2017	SCM	SSD	US	CPU	P	K	CPU	P	API	-	-	Database
MONDRIAN [105]	2017	MM	C3D	S	CPU	P	K	CPU	A+S	API	-	Y	Data analytics
GraphPIM [332]	2017	MM	DRAM	US	ACC	F	I	CPU	S	API	Y	N	Graph
MCN [15]	2018	MM	DRAM	US	CPU	P	K	CPU	P	TCP/IP	Y	Y	Generic
DNN-PIM [280]	2018	MM	C3D	S	CPU + ACC	P+F	K	CPU	P+S	OpenCL	Y	N	DNN training
Boroumand [57]	2018	MM	C3D	S	CPU+ACC	P+F	K	CPU	S	-	Y	-	Google workloads
GRIM-Filter [234]	2018	MM	C3D	S	ACC	F	K	CPU	S	-	Y	-	Read mapping
CompStor [463]	2018	SCM	SSD	US	CPU	P	A	CPU	P	API	-	Y	Text search
RecNMP [225]	2020	MM	DRAM	US	ACC	F	K	CPU	S	API	Y	Y	Recommendation system
GenASM [68]	2020	MM	C3D	S	ACC	F	K	CPU	S	API	Y	-	String matching
NATSA [132]	2020	MM	C3D	S	ACC	F	K	-	S	API	-	-	Time series analysis
NERO [434]	2020	MM	C3D	S	ACC	R	K	CPU	P	API	Y	Y	Weather prediction modeling
FIMDRAM [247]	2021	MM	C3D	S	ACC	P	I	-	P	API	Y	Y	Machine learning

First, the efficacy of architectural proposals has mostly been tested using simulators. A few works emulate [33, 160, 199, 219, 241, 415] their proposal on an FPGA. Recently, HBM [179] has been adopted by GPU and FPGA vendors. In the future, we expect more evaluation studies on these HBM-equipped platforms and upcoming platforms with NMC capabilities, such as FIMDRAM [259] and UPMEM [155].

Second, the majority of research papers published over the years have proposed

homogeneous processing units near the main memory. However, the logic considered varies in its compute capabilities, e.g., simple in-order cores [11, 15, 105, 241, 260, 334, 382, 407, 463], graphics processing units [88, 182, 365, 527], field-programmable gate arrays [145, 199, 212], and application-specific accelerators [12, 132, 154, 160, 183, 225, 280, 332, 478, 510].

Third, the majority of the NMC proposals are targeted towards data-intensive applications e.g., graph processing [11, 332, 527], MapReduce [88, 129, 382], machine learning [260, 280], and database [160, 199, 219, 241, 407, 510].

Fourth, most of the architectures propose adding compute capabilities in the logic layer of HMC-based memory [11, 12, 57, 68, 105, 132, 145, 154, 182, 183, 225, 259, 260, 280, 334, 365, 382, 478, 527]. However, memory vendors such as Micron have announced to pursue HBM instead of focusing on HMC [315]. Fifth, despite the promises made by existing proposals on NMC, the support for virtual memory, memory coherence, and compiler support is fairly limited. In most of the works [105, 160, 199, 241, 260, 332, 463, 478], the programmers are expected to re-write their code using specialized APIs in order to reap the benefits of NMC.

Based on the above observations, we make the following three conclusions.

1. HBM-equipped specialized hardware has the potential to reduce the memory bandwidth bottleneck, but a study of their advantages for a real-world data-intensive application is still missing.
2. The idea of populating homogeneous processing units near-memory to accelerate a specific class of workloads is limited in the sense that NMC enabled servers that would be deployed in the data centers are expected to host a wide variety of workloads. Hence, these systems would need heterogeneous processing units near the memory [57, 145, 280] to support the complex mix of data center workloads.
3. For broader adoption of the NMC by the application programmers, we would require methods that enable transparent offloading to the NMC units. Transparent offloading requires the compiler or the run-time system to identify NMC-suitable code regions based on some application characteristics, such as the number of last-level cache misses [12, 33, 34, 154, 169] and bandwidth utilization [183, 280, 527]. Unfortunately, integrating a profiler (such as Linux perf [375] or Intel Pin [395]) in a compiler or run-time system is still a challenging task [169] due to its dynamic nature. Therefore, current solutions rely on commercial profiling tools, such as Intel VTune [195], to detect the offloading kernels [33, 34, 183].

2.3 Challenges of Near-Memory Computing

In this section, we highlight five critical challenges in the domain of NMC. The challenges include evaluation tools, virtual memory support, memory coherency, task scheduling, and data mapping. We need to address these challenges before NMC can be established as a de facto solution for modern data-intensive workloads.

2.3.1 Performance Evaluation Tools and Benchmarks

As mentioned in Section 1.1, architects often use various evaluation techniques to navigate the design space of a new architecture. Based on the level of detail required, architects make use of analytic models or more detailed simulation-based techniques. **(1) Analytic modeling** abstracts low-level system details and provide quick performance estimates at the cost of accuracy. In the early design stage, system architects are faced with large design choices that range from semiconductor physics and circuit level to micro-architectural properties and cooling concerns [210]. Thus, during the first stage of design-space exploration, analytic models can provide quick estimates. **(2) Simulation-based modeling** allows us to achieve more accurate performance numbers by precisely modeling various micro-architectural mechanisms. This approach, however, can be quite slow compared to analytic techniques. There have been various academic efforts [20, 203, 261, 402] to build open-source NMC simulators. However, there is a large room for improvement for developing a cycle-accurate simulator that can allow us to explore a wide range of near-memory compute configurations. In Table 2.3, we mention some of the academic efforts to create NMC simulation infrastructure.

Table 2.3: Academic NMC simulators

Simulator	Year	NMC capabilities
Sinuca [20]	2015	Yes
HMC-SIM [261]	2016	Limited
CasHMC [203]	2016	No
SMC [37]	2016	Yes
CLAPPS [351]	2017	Yes
Ramulator-PIM [402]	2019	Yes

As the field of NMC does not have very sophisticated tools and techniques, researchers often spend a significant amount of time building the appropriate evaluation environment [351, 437]. Additionally, there is a critical need for near-memory specific benchmarks of workloads that could benefit from NMC [352]. Such a benchmark suite can allow researchers to evaluate different architectural proposals and faithfully reproduce results.

2.3.2 Virtual Memory Support

To access data inside the main memory, the CPU performs address translation from a data's virtual address to the actual physical address in the main memory. The address translation can be achieved by using the following two mechanisms: *segmentation* or *paging*. Segmentation [255, 522] consists of a simplified approach where part of the linear virtual address space is mapped to physical memory using a direct segment. However, segmentation requires frequent swapping of segments between the main memory and the storage, leading to fragmentation. Therefore, the use of a paging mechanism is gaining wider adoption.

Paging is a memory management mechanism that entails dividing virtual address space into blocks of addresses referred to as pages. A page table stores mapping between virtual to physical address and cache recently used mapping into a translation lookaside buffer (TLB). A miss in the TLB would lead to a long-latency table walk, which can degrade the application performance. Several studies have been proposed to improve the efficiency of address translation, such as by speeding up address translation [43, 360], increasing the TLB reach [32, 97], and introducing caches to store page table address [42, 51, 53].

In an NMC-based system, if an NMC accelerator requires many page table walks for the host CPU, it would substantially reduce the overall performance. Therefore, we need an effective address translation mechanism for NMC architectures. As an example, Hsieh *et al.* [183] design an NMC-side page table for their NMC accelerator, which avoids the use of CPU-side address translation. Past works adopt either a software-based [146, 182, 449, 498] or a hardware-based [37] approach to map between virtual and physical addresses.

2.3.3 Memory Coherency

Coherency is one of the most critical challenges in the adoption of NMC. An NMC processing unit could modify the data, which the host CPU might require. Therefore, we need to maintain a coherence protocol between the shared memory. A fine-grain coherence mechanism might lead to a large number of coherence messages between the NMC cores and the host cores. Therefore, the employed coherence mechanism can drastically affect the performance and the programming model. In NMC, researchers try to overcome this issue by following the two approaches listed below.

(1) Restricted memory region-based techniques such as the one used by Farmahini *et al.* [129] divide the memory into two parts: one for the host processor and another for the accelerator, which is uncacheable. Ahn *et al.* [11] use a similar approach for graph processing algorithms. Another strategy proposed by Ahn *et al.* [12] provides a simple hardware-based solution in which the NMC operations are restricted to only

one last-level cache block, due to which they can monitor the cache block and request for invalidation or write-back if required.

(2) Non-restricted memory region-based techniques allow NMC units to access the entire memory space. Pattnaik *et al.* [365] propose maintaining coherence between the host GPU and near-memory compute units by flushing the L2 cache in the host GPU after kernel execution. However, this approach could evict potentially useful data from the cache. Another way is to implement a look-up table-based mechanism, as Hsieh *et al.* [182]. The NMC units record the cache line address that the offloaded block has updated, and once the offloaded block is processed, the NMC units send this address back to the host system. Subsequently, the host system gets the latest data from memory by invalidating the reported cache lines. More recently, Boroumand *et al.* [58] overcome the coherence issue with a specialized coherence protocol that batches and compresses multiple coherence requests from NMC units. As a result of this, the authors can achieve a near-ideal coherence mechanism.

2.3.4 Task Scheduling

A critical challenge in adopting NMC is to support a heterogeneous processing environment comprising a host system and NMC processing units. It is not trivial to determine which part of an application should run on the NMC processing units. Works such as [169, 182] leave this effort on the compiler, while others [12, 148, 510] assume the programmer would manage the scheduling of tasks. Another approach [12, 260, 332] uses some special set of NMC instructions, which invokes NMC processing units. This approach, however, calls for a sophisticated mechanism as it affects most of the software stack from the application down to the instruction set architecture.

To this end, a run-time system capable of dynamically profiling applications to identify the potential offloads candidates for NMC processing units [182, 280] can significantly help with task scheduling. Therefore, there is still a lot of research required in coming up with an efficient approach to ease the programming burden.

2.3.5 Data Mapping

The problem of data mapping and data layout have been analyzed in various contexts to improve the spatial locality of a workload [75, 228, 306, 502]. The absence of an adequate data mapping mechanism can severely hamper the benefits of processing close to memory. A data mapping scheme should map data in such a way that the data required by the NMC processing units is readily available in the vicinity (data and code co-location). Hence, it is crucial to look into effective data mapping schemes. Hsieh *et al.* [182] propose a hardware/software co-design method to predict which pages of the memory would be used by the offloaded code segment, following which

they place those pages in the memory stack closest to the offloaded code segment.

Yitbarek *et al.* [522] propose a data mapping scheme to place contiguous addresses in the same vault of an HMC-based memory allowing accelerators to access data directly from their local vault. Xiao *et al.* [512] propose to model an application as a two-layer graph through the LLVM-intermediate representation (LLVM-IR), to distinguish between memory and computation operations. On building one such graph, their framework detects groups of vertices, called *community*, that have a higher probability of connection with each other. Each community is mapped to a different vault of an HMC-based memory. Thus, this technique allows multiple NMC units to perform computation in parallel on multiple data elements.

2.4 Conclusion

Data-centric computing aims to reduce the data movement overhead by implementing processing capabilities close to where the data resides. With “close” being a relative term, there is a wide range of possibilities to bring computation closer to the data, resulting in various architectures being investigated today. Data-centric computing is attributed as one of the few real solutions to address the current scaling issues in HPC systems to realize exascale computers needed for modern and future data-intensive workloads. There are two different approaches to enable data-centric computing. First, near-memory computing (NMC), which adds processing capabilities closer to the existing memory architectures. Second, computation-in memory (CIM), which exploits the memory architecture and intrinsic properties of emerging technologies to perform operations using memory itself. This thesis focuses on NMC-based architectures and techniques to overcome the data movement bottleneck.

This chapter analyzes NMC-based architectures across various dimensions and highlights that NMC is still in its infancy. We need to address multiple architectural challenges before NMC can be established as an essential component of HPC systems to accelerate data-intensive workloads. Besides designing and evaluating NMC processing capabilities for data-intensive workloads, we stress the demand for sophisticated tools and techniques to enable the design space exploration for these novel architectures. Further, we need to solve various challenges related to the overall system integration. To overcome these challenges, we should consider data as a paramount resource and provide various mechanisms to handle and leverage the vast amount of data. In this dissertation, we tackle the above challenges in three different ways. First, we demonstrate NMC processing capabilities for a real-world data-intensive weather prediction application. Second, we provide data-driven machine learning-based solutions that allow quick and accurate performance estimation during the design-time. Third, we leverage the vast amount of available data to drive run-time system-level decisions.

Chapter 3

NERO: A Near-High Bandwidth Memory Stencil Accelerator for Weather Prediction Modeling

Modern data-intensive applications demand high compute capabilities with strict power constraints. Unfortunately, such applications suffer from a significant waste of both execution cycles and energy in current computing systems due to the costly data movement between the compute units and the memory units. Weather prediction modeling is one such data-intensive application where we generate petabytes of data. Moreover, ongoing climate change calls for fast and accurate weather and climate modeling. However, when solving large-scale weather prediction simulations, state-of-the-art CPU and GPU implementations suffer from limited performance and high energy consumption. These implementations are dominated by complex irregular memory access patterns and low arithmetic intensity that pose fundamental challenges to acceleration. To overcome these challenges, in this chapter, we propose and evaluate the use of near-memory acceleration using a reconfigurable fabric with high-bandwidth memory (HBM).

The content of this chapter was published as “*NERO: A Near High-Bandwidth Memory Stencil Accelerator for Weather Prediction Modeling*” in FPL 2020. (*Nominated for the Stamatis Vassiliadis Memorial Best Paper Award*)

Our earlier work was published as “*NARMADA: Near-Memory Horizontal Diffusion Accelerator for Scalable Stencil Computations*” in FPL 2019 where we accelerate only horizontal diffusion kernel from the COSMO (Consortium for Small-Scale Modeling) model.

3.1 Introduction

Accurate weather prediction using detailed weather models is essential to make weather-dependent decisions in a timely manner. The Consortium for Small-Scale Modeling (COSMO) [116] built one such weather model to meet the high-resolution forecasting requirements of weather services. The COSMO model is a non-hydrostatic atmospheric prediction model currently being used by a dozen nations for meteorological purposes and research applications.

The central part of the COSMO model (called *dynamical core* or *dycore*) solves the Euler equations on a curvilinear grid and applies implicit discretization (i.e., parameters are dependent on each other at the same time instance [56]) in the vertical dimension and explicit discretization (i.e., a solution is dependent on the previous system state [56]) in the horizontal dimension. The use of different discretizations leads to three computational patterns [458]: 1) horizontal stencils, 2) tridiagonal solvers in the vertical dimension, and 3) point-wise computation. These computational kernels are compound stencil kernels that operate on a three-dimensional grid [167]. *Vertical advection* (`vadv`) and *horizontal diffusion* (`hdiff`) are such compound kernels found in the *dycore* of the COSMO weather prediction model. These kernels are representative of the data access patterns and algorithmic complexity of the entire COSMO model. They are similar to the kernels used in other weather and climate models [227, 338, 529]. Their performance is dominated by memory-bound operations with unique irregular memory access patterns and low arithmetic intensity that often results in <10% sustained floating-point performance on current CPU-based systems [290].

Figure 3-1 shows the roofline plot [501] for an IBM 16-core POWER9 CPU (IC922).¹ After optimizing the `vadv` and `hdiff` kernels for the POWER architecture by following the approach in [515], they achieve 29.1 GFLOP/s and 58.5 GFLOP/s, respectively, for 64 threads. Our roofline analysis indicates that these kernels are constrained by the host DRAM bandwidth. Their low arithmetic intensity limits their performance, which is one order of magnitude smaller than the peak performance, and results in a fundamental memory bottleneck that standard CPU-based optimization techniques cannot overcome.

Our goal is to overcome the memory bottleneck of weather prediction kernels by exploiting near-memory computation capability on FPGA accelerators with high-bandwidth memory (HBM) [179, 251, 252] that are attached to the host CPU. Figure 3-1 shows the roofline models of the two FPGA cards (AD9V3 [5] and AD9H7 [4]) used in this chapter. FPGAs can handle irregular memory access patterns efficiently and offer significantly higher memory bandwidth than the host CPU with their on-chip URAMs

¹IBM and POWER9 are registered trademarks or common law marks of International Business Machines Corp., registered in many jurisdictions worldwide. Other product and service names might be trademarks of IBM or other companies.

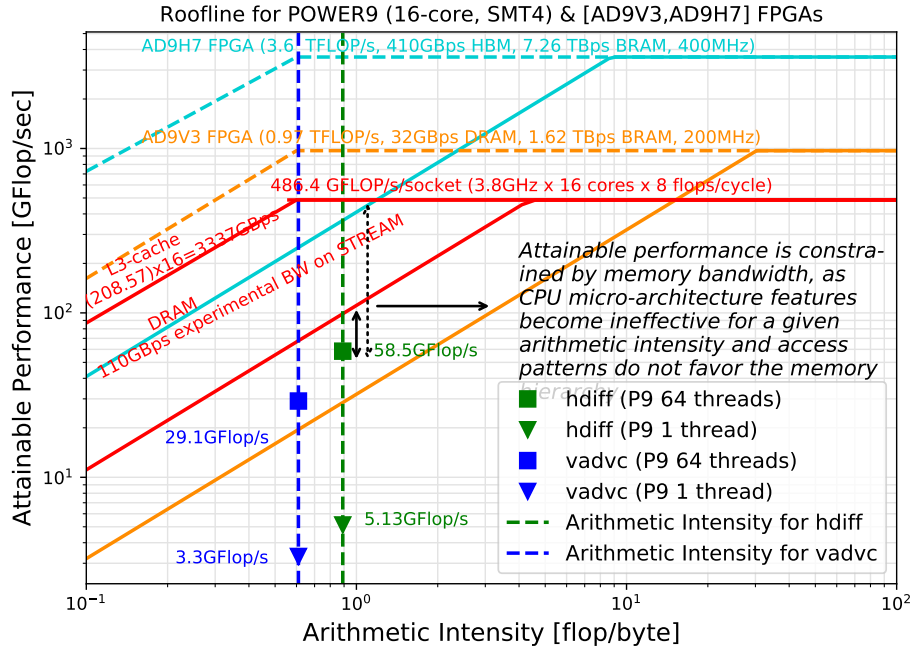


Figure 3-1: Roofline [501] for POWER9 (1-socket) showing vertical advection (vadvc) and horizontal diffusion (hdiff) kernels for single-thread and 64-thread implementations. The plot shows also the rooflines of the FPGAs used in this chapter

(UltraRAM), BRAMs (block RAM), and off-chip HBM (high-bandwidth memory for the AD9H7 card). However, taking full advantage of FPGAs for accelerating a workload is not a trivial task. To compensate for the higher clock frequency of the baseline CPUs, our FPGAs must exploit at least one order of magnitude more parallelism in a target workload. This is challenging, as it requires sufficient FPGA programming skills to map the workload and optimize the design for the FPGA microarchitecture.

As mentioned in Section 1.1.1, modern FPGA boards deploy new cache-coherent interconnects, such as IBM Coherent Accelerator Processor Interface (CAPI) [444], Cache Coherent Interconnect for Accelerators (CCIX) [49], and Compute Express Link (CXL) [421], which allow tight integration of FPGAs with CPUs at high bidirectional bandwidth (on the order of tens of GB/s). However, memory-bound applications on FPGAs are limited by the relatively low DDR4 bandwidth (72 GB/s for four independent dual-rank DIMM interfaces [513]). To overcome this limitation, FPGA vendors have started offering devices equipped with HBM [180, 194, 252, 514] with a theoretical peak bandwidth of 410 GB/s. HBM-equipped FPGAs have the potential to reduce the memory bandwidth bottleneck, but a study of their advantages for real-world memory-bound applications is still missing.

We aim to answer the following research question: **Can FPGA-based accelerators with HBM mitigate the performance bottleneck of memory-bound compound weather prediction kernels in an energy-efficient way?** As an answer to this question, we present NERO, a near-HBM accelerator for weather prediction. We design and implement NERO on an FPGA with HBM to optimize two kernels (vertical advection and horizontal diffusion), which notably represent the spectrum of computational diversity found in the COSMO weather prediction application. We co-design a hardware-software framework and provide an optimized API to interface efficiently with the rest of the COSMO model, which runs on the CPU. Our FPGA-based solution for `hdiff` and `vadv` leads to performance improvements of $4.2\times$ and $8.3\times$ and energy reductions of $22\times$ and $29\times$, respectively, with respect to optimized CPU implementations [515].

3.2 Background

In this section, we first provide an overview of the `vadv` and `hdiff` compound stencils, which represent a large fraction of the overall computational load of the COSMO weather prediction model. Second, we introduce the CAPI SNAP (Storage, Network, and Analytics Programming) framework² that we use to connect our NERO accelerator to an IBM POWER9 system.

3.2.1 Representative COSMO Stencils

A stencil operation updates values in a structured multidimensional grid based on the values of a fixed local neighborhood of grid points. Vertical advection (`vadv`) and horizontal diffusion (`hdiff`) from the COSMO model are two such compound stencil kernels, which represent the typical code patterns found in the *dycore* of COSMO. Algorithm 1 shows the pseudo-code for `vadv` and `hdiff` kernels. The horizontal diffusion kernel iterates over a 3D grid performing *Laplacian* and *flux* to calculate different grid points, as shown in Figure 3-2. Vertical advection has a higher degree of complexity since it uses the Thomas algorithm [460] to solve a tri-diagonal matrix of the velocity field along the vertical axis. Unlike the conventional stencil kernels, vertical advection has dependencies in the vertical direction, which leads to limited available parallelism.

Such compound kernels are dominated by memory-bound operations with complex memory access patterns and low arithmetic intensity. This poses a fundamental challenge to acceleration. CPU implementations of these kernels [515] suffer from

²<https://github.com/open-power/snap>

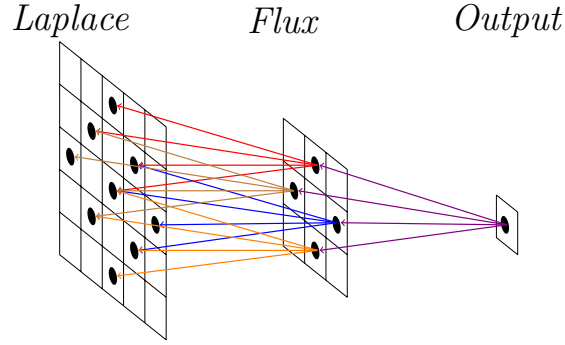


Figure 3-2: Horizontal diffusion compound kernel composition in a two dimensional plane

Algorithm 1 Pseudo-code for vertical advection and horizontal diffusion kernels used by the COSMO [116] weather prediction model

```

1: function VERTICALADVECTION(float * ccol, float * dcol, float * wcon, float * ustage,
                             float * upos, float * utens, float * utensstage)
2:   for c ← 2 to column - 2 do
3:     for r ← 2 to row-2 do
4:       function FORWARDSWEEP(float * ccol, float * dcol, float * wcon, float * ustage,
                               float * upos, float * utens, float * utensstage)
5:         for d ← 1 to depth do
6:           /* forward sweep calculation */
7:           function BACKWARDSWEEP(float * ccol, float * dcol, float * wcon, float * ustage,
                                   float * upos, float * utens, float * utensstage)
8:             for d ← depth - 1 to 1 do
9:               /* backward sweep calculation */
10: function HORIZONTALDIFFUSION(float * src, float * dst)
11:   for d ← 1 to depth do
12:     for c ← 2 to column - 2 do
13:       for r ← 2 to row-2 do
14:         /* Laplacian calculation */
15:         lapCR = laplaceCalculate(c, r)
16:         /* row-laplacian */
17:         lapCRm = laplaceCalculate(c, r - 1)
18:         lapCRp = laplaceCalculate(c, r + 1)
19:         /* column-laplacian */
20:         lapCmR = laplaceCalculate(c - 1, r)
21:         lapCpR = laplaceCalculate(c + 1, r)
22:         /* column-flux calculation */
23:         fluxC = lapCpR - lapCR
24:         fluxCm = lapCR - lapCmR
25:         /* row-flux calculation */
26:         fluxR = lapCRp - lapCR
27:         fluxRm = lapCR - lapCmR
28:         /* output calculation */
29:         dest[d][c][r] = src[d][c][r] - c1 * (fluxCR - fluxCmR) + (fluxCR - fluxCRm)

```

limited data locality and inefficient memory usage, as our roofline analysis in Figure 3-1 exposes.

3.2.2 CAPI SNAP Framework

The OpenPOWER Foundation Accelerator Workgroup [353] created the CAPI SNAP framework, an open-source environment for FPGA programming productivity.

CAPI SNAP provides two key benefits [499]: (i) it enables an improved developer productivity for FPGA acceleration and eases the use of CAPI’s cache-coherence mechanism, and (ii) it places FPGA-accelerated compute engines, also known as FPGA *actions*, closer to relevant data to achieve better performance. SNAP provides a simple API to invoke an accelerated *action*, and also provides programming methods to instantiate customized accelerated *actions* on the FPGA side. These accelerated *actions* can be specified in C/C++ code that is then compiled to the FPGA target using the Xilinx Vivado High-Level Synthesis (HLS) tool [484].

3.3 Design Methodology

3.3.1 NERO, A Near HBM Weather Prediction Accelerator

The low arithmetic intensity of real-world weather prediction kernels limits the attainable performance on current multi-core systems. This sub-optimal performance is due to the kernels’ complex memory access patterns and their inefficiency in exploiting a rigid cache hierarchy, as quantified in the roofline plot in Figure 3-1. These kernels cannot fully utilize the available memory bandwidth, which leads to high data movement overheads in terms of latency and energy consumption. We address these inefficiencies by developing an architecture that combines fewer off-chip data accesses with higher throughput for the loaded data. To this end, our accelerator design takes a data-centric approach [11, 12, 57, 147, 182, 183, 234, 330, 432, 437] that exploits near high-bandwidth memory acceleration.

Figure 3-3a shows a high-level overview of our integrated system. An HBM-based FPGA is connected to a server system based on an IBM POWER9 processor using the Coherent Accelerator Processor Interface version 2 (CAPI2). The FPGA consists of two HBM stacks³, each with 16 *pseudo-memory channels* [35]. A channel is exposed to the FPGA as a 256-bit wide port, and in total, the FPGA has 32 such ports. The HBM IP provides 8 memory controllers (per stack) to handle the data transfer to and from the HBM memory ports. Our design consists of an *accelerator functional unit* (AFU) that interacts with the host system through the power service layer (PSL), which is the CAPI endpoint on the FPGA. An AFU comprises of multiple *processing elements* (PEs) that perform compound stencil computation. Figure 3-4 shows the architecture overview of NERO. As vertical advection is the most complex kernel, we depict our architecture design flow for vertical advection. We use a similar design for the horizontal diffusion kernel.

The weather data, based on the atmospheric model resolution grid, is stored in

³We enable only a single stack based on our resource and power consumption analysis for the vadvc kernel.

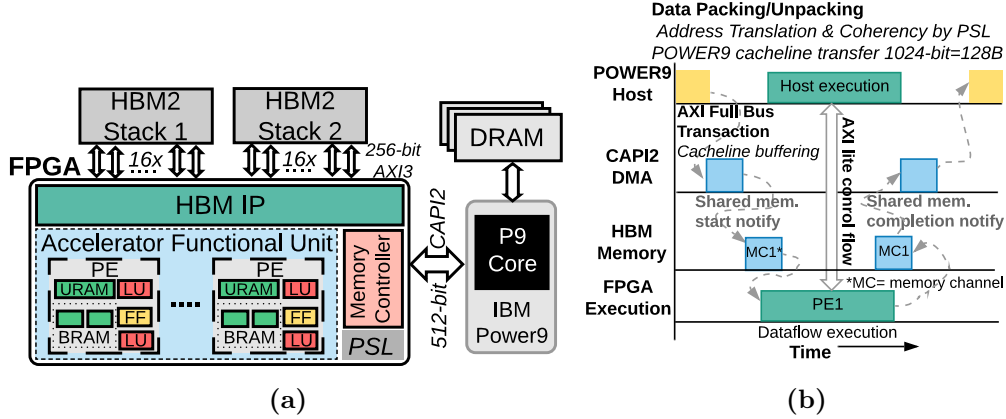


Figure 3-3: (a) Heterogeneous platform with an IBM POWER9 system connected to an HBM-based FPGA board via CAPI2. (b) Execution timeline with data flow sequence from the host DRAM to the onboard FPGA memory

the DRAM of the host system (❶ in Figure 3-4). We employ the double buffering technique between the CPU and the FPGA to hide the PCIe (Peripheral Component Interconnect Express [305]) transfer latency. By configuring a buffer of 64 cache lines, between the AXI4 interface of CAPI2/PSL and the AFU, we can reach the theoretical peak bandwidth of CAPI2/PCIe (x8 PCIe Gen4 interface with a theoretical peak bandwidth 15.75 GB/s and a transfer rate of 16 GT/s). We create a specialized memory hierarchy from the heterogeneous FPGA memories (i.e., URAM, BRAM, and HBM). By using a greedy algorithm, we determine the best-suited hierarchy for our kernel. The memory controller (shown in Figure 3-3a) handles the data placement to the appropriate memory type based on programmer’s directives.

On the FPGA, following the initial buffering (❷), the transferred grid data is mapped onto the HBM memory (❸). As the FPGA has limited resources, we propose a 3D window-based grid transfer from the host DRAM to the FPGA, facilitating a smaller, less power-hungry deployment. The window size represents the portion of the grid a processing element (PE in Figure 3-3a) would process. Most FPGA developers manually optimize for the right window size. However, manual optimization is tedious because of the huge design space, and it requires expert guidance. Further, selecting an inappropriate window size leads to sub-optimal results. Our experiments (in Section 3.4.2) show that: (1) finding the best window size is critical in terms of the area vs. performance trade-off, and (2) the best window size depends on the datatype precision. Hence, instead of pruning the design space manually, we formulate the search for the best window size as a multi-objective auto-tuning problem taking into account the datatype precision. We make use of OpenTuner [26], which uses machine-learning techniques to guide the design-space exploration.

Our design consists of multiple PEs (shown in Figure 3-3a) that exploit data-level

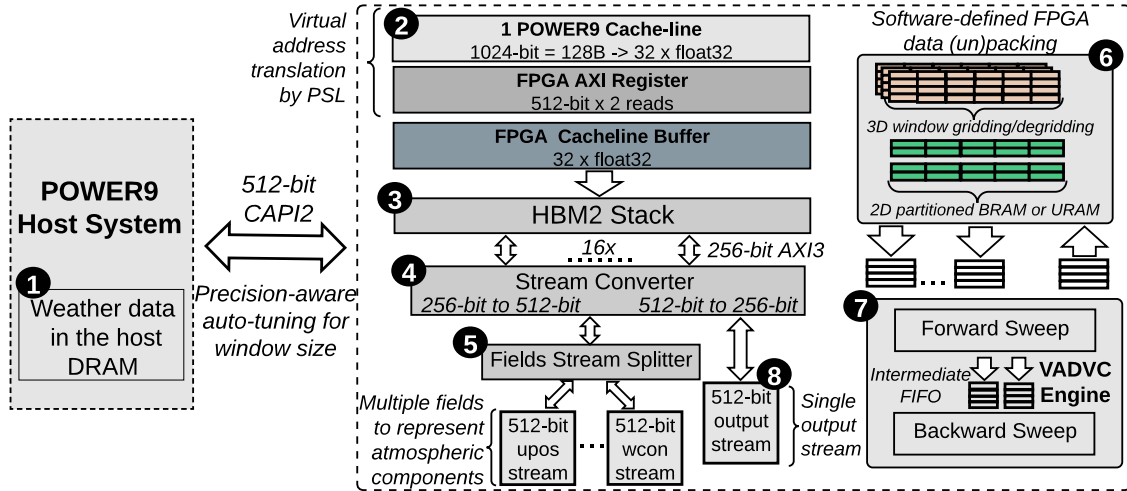


Figure 3-4: Architecture overview of NERO with data flow sequence from the host DRAM to the on-board FPGA memory via POWER9 cachelines. We depict a single processing element (PE) fetching data from a dedicated HBM port. The number of HBM ports scales linearly with the number of PEs. Heterogeneous partitioning of on-chip memory blocks reduces read and write latencies across the FPGA memory hierarchy

parallelism in COSMO weather prediction kernels. A dedicated HBM memory port is assigned to a specific PE; therefore, we enable as many HBM ports as the number of PEs. This allows us to use the high HBM bandwidth effectively because each PE fetches from an independent port. In our design, we use a switch, which provides the capability to bypass the HBM, when the grid size is small, and map the data directly onto the FPGA’s URAM and BRAM. The HBM port provides 256-bit data, which is half the size of the CAPI2 bitwidth (512-bit). Therefore, to match the CAPI2 bandwidth, we introduce a stream converter logic (4) that converts a 256-bit HBM stream to a 512-bit stream (CAPI compatible) or vice versa. From HBM, a PE reads a single stream of data that consists of all the fields⁴ that are needed for a specific COSMO kernel computation. The PEs use a fields stream splitter logic (5) that splits a single HBM stream to multiple streams (512-bit each), one for each field.

To optimize a PE, we apply various optimization strategies. First, we exploit the inherent parallelism in a given algorithm through hardware pipelining. Second, we partition on-chip memory to avoid the stalling of our pipelined design, since the on-chip BRAM/URAM has only two read/write ports. Third, all the tasks execute in a dataflow manner that enables task-level parallelism. `vadvc` is more computationally complex than `hdiff` because it involves forward and backward sweeps

⁴Fields represent atmospheric components like wind, pressure, velocity, etc. that are required for weather calculation.

with dependencies in the z-dimension. While `hdiff` performs only Laplacian and flux calculations with dependencies in the x- and y-dimensions. Therefore, we demonstrate our design flow by means of the `vadvc` kernel (Figure 3-4). Note that we show only a single port-based PE operation. However, for multiple PEs, we enable multiple HBM ports.

We make use of memory reshaping techniques to configure our memory space with multiple parallel BRAMs or URAMs [113]. We form an intermediate memory hierarchy by decomposing (or slicing) 3D window data into a 2D grid. This allows us to bridge the latency gap between the HBM memory and our accelerator. Moreover, it allows us to exploit the available FPGA resources efficiently. Unlike traditionally-fixed CPU memory hierarchies, which perform poorly with irregular access patterns and suffer from cache pollution effects, application-specific memory hierarchies are shown to improve energy and latency by tailoring the cache levels and cache sizes to an application’s memory access patterns [465].

The main computation pipeline (⑦) consists of a forward and a backward sweep logic. The forward sweep results are stored in an intermediate buffer to allow for backward sweep calculation. Upon completion of the backward sweep, results are placed in an output buffer that is followed by a degridding logic (⑥). The degridding logic converts the calculated results to a 512-bit wide output stream (⑧). As there is only a single output stream (both in `vadvc` and `hdiff`), we do not need extra logic to merge the streams. The 512-bit wide stream goes through an HBM stream converter logic (④) that converts the stream bitwidth to HBM port size (256-bit).

Figure 3-3b shows the execution timeline from our host system to the FPGA board for a single PE. The host offloads the processing to an FPGA and transfers the required data via DMA (direct memory access) over the CAPI2 interface. The SNAP framework allows for parallel execution of the host and our FPGA PEs while exchanging control signals over the AXI lite interface [36]. On task completion, the AFU notifies the host system via the AXI lite interface and transfers back the results via DMA.

3.3.2 NERO Application Framework

Figure 3-5 shows the NERO application framework to support our architecture. A software-defined COSMO API (①) handles offloading jobs to NERO with an interrupt-based queuing mechanism. This allows for minimal CPU usage (and, hence, power usage) during FPGA operation. NERO employs an array of processing elements to compute COSMO kernels, such as vertical advection or horizontal diffusion. Additionally, we pipeline our PEs to exploit the available spatial parallelism. By accessing the host memory through the CAPI2 cache-coherent link, NERO acts as a peer to the CPU. This is enabled through the Power-Service Layer (PSL) (②). SNAP (③)

allows for seamless integration of the COSMO API with our CAPI-based accelerator. The job manager (④) dispatches jobs to streams, which are managed in the stream scheduler (⑤). The execution of a job is done by streams that determine which data is to be read from the host memory and sent to the PE array through DMA transfers (⑥). The pool of heterogeneous on-chip memory is used to store the input data from the main memory and the intermediate data generated by each PE.

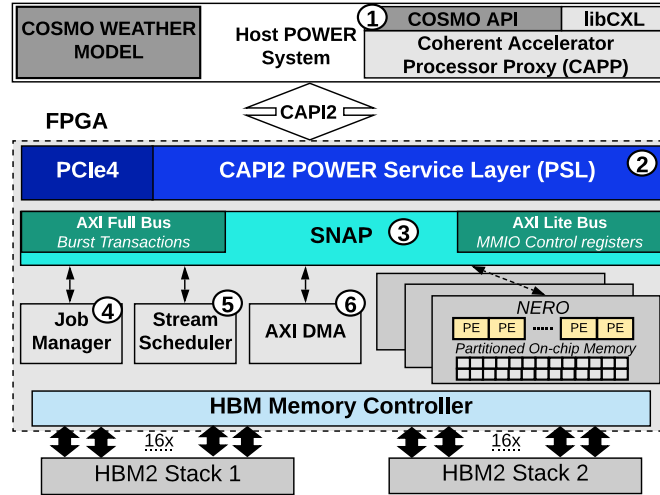


Figure 3-5: NERO application framework. We co-design our software and hardware using the SNAP framework. COSMO API allows the host to offload kernels to our FPGA platform

3.4 Results

3.4.1 System Integration

We implemented our design on an Alpha-Data ADM-PCIE-9H7 card [4] featuring the Xilinx Virtex Ultrascale+ XCVU37P-FSVH2892-2-e [479] and 8GiB HBM2 (i.e., two stacks of 4GiB each) [179] with an IBM POWER9 as the host system. The POWER9 socket has 16 cores, each of which supports four-thread simultaneous multi-threading. We compare our HBM-based design to a conventional DDR4 DRAM [5] based design. We perform the experiments for the DDR4-based design on an Alpha-Data ADM-PCIE-9V3 card featuring the Xilinx Virtex Ultrascale+ XCVU3P-FFVC1517-2-i [479].

Table 3.1 provides our system parameters. We have co-designed our hardware and software interface around the SNAP framework while using the HLS design flow.

Table 3.1: System parameters and hardware configuration for the CPU and the FPGA board

Host CPU	16-core IBM POWER9 AC922 @3.2 GHz, 4-way SMT
Cache-Hierarchy	32 KiB L1-I/D, 256 KiB L2, 10 MiB L3
System Memory	16x32GiB RDIMM DDR4 2666 MHz
HBM-based FPGA Board	Alpha Data ADM-PCIE-9H7 Xilinx Virtex Ultrascale+ XCVU37P-2 8GiB (HBM2) with PCIe Gen4 x8
DDR4-based FPGA Board	Alpha Data ADM-PCIE-9V3 Xilinx Virtex Ultrascale+ XCVU3P-2 8GiB (DDR4) with PCIe Gen4 x8

3.4.2 Evaluation

We run our experiments using a $256 \times 256 \times 64$ -point domain similar to the grid domain used by the COSMO weather prediction model. We employ an auto-tuning technique to determine a Pareto-optimal solution (in terms of performance and resource utilization) for our 3D window dimensions. The auto-tuning with OpenTuner exhaustively searches for every tile size in the x- and y-dimensions for `vadvc`.⁵ For `hdiff`, we consider sizes in all three dimensions. We define our auto-tuning as a multi-objective optimization with the goal of maximizing performance with minimal resource utilization. Section 3.3 provides further details on our design. Figure 3-6 shows hand-tuned and auto-tuned performance and FPGA resource utilization results for `vadvc`, as a function of the chosen tile size. From the figure, we draw two observations.

First, by using the auto-tuning approach and our careful FPGA microarchitecture design, we can get Pareto-optimal results with a tile size of $64 \times 2 \times 64$ for single-precision `vadvc`, which gives us a peak performance of 8.49 GFLOP/s. For half-precision, we use a tile size of $32 \times 16 \times 64$ to achieve a peak performance of 16.5 GFLOP/s. We employ a similar strategy for `hdiff` to attain a single-precision performance of 30.3 GFLOP/s with a tile size of $16 \times 64 \times 8$ and a half-precision performance of 77.8 GFLOP/s with a tile size of $64 \times 8 \times 64$.

Second, in FPGA acceleration, designers usually rely on expert judgement to find the appropriate tile-size and often adapt the design to use homogeneous tile sizes. However, as shown in Figure 3-6, such hand-tuned implementations lead to sub-optimal results in terms of either resource utilization or performance.

We conclude that the Pareto-optimal tile size depends on the data precision used: a good tile-size for single-precision might lead to poor results when used with half-precision.

⁵`vadvc` has dependencies in the z-dimension; therefore, it cannot be parallelized in the z-dimension.

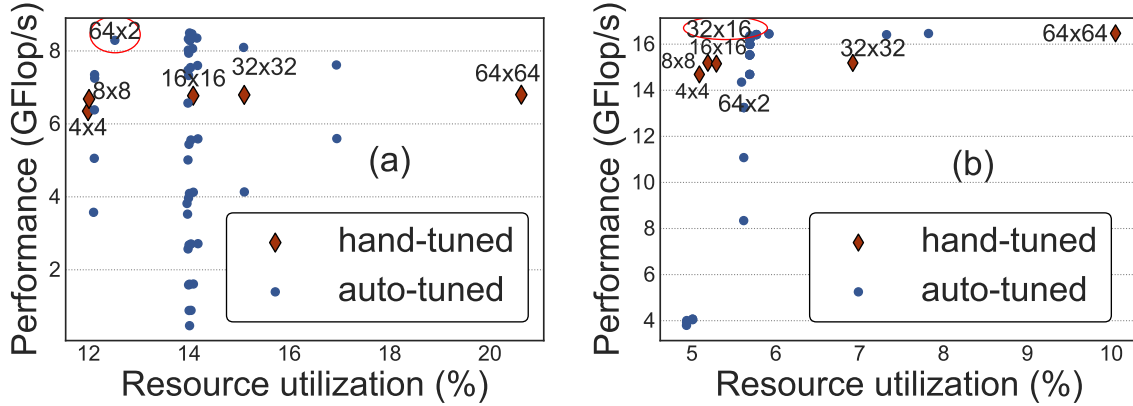


Figure 3-6: Performance and FPGA resource utilization of single vadvc PE, as a function of tile-size, using hand-tuning and auto-tuning for (a) single-precision (32-bit) and (b) half-precision (16-bit). We highlight the Pareto-optimal solution that we use for our vadvc accelerator (with a red circle). Note that the Pareto-optimal solution changes with precision

Figure 3-7 shows single-precision performance results for the (a) vertical advection and (b) horizontal diffusion kernels. For both kernels, we implement our design on an HBM- and a DDR4-based FPGA board. To compare the performance results, we scale the number of PEs and analyze the change in execution time. For the DDR4-based design, we can accommodate only 4 PEs on the 9V3 board, while for the HBM-based design, we can fit 14 PEs before exhausting the on-board resources. We draw four observations from the figure.

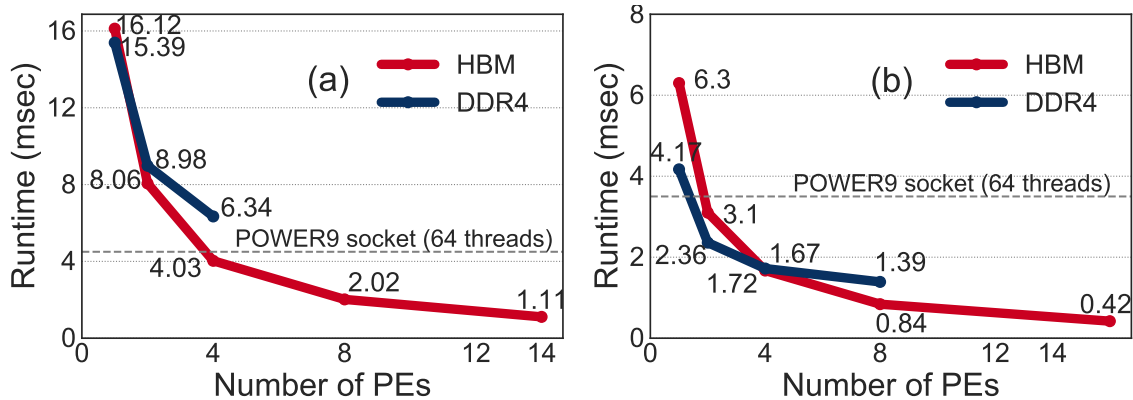


Figure 3-7: Single-precision performance for (a) vadvc and (b) hdiff, as a function of accelerator PE count on the HBM- and DDR4-based FPGA boards. We also show the single socket (64 threads) performance of an IBM POWER9 host system for both vadvc and hdiff

First, our full-blown HBM-based vadvc and hdiff implementations provide 157.1 GFLOP/s and 608.4 GFLOP/s performance, which are $4.2\times$ and $8.3\times$ higher than the performance of a complete POWER9 socket. For half-precision, if we use the

same amount of PEs as in single precision, our accelerator reaches a performance of 247.9 GFLOP/s for `vadvc` ($2.1\times$ the single-precision performance) and 1.2 TFLOP/s for `hdiff` ($2.5\times$ the single-precision performance). Our DDR4-based design achieves 34.1 GFLOP/s and 145.8 GFLOP/s for `vadvc` and `hdiff`, respectively, which are $1.2\times$ and $2.5\times$ the performance on the POWER9 CPU.

Second, for a single PE, which fetches data from a single memory channel, the DDR4-based design provides higher performance than the HBM-based design. This is because the DDR4-based FPGA has a larger bus width (512-bit) than an HBM port (256-bit). This leads to a lower transfer rate for an HBM port ($0.8\text{-}2.1$ GT/s⁶) than for a DDR4 port ($2.1\text{-}4.3$ GT/s). One way to match the DDR4 bus width would be to have a single PE fetch data from multiple HBM ports in parallel. However, using more ports leads to higher power consumption (~ 1 Watt per HBM port).

Third, as we increase the number of PEs, we observe a linear reduction in the execution time of the HBM-based design. This is because we can evenly divide the computation between multiple PEs, each of which fetches data from a separate HBM port.

Fourth, in the DDR4-based design, the use of only a single channel to feed multiple PEs leads to a congestion issue that causes a non-linear run-time reduction. As we increase the number of accelerator PEs, we observe that the PEs compete for a single memory channel, which causes frequent stalls. This phenomenon leads to worse performance scaling characteristics for the DDR4-based design as compared to the HBM-based design.

3.4.3 Energy Analysis

We compare the energy consumption of our accelerator to a 16-core POWER9 host system. For the POWER9 system, we use the AMESTER⁷ tool to measure the active power⁸ consumption. We measure 99.2 Watts for `vadvc`, and 97.9 Watts for `hdiff` by monitoring built-in power sensors in the POWER9 system.

By executing these kernels on an HBM-based board, we reduce the energy consumption by $22\times$ for `vadvc` and $29\times$ for `hdiff` compared to the 16-core POWER9 system. Figure 3-8 shows the energy efficiency (GFLOPS per Watt) for `vadvc` and `hdiff` on the HBM- and DDR4-based designs. We make three major observations from the figure.

First, with our full-blown HBM-based designs (i.e., 14 PEs for `vadvc` and 16 PEs for `hdiff`), we achieve energy efficiency values of 1.5 GFLOPS/Watt and 17.3 GFLOP-

⁶Gigatransfers per second.

⁷<https://github.com/open-power/amester>

⁸Active power denotes the difference between the total power of a complete socket (including CPU, memory, fans, I/O, etc.) when an application is running compared to when it is idle.

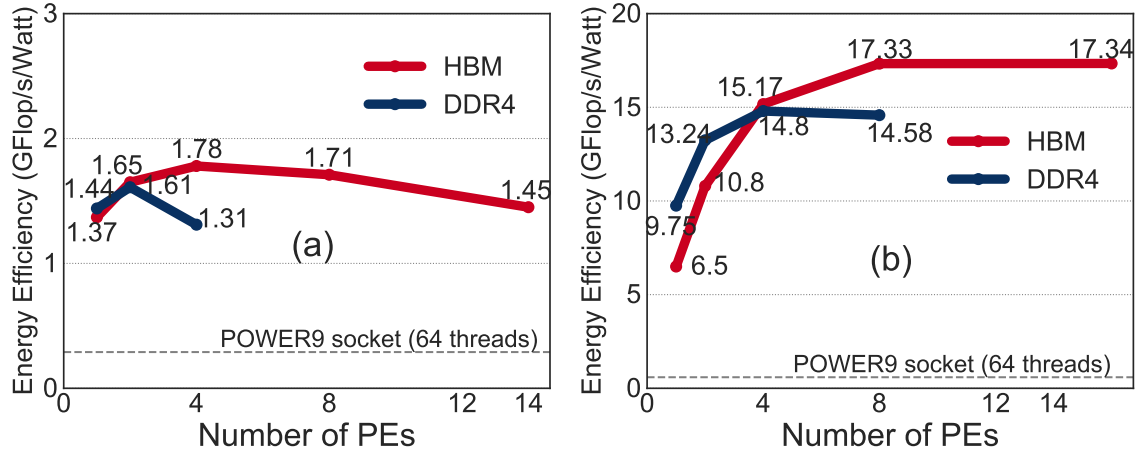


Figure 3-8: Energy efficiency for (a) `vadvc` and (b) `hdiff` on HBM- and DDR4-based FPGA boards. We also show the single socket (64 threads) energy efficiency of an IBM POWER9 host system for both `vadvc` and `hdiff`

S/Watt for `vadvc` and `hdiff`, respectively.

Second, the DDR4-based design is more energy efficient than the HBM-based design when the number of PEs is small. This observation is inline with our discussion about performance with small PE counts in Section 3.4.2. However, as we increase the number of PEs, the HBM-based design provides better energy efficiency for memory-bound kernels. This is because more HBM data can be fetched and processed in parallel via multiple ports.

Third, kernels like `vadvc`, with intricate memory access patterns, are not able to reach the peak computational power of FPGAs. The large amount of control flow in `vadvc` leads to large resource consumption. Therefore, when increasing the PE count, we observe a high increase in power consumption with low energy efficiency.

We conclude that enabling many HBM ports might not always be beneficial in terms of energy consumption because each HBM port consumes ~ 1 Watt of power consumption. However, data-parallel kernels like `hdiff` can achieve much higher performance in an energy efficient manner with more PEs and HBM ports.

3.4.4 FPGA Resource Utilization

Table 3.2 shows the resource utilization of `vadvc` and `hdiff` on the AD9H7 board. We draw two observations. First, there is a high BRAM consumption compared to other FPGA resources. This is because we implement input, field, and output signals as `hls::streams`. In high-level synthesis, by default, streams are implemented as FIFOs that make use of BRAM. Second, `vadvc` has a much larger resource consumption than `hdiff` because `vadvc` has higher computational complexity and requires a larger number of fields to perform the compound stencil calculation. Note that for `hdiff`,

we can accommodate more PEs, but in this thesis, we make use of only a single HBM stack. Therefore, we use 16 PEs because a single HBM stack offers 16 memory ports.

Table 3.2: FPGA resource utilization in our highest-performing HBM-based designs for `vadv` and `hdiff`

Algorithm	BRAM	DSP	FF	LUT	URAM
<code>vadv</code>	81%	39%	37%	55%	53%
<code>hdiff</code>	58%	4%	6%	11%	8%

3.5 Related Work

To our knowledge, this is the first thesis to evaluate the benefits of using FPGAs equipped with high-bandwidth memory (HBM) to accelerate stencil computation. We exploit near-memory capabilities of such FPGAs to accelerate important weather prediction kernels.

Modern workloads exhibit limited locality and operate on large amounts of data, which causes frequent data movement between the memory subsystem and the processing units [57, 147, 329, 330]. This frequent data movement has a severe impact on overall system performance and energy efficiency. A way to alleviate this *data movement bottleneck* [57, 147, 329, 330, 432] is *near-memory computing* (NMC), which consists of placing processing units closer to memory. NMC is enabled by new memory technologies, such as 3D-stacked memories [179, 233, 251, 252, 367], and also by cache-coherent interconnects [49, 421, 444], which allow close integration of processing units and memory units. Depending on the applications and systems of interest (e.g., [11, 12, 13, 31, 38, 57, 59, 86, 129, 146, 175, 176, 183, 219, 231, 257, 260, 285, 323, 332, 418]), prior works propose different types of near-memory processing units, such as general-purpose CPU cores [11, 15, 57, 58, 59, 105, 241, 260, 334, 382, 407], GPU cores [149, 182, 365, 527], reconfigurable units [145, 199, 212, 435], or fixed-function units [12, 160, 175, 176, 183, 234, 280, 332].

FPGA accelerators are promising to enhance overall system performance with low power consumption. Past works [17, 18, 19, 78, 112, 151, 185, 204, 212, 222, 256] show that FPGAs can be employed effectively for a wide range of applications. The recent addition of HBM to FPGAs presents an opportunity to exploit high memory bandwidth with the low-power FPGA fabric. The potential of high-bandwidth memory [179, 252] has been explored in many-core processors [149, 376] and GPUs [149, 539]. A recent work [495] shows the potential of HBM for FPGAs with a memory benchmarking tool. NERO is the first work to accelerate a real-world HPC weather prediction application using the FPGA+HBM fabric. Compared to a previous work [435] that optimizes

only the horizontal diffusion kernel on an FPGA with DDR4 memory, our analysis reveals that the vertical advection kernel has a much lower compute intensity with little to no regularity. Therefore, this thesis accelerates both kernels that together represent the algorithmic diversity of the entire COSMO weather prediction model. Moreover, compared to [435], NERO improves performance by $1.2\times$ on a DDR4-based board and $37\times$ on an HBM-based board for horizontal diffusion by using a dataflow implementation with auto-tuning.

Enabling higher performance for stencil computations has been a subject of optimizations across the whole computing stack [30, 87, 94, 103, 134, 157, 167, 177, 309, 406, 443, 454, 487]. Szustak *et al.* accelerate the MPDATA advection scheme on multi-core CPU [452] and computational fluid dynamics kernels on FPGA [245]. Bianco *et al.* [54] optimize the COSMO weather prediction model for GPUs while Thaler *et al.* [458] port COSMO to a many-core system. Wahib *et al.* [486] develop an analytical performance model for choosing an optimal GPU-based execution strategy for various scientific applications, including COSMO. Gysi *et al.* [167] provide guidelines for optimizing stencil kernels for CPU-GPU systems.

3.6 Conclusion

We introduce NERO, the first design and implementation on a reconfigurable fabric with high-bandwidth memory (HBM) to accelerate representative weather prediction kernels, i.e., vertical advection (`vadv`) and horizontal diffusion (`hdiff`), from a real-world weather prediction application. These kernels are compound stencils that are found in various weather prediction applications, including the COSMO model. We show that compound kernels do not perform well on conventional architectures due to their complex data access patterns and low data reusability, which make them memory-bounded. Therefore, they greatly benefit from our near-memory computing solution that takes advantage of the high data transfer bandwidth of HBM.

NERO’s implementations of `vadv` and `hdiff` outperform the optimized software implementations on a 16-core POWER9 with 4-way multithreading by $4.2\times$ and $8.3\times$, with $22\times$ and $29\times$ less energy consumption, respectively. We conclude that hardware acceleration on an FPGA+HBM fabric is a promising solution for compound stencils present in weather prediction applications. We hope that our reconfigurable near-memory accelerator inspires developers of different high-performance computing applications that suffer from the memory bottleneck.

Chapter 4

Low Precision Processing for High Order Stencil Computations

Modern scientific workloads have demonstrated the inefficiency of using high-precision formats. Moving to a lower bit format or even to a different number system can provide tremendous gains in terms of performance and energy efficiency. This chapter explores the applicability of different number formats and searches for the appropriate bit-width for three-dimensional stencil kernels, which are among the most widely used scientific workloads. Further, we demonstrate the achievable performance of these kernels on state-of-the-art hardware that includes a host CPU connected to an FPGA. An FPGA provides us with the capability to implement arbitrary fixed-point precision. Thus, this chapter fills the gap between current hardware capabilities and future systems for stencil-based scientific applications.

4.1 Introduction

Stencil computation is essential for numerical simulations of finite difference methods (FDM) [357] and is applied in iterative solvers of linear equation systems. We use stencil computation in a wide range of applications, including computational fluid dynamics [187], image processing [178], weather prediction modeling [116], etc. A stencil operation [167] defines a computation sequence where elements in a multidimensional grid are updated using data values from a subset of its neighbors based on a fixed pattern.

Stencil computation is applied to data structures that are generally much larger

The content of this chapter was published as “*Low Precision Processing for High Order Stencil Computations*” in Springer LNCS 2019.

than the available system’s cache capacity [104]. Stencils are cache-unfriendly because the amount of data reuse within a stencil iteration is limited to the number of points in a stencil. Due to the cache-unfriendly, complex data access patterns, and low operational intensity [434, 515], stencil compute kernels do not perform well on traditional CPU or GPU-based systems.

High-performance implementations of stencils on modern processors operate using a single-precision or a double-precision floating-point data type. The floating-point format is the most widely supported datatypes by our current hardware devices. Using this data type in real-world applications, which use large grid sizes, puts enormous stress on the memory subsystem. Therefore, storing data in the memory using a smaller number of bits can decrease the memory footprint and provide reductions in latency and energy consumption. The industry trend [136] shows a clear shift away from using floating-point representation. For example, applications like neural networks can use an 8-bit fixed-point format or lower precision without significant loss in accuracy [200]. Hence, in this chapter, we examine the use of different number systems – fixed-point, posits, floating-point – and analyze the precision tolerance of three-dimensional stencil kernels, one of the most widely used kernels in real-world applications.

4.2 Background

This section provides details on the stencil kernels used and discusses the relevance of the precision analysis.

4.2.1 Stencil Benchmark

Stencil computation updates a multi-dimensional grid based on a specific computation pattern. A stencil kernel’s performance on the current multicore system depends heavily on the data mapping of the grid. For instance, suppose a 3D grid in $(row, column, depth)$. When the grid is stored by row , accessing data elements in the other dimensions typically results in cache eviction. This issue is because, for real-world applications, the problem size is too large to fit in the processor cache. This chapter focuses on both a **7-point** and **25-point** 3D elementary stencil and a compound horizontal diffusion (**hdiff**) stencil, shown in Figure 4-1. These kernels access a three-dimensional grid and have complex access patterns. The 3D **7-point** and **25-point** (see Figure 4-1a) stencils commonly arise from the finite difference method for solving partial differential equations [515]. The **7-point** stencil performs eight FLOPS per grid point, while the **25-point** stencil performs twenty-seven FLOPS per grid point (without any common subexpression elimination). Thus, the arithmetic intensity, the ratio of FLOPS performed for each byte of memory traffic, is much

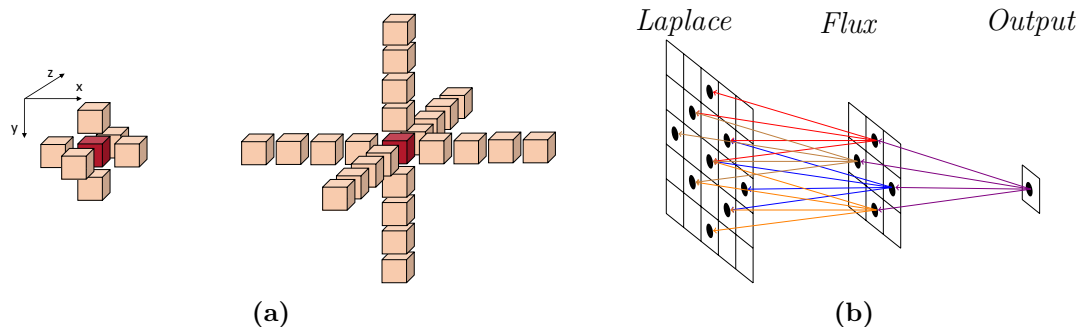


Figure 4-1: (a) 7-point stencil and 25-point elementary stencils (b) Compound horizontal diffusion stencil that is used by the COSMO weather prediction model

higher for the 25-point stencil than the 7-point stencil.

As discussed in Chapter 3, stencil patterns in a real-world weather prediction application consist of a collection of stencils that performs a sequence of element-wise computations. Horizontal diffusion kernel is an example of one such kernel that executes each stencil using a separate loop nest. It iterates over a 3D grid that performs *laplacian* and *flux*, as depicted in Figure 4-1b, as well as calculations for different grid points. Such compound kernels have intricate memory access patterns because they apply a series of elementary stencil operations. Although such implementations may be straightforward to write, they are not efficient in terms of data locality, memory usage, or parallelism.

4.2.2 Precision Optimization

IEEE-754 floating-point representation has become the universal standard in modern computing systems. Floating-point numbers have a mantissa and exponent component with an additional bit to represent the sign of a number. In terms of computing resources, this floating-point arithmetic requires complex circuitry leading to high latency and power consumption [136].

The use of low-precision arithmetic with a minimal loss in the accuracy has been proposed as a promising alternative to the commonly used floating-point arithmetic for emerging workloads, e.g., machine learning and graph processing. From the system perspective, there are two main benefits of moving to a lower precision. First, the hardware resources for a given silicon area may enable higher operations per second (OPS) at a lower precision as these operations require less hardware area, and thus power. Note, this also necessitates efficient memory traffic management. Secondly, many operations are memory bandwidth bound [432, 437], and reducing precision would allow for better cache usage and reduction of bandwidth bottlenecks. Thus, data can be moved faster through the memory hierarchy to maximize the utilization of computing resources.

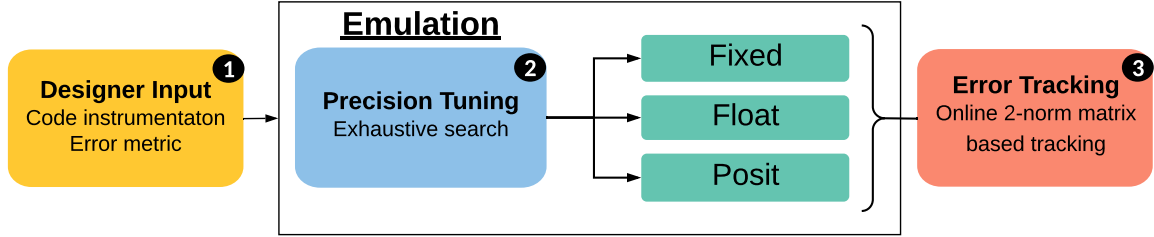


Figure 4-2: Overview of application precision exploration. The designer inputs the code with an appropriate precision template. Exhaustive precision exploration is performed for different number systems that include fixed-point arithmetic, floating-point arithmetic, and posit arithmetic. While exploring, error tracking is performed using the 2-norm matrix approach

4.3 Methodology

The following section provides detail on our methodology to explore precision for different number systems, as depicted in Figure 4-2. In the first phase (1), we analyze and instrument a part of an application for which the precision exploration needs to be performed. In the next phase (2), we execute an exhaustive search to find the appropriate precision based on the number system used. In this chapter, we make use of fixed-point, floating-point, and posit number systems. During the exhaustive design space exploration, continuous error tracking (3) is performed to measure the extent of accuracy deviation compared to the IEEE floating-point arithmetic format.

Accuracy: In our experiments, for precision tuning, we consider the induced 2-norm of a matrix [24] as our measure of the accuracy. A matrix norm is a vector norm in a vector space. The induced 2-norm of an $m \times n$ matrix A is the supremum of the ratio between the 2-norm of a vector Ax and the 2-norm of x , where x is an n -dimensional vector. We calculate the relative norm or mean relative error (MRE) ϵ_i to indicate how close the predicted value A'_i is to the actual value A_i . MRE provides an unbiased estimate of the error variance between two matrices.

$$\epsilon_i = \frac{\|A'_i - A_i\|_2}{\|A_i\|_2} \quad (4.1)$$

4.3.1 Evaluated Arbitrary Precision

As an alternative to the currently used IEEE single and double-precision floating-point representation, we explore the precision tolerance of 3D stencil kernels using the following number formats (see Figure 4-3):

1) Fixed-Point Arithmetic: A fixed-point consists of an integer and a fraction part where total width could be any multiple of 2, based on the bit-width of the data path. Compared to the floating-point format, fixed-point numbers simplify the logic

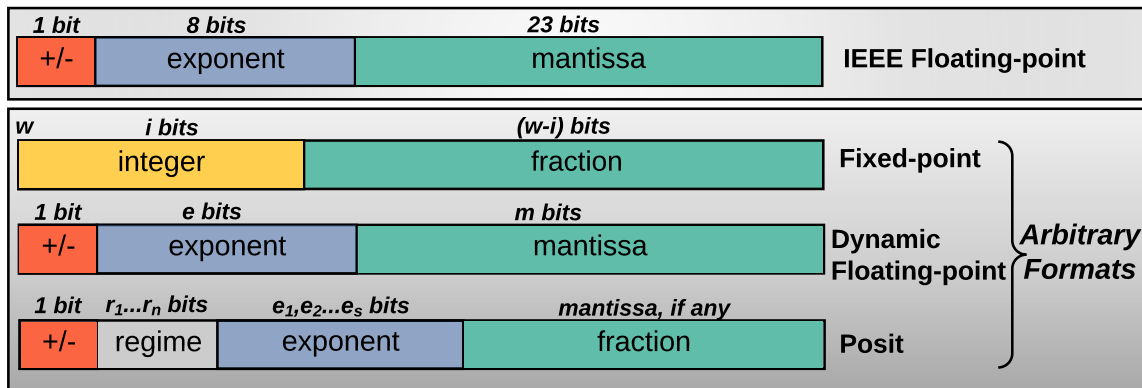


Figure 4-3: Arithmetic types used with widths indicated above each field. IEEE single precision floating-point number is 32-bit where a positive sign bit is represented by a 0 and a negative by 1. Fixed-point has fixed integer and fraction bits where w (total bits) could be any multiple of 2, based on the bitwidth of the data path. Dynamic floating-point arithmetic uses arbitrary exponent and mantissa bits. A posit number [165] is similar to floating-point with additional bits for the regime part. It has e_s exponent bits, but depending upon the data this could be omitted (same is valid for mantissa bits)

by fixing the radix point.

In an FPGA, the fixed-point format offers a more resource-efficient alternative to the floating-point implementation. This efficiency is because floating-point support often uses more than $100\times$ as many gates compared to fixed-point support [136].

2) Dynamic Floating-Point Arithmetic: By lowering the precision of a floating-point format, we could retain the advantages of floating-point arithmetic (e.g., higher dynamic range) with a lower bit-width. Dynamic floating-point arithmetic uses an arbitrary number of bits for the exponent and significand (or mantissa) parts of a floating-point number.

3) Posit Arithmetic: Posit[165] borrows most of the components from the IEEE 754 floating-point scheme, such as the exponent and fraction (or mantissa) fields. However, posit has an additional *regime* bit introduced to create a tapered accuracy, which lets small exponents have more accuracy. One could choose to either represent a large number by assigning more bits to the exponent field or opt for more decimal precision by having more fraction bits.

Figure 4-3 shows the different datatypes explored in this chapter. While analyzing these types, there are several things to take into account. Firstly, posit can provide the highest dynamic range compared to the other number systems, and fixed-point offers the lowest [71]. Additionally, floating-point numbers are susceptible to rounding errors and could lead to an overflow or underflow [165]. We determine the precision bit-width through bit accurate simulations for different bit-width configurations. While changing bitwidth, we analyze the trend of the relative error.

4.4 Evaluation

We use IBM[®] POWER9 as the host system comprising of 16 cores, each of which supports four-thread simultaneous multi-threading. Table 4.1 provides complete details of our system parameters. To provide a full-scale analysis of stencil optimization techniques, we set the grid size of all stencil kernels as $1280 \times 1080 \times 960$, much larger than the on-chip cache capacity of POWER9, with input data distribution as a Gaussian function. The problem size dictates which input dataset would reside in the cache; hence is an important parameter while measuring the system performance. Note: in Chapter 3, we use a grid domain used by the COSMO weather prediction model.

Table 4.1: System parameters and hardware configuration for the CPU and the FPGA board

Host CPU	16-core IBM POWER9 AC922 @3.2 GHz, 4-way SMT
Cache-Hierarchy	32 KiB L1-I/D, 256 KiB L2, 10 MiB L3
System Memory	16x32GiB RDIMM DDR4 2666 MHz
DDR4-based FPGA Board	Alpha Data ADM-PCIE-9V3 Xilinx Virtex Ultrascale+ XCVU3P-2 8GiB (DDR4) with PCIe Gen4 x8

For precision tuning of the fixed-point number system, we use the Xilinx fixed-point library from the Vivado 2018.2 tool [483]. We use the C++ template-based *FloatX* (Float eXtended) library¹ to explore arbitrary precision for floating-point arithmetic. Software-based posit implementation is available as part of the ongoing efforts to develop an ecosystem for posit evaluation². All three libraries are provided as a C++ header format, which allows us to replace the data types in the source code of the application and study the effect of low precision using the same software toolchain as that of the application itself. We develop a highly optimized FPGA accelerator for all the kernels to make a performance comparison between floating-point and fixed-point number systems. We implement these designs on an Alpha-Data ADM-PCIE-9V3 [5] card featuring the Xilinx Virtex Ultrascale+ XCVU3P-FFVC1517-2-i device.

4.4.1 Emulated Precision Tuning

The tuning process analyzes multiple configurations for each of the arithmetic types considered. The tuner re-executes the program for each configuration and

¹<https://github.com/oprecomp/FloatX>

²<https://github.com/stillwater-sc/universal>

computes the error on its output values to provide a measure of the resultant accuracy. Figure 4-4 shows the precision results for the considered workloads for three different number systems. The accuracy is compared to the most ubiquitously used IEEE single-precision floating number system.

For all the kernels, we can achieve full accuracy with much lower bits. Moreover, as the error tolerance increases, we could use a lower number of total bits. Based on this, we make three observations. First, in the case of a 7-point and 25-point stencil, we could reduce bits by more than 50% for the considered three data types, with a precision loss of only 1%. Second, elementary 3D stencil kernels (7-point and 25-point) could not exploit the high dynamic range offered by posit. Therefore, with a lower bit-width floating-point arithmetic, we could achieve better results. Third, the weather compound kernel comparatively needs a higher dynamic range; therefore, with 0.1% tolerance in the accuracy, we could cut the number of bits to half compared to the IEEE floating-point and move to a posit of (16,2). This observation motivates the use of posit number format can be useful in the domain of weather prediction modeling.

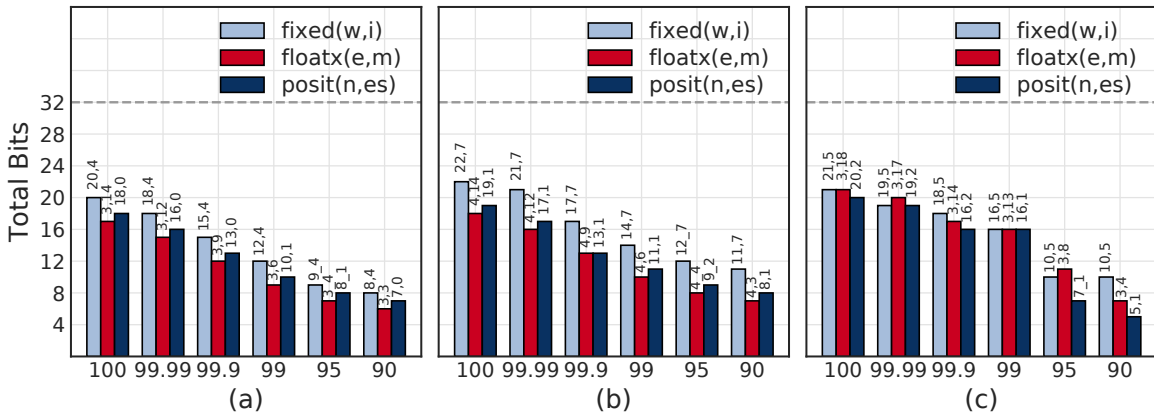


Figure 4-4: Total bits vs accuracy (percentage) for (a) 7-point, (b) 25-point, and (c) horizontal diffusion compared to single-precision IEEE floating-point representation. Notation fixed (w,i) defines a fixed number with total w bits including i integer bits. With floatx, e refers to the exponent bits and m defines the mantissa. In the case of the posit number system, n is the total number of bits with es bits for the exponent part

4.4.2 Case Study for Current Multi-Core Systems and Arbitrary Precision Supported Hardware

We perform a case study to measure the capabilities of current state-of-the-art hardware platforms. We tune the considered stencil kernels both for IBM POWER9 CPU and for a high-end FPGA platform. Our FPGA is coherently attached to our

host CPU through the CAPI2 link. For the FPGA and the POWER9 node, we use the AMESTER³ tool to measure the active power consumption.

Our current FPGA devices only support floating-point and arbitrary fixed-point arithmetic. Therefore, we compared hardware implementations across the stencil benchmarks for floating-point single and half precision with fixed-point datatype for the bit width that gave similar accuracy to the floating-point. Note, as current state-of-the-art hardware devices do not support the posit data type, we did not include it in our hardware comparison because the emulation of posit data type would be expensive in an FPGA and would lead to unfair comparisons with other data types. In Appendix B, we develop PreciseFPGA, an automated framework to obtain an application-aware optimal fixed-point configuration without exhaustively searching the entire design space.

In Figure 4-5a, we show a high-level overview of our integrated system. The FPGA is connected to a server system, based on the IBM[®] POWER9 processor, using IBM[®] coherent accelerator processor interface 2.0 (CAPI 2.0). The FPGA implementation consists of accelerator function units (AFU) that interact with the power service layer (PSL), which is the CAPI endpoint on the FPGA. The co-designed execution flow is shown in Figure 4-5b. We provide the experimental results of tuning stencil kernels for current CPU and FPGA-based systems.

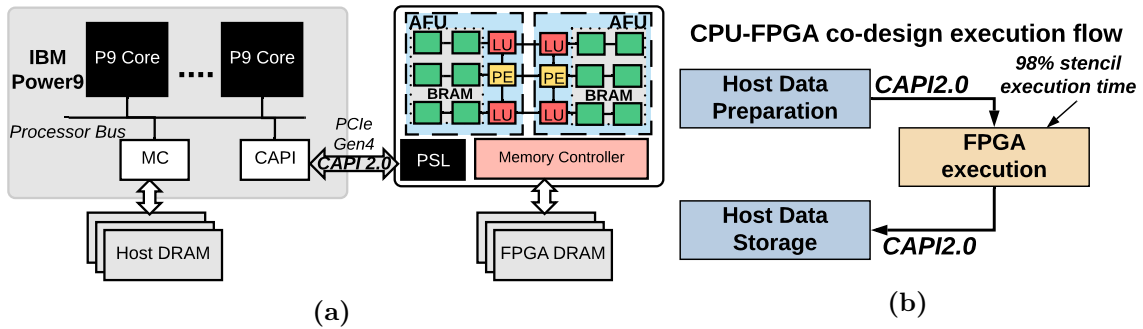


Figure 4-5: (a) CAPI 2-based accelerator platform with IBM[®] POWER9 (b) FPGA is acting as a peer to the CPU by accessing the main memory through a high-performance CAPI2 link, enabled by PSL. Data flow sequence from the Host DRAM to the onboard FPGA memory. A software-defined API handles offloading jobs to accelerators with an interrupt-based queuing mechanism that allows minimal CPU usage (thus, power) during FPGA use

Figure 4-6 shows the roofline of the three stencil kernels (7-point, 25-point, and `hdiff`) that we use in this study. By mapping both, arithmetic intensity of all examined stencils and peak attainable GFLOP/sec (GOP/sec for fixed-point) on the roofline of our heterogeneous system (CPU+FPGA), we make the following three observations. First, we observe that compiler and tiling optimizations [515] lead to

³<https://github.com/open-power/amester>

125.2 \times 119.4 \times and 90.4 \times speedup compared to non-optimized CPU implementations for 7-point, 25-point, and `hdiff`, respectively. The memory bandwidth constrains the performance of elementary stencils (7-point, 25-point) since the stencil data for the 3D grid cannot be mapped to contiguous memory location leading to limited cache locality. Although `hdiff` has a higher arithmetic intensity, its access patterns are more complex because it applies a series of elementary stencil operations with different stencil patterns.

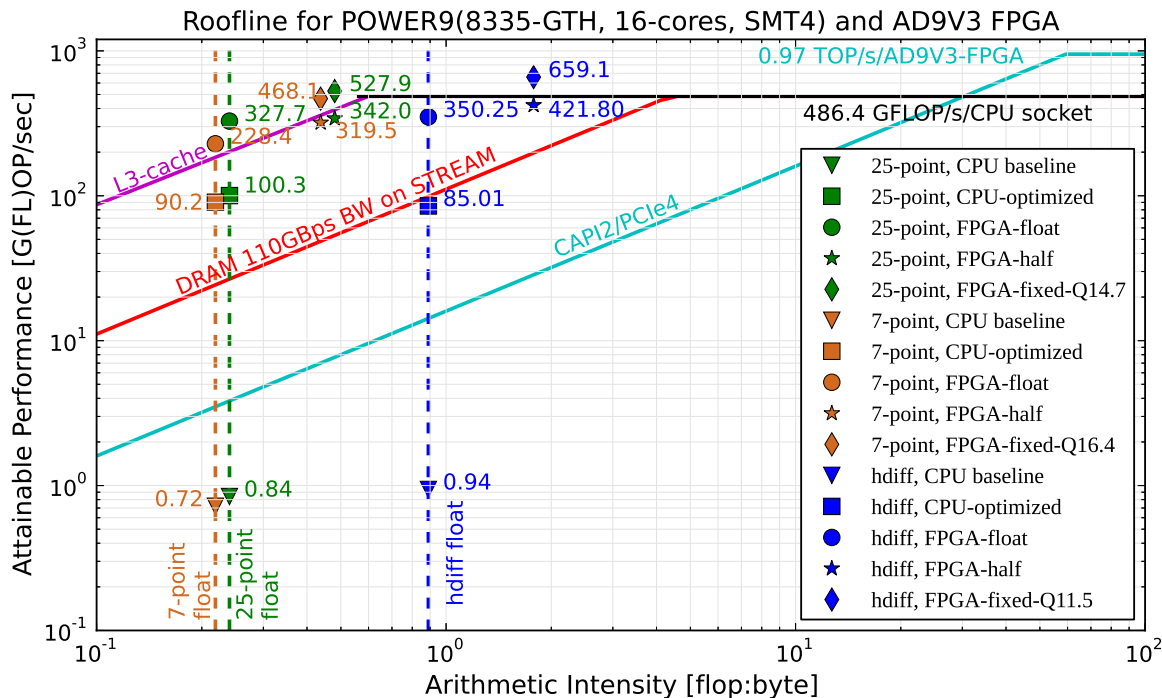


Figure 4-6: Roofline [501] for POWER9 (1-socket) showing elementary stencil (7-point and 25-point) and horizontal diffusion (`hdiff`) kernels for single-thread baseline and 64-thread fully-optimized implementations. The plot shows also the roofline of the FPGA with attained performance of our examined stencils using different precision data types

Second, we observe that the floating-point FPGA implementations increase the additional speedup to 2.5 \times , 3.3 \times , and 4.1 \times compared to the CPU-optimized implementation for 7-point, 25-point, and `hdiff`, respectively. By effectively using the FPGA’s on-chip memory, the FPGA-based implementations are not constrained by the DRAM memory bandwidth. However, the CAPI2/PCIe4 link offers an order of magnitude less bandwidth than that of the host CPU’s DRAM. Since our platform offers memory-coherent access of FPGA to the system memory, we build a pipelined execution, where communication time for transferring data from host to FPGA memory is masked with the actual FPGA processing [112]. This technique allows us to exploit FPGA processing capabilities completely.

Third, we have measured additional gains by replacing a single-precision floating-point data type with a lower precision data type. Specifically, in the roofline of Figure 4-6, we plot the performance of three stencils using half and fixed-point data types. The specific bit-width for the integer and fractional part of the fixed point was selected at 99% accuracy, i.e., Q14.7 for 25-point, Q16.4 for 7-point, and Q11.5 for `hdiff`. Arithmetic intensity is improved for both half and fixed data types since the bytes fetched from memory are half that of the single-precision floating-point (i.e., 2 bytes instead of 4 bytes). Since fixed-point implementations use fewer resources on an FPGA than float and half, we were able to add more accelerators on the same FPGA device, allowing us to measure 468.1, 527.9, and 659.1 GOPs/sec for 7-point, 25-point, and `hdiff`, respectively. These numbers are very close to the theoretical peak performance of 0.97 TOPs/s offered by our FPGA device ⁴.

Table 4.2 shows the resource utilization for our examined stencil kernels on an FPGA using different precision data types. In all the scenarios, going from single to half-precision increases the performance with a corresponding reduction in the number of resources. Further, moving to fixed-point arithmetic representation increases the performance due to a decrease in the number of bytes loaded at the cost of LUT utilization. However, the utilization of other FPGA resources is reduced. Figure 4-7 shows the achieved energy efficiency with different precision data types. As the number of bits reduces, we see an increase in energy efficiency for all considered kernels. Designs implemented in fixed-point will always be more efficient than their equivalent in floating-point alternative because fixed-point implementations consume fewer resources and less power (see Table 4.2). As these stencil kernels do not require the high dynamic range achievable with floating-point, moving to fixed-point implementations could provide better energy efficiency. In the case of `hdiff`, we see a huge increase in energy efficiency on moving to a lower precision. This increase is because `hdiff` is a compound kernel; therefore, each elementary stencil's energy improvement with lower precision leads to much higher cumulative gains.

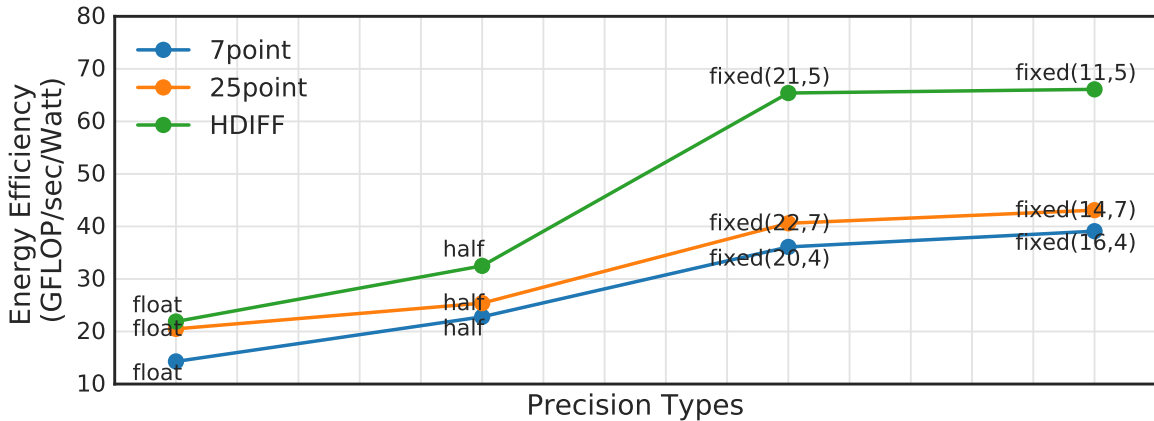
4.5 Related Work

Floating-point representation is the most widely supported data type by current hardware devices. Recently, in many application domains, there has been a significant amount of research to explore error resilience across the complete stack of computer architecture from application to device physics. A large body of literature [106, 124, 168, 181, 200, 307, 308] has analyzed the benefits of using lower precision fixed-point

⁴While the three stencils comprise different access patterns and acceleration kernels, the primary operations, i.e., vectorized multiply-accumulate computation (MAC), which define the FPGA micro-architecture, remain the same. Using vectorized MAC, we have calculate 0.97 TOPs/s theoretical top performance for stencils for our AD9V3 FPGA.

Table 4.2: FPGA resource utilization and performance for the examined stencil kernels on FPGA testbeds, with different precisions

Kernel	Precision	Accuracy (%)	Utilization (%)				Performance (GLOP/s)	Energy (mJ)
			BRAM	DSP	FF	LUT		
7-point	float	100	38	35	18	29	228.4	4617.2
7-point	half	99.95	25	24	15	28	319.5	2887.6
7-point	fixed (20,4)	100	16	12	49	95	467.6	1832.3
7-point	fixed (16,4)	99.96	12	12	47	92.5	468.1	1689.4
25-point	float	100	42	62	36	44	327.7	1608.7
25-point	half	99.06	32	43	32	43	342.1	1541.5
25-point	fixed (22,7)	100	29	21	56	95	527.9	1510.3
25-point	fixed (14,7)	99.05	19	21	55	91	528.9	1497.9
hdiff	float	100	52	89	65	61	350.3	3010.5
hdiff	half	98.02	44	84	35	57	421.8	2031.1
hdiff	fixed (21,5)	100	24	45	77	76	653.9	1007.9
hdiff	fixed (11,5)	97.92	14	35	69	71	659.1	997.9

**Figure 4-7: Evaluated design points for different stencil kernels. The plot shows energy efficiency (GFLOPS/Watt) with different precision implementations on an Alpha-Data ADM-PCIE-9V3 [5] card featuring the Xilinx Virtex Ultrascale+XC7VU3P-FFVC1517**

computation compared to floating-point for different application domains. With the emergence of the posit number system [165], research into lower precision with these alternate number systems is regaining attention. In neural-networks, Langroudi *et al.* [248] demonstrate a minimum accuracy degradation by using a 7-bit posit format. In another study, Klöwer *et al.* [239] show the applicability of posit in weather modeling. However, they used a different weather prediction model than COSMO, which uses different numerical solvers for predicting weather.

High-performance implementations of stencils on modern processors usually use the IEEE single-precision or double-precision floating-point data types. There have been various efforts to improve these kernels for different architectures using various software-based optimization techniques. Datta *et al.* [104] optimized the 2D and 3D stencil for multicore architectures using several hardware adherent optimizations. Similarly, Nguyen *et al.* [340] worked on algorithm optimization for CPU and GPU-

based systems. Gysi *et al.* [167] provided guidelines for optimizing complex kernels for CPU–GPU systems using analytic models. Gan *et al.* [143] use a mixed-precision approach for 13-point shallow water equation (SWE) stencils. The authors use fixed-point representation for variables that require a lower precision, while floating point precision for other variables. However, to the best of our knowledge, this thesis is the first to study the precision tolerance for scientific 3D stencil kernels, including a compound weather prediction stencil kernel, for a wide range of number systems, i.e., fixed-point arithmetic, floating-point arithmetic, and posit arithmetic.

4.6 Conclusion

Stencils are one of the most widely used computational kernels across various real-world applications. This chapter analyzed the precision tolerance for different 3D stencil kernels using fixed-point, floating-point, and posit number systems. We demonstrated by exhaustive precision exploration that these kernels have a margin to move to a lower bit-width with minimal loss of accuracy using different number formats.

Further, in a case study, we measured the performance of these kernels on a state-of-the-art multi-core platform and designed lower bit-width-based accelerators for all considered 3D stencil kernels on an FPGA platform. FPGA is the only device that gives us the capability to implement arbitrary fixed-point precision data types. Hence, we leveraged this capability to show the advantages of accelerating these kernels with lower precision compared to the ubiquitous IEEE floating-point format. In the future, we can use this analysis technique in an integrated design-flow to build efficient systems for stencil-based applications. Another future direction would be to study the effects of low precision processing not only for streaming applications, e.g., stencil and convolution, where computation is done locally but also for iterative applications where errors accumulate.

Chapter 5

NAPEL: Near-Memory Computing Application Performance Prediction via Ensemble Learning

To harness the power of near-memory computing architectures, having a high-level performance model can offer fast turnaround times in early design stages. This chapter proposes an NMC model that combines technology parameters and application specific characteristics to evaluate the performance of a workload. A statistical design of experiment (DoE) methodology is first employed to select a set of representative design points for simulation. These sampled points well represent the whole space of possible input configurations. Then, ensemble learning is leveraged to develop a model that can predict performance metrics for new unseen applications on these novel architectures. Further, this model can act as a classifier to predict whether or not should an application be offloaded to NMC cores.

5.1 Introduction

As discussed in Chapter 2, past works [11, 12, 37, 57, 58, 59, 182, 183, 234] show that NMC architectures can be employed effectively for a wide range of applications, including graph processing, databases, neural networks, bioinformatics. However, a common challenge all such past works face is how to evaluate the performance and energy consumption of the NMC architectures for different workloads systematically

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and accurately in a reasonable amount of time [330, 431]. In the early design stage, system architects use simulation techniques (e.g., [11, 37, 59, 182, 235]) for architectural performance and energy evaluation. However, this approach is extremely slow, because a single simulation for a real-world application with a representative dataset typically takes hours or even days. Specifically, the speed of a cycle-accurate simulator is in the range of a few thousand instructions per second [405], which is orders of magnitude slower than native execution.

Our goal is to enable fast early-stage design space exploration of NMC architectures without having to rely on time-consuming simulations. To this end, we propose the *NMC Application performance and energy Prediction framework using Ensemble machine Learning* (NAPEL). The key idea is to use ensemble learning to build a model that, once trained for a fraction of programs on a number of architecture configurations, can predict the performance and energy consumption of *different* applications on the same NMC architecture. The ensemble learning mechanism we use is random forest (RF) [61]. NAPEL can make performance and energy predictions for an average application on a specific architecture $220\times$ faster than using simulation. Previous ML-based approaches [69, 503, 505] perform extrapolations to predict, for example, the performance of a known application for a bigger dataset. In contrast, NAPEL can make predictions for *previously-unseen* applications, after being trained with data from applications that are different from the applications that we want to predict.

NAPEL still needs to run simulations to gather training data that is required to construct its predictive model. As discussed above, running simulations is very time-consuming if we apply a brute-force approach to run all the application-input configurations needed for training data. To alleviate this problem, we use a technique called *design of experiments* (DoE) [336] to extract representative data with a small number of experimental runs (between 11 and 31 for the evaluated applications). Specifically, we employ a DoE variant called *central composite design* (CCD), which allows us to explore the interactions and nonlinear effects between the application input parameters and the output response (i.e., performance and energy consumption).

5.2 NAPEL

NAPEL is a performance and energy estimation framework that targets the early stages of NMC system design. In this section, we describe the main components of the framework. First, we give an overview of NAPEL training and prediction (Section 5.2.1). Second, we describe the target NMC architecture we consider in this chapter (Section 5.2.2). Third, we explain the code-instrumentation process for the applications used to generate training datasets and for the applications under performance and energy prediction (Section 5.2.3). Fourth, we describe the two most

important components of NAPEL training: the design of experiments methodology (Section 5.2.4) and the ensemble machine learning (ML) technique (Section 5.2.5).

5.2.1 Overview

NAPEL is based on ensemble learning. Thus, it needs to be trained before it can predict performance and energy consumption. Figure 5-1 depicts the key components of NAPEL training and prediction.

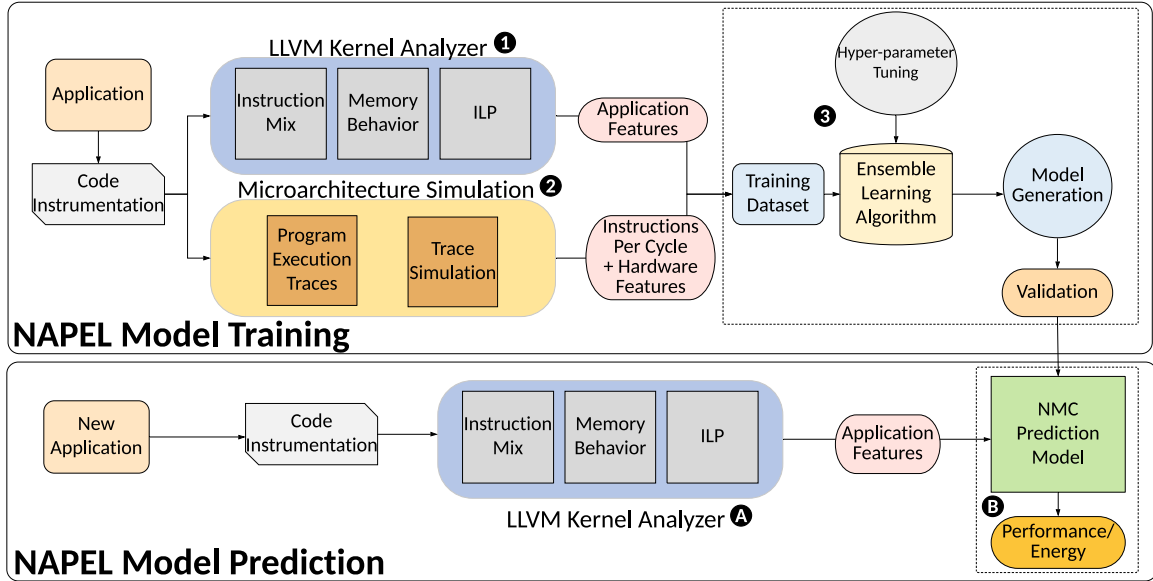


Figure 5-1: Overview of NAPEL training and prediction

Model Training. NAPEL training consists of three phases. The first phase (1 in Figure 5-1) is an LLVM-based [249] kernel analysis phase (Section 5.2.3), which extracts architecture-independent workload characteristics. First, we instrument applications or parts of them that we use to gather data for model training. We consider the instrumented codes for execution on NMC compute units with a specific architecture configuration. Second, we characterize the instrumented codes in a microarchitecture-independent manner by using a specialized plugin of the LLVM compiler framework [25]. This type of characterization excludes any hardware dependence and captures the inherent characteristics of workloads.

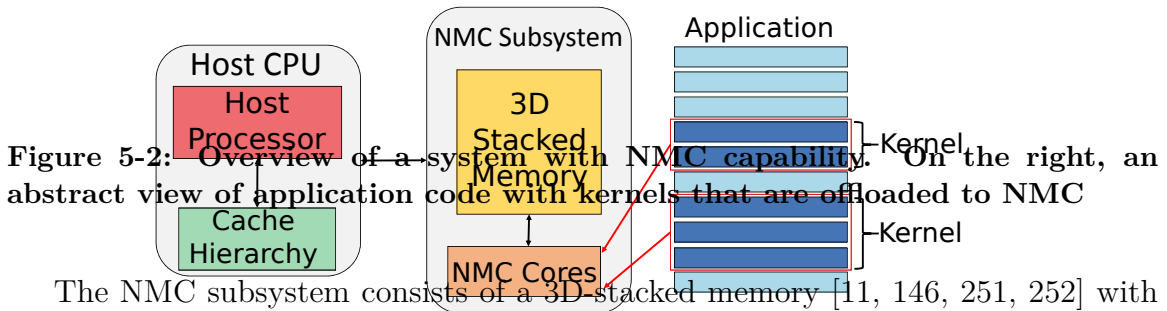
In the second phase (2), microarchitectural simulations are performed to gather architectural responses for training. For the simulations, we use central composite design (CCD) [300], a technique for the design of experiments (DoE) method [321]. With CCD, we can minimize the number of simulation experiments to gather training data for NAPEL while ensuring good quality of the training data (Section 5.2.4). The generated simulator responses along with application properties from the first phase and the microarchitectural parameters form the input to our ML algorithm.

In the third phase ③, we train our ML algorithm (Section 5.2.5). During this phase, we perform additional tuning of our ML algorithm’s hyper-parameters. Hyper-parameters are sets of ML algorithm variables that can be tuned to optimize the accuracy of the prediction model. We validate the prediction model against performance and energy simulation results from the second phase. Once trained, the framework can predict the performance and energy of a previously-unseen application on a specific NMC architecture.

Model Prediction. NAPEL prediction has only two phases. The first phase (Ⓐ in Figure 5-1) is the same LLVM-based kernel analysis phase as in NAPEL training. This phase extracts architecture-independent features of the workload for which NAPEL will predict the performance and energy consumption. The second phase (Ⓑ) performs the prediction by using the trained model. We feed the model with the architecture-independent workload features and the model provides the performance and energy estimations.

5.2.2 NMC Architecture

Figure 5-2 depicts the reference computing platform that we consider in this chapter. It contains a host processor and an external memory equipped with NMC compute units.



The NMC subsystem consists of a 3D-stacked memory [11, 146, 251, 252] with processing elements (PEs) embedded in its logic layer. The memory is divided into several vertical DRAM partitions, called vaults, each with its own DRAM controller in the logic layer. In this chapter, we model NMC PEs as in-order, single-issue cores with a private cache as proposed in previous work [11, 146], taking into account the limited thermal and area budget in the logic layer. NAPEL can be extended to support other types of general-purpose cores and accelerators by selecting the appropriate architectural features (see Table 5.1) for training the NAPEL model.

5.2.3 Code Instrumentation and Analysis

In the first phase of NAPEL training and prediction, the programmer annotates the region of the source code, called *kernel* (k), which is a candidate for offloading to NMC (i.e., execution on NMC processing elements). Then, that specific region is converted into an LLVM intermediate-representation (IR), which provides the basis for performing hardware-independent kernel analysis. Hardware-independent profiling enables us to generate an application profile p independently of the NMC design.

The application profile $p(k, d)$ is obtained by executing the instrumented application kernel k while processing a dataset d . $p(k, d)$ is a vector where each parameter is a statistic about an application feature f . Table 5.1 lists the main application features we extract by using the LLVM-based PISA analysis tool [25]. We select these features to analyze the memory access behavior of an application (data reuse distance, memory traffic, memory footprint, etc.), which is key for assessing the suitability of NMC for the application. Ultimately, the application profile p has 395 features, which includes all the sub-features of each metric we consider. Such a large number of features enables complex relationships to be identified between the analyzed application and its performance and energy consumption on the underlying NMC architecture [300].

Table 5.1: Main application and architectural features

Application Feature	Description
Instruction Mix	Fraction of instruction types (integer, floating point, memory read, memory write, etc.)
ILP	Instruction-level parallelism on an ideal machine.
Data/Instruction reuse distance	For a given distance δ , probability of reusing one data element/instruction (in a certain memory location) before accessing δ other unique data elements/instructions (in different memory locations).
Memory traffic	Percentage of memory reads/writes that need to access the main memory, assuming a cache of size equal to the maximum reuse distance.
Register traffic	Average number of registers per instruction.
Memory footprint	Total memory size used by the application.
NMC Arch. Features	Description
Core type	In-order
#PEs	Total number of near-memory processing units
Core frequency	Operating frequency of the core
Cache line size	Total size of a cache line (bytes)
#cache-lines	Number of cache lines
DRAM layers	Number of stacked DRAM layers
Size of DRAM	Total size of memory (bytes)
Cache access fraction	Cache hit ratio
DRAM access fraction	Cache miss ratio

5.2.4 Central Composite Design

In the second phase of NAPEL training, we use the design of experiments (DoE) method [321] as a way to minimize the number of experiments to train NAPEL without sacrificing the amount and quality of the information gathered by the experiments. DoE is a set of statistical techniques meant to locate a small set of points in a parameter space with the goal of representing the whole parameter space. The traditional brute-force approach to collecting training data is time-consuming: the sheer number of experiments renders detailed simulations intractable. Thus, the DoE strategy to gather a training dataset is a critical component of our model.

We apply the Box–Wilson central composite design (CCD) [300], the goal of which is to minimize the uncertainty of a nonlinear polynomial model that accounts for parameter interactions. While applying CCD, we treat the application input dataset d as a parameter vector (e.g., dataset size, number of threads, etc.) and each input configuration as a point in a multidimensional parameter space. For example, application *atax* from the PolyBench benchmark suite [378] has two significant parameters (*dimension*, *threads*) (see Table 5.2). In CCD, each input parameter in the vector d can have one of five levels: *minimum*, *low*, *central*, *high*, *maximum*. First, we select these levels for each parameter. For example, for *atax*, the levels of *dimension* are (500, 1250, 1500, 2000, 2300). Second, we place in the parameter space a point for each parameter combination (i.e., input configuration) with *low* and *high* levels (the corners of the solid-line square in Figure 5-3). In the case of *atax*, the points (*dimension*, *threads*) are (1250, 8), (1250, 32), (2000, 8), (2000, 32). Third, we draw a multidimensional sphere (represented as a circle in Figure 5-3) that circumscribes the initial square. This sphere generalizes the DoE to capture the nonlinearity in the system. Fourth, we obtain additional points on the sphere by combining the *central* level of each parameter with the *maximum* and *minimum* levels of the other parameters. For *atax*, these points (*dimension*, *threads*) are (1500, 4), (1500, 64), (500, 16), (2300, 16). Fifth, we include the *central* configuration, which is (1500, 16) for *atax*.

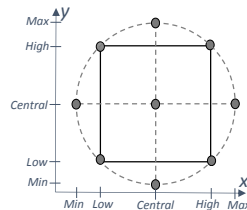


Figure 5-3: Central composite DoE for two parameters (x , y). For example, for *atax* (x , y) are (*dimension*, *threads*)

We run these DoE-selected application-input configurations on different architectural configurations to collect the training dataset. Table 5.2 lists the parameter levels for the evaluated applications. We include a *test* configuration, which we use in Section 5.3.4.

Table 5.2: Evaluated applications and their DoE parameters (“DoE param.”). For each DoE parameter, we show its five levels (*minimum, low, central, high, maximum*) and *test input*

Application			DoE Parameter Levels					
Name	Description	DoE Param.	Min	Low	Central	High	Max	Test
atax	Matrix Transpose and Vector Mult.	Dimensions	500	1250	1500	2000	2300	8000
		Threads	4	8	16	32	64	32
bfs	Breadth-first Search	Nodes	400k	800k	900k	1.2m	1.4m	1.0m
		Weights	1	2	4	25	49	4
		Threads	1	9	16	32	64	32
bp	Back-propagation	Iterations	30	40	65	70	80	95
		Layer Size	800k	1m	2m	3.5m	4m	1.1m
		Seed	2	4	5	10	12	5
		Threads	4	8	16	32	64	32
chol	Cholesky Decomposition	Iterations	1	3	9	16	25	9
		Dimensions	64	384	128	320	512	2000
		Threads	4	8	16	32	64	32
gemv	Vector Multiply and Matrix Addition	Iterations	10	20	30	50	80	60
		Dimensions	500	750	1250	2000	2250	8000
		Threads	4	8	16	32	64	32
gesu	Scalar, Vector, and Matrix Mult.	Iterations	50	60	80	100	150	60
		Dimensions	500	750	1250	2000	2250	8000
		Threads	4	8	16	32	64	32
gram	Gram-Schmidt Process	Iterations	10	20	40	50	60	50
		Dimension _i	64	384	128	320	512	2000
		Dimension _j	64	384	128	320	512	2000
kme	K-Means Clustering	Threads	4	8	16	32	64	32
		Data Size	100k	300k	700k	900k	1.2m	819k
		Clusters	3	5	6	7	8	5
lu	LU Decomposition	Threads	1	9	1	32	64	32
		Iterations	10	20	30	40	50	30
		Dimensions	196	256	320	420	512	2000
mvt	Matrix Vector Product	Threads	4	8	16	32	64	32
		Iterations	98	128	256	420	512	2000
		Dimensions	500	750	1250	2000	2250	2000
syrk	Symmetric Rank-k Operations	Threads	4	8	16	32	64	32
		Dimension _i	64	128	320	512	640	2000
		Dimension _j	64	128	320	512	640	2000
trmm	Triangular Matrix Multiply	Threads	4	8	16	32	64	32
		Dimension _i	196	256	320	420	512	2000
		Dimension _j	196	256	320	420	512	2000
		Threads	4	8	16	32	64	32

5.2.5 Ensemble Machine Learning

The third phase of NAPEL training is the training of the ML algorithm. As we retrieve hundreds of application features from the application analysis, we make use of the random forest (RF) [61] algorithm, which embeds automatic procedures to screen

many input features. RF is an ensemble ML algorithm, which, starting from a root node, constructs a tree and iteratively grows the tree by associating it with a splitting value for an input variable to generate two child nodes. Each node is associated with a prediction of the target metric equal to the mean observed value in the training dataset for the input subspace the node represents. This input subspace is randomly sampled from the entire training dataset.

We employ RF to capture the intricacies of new NMC architectures by predicting instructions per cycle (IPC) when executing an application near memory. Formally, we predict $IPC(p, a) \sim IPC(k, d, a)$, where p is the hardware-independent application profile representation of kernel k when processing input dataset d on an architecture configuration a . The input data gathered to train our RF model has three parts: (1) a hardware-independent application profile $p(k, d)$, (2) an architectural design configuration a , and (3) responses corresponding to each pair (p, a) . To gather the architectural responses, kernel k belonging to training set T with input dataset d is executed on an architectural simulator, simulating an architecture configuration a . This produces $IPC(k, d, a)$ for that configuration and is used as a *label* while training our RF algorithm.

We improve NAPEL training by tuning the algorithm’s hyper-parameters [369]. Hyper-parameter tuning can provide better performance estimates for some applications. First, we perform as many iterations of the cross-validation process as hyper-parameter combinations. Second, we compare all the generated models by evaluating them on the testing set, and select the best one.

After training our RF algorithm, we can predict the IPC of a kernel that is *not* in the training set. The predicted IPC can be used for performance evaluation of a kernel on an NMC system. The execution time Π_{NMC} of the kernel offloaded to NMC can be calculated as $\Pi_{\text{NMC}} = \frac{I_{\text{offload}}}{IPC \cdot f_{\text{core}}}$, where f_{core} is the frequency of the NMC processing cores and I_{offload} is the total number of offloaded instructions. Similarly, we build another model for energy prediction where we use energy consumption as a *label* when we train our RF algorithm.

5.3 Experimental Results

5.3.1 Experimental Setup

We consider different workloads from the PolyBench [378] and Rodinia [79] benchmark suites that cover a wide range of domains, such as image processing, machine learning, graph processing, radio astronomy. First, we instrument the region of code that is considered for offloading to NMC processing elements. Second, we apply CCD to these workloads to select a small set of application input configurations that represent the space of possible input configurations. Third, we carry out the LLVM-

based [249] microarchitecture-independent characterization to extract application metrics (Table 5.1) by using the PISA analysis tool [25].

We evaluate host performance on a real IBM POWER9 system [188] and NMC performance on a state-of-the-art simulator, Ramulator [235]. We extend Ramulator with a 3D-stacked memory model to simulate the NMC processing elements [402]. Table 5.3 summarizes the system details used for the host system and the NMC system. We collect dynamic execution traces of the instrumented code with a Pin tool. We feed the acquired traces to Ramulator. We use the simulation results as training data for our RF algorithm. Once trained, we use NAPEL to predict the performance and energy consumption of previously-unseen applications.

Table 5.3: System parameters and configuration

Host CPU System	
Configuration	IBM® POWER9 AC922 @2.3 GHz, 16 cores (4-way SMT), 32 KiB L1 cache, 256 KiB L2 cache, 10 MiB L3 cache, 16x32GiB RDIMM DDR4 2666 MHz
NMC System	
Cores	32× single issue, in-order execution @ 1.25 GHz
L1-I/D	2-way, cache size = 2 cache lines, 64B per cache line
DRAM Module	32 vaults, 8 stacked-layers, 256B row buffer; 4GB total size; closed-row policy
Off-chip Link	16-bit full duplex high-speed serializer/deserializer (SerDes) I/O link @ 15 Gbps [367]

5.3.2 Model Training and Prediction Time

Table 5.4 shows the time for performing training simulations (see “DoE run (mins)”) with the selected DoE configurations (“#DoE conf.”) to gather training data. The table also includes the time for training and tuning (“Train+Tune (mins)”) and the prediction time (“Pred. (mins)”) for each application. Once the model is trained, the DoE simulation time is amortized every time we predict performance and energy consumption for a previously unseen application. Thus, quick exploration and large prediction time savings compared to simulation are possible for a previously unseen application.

For all the evaluated applications, we compare the prediction time using trained NAPEL models with the prediction time using Ramulator simulations. Figure 5-4 shows NAPEL’s prediction speedup over Ramulator for 256 DoE configurations for all the evaluated workloads. We observe that NAPEL is, on average, 220× (min. 33×, max. 1039×) faster than simulation.

Table 5.4: Number of DoE configurations (“#DoE conf”) for gathering training data (“DoE run (mins)”), NAPEL training time (“Train+Tune (mins)”), including tuning, and NAPEL prediction time (“Pred. (mins)”).

Application Name	Training/Prediction Time			
	#DoE conf.	DoE run (mins)	Train+Tune (mins)	Pred. (mins)
atax	11	522	34.9	0.49
bfs	31	1084	34.2	0.48
bp	31	1073	43.8	0.47
chol	19	741	34.9	0.49
gemv	19	741	24.4	0.51
gesu	19	731	36.1	0.51
gram	19	773	36.5	0.52
kme	31	742	36.9	0.55
lu	19	633	37.9	0.51
mvt	19	955	38.0	0.54
syrk	19	928	35.7	0.51
trmm	19	898	37.6	0.48

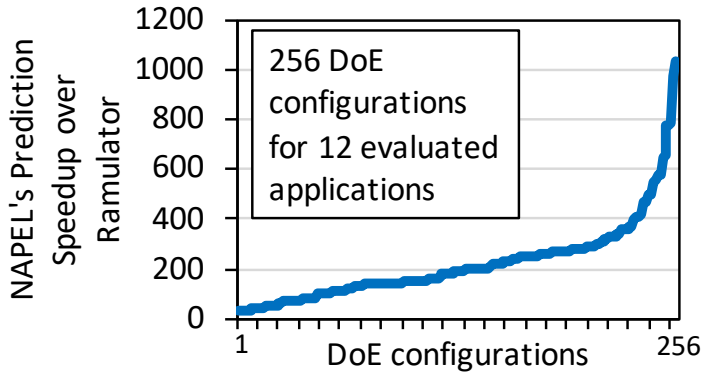


Figure 5-4: NAPEL’s prediction speedup (in increasing order) over Ramulator for 256 DoE configurations.

5.3.3 Accuracy Analysis

We analyze the accuracy of NAPEL for previously unseen applications by performing cross-validation [369]. To evaluate the prediction accuracy for a particular application, our training data comprises all the collected data (using an LLVM kernel analyzer and a microarchitecture simulator) for all applications *except* the application for which the prediction will be made. We repeat the same process to gather test prediction results for all applications, yet every time we test for a particular application, we do *not* include it in the training set. Therefore, when predicting performance and energy consumption of an application on NMC, we do *not* use any data related to that application. This makes the prediction more difficult because the ML algorithm has no knowledge of the application to be predicted. Thus, the test set differs from the training set as much as applications differ from each other. We evaluate the accuracy of the proposed model in terms of relative error ϵ_i to indicate how close the predicted value y'_i is to the actual value y_i . We calculate the mean relative error (MRE) for each application with Equation 5.1.

$$MRE = \frac{1}{N} \sum_{i=1}^N \epsilon_i = \frac{1}{N} \sum_{i=1}^N \frac{|y'_i - y_i|}{y_i} \quad (5.1)$$

Figure 5-5 shows NAPEL’s MRE for the workloads in Table 5.2. NAPEL’s average MRE is 8.5% for performance predictions and 11.6% for energy-consumption predictions. The highest error is for *bfs*, *bp*, and *kmeans* because these applications exhibit quite different characteristics compared to the other evaluated applications. In Figure 5-5, we also compare NAPEL with two other ML algorithms that can be used to predict performance and energy consumption: an artificial neural network (ANN) based on Ipek *et al.* [198] and a linear decision tree used by Guo *et al.* [163]. We make the following three observations. First, NAPEL is $1.7\times$ ($1.4\times$) and $3.2\times$ ($3.5\times$) more accurate in terms of performance (energy) prediction than the ANN and the linear decision tree, respectively. Second, the linear decision tree is very inaccurate, as shown by its high MRE. Decision trees are suitable mainly for linear regression, so they cannot capture the nonlinearity present in NMC performance and energy. Third, ANN is more accurate than the decision tree, but it is less accurate than NAPEL for almost all workloads. ANN requires a much larger training dataset to reach NAPEL’s accuracy. When running these experiments, we also observe that the ANN takes more training time than NAPEL with hyper-parameter tuning (up to $5\times$).

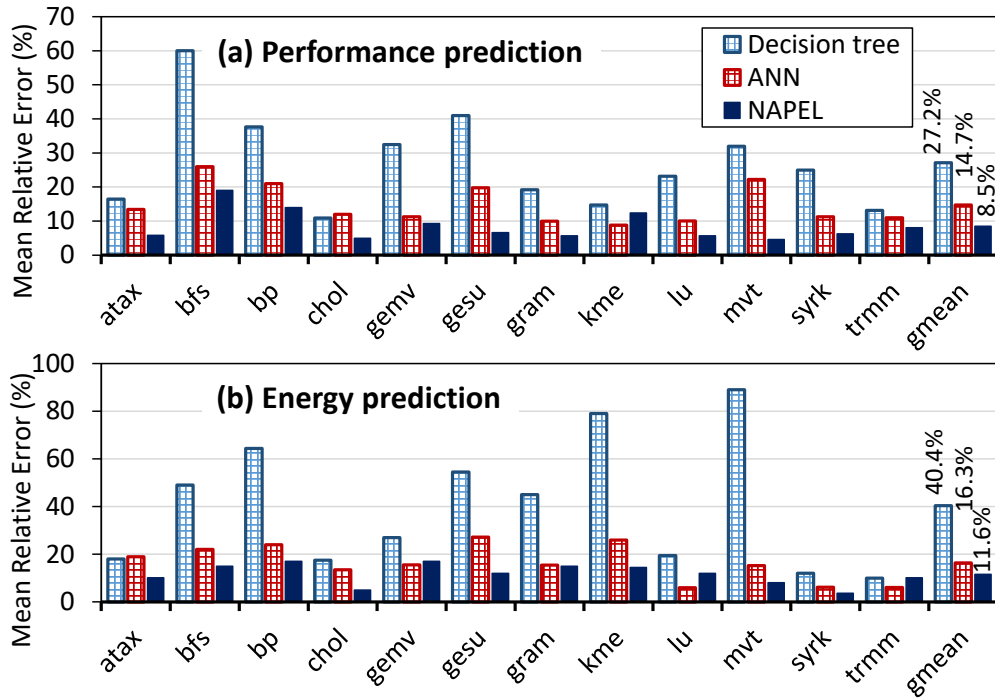


Figure 5-5: Mean relative error for performance (a) and energy (b) predictions using NAPEL vs. other methods.

5.3.4 Use Case: NMC-Suitability Analysis

In this section, we use NAPEL to perform an NMC-suitability analysis, i.e., to assess the potential benefit of offloading a workload to NMC. This analysis compares the energy-delay product (EDP) of executing a workload on the NMC units, which we obtain from NAPEL’s predicted NMC performance and energy consumption, to the measured EDP of executing the workload on a host processor. We use EDP as our major metric of reference in this analysis because both energy and performance are critical criteria for evaluating NMC suitability.

In order to obtain EDP results for the host system, we use a POWER9 system with 16 cores each supporting four-thread simultaneous multi-threading. We measure power consumption by monitoring built-in power sensors on our host system via the AMESTER¹ tool. Figure 5-6 shows the execution time and energy consumption of each workload on the POWER9. For the EDP results on the NMC system, we use NAPEL with tuned hyper-parameters.

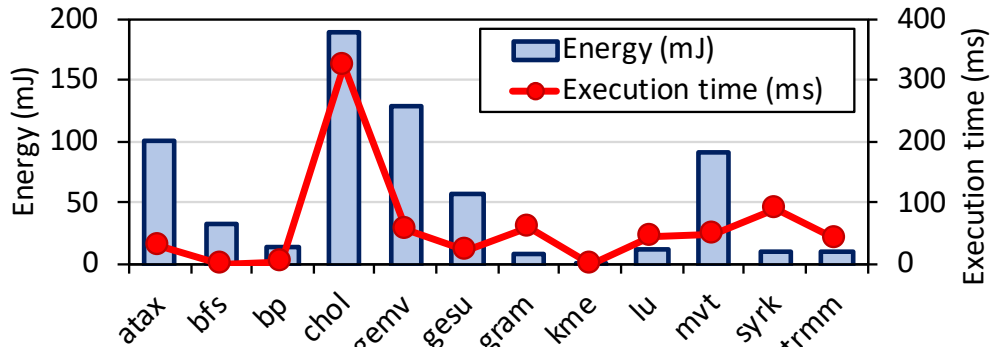


Figure 5-6: Execution time and energy on an IBM POWER9.

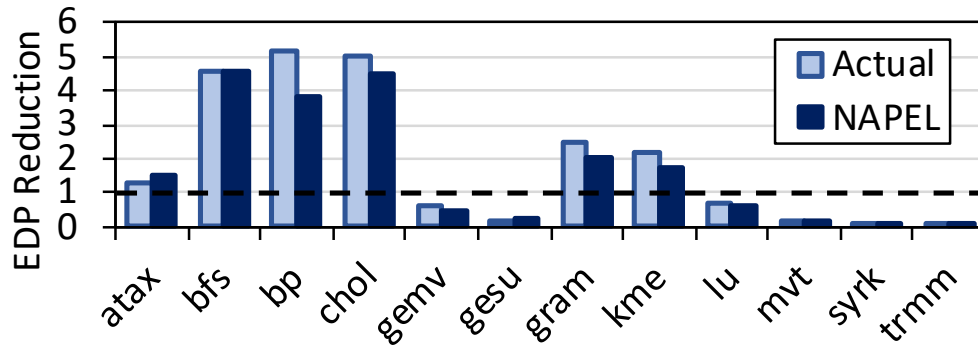


Figure 5-7: Estimated EDP reduction of offloading to NMC units versus execution on the baseline host CPU. “Actual” denotes the estimation with Ramulator. “NAPEL” denotes NAPEL’s prediction results.

Figure 5-7 shows estimated EDP reduction when executing each application on the NMC system compared to executing the same application on the host system using the *test* dataset (see Table 5.2). For each application, we show two bars: (1)

¹<https://github.com/open-power/amester>

NAPEL’s estimated EDP reduction, and (2) the estimated EDP reduction obtained by simulating the application using the cycle-accurate Ramulator [235] (“Actual”). We make five observations. First, NAPEL estimates the same workloads to be NMC suitable as Ramulator does (i.e., workloads with EDP reduction greater than 1). Second, the MRE of NAPEL’s EDP prediction is between 1.3% and 26.3% (14.1% on average). Third, *gemver*, *gesummv*, *lu*, *mvt*, *syrk*, and *trmm* are not suitable for NMC, since their EDP reduction is less than 1. These applications have enough data locality to leverage the host cache hierarchy. Fourth, *bfs*, *bp*, *cholesky*, *gramschmidt*, and *kmeans* are good fits for NMC. These applications are memory intensive and have irregular memory access patterns, so the host execution suffers from expensive offchip data movement. Fifth, *atax* benefits from the host cache hierarchy when performing vector multiplication, which has high data locality. However, it also performs matrix transposition, which is memory intensive. For *atax*-like workloads, the introduction of a small cache or scratchpad memory in the NMC compute units (larger than the 128B L1 cache in Table 5.3) can be beneficial, such that the data locality of the application can still be exploited.

5.4 Related Work

The lack of evaluation tools is a critical challenge to the adoption of near-memory computing (NMC) [330, 431]. The importance of architecture simulators is widely acknowledged. However, simulators are generally very slow as they may take hours to simulate even a single configuration [163, 405].

Recent works propose ML-based performance prediction methods for faster early-stage design space exploration of different architectures. Table 5.5 lists recent works (including NAPEL) that use different prediction techniques for several architectures.

Table 5.5: Related works in different domains

Name	Approach	Architecture	DoE
Joseph <i>et al.</i> [211]	Linear Regression	CPU	D-optimal Design
Ipek <i>et al.</i> [198]	ANN	CPU	Variance Based Sampling
Wu <i>et al.</i> [504]	ANN	GPU	None
Guo <i>et al.</i> [163]	Model Tree	CPU	None
Mariani <i>et al.</i> [300]	Random Forest, Genetic Algorithm	HPC	D-optimal Design, CCD
SemiBoost [263]	ANN	CPU	Latin Hypercube Sampling
NAPEL	Random Forest	NMC	CCD

Joseph *et al.* [211] and Guo *et al.* [163] use linear regression models to predict CPU performance. Linear models cannot accurately capture nonlinearity between application and processor responses, as shown in Figure 5-5. Wu *et al.* [504] use an

ANN for GPU performance prediction without applying the DoE technique. Unlike NAPEL, this work uses traditional, time-consuming brute-force techniques to collect the training dataset. In the HPC domain, Mariani *et al.* [300] predict the performance of applications on cloud architectures using random forest and genetic algorithms, which are trained using DoE techniques. Ipek *et al.* [198] use an ANN with variance-based sampling for CPU performance prediction. Likewise, Li *et al.* [263] use an ANN with Latin hypercube sampling for design-space exploration of multicore CPUs. To our knowledge, NAPEL is the first performance and energy-prediction framework for NMC architectures that uses machine-learning models. NAPEL can make accurate predictions for previously unseen applications on NMC architectures.

5.5 Conclusion

We introduce NAPEL, the first high-level machine learning-based prediction framework for fast and accurate early-stage performance and energy-consumption estimation on NMC architectures. NAPEL avoids time-consuming simulations to predict the performance and energy consumption of previously unseen applications on various NMC architecture configurations. To achieve this, NAPEL relies on random forest, an ensemble learning technique, to build its prediction models.

NAPEL is $220\times$ faster than a state-of-the-art NMC simulator, with an accuracy loss in performance (energy) prediction of only 8.5% (11.6%) compared to the simulator. Compared to an artificial neural network, NAPEL is $1.7\times$ ($1.4\times$) more accurate in performance (energy) prediction. NAPEL can accurately perform fast design-space exploration for different applications and NMC architectures. We hope the NAPEL approach enables faster development of NMC systems and inspires the development of other alternatives to simulation for NMC performance and energy estimation.

Chapter 6

LEAPER: Modeling FPGA-Based Systems via Few-Shot Learning

Machine-learning-based models have recently gained traction as a way to overcome the slow downstream implementation process of FPGAs by building models that provide fast and accurate performance predictions. However, these models suffer from two main limitations: (1) a model trained for a specific environment cannot predict for a new, unknown environment; (2) training requires large amounts of data (features extracted from FPGA synthesis and implementation reports), which is cost-inefficient because of the time-consuming FPGA design cycle. In a cloud system, where getting access to platforms is typically costly, error-prone, and sometimes infeasible, collecting enough data is even more difficult. FPGA-based cloud environments are usually $2\times$ more expensive than CPU-only cloud environments. Therefore, before deploying a cloud instance, a user cares whether the attained performance while using an FPGA would justify the incurred cost (both in terms of designing an accelerator and deploying in the cloud). To overcome these limitations, in this chapter, we propose LEAPER, a *transfer learning*-based approach for FPGA-based systems that adapts an existing ML-based model to a new, unknown environment.

6.1 Introduction

The need for energy-efficiency from edge to cloud computing has boosted the widespread adoption of FPGAs. In cloud computing [16, 21, 63, 89, 379, 384], FPGA’s

A part of this chapter is published as “*Modeling FPGA-Based Systems via Few-Shot Learning*” in FPGA 2021.

flexibility is not just about being able to make use of reconfigurable hardware for a diverse set of workloads [215]. Its flexibility can also be attributed to the cloud deployment model that spans from on-premises clusters to compute, storage, and networking capacity in public clouds and even out to the edge where AI and analytics are being increasingly deployed because of latency and data movement issues [330].

An FPGA is highly configurable as its circuitry can be tailored to perform any task [99, 223, 471, 472]. The large configuration space of FPGA and the complex interactions among configuration options lead many developers to explore individual optimization options in an ad-hoc manner. Moreover, FPGAs have infamously low productivity due to the time-consuming FPGA implementation process [345]. A common challenge that past works have faced is how to evaluate the performance of an FPGA implementation in a reasonable amount of time [346]. Thus, the development of efficient FPGA accelerators has required tremendous engineering effort due to the complexity of the FPGA configuration space and difficulties in evaluating performance. To overcome this problem, researchers have recently employed machine learning (ML)-based models [101, 298, 346, 490] to estimate the performance of an FPGA-based system quickly. These models are based, in turn, on traditional ML approaches.

Traditional ML models have four fundamental issues that can reduce the usability for assessing FPGA performance, especially in a cloud environment. First, they are trained for specific workloads, fixed hardware, and/or a set of inputs. Therefore, when presented with a different feature-space distribution because of a new workload or hardware, an ML model must be retrained from scratch. Otherwise, the model will perform poorly because the trained model does not have a notion of the new, unknown environment.¹ Therefore, traditional ML-based models have limited *re-usability*.

Second, learning-based approaches, such as neural networks, require a considerable number of samples to construct a useful prediction model. Collecting such a large number of samples is often slow and time-consuming due to the very long FPGA implementation cycle. Similarly, in settings such as cloud computing, where getting access to platforms is typically *costly*, *error-prone*, and sometimes *infeasible*, the data collection process is even more difficult.

Third, traditional machine learning with limited samples is prone to serious *over-fitting* problems (i.e., when a model matches too closely to the training data) [102], limiting model generalization. Fourth, it is impossible to construct one model for all different scenarios as the interpretation of data changes over time. Thus, ML models are prone to *concept drift*, where the accuracy of an ML-based model could degrade due to a change in the statistical properties of a target variable (e.g., using a different dataset for an application than the one used during the training of an ML-model) [468].

¹In this chapter, we consider an application or hardware platform as an environment.

Our research aims to answer the following question: for an FPGA-based system, can we leverage an ML-based performance model trained on a low-end local system to predict the performance in a new, unknown, high-end FPGA-based system?

As an answer to this question, we present LEAPER², a transfer learning-based model that predicts the performance of a new, unknown high-end FPGA-based system. We train LEAPER on a low-end local system. LEAPER uses predictive modeling to train an ML-based model and statistical techniques to collect representative training data set efficiently. LEAPER uses *transfer learning* [359] to leverage a trained *base model* (for a low-end system) and adapt it efficiently to an unknown *target* environment (i.e., a high-end system) with a few samples from the target environment as possible.

Figure 6-1 demonstrates the traditional approach of building models and the LEAPER transfer learning-based approach. Using the traditional approach, we would need to create two separate prediction models, one for the low-end edge environment and another for the high-end cloud environment, each one requiring a large number of samples. In contrast, LEAPER provides the ability to reuse the prediction model built on an *inexpensive* edge FPGA for performance prediction on a target cloud environment³ using only a few samples from the target environment. This allows developers to avoid the slow downstream implementation process of FPGAs by generating cheaper and faster performance models using transfer learning. This paradigm is also referred to as *few-shot learning* [493]. The idea behind few-shot learning is that, similar to humans, algorithms can learn from past experiences and transfer the knowledge to accomplish previously-unknown tasks more efficiently. The transferred models usually have high generality [493] and can overcome concept drift [142].

6.2 LEAPER

LEAPER is a performance and resource estimation approach to *transfer* ML-based models across different FPGA-based platforms. First, we give an overview of LEAPER (Section 6.2.1). Second, we describe the two components of LEAPER that are used to generate training datasets: (1) FPGA-based accelerator configuration options and application features used for training our base model (Section 6.2.2), and (2) the *design of experiments* (DoE) [321] methodology (Section 6.2.3). Third, we briefly describe the base model training (Section 6.2.4). Fourth, we explain the key component of LEAPER: the transfer learning technique (Section 6.2.5).

²We call our mechanism LEAPER because it allows us to hop or “leap” between machine learning models.

³Note: LEAPER is not limited to a cloud environment.

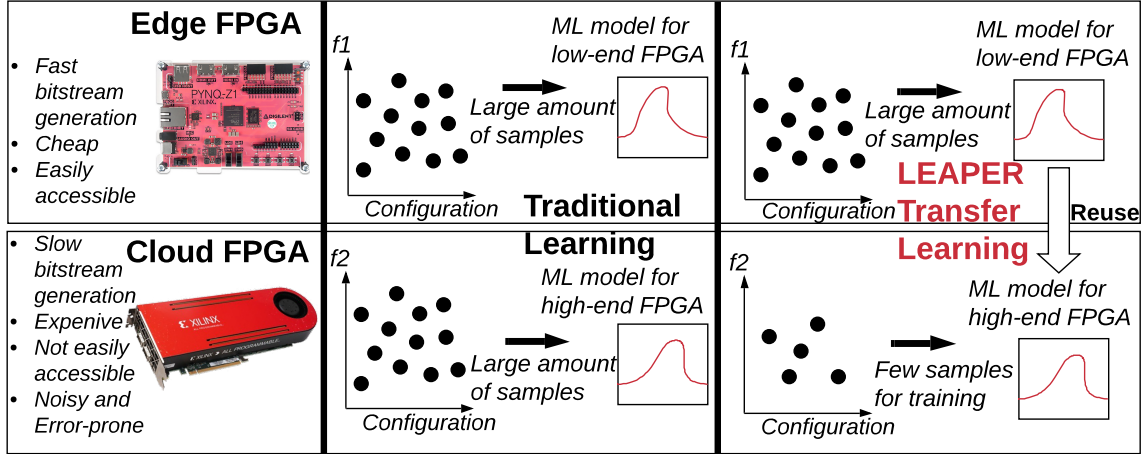


Figure 6-1: Comparison of traditional learning approach and LEAPER. Traditional learning methods are costly because they build models only for a specific environment. LEAPER allows transfer of models from a low-cost edge FPGA, where data collection is easier, to a high-cost cloud FPGA environment to build cheaper and faster models.

6.2.1 Overview

Figure 6-2 depicts the key components of LEAPER. The upper part of the figure describes the construction of the base model, while the lower part shows the phases for the target model.

Base Model Building. LEAPER base model building consists of three phases. In the first phase (❶ in Figure 6-2), we employ *Latin hypercube sampling* (LHS) [263] to select a small set of input configurations that well represent the entire space of input configurations (c_{lhs}) to build a highly accurate *base learner*. We use LHS to minimize the number of experiments needed to gather training data for LEAPER while ensuring good quality training data (Section 6.2.3). In the second phase (❷), FPGA implementations are made with a software-hardware co-design process. Once the FPGA design has been implemented, the resulting FPGA-based accelerator is deployed in a system with a host CPU. Then, we run the c_{lhs} configurations on this FPGA-based system to gather responses for training our base model. The generated responses, along with the applied configuration options (*ref.* Table 6.1), form the input to our base ML algorithm. In the third phase (❸), we train our ML algorithm (Section 6.2.4) using ensemble learning [355]. We divide our dataset into 10 equal subsamples during cross-validation, of which 1 set is used for validation. Once trained, the framework can predict the performance and resource usage on the base system (with a low-end FPGA) of previously-unseen configurations, which are not part of the c_{lhs} configurations used during training.

Target Model Building. To transfer the base model, which we built in the previous

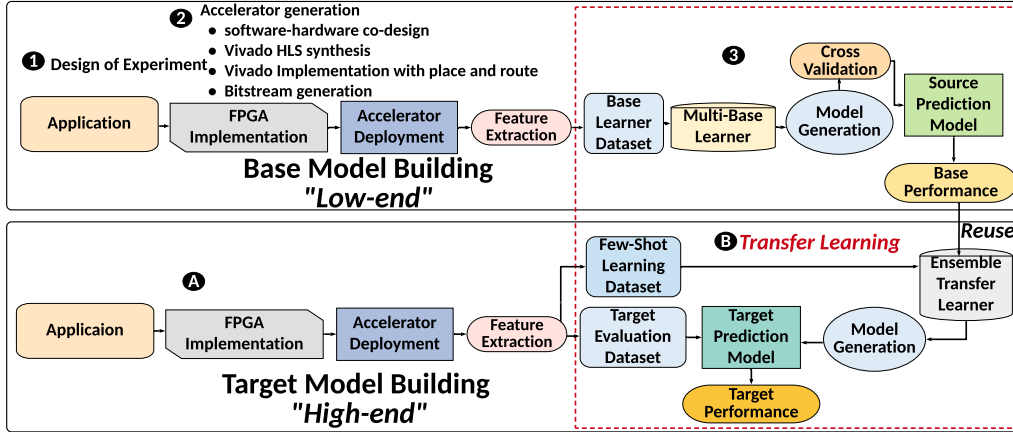


Figure 6-2: Overview of LEAPER. **Base Model Building:** LEAPER builds ML models that predict performance and resource usage for an application on an FPGA. **Target Model Building:** with *few-shot learning*, LEAPER adapts base models to a new, unknown environment, from which only a few labeled samples are needed.

stage, to a target cloud environment, we introduce the *few-shot learning* target model stage. In the first phase (A in Figure 6-2) of the target model building, we repeat the accelerator generation step to get a few samples. We perform this step to create our *few-shot* transfer learning dataset (c_H), which is used to adapt the base model to the target cloud environment. In the final phase (B), we train our transfer learners (see Section 6.2.5) to leverage the base model to perform predictions for a new, unknown target environment (new application or hardware).

6.2.2 FPGA Configuration Options and Application Features

The ML feature vector used for training an ML model is composed of FPGA configuration options (Table 6.1) and application features (Table 6.2). Table 6.1 describes commonly used HLS pragmas that belong to our FPGA configuration options for both the base and the target environment and constitute part of our ML feature vector. We select these HLS pragmas because they are used to optimize and tune the performance of FPGA implementations [483].

Both *loop pipelining* (PL) and *loop unrolling* (U) can improve application performance significantly. To enable simultaneous memory accesses, *array partitioning* (PR) divides arrays into smaller memory units of arbitrary dimensions to map them to different memory banks. This optimization produces considerable speedups but consumes more resources. *Inlining* (I) ensures that a function is instantiated as dedicated hardware. *Dataflow* (D) allows parallel execution of tasks, which is similar to multi-threading in CPUs. In addition, *burst read* (R) and *write* (W) access to/from the

Table 6.1: The FPGA configuration options used to train our ML-models.

Configuration	Description
Pipelining (PL)	Enabled/Disabled
Partitioning (PR)	Block/Cyclic/Complete (Factor: $2^n, 1 \leq n \leq 6$)
Inlining (I)	Enabled/Disabled function inlining
Dataflow (D)	Task level pipelining
Read burst (R)	Read data burst from the host
Write burst (W)	Write data burst from the host
Unrolling (U)	Unrolling factor (Factor: $2^n, 1 \leq n \leq 6$)
FPGA Frequency (F)	Four-different frequency levels for the FPGA logic

host guarantee that the accelerator is not stalled for data. Moreover, *FPGA frequency* (F) affects not only performance but also resource consumption. For instance, to meet the FPGA timing requirements, the FPGA tool tries to insert registers between the flip-flops, which increases the resource consumption.

In total, our configuration options for a particular application consist of up to 4,608 configurations. The actual configuration space of an application depends on the specific application characteristics (see Table 6.3). For example, we include loop unrolling in the configuration space when an application contains loops that can be unrolled.

For each application kernel k processing a dataset d , we obtain an application profile $p(k, d)$. $p(k, d)$ is a vector where each parameter is a statistic about an application feature. Table 6.2 lists the main application features we extract by using the LLVM-based PISA analysis tool [25]. We select these features to analyze the behavior of an application (data reuse distance, memory traffic, memory footprint, etc.). Ultimately, the application profile p has 395 features, which includes all the sub-features of each metric we consider.

Table 6.2: Main application features extracted from LLVM.

Application Feature	Description
Instruction Mix	Fraction of instruction types (integer, floating point, memory read, memory write, etc.)
ILP	Instruction-level parallelism on an ideal machine.
Data/Instruction reuse distance	For a given distance δ , probability of reusing one data element/instruction (in a certain memory location) before accessing δ other unique data elements/instructions (in different memory locations).
Register traffic	Average number of registers per instruction.
Memory footprint	Total memory size used by the application.

6.2.3 Latin Hypercube Statistical Sampling

Running experiments to collect training data for all available optimization options can be an extremely time-consuming process. For example, the configuration options (CO) of only eight parameters with two possible values each entails $2^8 = 256$ different configuration inputs. If we spend 6 hours (e.g., FPGA downstream implementation process on an ADM-PCIE-KU3 FPGA board [6]) to collect one training point, it would take us ~ 64 days to collect data for all configurations for just *one* application on a *single* platform. This “brute-force” approach to collecting training data is too time-consuming: the sheer number of experiments renders a detailed implementation intractable.

To create a cost-effective model, we use the *design of experiments* (DoE) methodology [321] to minimize the number of experiments needed for training data collection without sacrificing the amount and quality of the information gathered from the experiments. DoE is a set of statistical techniques meant to locate a small set of points in parameter space to represent the entire parameter space. In particular, we make use of a type of DoE called *Latin hypercube sampling* (LHS) [263] because it allows each of the critical parameters to be represented in a fully stratified manner (i.e., dividing the configuration space into subgroup before further sampling), which provides a better coverage [127].

LHS divides each parameter range into k intervals and takes only one sample from each interval with equal probability, which is more efficient than a random approach and more cost-effective than a “brute-force” approach. To apply LHS, we choose m sample points, each from a specific interval, which together we refer to as c_{lhs} . Thus, LHS guarantees effective space-filling, i.e., LHS spreads out points with the aim of encouraging a diversity of data [263]. Figure 6-3 illustrates LHS with two parameters $x1$ and $x2$, which create an input space that is divided into equal-area intervals.

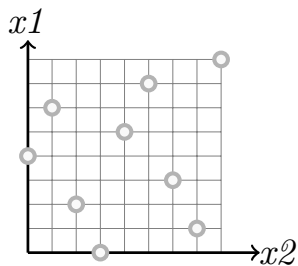


Figure 6-3: LHS with 2 parameters where the input space is divided into equal intervals and 9 non-overlapping sample points are chosen.

6.2.4 Base Model Building

The third phase of LEAPER is the base learner training phase. Formally, in a learning task, \mathcal{X} represents feature space with label \mathcal{Y} , where a machine learning model is responsible for estimating a function $f : \mathcal{X} \rightarrow \mathcal{Y}$. LEAPER predicts the

execution time (resource consumption) \mathcal{Y} for a tuple (p, k, c) that belongs to the ML feature space \mathcal{X} , where p is an FPGA-based configuration option (see Section 6.2.2) that runs an application characteristics k , with an optimization configuration vector c .

We use two base learners. Our base learners are non-linear algorithms that can capture the intricacies of FPGA architectures by predicting the execution time or resource consumption. Our first algorithm is the *random forest* (RF) [61]. RF consists of an ensemble of learners where it aggregates the predictions of the weak learners to select the best prediction. This technique is called *bagging*. We use RF to avoid a complex feature-selection scheme since RF embeds automatic procedures that are able to screen many input features [300], like the ones we selected in the previous section. Starting from a root node, RF constructs a tree and iteratively grows the tree by associating a node with a splitting value for an input feature to generate two child nodes. Each node is associated with a prediction of the target metric, equal to the observed mean value in the training dataset for the input subspace that the node represents. Our second learner is *gradient boosting* [137], which consists of an ensemble of learners. Gradient boosting aims to *boost* the accuracy of a weak learner by using other learners to correct its predictions. Bagging reduces model variance and boosting decreases errors [242]. Therefore, we use random forest and gradient boosting together to increase the predictive power of our final base model.

The training dataset for our base model has two parts: (1) an optimization configuration vector c , whose representation remains invariant across different environments, and (2) the responses corresponding to each tuple (p, k, c) . To gather the architectural responses, we run each application k belonging to the training set \mathbb{T} with an input dataset d on an FPGA-based platform p , deploying a configuration c . This way, we obtain the execution time for the tuple (p, k, d) , which we can use as a *label* (\mathcal{Y}) for training our base learner for performance prediction. We build a similar model to predict resource consumption, where we use the resource consumption $(\eta_{\{BRAM,FF,LUT,DSP\}})$ of the tuple (p, k, d) as a *label* when we train our base learner for resource consumption. After training our base learners, we can predict the execution time (resource usage) $(\hat{f}_s : \mathcal{X}_s \rightarrow \mathcal{Y}_s)$ of tuples (p, k, d) that are *not* in the training set. We use 10-fold cross-validation to validate our base learner’s performance, whereby the data is divided into ten validation sets.

6.2.5 Cloud Model Building via Transfer Learner

The real strength of LEAPER comes from its ability to transfer trained FPGA models. LEAPER defines a target environment τ_t as an environment for which we wish to build a prediction model \hat{f}_t where, however, data collection is expensive, and a source environment τ_s as an environment for which we can *cheaply* collect many samples to build an ML model f_s . In our case, τ_s is a low-cost edge FPGA, while τ_t is

a high-cost cloud FPGA. LEAPER then transfers the ML model for τ_s to τ_t .

Algorithm 2 presents LEAPER’s transfer learning approach. LEAPER trains transfer learners (TL) that transform the source performance and utilization model f_s to the target model f_t by using a few sample observations from both the source and the target environments, which we refer to as c_{tl} . This helps us to avoid measuring all c_{lhs} from a cost-prohibitive target cloud environment. We select c_{tl} from c_{lhs} by applying a probability-based sampling technique called *reservoir sampling* [480]. Reservoir sampling assigns an equal probability of being selected to every element of a population (i.e., c_{lhs}). By using the selected c_{tl} , we generate a transfer model \hat{h}_t . Finally, to build \hat{f}_t from f_s we use \hat{h}_t that performs a non-linear transformation of the predictions of f_s . We use non-linear transfer learners because, based on our analysis (Section 6.3.5), non-linear models can capture the nonlinearity present in the FPGA performance and configuration options.

Algorithm 2 LEAPER’s transfer learning

- 1: **Input:**(1) Base learner (f_s) i.e., trained low-end edge FPGA prediction model,
 - 2: (2) Sub-sampled *few-shot learning* dataset $c_{tl} \subset c_{lhs}$ from the
 - 3: base and the target model
 - 4: **Output:** Target cloud FPGA model $\hat{f}_t : \mathcal{X}_t \rightarrow \mathcal{Y}_t$
 - 5: **Initialization:** Maximum number of iterations M
 - 6: **while** $M \neq 0$ **do**
 - 7: Normalize the feature vector
 - 8: Train ensemble transfer learners (TL) with c_{tl}
 - 9: Find the candidate TL (\hat{f}_t):
 - 10: $\hat{h}_t : \mathcal{X}_{tl} \rightarrow \mathcal{Y}_{tl}$ that minimizes the error over the $c_{lhs} - c_{tl}$
 - 11: Compute the mean relative error:
 - 12:
$$\epsilon_{mre} = \frac{1}{c_{lhs} - c_{tl}} \sum_{i=1}^{c_{lhs} - c_{tl}} \frac{|y_t^{acc} - y_t^{pred}|}{y_t^{acc}}$$
 - 13: Use identified \hat{h}_t to transform predictions of f_s :
 - 14: $\hat{f}_t = \hat{h}_t(f_s)$ where $f_s : \mathcal{X}_s \rightarrow \mathcal{Y}_s$
 - 15: $M \leftarrow M - 1$
 - return** \hat{f}_t
-

In transfer learning, a weak relationship between the base and the target environment can decrease the predictive power for the target environment model. This degradation is referred to as a *negative transfer* [202]. To avoid this, we use an ensemble model trained on the transfer set (i.e., the *few-shot learning* dataset in Figure 6-2) as our transfer learners (TLs). Our first TL is based on TrAdaBoost [102], a boosting algorithm, which is a learning framework that fuses many weak learners into one strong predictor by adjusting the weights of training instances. The motivation behind such an approach is that by fusing many weak learners boosting can improve the overall

predictions in areas where the previously grown learners did not perform well. We use Gaussian process regression [393] as our second TL. It is a Bayesian non-parametric algorithm that calculates the probability distribution over all the appropriate functions that fit the data. To transfer a trained model, we train TrAdaBoost and Gaussian progression, which are our candidate TLs. We choose the one that has minimum transfer error (see Line 10).

6.3 Evaluation

We evaluate LEAPER using six benchmarks (see Table 6.3), which are hand-tuned for FPGA execution covering several application domains, i.e., **(1) image processing:** histogram calculation (*hist*) [156], and canny edge detection (*cedd*) [156]; **(2) machine learning:** binary long short term memory (*blstm*) [112], digit recognition (*digit*) [538]; **(3) databases:** relational operation (*select*) [289]; and **(4) data reorganization:** stream compaction (*sc*) [156]. These kernels are specified in C/C++ code that is compiled to the FPGA target.

6.3.1 Hardware Platform and Tools

With high adoption of FPGAs in the cloud, various emerging CPU-FPGA platforms with competing cache-coherent interconnect standards are being developed, such as the IBM Coherent Accelerator Processor Interface (CAPI) [444], the Cache Coherent Interconnect for Accelerators (CCIX) [49], the Ultra Path Interconnect (UPI) [196], and the Compute Express Link (CXL) [421].

The benefits of employing such cache-coherent interconnect links for attaching FPGAs to CPUs, as opposed to the traditional DMA-like communication protocols (e.g., PCIe), are not only the ultra lower-latency and the higher bandwidth of the communication, but most importantly, the ability of the accelerator to access the entire memory space of the CPU coherently, without consuming excessive CPU cycles. Traditionally, the host processor has a shared memory space across its cores with coherent caches. Attached devices such as FPGAs, GPUs, network and storage controllers are memory-mapped because of which they use a DMA to transfer data between local and system memory across an interconnect such as PCIe. The attached devices can not see the entire system memory but only a part of it. Communication between the host processor and attached devices requires an inefficient software stack, including user-space software, drivers, and kernel-space modules, in comparison to the communication scheme between CPU cores using shared memory. Especially when DRAM memory bandwidth becomes a constraint, requiring extra memory-to-memory copies to move data from one address space to another is cumbersome [126]. This is

the driving force of the industry to push for coherency and shared memory across CPU cores and attached devices, like FPGAs. This way, the accelerators act as peers to the processor cores.

Based on this upcoming trend, in this thesis, we adopt cache-coherent FPGA accelerators, both for the low-end and the high-end systems. Specifically, we select a *low-end* edge PYNQ-Z1 [385] as the source platform to build base learners. We use the Accelerator Coherency Port (ACP) port [1] for attaching accelerators to the ARM Cortex A9 CPU of PYNQ-Z1. In addition, we select a CAPI-based system as the target platform that provides the most mature coherent accelerator-based ecosystem with a production-ready cloud offering through Nimbix Cloud [342].

We make use of CAPI in a coarse-grained way since we offload the entire application to the FPGA. In this case, CAPI ensures that the FPGA accelerators access the entire CPU memory with the minimum number of memory copies between the host and the FPGA, e.g., avoiding the intermediate buffer copies that a traditional PCIe-based DMA invokes [90]. However, depending on the application, the CAPI protocol can be employed in finer-grained algorithm-hardware co-design, like *Extra V* [256], where the authors aggressively utilize the fine-grained communication capability of CAPI to boost graph analytics performance. Table 6.4 summarizes the system details of the source and our on-premise research cloud environment as our target platform.

For accelerator implementation and deployment, we leverage CAPI-compatible tools offered by Xilinx. In particular, we use the Xilinx SDSoc [411] design tool for implementing the low-end system τ_s and the Vivado HLS [484] with IBM CAPI-SNAP framework⁴ for the high-end system τ_t . The SNAP framework provides seamless integration of an accelerator [72] and allows to exchange of control signals between the host and the FPGA processing elements over the AXI lite interface [36]. On task completion, the processing element notifies the host system via the AXI lite interface and transfers back the results via CAPI-supported DMA transactions.

As derived from the indicative prices listed at the right column of Table 6.4, the total cost of ownership (TCO) of a high-end system can be more than 100x of that of the low-end one; thus, it can be prohibitive for a bare-metal deployment for many users. Complementary, moving a workload to a cloud FPGA instance should offer such a speedup that it compensates for the extra design time, effort, and cost of this decision by the end-user. LEAPER helps a user to rapidly quantify such a decision by experimenting with low-cost and broadly available FPGAs, like the PYNQ-Z1.

⁴<https://github.com/open-power/snap>

Table 6.3: Evaluated applications; description including their major kernels and the input dataset. For major kernels, we mention the optimization space where \times represents the optimization being applied to multiple loops or elements. see Table 6.1 for description of the optimization options.

Application	Domain	Major Kernels	Dataset	Optimization space
blstm [112]	Machine learning	Hidden lay. fw	Fraktur OCR [525]	$2\times\text{PL}$, $3\times\text{PR}(2,4)$ I, $2\times\text{U}$
		Hidden lay. back		$2\times\text{PL}$, I, $2\times\text{U}$
		Output layer		PL, I, U+D, R, W, F
cedd [156]	Image proc.	Gaussian filter	Frame- 354×626 1000 frames	PL, PR(2,4), I, U
		Sobel filter		PL, PR(2,4), I, U
		Suppress. filter		PL, PR(2,4), I, U
		Hysteresis filter		PL, I, U+D, R, W, F
digit [538]	Machine learning	Hamming dist.	MNIST 18000 train 2000 test	$2\times\text{PL}$, $3\times\text{PR}(2,4)$, I, $4\times\text{U}$
		KNN voting		I+R,W,F
hist [156]	Image proc.	Histogram avg.	Input- 1536×1024 Bins-256	PL, PR(all), I, D, R, W, U, F
select [156]	Data-base	Selection	1048576 inputs	PL, I, D, R, W, F
sc [156]	Data reorg.	Count Compact	1048576 inputs	PL, I, D, R, W, U, F

6.3.2 Target Model Accuracy Analysis

LEAPER is used to transfer a trained model using *few-shot learning* to the τ_t 's optimization space. We then analyze the accuracy of the newly-built target model to predict the performance and resource utilization of all the other configurations in τ_t . We evaluate the accuracy of the transferred model in terms of the relative error ϵ_i to indicate the proximity of the predicted value y'_i to the actual value y_i across N test samples. The mean relative error (MRE) is calculated with Equation 6.1.

$$MRE = \frac{1}{N} \sum_{i=1}^N \epsilon_i = \frac{1}{N} \sum_{i=1}^N \frac{|y'_i - y_i|}{y_i}. \quad (6.1)$$

Performance Model Transfer. Figure 6-4 shows LEAPER's accuracy for transferring *across different cloud platforms*. We make the following four observations.

First, as we increase the number of labeled samples, the target model accuracy increases. However, the accuracy saturates and, with 5-10 *shots*, we can achieve an accuracy as high as 80 to 90%.

Second, compared to applications with multiple complex kernels (*blstm*, *cedd*, *digit*), simpler kernels (*hist*, *sc*, *select*) can be more easily transferred using fewer samples. Applications with multiple kernels have a larger optimization space. The large optimization space leads to more complex interactions that have compounding effects with other optimization options because we are modeling for multiple kernels

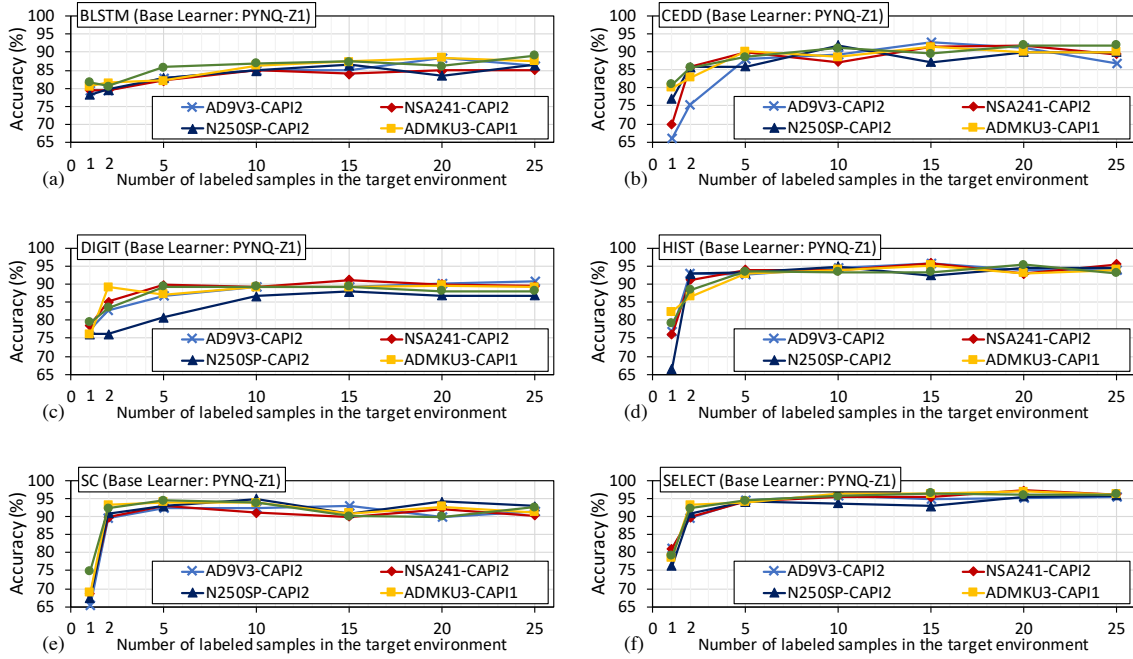


Figure 6-4: LEAPER’s accuracy for transferring base models across CAPI-enabled cloud FPGA-based systems. The legends indicate the target platforms. The base model was trained on a low-end PYNQ-Z1 board and, for each application, we *transfer* this model to different high-end cloud FPGA-based platforms using different samples (horizontal axis) from the target platform. Once trained using *few shot*, the transferred model makes predictions for all other configurations in the target platform.

rather than just a single kernel. Additionally, simple kernels such as *sc* and *select* have been implemented using *hls stream* interfaces. Here rather than storing intermediate data in local FPGA memories, we read streams of data, and hence certain complex optimizations (like array partitioning) cannot be applied. This leads to a change in the feature space of different environments.

Third, less severe changes are more amenable to transfer as the source, and target models are more closely related, e.g., transferring to CAPI1 (PCIe Gen3 with ~ 3.3 GB/s bandwidth) from low-end PYNQ with PCIe Gen2 ~ 1.2 GB/s bandwidth entails a smaller increment in bandwidth than moving to CAPI2, which offers R/W bandwidth of ~ 12.3 GB/s.

Fourth, change in the technology node from one FPGA to another has a lower impact than changing the external bandwidth to a new interconnect standard on the transferring process.

Figure 6-5 shows LEAPER’s accuracy for transferring ML models *across different applications*. We make the following three observations. First, we make a similar observation in the case of transferring models across different platforms: as we increase

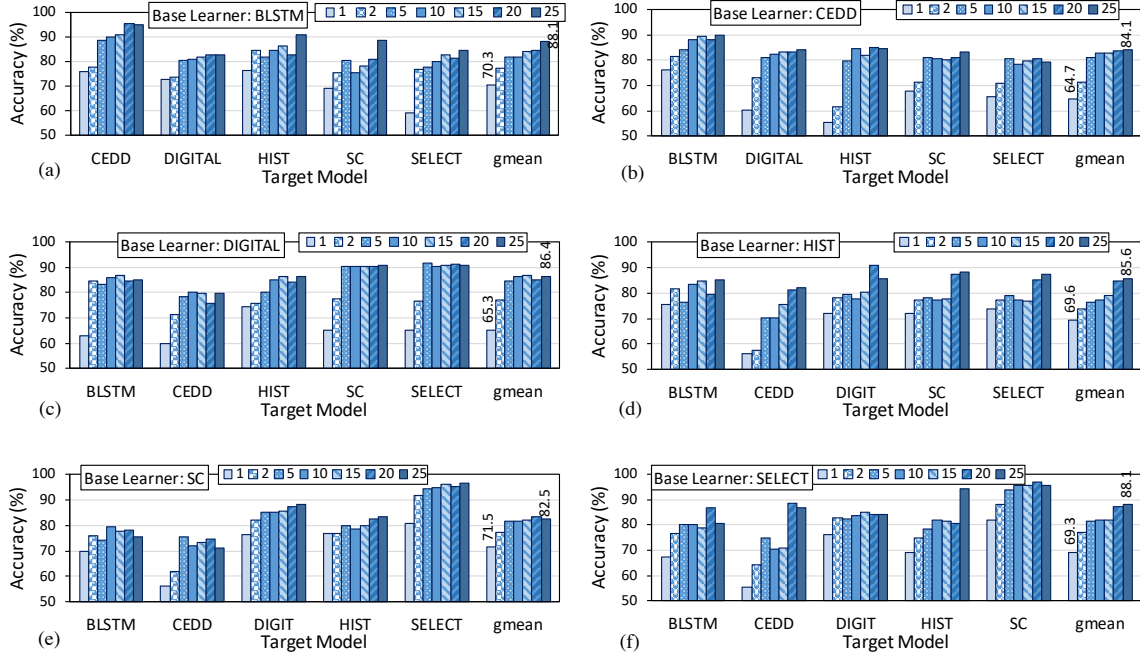


Figure 6-5: LEAPER’s accuracy for transferring base models across various applications. The legends indicate the number of samples. Each plot represents a different application as a base learner. We *transfer* these base learners, trained on the PYNQ-Z1 platform, by using invariant configuration features to build a target application model.

the number of training samples, the mean relative error for most applications decreases. Second, we notice that the most considerable improvement in accuracy occurs when our sample size (c_{tl}) is between 2 to 10. In most cases, the accuracy saturates after 20 samples. Third, in some cases, we see a decrease in accuracy when increasing the number of samples. This result could be attributed to training with a small amount of data, which can sometimes lead to overfitting [102].

We further explain our results by measuring the divergence of performance distributions to quantify the statistical distance between the source and target models, see Section 6.3.5. We also compare the average accuracy of predicting performance across boards and applications using different TMs (see Table 6.5).

Resource Model Transfer. By using LEAPER, we can also train a resource consumption model on a *low-end* source environment and transfer it to a high-end cloud target environment. Figure 6-6 shows the accuracy of a target model trained by *5-shot* transfer learning for predicting a resource utilization vector $\eta_{\{BRAM, FF, LUT, DSP\}}$. Note: the reported accuracy is for the transferred model, i.e., using a base model (low-end FPGA) to predict a target model (high-end cloud FPGA) after few-shot learning.

Table 6.4: System parameters and configuration.

Low-end base system		Indicative price		
Embedded Board	PYNQ-Z1 ZYNQ [385] XC7Z020-1CLG400C ARM Cortex-A9 processor @650MHz, dual-core	\$199 ⁵		
On-prem cloud target system with OpenStack[354] and KVM Hypervisor				
Host Configuration	IBM® POWER9 AC922 @2.3 GHz, 16 cores 4-way SMT, 32 KiB L1 cache, 256 KiB L2 cache, 10 MiB L3 cache, 16x32GiB RDIMM DDR4 2666 MHz ⁷	\$55000-\$75000 ⁶		
FPGA Description				
Board	FPGA Family	Device	Interface	
ADM-PCIE-8K5 [3]	Kintex UltraScale	XCKU115-2	CAPI-1	N/A
ADM-PCIE-KU3 [6]	Kintex UltraScale	XCKU060-2	CAPI-1	N/A
Semptian NSA241 [344]	Virtex UltraScale	XCVU9P-2	CAPI-2	N/A
ADM-PCIE-9V3 [5]	Virtex UltraScale	XCVU3P-2	CAPI-2	N/A
N250SP [335]	Kintex UltraScale	KU15P-2	CAPI-2	N/A

⁶ <https://store.digilentinc.com/pynq-z1-python-productivity-for-zynq-7000-arm-fpga-soc/>, Accessed 12 Jan. 2021.

⁷ <https://www.microway.com/product/ibm-power-systems-ac922/>, Accessed 12 Jan. 2021.

N/A⁸: Not available indicative price from an online store, but in the region of \$2500-\$5000 for our purchased on-prem cards.

Table 6.5: Average accuracy (%) comparison of LEAPER with decision tree (DT) and adaBoost (ADA) as TL for 5-shot transfer.

Environment	DT	ADA	LEAPER
Across Board	77.7	83.2	89.8
Across Application	70.6	73.5	81.2

In Figure 6-6a, the horizontal axis depicts the target platform, while the base learner is trained on a PYNQ-Z1 board. In the case of an application model transfer (Figure 6-6b), the platform remains unchanged (PYNQ-Z1), while the base learner application changes (horizontal axis). We make three observations. First, the resource model shows low error rates for predicting BRAM and DSP. This is attributed to the fact that the technological configuration of these resources remains relatively unchanged across platforms (e.g., BRAM is implemented as 18 Kbits in both the source and target platforms). Second, flip-flops and look-up-tables have comparably higher error rates because the configuration of CLB⁹ slices varies with the transistor technology and FPGA family. Third, Figure 6-6b shows the mean accuracy for transferring different application-based models on a fixed FPGA board. We observe relatively low accuracy for DSP consumption while transferring a base model trained on *hist*. This low accuracy is because the *hist* FPGA implementation does not make use of DSP units. However, all other applications utilize DSPs. Therefore, the ML model trained on *hist* is not able to perform well in other *transferred* environments.

⁹A configurable logic block (CLB) is the fundamental component of an FPGA, made up of look-up-tables (LUTs) and flip-flops (FF).

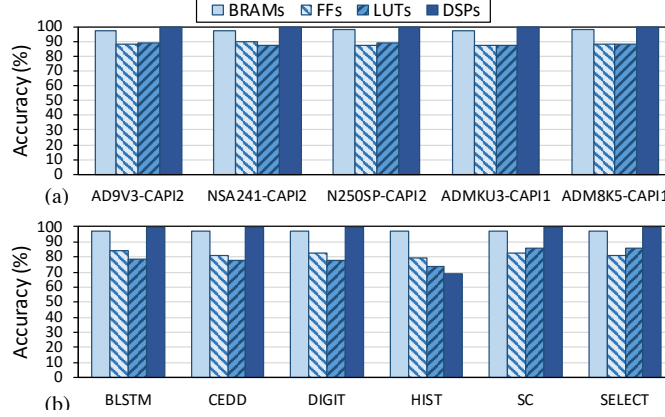


Figure 6-6: LEAPER’s average accuracy for transferring FPGA resource usage models through 5-shot using (a) a base learner trained on a low-end PYNQ-Z1 to different high-end target FPGA boards (horizontal axis), and (b) different applications as base learners (horizontal axis) to all the target applications, on low-end PYNQ-Z1 board.

6.3.3 Target Cloud FPGA Model Building Cost

Table 6.6 shows the time for collecting (see “DoE run (hours)”) the 50 sampled DoE configurations (c_{hs}) that we use to gather training data. Please note that while the process of synthesis and P&R of the high-end system’s FPGA, which is needed to obtain the maximum operating clock frequency and the resources’ utilization, can be carried out offline, most of the cloud providers are offering VMs with all the appropriate software, IPs and licenses needed to generate an FPGA image ready to be deployed at their cloud infrastructure (e.g., the Vivado AMI of AWS [482]). This justifies the argument of the cost of the cloud environment for DoE runs. Specifically, we use a Linux image with FPGA and SoC development tools, IPs, and licenses to generate bitstreams for the selected Xilinx devices of Table 6.4 on the Nimbix cloud.

Table 6.6 also includes the execution time on the ADM-PCIE-KU3 cloud platform (“Exec (msec)”) and the transfer time (“Transfer (msec)”) for each model. By using transfer learning, the DoE runtime is amortized and, by using a few labeled samples c_{tl} (“5-shot (hours)”) from the target platform, we can transfer a previously trained model and make predictions for all the other configurations for the target platform. As a result, quick exploration and significant time savings (at least $10.2\times$) are possible when transferring a model (i.e., “5-shot (hours)” + “Transfer (msec)”) as compared to building a new model from scratch (i.e., “DoE run (hours)” + “Exec (msec)”). Note, LHS reduces training samples from 500+ to 50, while 5-shot transfer learning further reduces this space to 5, so we achieve $100\times$ effective speedup compared to a traditional “brute-force” approach.

Table 6.7 mentions the performance and resource utilization for our considered

Table 6.6: DoE time for gathering sampled data points for a single CPU-FPGA platform (“DoE run (hours)”), DoE execution time on the deployed platform (“Exec (ms)”), Estimated Cost on a cloud platform (“Est. Cost (\$)”), time for gathering 5 labeled samples (“5-shot (hours)”), LEAPER time including the transfer time (“Transfer (msec)”), “Speedup” over building a new model from scratch using just the DoE data (still more cost-efficient than traditional “brute-force” training).

Application Name	Transfer Time						Speedup
	DoE run (hours)	Exec (msec)	Est.Cost ⁷ (\$)	5-shot (hours)	Transfer (msec)	Est.Cost ⁷ (\$)	
blstm	135	1245	168.7	13	55.6	16.2	10.4
cedd	124	2217	155.0	12	26.5	15.0	10.3
digit	122	873	152.5	12	58.8	14.9	10.2
hist	97	1104	121.2	9	17.1	11.3	10.8
sc	104	4018	130.0	10	27.9	12.4	10.4
select	106	3978	132.5	10	27.6	12.5	10.6

⁷The cost is estimated based on an enterprise online cost estimator [341], using a public-cloud system with configuration akin to our on-prem system. Specifically, we have selected an *n2* (8-core, 64GB RAM VM - 1.25\$/h) for bitstream generation (x86) and an *np8f1* instance (160-thread POWER8, 1TB RAM, ADM-PCIE-KU3 with CAPI-1 - 3\$/h) for deployment.

applications both on a low-end system and a high-end cloud system. We use LEAPER to obtain the performance and resource utilization for the high-end cloud configuration.

Table 6.7: Execution time and resource utilization for low-end base configuration (PYNQ-Z1) and high-end cloud configuration, a Nimbix *np8f1* instance (POWER8, ADM-PCIE-KU3 with CAPI-1).

Application	Config.	Exec (msec)	BRAM	DSP	FF	LUT
blstm	low-end	4200	80%	15%	24%	47%
	high-end	1245	62%	8%	12%	21%
cedd	low-end	10254	83%	37%	95%	97%
	high-end	2217	56%	3%	75%	94%
digit	low-end	2458	94%	33%	79%	85%
	high-end	873	84%	12%	24%	75%
hist	low-end	6173	94%	0%	11%	37%
	high-end	1104	67%	0%	5%	30%
sc	low-end	19306	82%	0.4%	12%	25%
	high-end	4018	91%	0.1%	12%	23%
select	low-end	18306	82%	0.4%	12%	25%
	high-end	3918	91%	0.1%	12%	23%

6.3.4 Base Model Accuracy Analysis

We also evaluate the accuracy of our base model. The base model (Section 6.2.4) is trained on our low-end edge PYNQ board using $c_{l_{hs}}$ configurations sampled using

LHS. The base can predict performance (resource utilization) outside the base learner dataset (DoE configurations) c_{lhs} (see Figure 6-2). To assess our base model, we use 30 previously unseen configurations that are not part of c_{lhs} on the base system, and we evaluate the mean relative error for all 30 unseen configurations on all six applications. Figure 6-7 shows LEAPER’s base model accuracy results.

We compare LEAPER to three other ML algorithms that are also trained using c_{lhs} configurations to predict performance and resource consumption: XG-Boost (XGB) based on Dai *et al.* [101], an artificial neural network (ANN) used by Makrani *et al.* [298] and a traditional decision tree (DT). We make three observations. First, on average, LEAPER is more accurate in terms of performance (resource utilization) prediction than the other ML models. Second, XGBoost is more data-efficient than ANNs [101] and can perform better than decision trees [437]. Third, ANN is more accurate than the decision tree, but it is less accurate than LEAPER. This is because ANN requires a much larger training dataset to reach LEAPER’s accuracy [263].

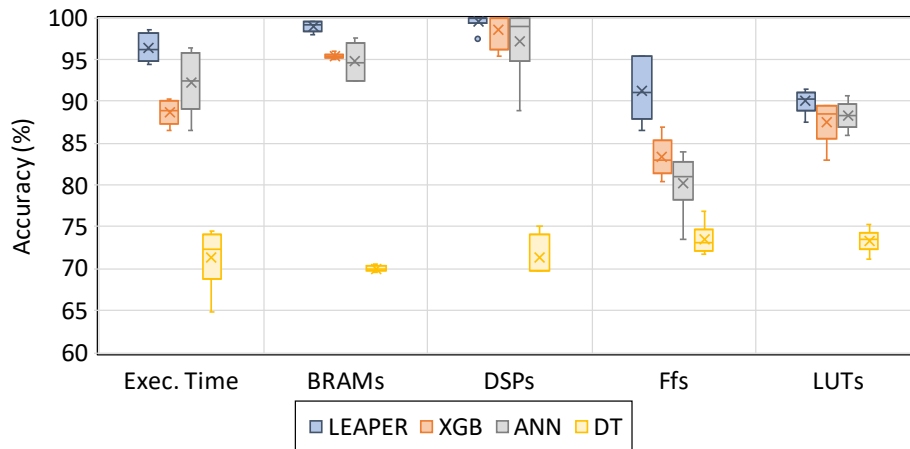


Figure 6-7: Mean accuracy for performance and resource utilization predictions using LEAPER’s base model vs. other methods: XGB (XGBoost), an artificial neural network (ANN), and a decision tree (DT).

6.3.5 Why Does LEAPER Work?

To explain our transfer learning results, we analyze the degree of *relatedness* between the source and target environments. We perform a correlation analysis followed by a divergence analysis of the performance distributions of the environments.

Using the correlation analysis, we make the following four observations. First, we see a high correlation of 0.76 to 0.97 between the source and target execution time for different target hardware platforms, which indicates that the target model’s performance behavior can easily be learned using the source environment. As the linear correlation is not 1 for all platforms, the use of a nonlinear transfer model is

substantiated. Second, as we increase the external bandwidth of the target platform (i.e., CAPI1 to CAPI2), the correlation becomes lower because the hardware change is much more *severe*, coming from a low-end FPGA with limited external bandwidth. Third, compared to using a single transfer learner, an ensemble of learners can perform more accurate and robust predictions (see Figure 6-4, Figure 6-5, and Figure 6-6). Fourth, the correlation between applications on a single platform is lower (0.45 to 0.9) because of the varying application characteristics and optimization space.

We measure the relatedness of the performance distributions of the source ($P(\tau_s)$) and the target applications ($P(\tau_t)$) because application-based environments exhibit a low linear correlation. We employ the Jensen-Shannon Divergence (JSD) [273] (see Table 6.8) to quantify the statistical distance between $P(\tau_s)$ and $P(\tau_t)$. The lower the values of JSD, the more similar the target environment is to the source (i.e., if $D_{JSD}(P(\tau_t)||P(\tau_s)) = 0$ implies the distributions are identical, and 1 indicates unrelated distributions). This analysis confirms the trend observed from transferring application models (Figure 6-5), i.e., the more closely related the source and target applications, the fewer samples are required to train our nonlinear transfer learners. The measured distance between the tasks is proportional to the error of the target task. As can be seen from Table 6.8 for many applications, transfer learning to build accurate models is feasible since their JSD is limited. Similar trends are observed for the resource utilization model.

Table 6.8: Jensen-Shannon Divergence (JSD) [273] between performance distributions of different applications. JSD measures statistical distance between two probability distributions.

		Base Learner					
		blstm	cedd	digit	hist	sc	select
Target Model	blstm	0.00	0.24	0.34	0.25	0.31	0.30
	cedd	0.24	0.00	0.49	0.54	0.41	0.40
	digit	0.34	0.49	0.00	0.25	0.21	0.21
	hist	0.25	0.54	0.25	0.00	0.25	0.24
	sc	0.30	0.40	0.21	0.24	0.00	0.05
	select	0.30	0.41	0.21	0.25	0.05	0.00

6.3.6 Discussion and Limitations

Transfer to a new platform and application simultaneously. In supervised learning, transferring both to a new platform and application at the same time would lead to sub-optimal results (as observed in [28]). This is because we would perform two-levels of the transfer. Moreover, the ML model needs to have some notion of the target environment. Therefore, we explicitly exclude this option in this chapter.

FPGA resource-constrained environments. During partial reconfiguration [46] or in a multi-tenant environment [379], we are often constrained by limited resources [461]. In such scenarios, resource management is more efficient to be controlled by a middleware layer [474]. We do not assume such as a middleware. Therefore, our analysis targets bare-metal systems. In the future, we aim to extend our work to such scenarios as well.

LEAPER generality to other platforms. LEAPER, in essence, is a framework for building and then transferring models from a small edge platform to any new, unknown FPGA-based environment. We demonstrated our approach using the cloud as our target environment because cloud systems often use expensive, high-end FPGAs, e.g., Amazon AWS F1 cloud [21], Alibaba Elastic cloud with FPGAs [16], etc. Thus, we can achieve tangible gains in terms of cost, efficiency, and performance.

Effect of FPGA resource saturation. An FPGA gives us the flexibility to map operations to different resources. For example, we can map a multiplication operation either to a CLB or a DSP slice. The deciding factor is the operand width (as shown in Appendix B). If the operand width is smaller than the DSP slice width, the operation is mapped to a CLB else to a DSP unit. An ML-model can be trained to learn such relations. However, we avoid it in our current chapter.

6.4 Related Work

Transfer Learning. Recently, transfer learning [44, 81, 359] has gained traction to decrease the cost of learning by transferring knowledge. Valov *et al.* [475] investigated the transfer of application models across different CPU-based environments using linear transformations. Jamshidi *et al.* [202] demonstrated the applicability of using nonlinear models to transfer CPU-based performance models. The works above influenced the design of LEAPER. In contrast, we focus on FPGA-based systems, where we tailor the hardware circuitry to an application by leveraging the large high-dimensional optimization space and has very low productivity due to the time-consuming downstream implementation process. Moreover, we use an ensemble of transfer learners that transfers accurate models to a target environment via *few-shot learning*.

ML-based FPGA Modeling. Recent works propose ML-based methods to overcome the issue of low productivity with FPGAs. O’Neal *et al.* [346] use CPU performance counters to train several ML-based models to predict FPGA performance and power consumption. Makrani *et al.* [298] trained an ANN to predict application speedup across different FPGAs. Dai *et al.* [101] use ML to predict post-implementation

resource utilization from pre-implementation results. However, these solutions become largely impractical once the platform, the application, or even the size of the workload changes. LEAPER proposes to reuse previously built models on a low-end source environment to accelerate the learning of ML models on a high-end target environment through transfer learning. Unlike LEAPER, past works [536] apply traditional, time-consuming brute-force techniques to collect training dataset. These techniques quickly become intractable when the number of optimization parameters increases due to the curse of dimensionality [48].

Analytical FPGA Modeling. Analytic models abstract low-level system details and provide quick performance estimates at the cost of accuracy. These approaches [91, 532, 535] analyze dataflow graphs and apply mathematical equations to approximate resource usage or performance after the HLS pre-implementation phase. These approaches enable quick early-stage design studies, however, analytical models cannot model the intricacies of the complete FPGA implementation process [101]. Therefore, these approaches provide crude estimates of the actual performance. Moreover, these models require expert knowledge to form mathematical equations. In contrast, LEAPER does not require expert knowledge to construct equations. LEAPER learns from the data, taking into account the complete downstream implementation process, and provides the capability to transfer models from an edge-FPGA to a high-end cloud FPGA environment.

LEAPER is the first method to deal with transfer learning on FPGAs, which are infamous for low productivity due to the time-consuming mapping process. LEAPER not only allows us to predict performance for different configurations (Figure 6-2 “Base model building” stage) but also provides the ability to transfer the models (Figure 6-2 “Target model building - Few-shot learning” stage). LEAPER is orthogonal to previous approaches (ML and non-ML) as it also provides the ability to “transfer” models in milli-seconds (*ref.* Table 6.6). Additionally, in this chapter, we leverage the *design of experiment* techniques to reduce the training overhead dramatically and still build accurate models.

6.5 Conclusion

We introduce LEAPER, the first *transfer learning*-based approach for FPGA-based systems. LEAPER combines statistical techniques and transfer learning to minimize the ML training data collection overhead. It overcomes the inefficiency of traditional ML-based methods by accurately *transferring* an existing ML model built on an inexpensive, low-end FPGA platform to a new, unknown, high-end environment.

The experimental results show that we can develop cheaper (with *5-shot*), faster (up to $10\times$), and highly accurate (on average 85%) models to predict performance and resource consumption in a new, unknown target cloud environment. We believe that LEAPER would open up new avenues for research on FPGA-based systems from edge to cloud computing, and hopefully, inspires the development of other alternatives to traditional ML-based models.

Chapter 7

Sibyl: Adaptive and Extensible Data Placement in Hybrid Storage Systems Using Online Reinforcement Learning

Hybrid storage systems (HSS) use multiple different storage devices to provide high and scalable storage capacity at high performance. Data placement across different devices is critical to maximize the benefits of such a hybrid system. Recent research proposes various techniques that aim to accurately identify performance-critical data to place it in a “best-fit” storage device. Unfortunately, most of these techniques are rigid, which (1) limits their adaptivity to perform well for a wide range of workloads and storage device configurations, and (2) makes it difficult for designers to extend these techniques to different storage system configurations (e.g., with a different number or different types of storage devices) than the configuration they are designed for. Our goal is to design a new data placement technique for hybrid storage systems that overcomes these issues and provides: (1) *adaptivity*, by *continuously learning* from and adapting to the workload and the storage device characteristics, and (2) *easy extensibility* to a wide range of workloads and HSS configurations.

We introduce *Sibyl*, the first technique that uses reinforcement learning for data placement in hybrid storage systems. *Sibyl* observes different features of the running workload as well as the storage devices to make system-aware data placement decisions. For every decision it makes, *Sibyl* receives a reward from the system that it uses to

evaluate the long-term performance impact of its decision and continuously optimizes its data placement policy online.

We implement Sibyl on *real* systems with various HSS configurations, including dual- and tri-hybrid storage systems, and extensively compare it against four previously proposed data placement techniques (both heuristic- and machine learning-based) over a wide range of workloads. Our results show that Sibyl provides 21.6%/19.9% performance improvement in a performance-oriented/cost-oriented HSS configuration compared to the best previous data placement technique. Our evaluation using an HSS configuration with three different storage devices shows that Sibyl outperforms the state-of-the-art data placement policy by 23.9%-48.2%, while significantly reducing the system architect’s burden in designing a data placement mechanism that can simultaneously incorporate three storage devices. We show that Sibyl achieves 80% of the performance of an oracle policy that has complete knowledge of future access patterns while incurring a very modest storage overhead of only 124.4 KiB.

7.1 Introduction

Hybrid storage systems (HSS) take advantage of both fast-yet-small storage devices and large-yet-slow storage devices to deliver high storage capacity at low latency [27, 39, 40, 55, 62, 70, 74, 76, 82, 84, 100, 115, 130, 184, 229, 230, 238, 244, 253, 258, 267, 270, 274, 283, 284, 287, 288, 291, 312, 343, 347, 349, 356, 396, 408, 409, 439, 441, 453, 456, 489, 511, 517, 518, 520, 530, 531, 540]. The key challenge in designing a high-performance and cost-effective hybrid storage system is to accurately identify the performance-criticality of application data and place data in the “best-fit” storage device [343].

Past works [80, 83, 117, 122, 162, 186, 189, 268, 293, 295, 303, 361, 389, 398, 403, 423, 446, 476, 492, 506, 507, 508, 516, 528, 533] propose many different data placement techniques to improve the performance of an HSS. We identify two major shortcomings of prior proposals that significantly limit their performance: lack of (1) adaptivity to workload changes and the storage device characteristics, and (2) extensibility.

(1a) Lack of adaptivity to workload changes. To guide data placement, past techniques consider only a limited number of workload characteristics [80, 122, 162, 268, 293, 294, 303, 322, 446, 476, 492]. Designers statically tune the parameters values for all considered workloads at design time based on empirical analysis and designer experience, and expect those statically-fixed values to be equally effective for a wide range of dynamic workload demands and system configurations seen in the real world. As a result, such data placement techniques cannot easily adapt to a wide range of dynamic workload demands and significantly underperform when compared to an oracle technique that has complete knowledge of future storage access patterns (up to

41.1% lower performance, ref. Section 7.3).

(1b) Lack of adaptivity to changes in device types and configurations. Most prior HSS data placement techniques (e.g., [80, 117, 122, 162, 268, 293, 303, 398, 446, 476, 492]) do not adapt well to changes in the underlying storage device characteristics (e.g., changes in the level of asymmetry in the read/write latencies, or the number and types of storage devices). As a result, existing techniques cannot effectively take into account the cost of data movement between storage devices while making data placement decisions. This lack of adaptivity leads to highly inefficient data placement policies, especially in HSSs with significantly-different device access latencies than what prior techniques were designed for (as shown in Section 7.3).

(2) Lack of extensibility. A large number of prior data placement techniques (e.g., [80, 122, 162, 268, 293, 303, 446, 492]) are typically designed for an HSS that consists of only two storage devices. As modern HSSs already incorporate more than two types of storage devices [303, 304, 398], system architects need to put significant effort into extending prior techniques to accommodate more than two devices. We observe that a state-of-the-art heuristic-based data placement technique optimized for an HSS with two storage devices [304] often leads to suboptimal performance in an HSS with three storage devices (up to 48.2% lower performance, ref. Section 7.8.7).

Our goal is to develop a new, efficient, and high-performance data placement mechanism for hybrid storage systems that provides (1) *adaptivity*, by *continuously learning* from and adapting to the workload and storage device characteristics, and (2) *easy extensibility* to a wide range of workloads and HSS configurations.

Key ideas. To this end, we propose Sibyl, a reinforcement learning-based data placement technique for hybrid storage systems.¹ Reinforcement learning (RL) [450] is a goal-oriented decision-making process in which an autonomous agent learns to take optimal actions that maximize a reward function by interacting with an environment. The key idea of Sibyl is to design the data placement module in hybrid storage systems as a reinforcement learning agent that *autonomously learns* and adapts to the best-fit data placement policy for the running workload and the current hybrid storage system configuration. For every storage page access, Sibyl observes different features from the running workload and the underlying storage system (e.g., access count of the current request, remaining capacity in the fast storage, etc.). It uses the features as *state* information to take a data placement *action* (i.e., which device to place the page into). For every action, Sibyl receives a delayed *reward* from the system in terms of per-request latency. This reward encapsulates the internal device characteristics of an HSS (such as read/write latencies, latency of garbage collection, queuing delays, error handling latencies, and write buffer state). Sibyl uses this reward to estimate the long-term impact of its action (i.e., data placement

¹In Greek mythology, Sibyl is an oracle who makes accurate prophecies [500].

decision) on the overall application performance and continuously optimizes its data placement policy online to maximize the long-term benefit (i.e., reward) of its actions.

Benefits. Formulating the data placement module as an RL agent enables a human designer to specify only *what* performance objective the data placement module should target, rather than designing and implementing a new data placement policy that requires explicit specification of *how* to achieve the performance objective. The use of RL not only enables the data placement module to *autonomously* learn the “best-fit” data placement strategy for a wide range of workloads and hybrid storage system configurations but also significantly reduces the burden of a human designer in finding a good data placement policy.

Challenges. While RL provides a promising alternative to existing data placement techniques, we identify two main challenges in applying RL to data placement in an HSS.

(1) Problem formulation. The RL agent’s effectiveness depends on how the data placement problem is cast as a reinforcement learning-based task. Two key issues arise when formulating HSS data placement as an RL problem: (1) taking into account the latency asymmetry within and across storage devices, and (2) deciding which actions to reward and penalize (also known as the *credit assignment problem* [317]). First, we need to make the agent aware of the asymmetry in read and write latencies of each storage device and the differences in latencies across multiple storage devices. Real-world storage devices could have dynamic latency variations due to their complex hardware and software components (e.g., internal caching, garbage collection, error handling, multi-level cell reading, etc.) [64, 65, 66, 67, 98, 159, 213, 362]. Second, if the fast storage is running out of free space, there might be evictions in the background from the fast storage to the slow storage.

As a result, when we reward the agent, not only there is a variable and delayed reward, but it is also hard to properly assign *credit* or *blame* to different decisions.

(2) Implementation overhead. A workload could have hundreds of thousands of pages of storage data, making it challenging to efficiently handle the large data footprint with a low design overhead for the learning agent.

To address the first challenge, we use two main techniques. First, we design a *reward* structure in terms of *request latency*, which allows Sibyl to learn the workload and storage device characteristics when continuously and frequently interacting with a hybrid storage system. We add a negative penalty to the reward structure in case of eviction, which helps with handling the credit assignment problem and encourages the agent to place only performance-critical pages in the fast storage. Second, we perform thorough hyper-parameter tuning to find parameter values that work well for a wide variety of workloads. To address the second challenge, we use two main techniques. First, we divide states into a small number of bins that reduce the

state space, which directly affects the implementation overhead. Second, instead of adopting a traditional table-based RL approach (e.g., [197]) to store the agent’s state-action information (collected by interacting with an HSS), which can easily introduce significant performance overheads in the presence of a large state/action space, we use a simple feed-forward neural network [526] with only two hidden layers of 20 and 30 nodes, respectively.

Key results. We evaluate Sibyl using two different dual-HSS configurations and two different tri-HSS configurations. We use fourteen diverse storage traces from Microsoft Research Cambridge (MSRC) [324] collected on real enterprise servers. We evaluate Sibyl on workloads from FileBench [455] on which it has never been trained. We compare Sibyl to four state-of-the-art data placement techniques. We demonstrate four key results. First, Sibyl provides 21.6%/19.9% performance improvement in a performance-oriented/ cost-oriented HSS configuration compared to the best previous data placement technique. Second, Sibyl outperforms the best-performing supervised learning-based technique on workloads it has never been trained on by 46.1% and 54.6%, on average, in performance-oriented and cost-oriented HSS configurations, respectively. Third, Sibyl provides 23.9%-48.2% higher performance in tri-hybrid storage systems than a state-of-the-art heuristic-based data placement technique demonstrating that Sibyl is easily extensible and alleviates the designer’s burden in finding sophisticated data placement mechanisms for new and complex HSS configurations. Fourth, Sibyl’s performance benefits come with a low storage implementation overhead of only 124.4 KiB.

This work makes the following **major contributions**:

- We show on real hybrid storage systems (HSSs) that prior state-of-the-art HSS data placement mechanisms fall short of the oracle placement due to: lack of (1) adaptivity to workload changes and storage device characteristics, and (2) extensibility.
- We propose Sibyl, a new self-optimizing mechanism that uses reinforcement learning to make data placement decisions in hybrid storage systems. Sibyl dynamically *learns*, using both multiple workload features and system-level feedback information, how to continuously adapt its policy to improve its long-term performance for a workload.
- We conduct an in-depth evaluation of Sibyl on real systems with various HSS configurations, showing that it outperforms four state-of-the-art techniques over a wide variety of applications with a low implementation overhead.
- We provide an in-depth explanation of Sibyl’s actions that show that Sibyl performs dynamic data placement decisions by learning changes in the level of asymmetry in the read/write latencies and the number and types of storage devices.
- We freely open-source Sibyl to aid future research in data placement for storage

systems [95].

7.2 Background

7.2.1 Hybrid Storage Systems (HSSs)

Figure 7-1 depicts a typical HSS consisting of a fast-yet-small storage device (e.g., [190, 404]) and a large-yet-slow storage device (e.g., [2, 191, 192, 412]). Traditional hybrid storage systems [80, 131, 313] were designed with a smaller NAND flash-based SSD and a larger HDD. Nowadays, hybrid storage systems come with emerging NVM devices (e.g., [92, 224, 232, 466]) coupled with slower high-density NAND flash devices [254, 303, 348, 350]. The storage management layer can be implemented either as system software running on the host system or as the firmware of a hybrid storage device (e.g., flash translation layer (FTL) in flash-based SSDs [64, 141]), depending on the configuration of the HSS. In this chapter, we demonstrate and implement our ideas in the storage management layer of the operating system (OS), but they can be easily implemented in firmware as well. The storage management layer in the OS orchestrates host I/O requests across heterogeneous devices, which are connected via an NVM Express (NVMe) [125] or SATA [158] interface. The storage management layer provides the operating system with a unified logical address space (like the multiple device driver (md) kernel module in Linux [277]). As illustrated in Figure 7-1, the unified logical address space is divided into a number of logical pages (e.g., 4 KiB pages). The pages in the logical address space are assigned to an application. The storage management layer translates a read/write performed on a logical page into a read/write operation on a target storage device based on the data placement policy. In addition, the storage management layer manages data migration between the storage devices in an HSS. When data currently stored in the slow storage device is moved to the fast storage device, it is called *promotion*. Promotion is usually performed when a page in the slow storage device is accessed frequently. Data is moved from the fast storage device to the slow storage device during an *eviction*. Eviction typically occurs when the data in the fast storage device is infrequently accessed or when the fast storage device becomes full.

The performance of a hybrid storage system highly depends on the ability of the storage management layer (Figure 7-1) to effectively manage diverse devices and workloads [303, 398]. This diversity presents a challenge for system architects when they design an intelligent data placement policy. A desirable policy has to effectively utilize the low latency characteristics of the fast device while making optimal use of its small capacity and should provide easy extensibility to a wide range of workloads and HSS configurations.

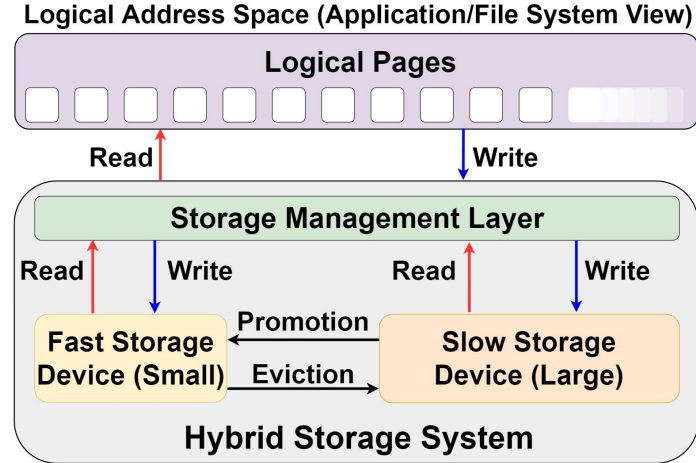


Figure 7-1: Overview of a hybrid storage system

7.3 Motivation

To assess the effectiveness of existing HSS data placement techniques under diverse workloads and hybrid storage configurations, we evaluate state-of-the-art heuristic-based (*CDE* [303] and *HPS* [310]) and supervised learning-based (*Archivist* [398]) techniques. We also implement an RNN-based data placement technique (*RNN-HSS*), adapted from hybrid main memory [117]. To evaluate the effect of underlying storage device technologies, we use three different storage devices: high-end (H) [190], middle-end (M) [192], and low-end (L) [412], configured into two different hybrid storage configurations: a performance-oriented HSS (*H&M*) and a cost-oriented HSS (*H&L*). Table 7.3 provides details of our system and devices. We restrict the fast storage capacity to 10% of the working set size of a workload, which ensures eviction of data from fast storage to slow storage when fast storage capacity is full.

CDE [303] allocates hot or random write requests in the faster storage, whereas cold and sequential write requests are evicted to the slower device. *HPS* [310] uses the access count of pages to periodically migrate cold pages to the slower storage device. *Archivist* [398] uses a neural network classifier to predict the target device for data placement. *RNN-HSS*, adapted from [117], is a supervised learning-based mechanism that exploits recurrent neural networks (RNN) to predict the hotness of a page and place hot pages in fast storage. We compare the above policies with three extreme baselines: (1) *Slow-Only*, where all data resides in the slow storage device (i.e., there is no fast storage device), (2) *Fast-Only*, where all data resides in the fast storage device, and (3) *Oracle* [310], which exploits complete knowledge of future I/O-access patterns to perform data placement and to select victim data blocks for eviction from the fast device.

We identify two major shortcomings of the state-of-the-art baseline data place-

ment techniques: lack of (1) adaptivity to workload changes and the storage device characteristics, and (2) extensibility.

(1a) Lack of adaptivity to workload changes. Figure 7-2 shows the average request latency of all policies, normalized to **Fast-Only**, under two different hybrid storage configurations. We make the following three observations. First, all the baseline techniques are only effective under specific workloads, showing significantly lower performance than **Oracle** in most workloads. **CDE**, **HPS**, **Archivist**, and **RNN-HSS** achieve comparable performance to **Oracle** for specific workloads (e.g., *hm_1* for **HPS** in *H&M*, *usr_0* for **CDE** in *H&L*, *hm_1* for **Archivist** in *H&M*, and **RNN-HSS** in *proj_2* for **CDE** in *H&L*). Second, the baselines show a large average performance loss of 41.1% (32.6%), 37.2% (55.5%), 39.7% (66.7%), and 34.4% (47.6%) compared to **Oracle**'s performance, under the *H&M* (*H&L*) hybrid storage configuration, respectively. Third, in *H&M*, the baseline techniques provide a performance improvement of only 1.4%, 7.4%, 3.5%, and 11.3% compared to **Slow-Only**.

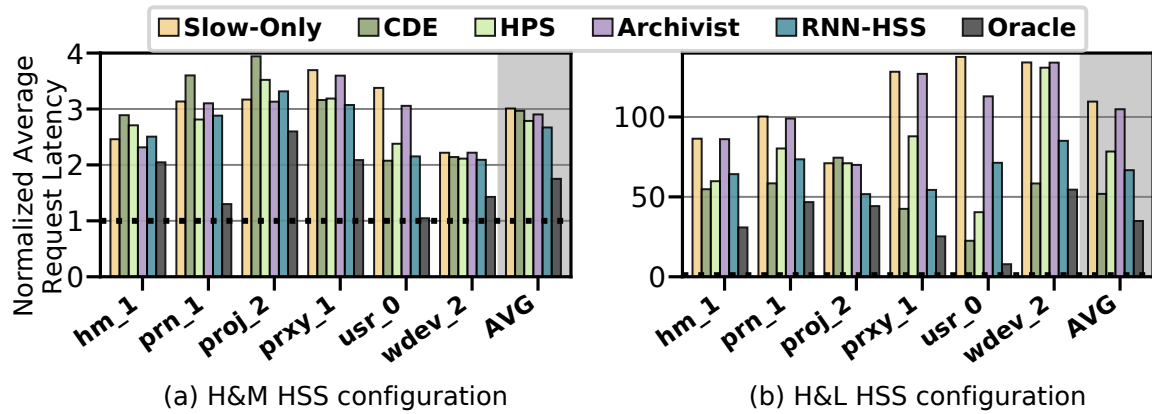


Figure 7-2: Average request latency normalized to **Fast-Only** policy

We conclude that all four baselines consider only a limited number of workload characteristics to construct a data placement technique, which leads to a significant performance gap compared to the **Oracle** policy. Thus, there is no single policy that works well for all the workloads.

To further analyze the characteristics of our evaluated workloads, we plot the average hotness (y-axis) and randomness (x-axis) in Figure 7-3. We provide details on these workloads in Table 7.4. In these workload traces, each storage request is labeled with a timestamp that indicates the time when the request was issued from the processor core. Therefore, the time interval between two consecutive I/O requests represents the time the core has spent computing. We quantify a workload's hotness (or coldness) using the average access count, which is the average of the access counts of all pages in a workload; the higher (lower) the average access count, the hotter (colder) the workload. We quantify a workload's randomness using the average request

size in the workload; the higher (lower) the average request size, the more sequential (random) the workload. From Figure 7-3, we make the following two observations. First, the average hotness and randomness vary widely between workloads. Second, we observe that each of our evaluated workloads exhibits highly dynamic behavior throughout its execution. For example, in Figure 7-4, we show the execution timeline of `rsrch_0`, which depicts the accessed addresses and request sizes. We conclude that an efficient policy needs to incorporate continuous adaptation to highly dynamic changes in workload behavior.

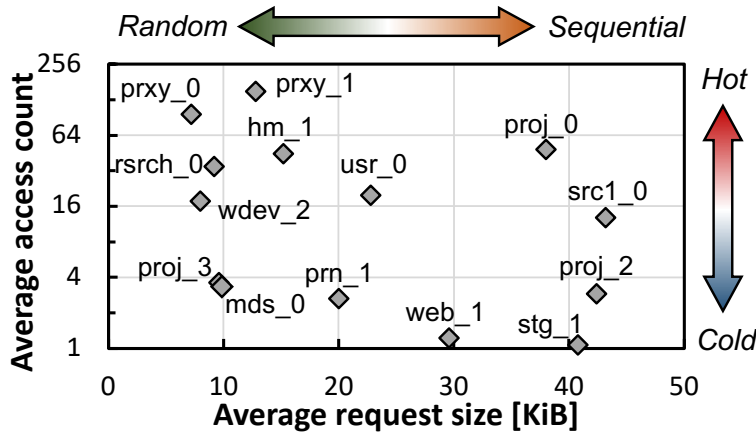


Figure 7-3: Randomness and hotness characteristics of real-world MSRC workloads [324]

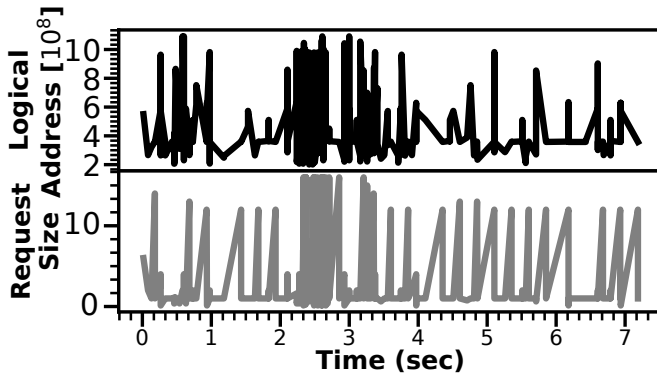


Figure 7-4: Timeline of accessed logical addresses and request sizes during the execution of `rsrch_0` workload

(1b) **Lack of adaptivity to changes in device types and configurations.** There are a wide variety and number of storage devices [2, 85, 92, 170, 190, 191, 192, 193, 224, 232, 254, 303, 314, 348, 350, 404, 412, 466] that can be used to configure an HSS. The underlying storage technology used in an HSS significantly influences the effectiveness of a data placement policy. We demonstrate this with an example observation from Figure 7-2. In the H&M configuration (Figure 7-2(a)), we observe that for certain workloads (`hm_1` and `prn_1`), both CDE and HPS provide rather low performance even compared to Slow-Only. Similarly, Archivist and RNN-HSS provide lower performance for `hm_1` and `proj_2` in H&M compared to Slow-Only. While in the H&L configuration (Figure 7-2(b)), we observe that CDE, HPS, Archivist, and RNN-HSS result in lower latency than Slow-Only for the respective workloads. Thus, we conclude that both heuristic-based and learning-based data placement policies lead to poor performance

due to their inability to holistically take into account the device characteristics. The high diversity in device characteristics makes it very difficult for a system architect to design a generic data-placement technique that is suitable for all HSS configurations.

(2) Lack of extensibility. As modern HSSs already incorporate more than two types of storage devices [303, 304, 312, 398], system architects need to put significant effort into extending prior data placement techniques to accommodate more than two devices. In Section 7.8.7, we evaluate the effectiveness of a state-of-the-art heuristic-based policy [304] for different tri-HSS configurations, comprising of three different storage devices. This policy is based on the CDE [303] policy that divides pages into hot, cold, and frozen data and allocates these pages to H, M, and L devices, respectively. A system architect needs to statically define the hotness values and explicitly handle the eviction and promotion between the three devices during design-time. Through our evaluation in Section 7.8.7, we conclude that such a heuristic-based policy (1) lacks extensibility, thereby increasing the system architect’s effort, and (2) leads to lower performance when compared to an RL-based solution (up to 48.2% lower).

Our empirical study shows that **the state-of-the-art heuristic- and learning-based data placement techniques are rigid and far from optimal**, which strongly motivates us to develop a new data placement technique to achieve significantly higher performance than existing policies. The new technique should provide (1) *adaptivity* to better capture the features and dynamic changes in I/O-access patterns and storage device characteristics, and (2) *easy extensibility* to a wide range of workloads and HSS configurations. Our goal is to develop such a technique using reinforcement learning.

7.4 Reinforcement Learning

7.4.1 Background

Reinforcement learning (RL) [450] is a class of machine learning (ML) algorithms that involve an *agent* learning to achieve an objective by interacting with its *environment*, as shown in Figure 7-5. The agent starts from an initial representation of its environment in the form of an initial state² $s_0 \in S$, where S is the set of all possible states. Then, at each *time step* t , the agent performs an *action* $a_t \in A$ in state s_t (A represents the set of possible actions) and moves to the next state s_{t+1} . The agent receives a numerical reward $r_{t+1} \in R$, which could be *immediate* or *delayed* in time, for action a_t that changes the environment state from s_t to s_{t+1} . The sequence of states and actions starting from an initial state to the final state is called an *episode*. The agent makes decisions and receives corresponding rewards while trying to maximize

²State is a representation of an environment using different features.

the *accumulated* reward, as opposed to maximizing the reward for only *each* action. In this way, the agent can optimize for the long-term impact of its decisions.

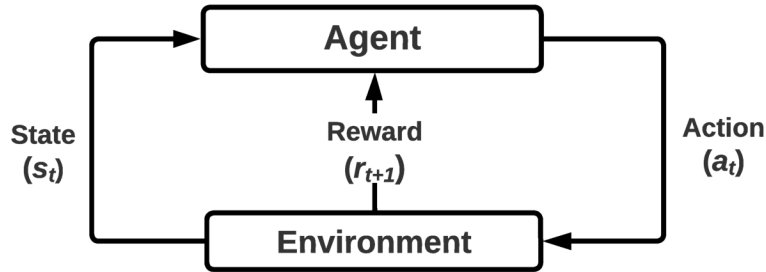


Figure 7-5: Main components of general RL

The policy π governs an agent’s action in a state. The agent’s goal is to find the optimal policy that maximizes the cumulative reward³ collected from the environment over time. The agent finds an optimal policy π^* by calculating the optimal action-value function (Q^*), also known as the **Q-value** of the state-action pair, where $Q(S, A)$ represents the expected cumulative reward by taking an action A in a given state S.

Traditional RL methods (e.g., [50, 197, 401, 496, 497]) use a tabular approach with a lookup table to store the Q-values associated with each state-action pair. These approaches can lead to high storage and computation overhead for environments with a large number of states and actions. To overcome this issue, *value function approximation* was proposed. [269, 319, 426, 427]. Value function approximation replaces the lookup table with a supervised-learning model [41, 269, 319, 426, 427, 451], which provides the capability to generalize over a large number of state-action pairs with a low storage and computation overhead.

7.4.2 Why Is RL a Good Fit for Data Placement in Hybrid Storage Systems?

We choose RL for data placement in HSS due to the following advantages compared to heuristic-based (e.g., [303, 310]) and supervised learning-based (e.g., [398]) techniques.

(1) Adaptivity. As discussed in Section 7.1 and Section 7.3, a data placement technique should have the ability to adapt to changing workload demands and underlying device characteristics. This adaptivity requirement of data placement makes RL a good fit to model data placement. The RL agent works autonomously in an HSS using the provided state features and reward to make data placement decisions without any human intervention.

³The total cumulative reward is also known as the *return* [450].

(2) Online learning. Unlike an *offline* learning-based approach, an RL agent uses an *online* learning approach. Online learning allows an RL agent to continuously adapt its decision-making policy using system-level feedback and specialize to the current workload and system configuration.

(3) Extensibility. RL provides the ability to easily extend a mechanism with a small effort required to implement the extension. As shown in Section 7.8.7, unlike heuristic-based mechanisms, RL can be easily extended to different types and number of storage devices. Such extensibility reduces the system architect’s burden in designing sophisticated data placement mechanisms.

(4) Design Ease. With RL, the designer of the HSS does not need to specify a data placement policy. They need to specify *what* to optimize (via reward function) but not *how* to optimize it.

(5) Implementation Ease. RL provides ease of implementation that requires a small computation overhead. As shown in Section 7.8, *function approximation*-based RL techniques can generalize over all the possible state-action pairs by using a simple feed-forward neural network to provide high performance at low implementation overhead (compared to sophisticated RNN-based mechanisms).

7.5 Sibyl: RL Formulation

Figure 7-6 shows our formulation of data placement as an RL problem. We design Sibyl as an RL agent that learns to perform accurate and system-aware data placement decisions by interacting with the hybrid storage system. With every storage request, Sibyl observes multiple workload and system-level features as a *state* to make a data placement decision. After every *action*, Sibyl receives a *reward* in terms of the served request latency that takes into account the data placement decision and internal storage system state. Sibyl’s goal is to find an optimal data placement policy that maximizes overall performance for the running workload and the current system configuration. To reach its performance goal, Sibyl needs to minimize the average request latency of the running workload by maximizing the use of the fast storage device while avoiding the eviction penalty due to non-performance critical pages.

Reward. After every data placement decision at time-step⁴ t , Sibyl gets a reward from the environment at time-step $t + 1$ that acts as a feedback to Sibyl’s previous action. To achieve Sibyl’s performance goal, we craft the reward function R as follows:

$$R = \begin{cases} \frac{1}{L_t} & \text{if no eviction of a page from the} \\ & \text{fast storage to the slow storage} \\ \max(0, \frac{1}{L_t} - R_p) & \text{in case of eviction} \end{cases} \quad (7.1)$$

⁴In HSS, a time-step is defined as a new storage request.

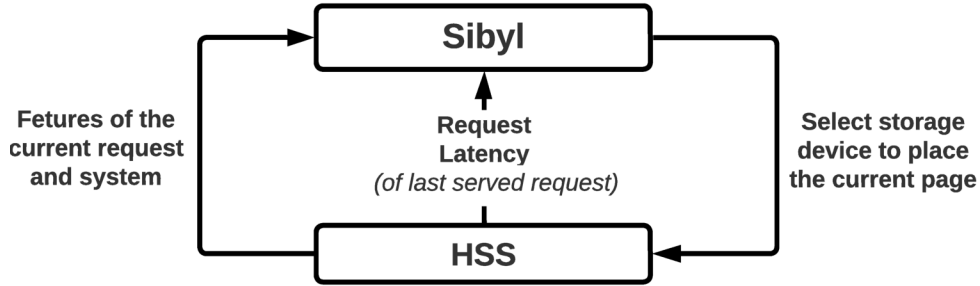


Figure 7-6: Formulating data placement as an RL problem

where L_t and R_p represent the last served request latency and eviction penalty, respectively. If the fast storage is running out of free space, there might be evictions in the background from the fast storage to the slow storage. Therefore, we add an eviction penalty (R_p) to guide Sibyl to place only performance-critical pages in the fast storage. We empirically select R_p to be equal to $0.001 \times L_e$ (L_e is the time spent in evicting pages from the fast storage to the slow storage), which prevents the agent from aggressively placing all requests into the fast storage device.

L_t (request latency) is the time taken to service the last read or write I/O request from the OS. Request latency can faithfully capture the status of the hybrid storage system, as it significantly varies depending on the request type, device type, and the internal state and characteristics of the device (e.g., such as read/write latencies, the latency of garbage collection, queuing delays, and error handling latencies). Intuitively, if L_t is low (high), i.e., if the agent serves a storage request from the fast (slow) device, the agent receives a high (low) reward. However, if there is an eviction, we penalize the agent so as to encourage the agent to place only performance-critical pages in the fast storage device. We need the eviction penalty to be large enough to discourage the agent from evicting and small enough not to deviate the learned policy too much on a placement decision that leads to higher latency.

State. At each time-step t , the state features for a particular read/write request are collected in an *observation* vector. We perform feature selection [237] to determine the best state features to include in Sibyl’s observation vector.

We use a limited number of features due to two reasons. First, a limited feature set allows us to reduce the implementation overhead of our mechanism (see 7.10). Second, we empirically observe that our RL agent is more sensitive to the reward structure than to the number of features in the observation vector. Specifically, using the request latency as a reward provides indirect feedback on the internal timing characteristics *and* the current state (e.g., queuing delays, buffer dependencies, effects of garbage collection, read/write latencies, write buffer state, and error handling latencies) of the hybrid storage system. Our observation aligns with a recent study [428] that argues that the reward is the most critical component in RL to find an optimal

decision-making policy.

In our implementation of Sibyl, the observation vector is a 6-dimensional tuple:

$$O_t = (size_t, type_t, intr_t, cnt_t, cap_t, curr_t). \quad (7.2)$$

Table 7.1 lists our six selected features. We quantize the representation of each state into a small number of bins to reduce the storage overhead of state representation. These features can be captured in the block layer of the storage system and stored in a separate metadata table (7.10). $size_t$ represents the size of the current request in terms of the number of pages associated with it. It indicates whether the incoming request is sequential or random. $type_t$ (request type) differentiates between read and write requests, important for data placement decisions since storage devices have asymmetric read and write latencies. $intr_t$ (access interval) and cnt_t (access count) represent the temporal and spatial reuse characteristics of the currently requested page, respectively. Access interval is defined as the number of page accesses between two references to the same page. Access count is defined as the total number of accesses to the page. These metrics provide insight into the dynamic behavior of the currently requested page.⁵ cap_t is a global counter that tracks the remaining capacity in the fast storage device, which is an important feature since our agent’s goal is to maximize the use of the limited fast storage capacity while avoiding evictions from the fast storage device. By including this feature, the agent can learn to avoid the eviction penalty (i.e., learn to restrain itself from placing in fast storage non-performance critical pages that would lead to evictions). $curr_t$ is the current placement of the requested page. Since every data placement decision affects the decision for future requests, $curr_t$ guides Sibyl to perform past-aware decisions.

Table 7.1: State features used by Sibyl

Feature	Description	# of bins	Encoding (bits)
$size_t$	Size of the requested page (in pages)	8	8
$type_t$	Type of the current request (read/write)	2	4
$intr_t$	Access interval of the requested page	64	8
cnt_t	Access count of the requested page	64	8
cap_t	Remaining capacity in the fast storage device	8	8
$curr_t$	Current placement of the requested page (fast/slow)	2	4

Action. At each time-step t , in a given state, Sibyl selects an action (a_t in Figure 7-6) from all possible actions. In a hybrid storage system with two devices, possible actions are: placing data in (1) the fast storage device or (2) the slow storage device. This is easily extensible to N storage devices, where $N \geq 3$.

⁵We did not use the reuse distance as a locality metric due to its high computation overhead during online profiling [537].

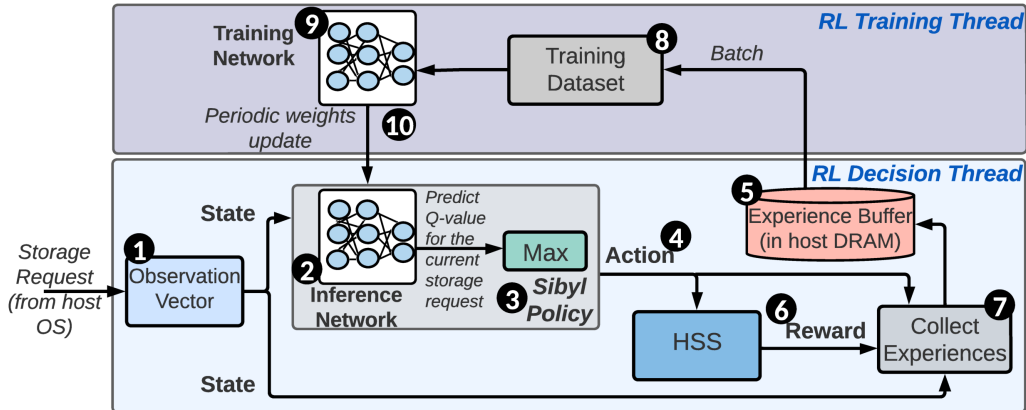


Figure 7-7: Overview of Sibyl

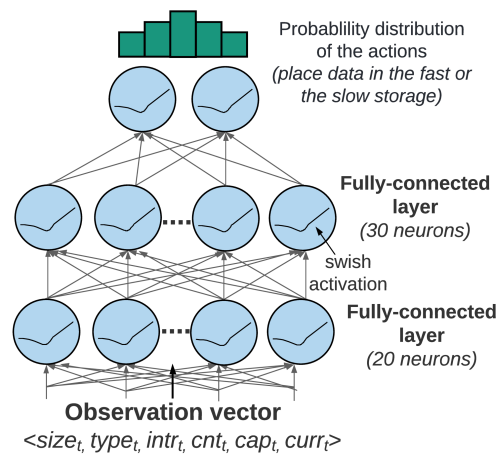


Figure 7-8: Training network design using as input the state features from Table 7.1. The inference network is identical except it is used only for inference

7.6 Sibyl: Design

We implement Sibyl in the storage management layer of the host system’s operating system. Figure 7-7 shows a high-level overview of Sibyl. Sibyl is composed of two parts, each implemented as a separate thread, that run in parallel (1) the *RL decision thread*, where Sibyl decides the data placement **4** of the current storage request while collecting information **7** about its decisions **4** and their effects **6** in an *experience buffer* **5**, and (2) the *RL training thread*, where Sibyl uses the collected *experiences*⁶ **8** to update its decision-making policy online **9**. Sibyl continuously learns from its

⁶Experience is a representation of a transition from one time step to another, in terms of $\langle State, Action, Reward, NextState \rangle$.

past decisions and their impact. Our two-threaded implementation avoids that the learning (i.e., training) interrupts or delays data placement decisions for incoming requests. To enable the parallel execution of the two threads, we duplicate the neural network that is used to make data placement decisions. While one network (called the *inference network* ❷) is deployed (i.e., makes decisions) the second network (called the *training network* ❸), is trained in the background. The inference network is used *only* for inference, while the training network is used *only* for training. Therefore, Sibyl does *not* perform a separate training step for the inference network and instead periodically copies the training network weights to the inference network ❹.

For every new storage request to the HSS, Sibyl uses the state information ❶ to make a data placement decision ❺. The inference network predicts the Q-value for each available action given the state information. Sibyl policy ❸ selects the action with the maximum Q-value or, with a low probability, a random action for exploration and performs the data placement.

7.6.1 Sibyl Data Placement Algorithm

Algorithm 3 describes how Sibyl performs data placement for an HSS. Initially, the experience buffer is allocated to hold e_{EB} entries (line 1), and the training and the inference network weights are initialized to random values (lines 2 and 3). When a storage request is received (line 4), Sibyl policy (❸ Figure 7-7) either (1) randomly selects an action with ϵ probability (lines 6-7) to perform exploration in an HSS environment, or (2) selects the action that maximizes the Q-value, based on information stored in the inference network (lines 8-9). After performing the selected action (line 10), Sibyl collects its reward, whose value depends on whether an eviction is needed from fast storage (lines 11-14). The generated experience is stored in the experience buffer (line 15). Once the experience buffer has e_{EB} entries (line 16), Sibyl trains the training network. During training, the training network samples a batch of experiences from the experience buffer (line 17) and updates its weights using stochastic gradient descent (SGD) [60] (line 18). Sibyl does *not* perform a separate training step for the inference network. Instead, the training network weights are copied to the inference network (line 19), which removes the training of the inference network from the critical path of decision-making.

7.6.2 Detailed Design of Sibyl

RL Decision Thread

In this thread, Sibyl makes data placement decisions while storing *experiences* in an experience buffer. Sibyl extracts the observation vector ❶ from the attributes of the incoming request and the current system state (e.g., access count, remaining

Algorithm 3 Sibyl’s reinforcement learning-based data placement algorithm

```

1: Initialize: the experience buffer  $EB$  to capacity  $e_{EB}$ 
2: Initialize: the training network with random weights  $\theta$ 
3: Initialize: the inference network with random weights  $\hat{\theta}$ 
4: Initialize: the observation vector  $O_t=O(s_1)$  with storage request  $s_1=\{req_t\}$ , and host and storage
   features
5: for all storage requests do
6:   if ( $\text{rand}() < \epsilon$ ) then ▷ with probability  $\epsilon$ , perform exploration
7:     random action  $a_t$ 
8:   else ▷ with probability  $1-\epsilon$ , perform exploitation
9:      $a_t = \text{argmax}_a Q_t(a)$  ▷ select action with the highest  $Q_t$  value from inference network
10:    execute  $a_t$  ▷ place the requested page to fast or slow storage
11:    if no eviction then ▷ reward, given no eviction of a page from fast to slow storage
12:       $r_t \leftarrow \frac{1}{L_t}$ 
13:    else ▷ reward with an eviction penalty in case of an eviction
14:       $r_t \leftarrow \max(0, \frac{1}{L_t} - R_p)$ 
15:    store experience  $(O_t, a_t, r_t, O(t+1))$  in  $EB$ 
16:    if ( $\text{num requests in } EB == e_{EB}$ ) then ▷ train training network when EB is full
17:      sample random batches of experiences from  $EB$ , which are in format  $(O_j, a_j, r_j, O(j+1))$  ▷ where
Oj represents an observation at a time instant j from EB
18:      Perform stochastic gradient descent ▷ update the training network weights
19:       $\hat{\theta} \leftarrow \theta$  ▷ copy the training network weights to the inference network

```

capacity in the fast storage) and uses the inference network ② to predict the Q-values for each possible action with the given state vector. While making data placement decisions, Sibyl balances the random *exploration* of the environment (to find a better policy without getting stuck at a suboptimal one) with the *exploitation* of its current policy (to maximize its reward based on the current inference network weights).

Sibyl policy. For every storage request, Sibyl policy selects the action that leads to the highest long-term reward ⑥. We use a Categorical Deep Q-Network (also known as C51) [47] to update $Q(s, a)$. C51’s objective is to learn the distribution of Q-values, whereas other variants of Deep Q-Networks [41, 269, 319, 426, 427, 451] aim to approximate a single value for $Q(s, a)$. This distribution helps Sibyl to capture more information from the environment to make better data placement decisions [174].

For tracking the state, we divide each feature into a small number of bins to reduce the state space (see Section 7.5), which directly affects the implementation overhead of Sibyl. We select the number of bins (Table 7.1) based on empirical sensitivity analysis. Our state representation uses a more relaxed encoding of 40 bits (than using only 20 bits for the observation vector) to allow for future extensions (e.g., features with more bins). Similarly, we use a relaxed 4-bit encoding for the action to allow extensibility to a different number of storage devices. For the reward structure, we use a half-precision floating-point (16-bit) representation.

Experience buffer. Sibyl stores *experiences* it collects while interacting with the HSS in an *experience buffer* [320]. The experience buffer is allocated in the host main memory (DRAM). To minimize its design overhead, we deduplicate data in the stored experiences. To improve the training quality, we perform batch training where each batch consists of randomly sampled experiences. This technique of randomly sampling experiences from the experience buffer is called *experience replay* [320].

Figure 7-9 shows the effect of different experience buffer sizes on Sibyl’s performance in the *H&M* configuration. We observe that Sibyl’s performance saturates at 1000 entries, which we select as the experience buffer size. Since the size of our state representation is 40 bits, to store a single experience tuple, we need 40-bit+4-bit+16-bit+40-bit, i.e., 100 bits. In total, for 1000 experiences, the experience buffer requires 100 KiB in the host DRAM.

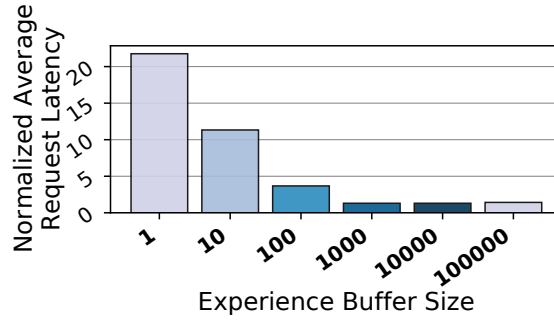


Figure 7-9: Effect of different experience buffer sizes on the average request latency (normalized to Fast-Only)

Exploration vs. exploitation. An RL agent needs to *explore* the environment to improve its policy to maximize its long-term reward beyond local maxima [450]. At the same time, the agent needs to *exploit* what it has already *experienced* so that it can take advantage of its learning so far. To balance exploration and exploitation, we use the ϵ -greedy policy [462]: the best-known action based on the agent’s experience is selected with $(1-\epsilon)$ probability, and otherwise, i.e., with ϵ probability, another action is chosen randomly. Exploration allows Sibyl to experience states it may not otherwise get into [450] and thus avoid missing higher long-term rewards. To perform exploration, Sibyl randomly chooses to place data to the fast or the slow storage device, so that it can get more information about the HSS and the workload. Based on the received reward, Sibyl updates its training network. Such exploration helps Sibyl to avoid making suboptimal data placement decisions in the long run.

RL Training Thread

This thread uses a batch of collected experiences ⑧ from the experience buffer to train the training network ⑨. The updated weights of the training network are transferred to the inference network after every 1000 requests ⑩.

Training and inference networks. The training and inference network allows the parallel execution of decision and training threads. We use an identical neural network structure for the training and inference networks. A deep neural network can be prohibitive due to the long time it requires for training and convergence, preventing Sibyl to adapt to new state-action pairs in a timely manner. Based on experiments, we

find that a simple feed-forward network [45] with only two hidden layers [107] provides good performance for Sibyl’s data placement task. Figure 7-8 shows the structure of our training network.⁷ The network takes the observation vector O_t as its input and produces a probability distribution of Q-values as its output. Before feeding the data to the network, we preprocess the data by normalizing and casting the data to low precision data types, which allows us to reduce memory in the experience buffer. Next, we apply two fully-connected hidden layers of 20 and 30 neurons, respectively. We select these neurons based on our extensive design space exploration with different numbers of hidden layers and neurons per layer. After the two hidden layers, we have an output layer of 2 neurons, one for each action. Sibyl policy **3** selects the action with the maximum Q-value. All fully-connected layers use the swish activation function [390], a non-monotonic function that outperforms ReLU [8].

During the training of the training network, the inference network’s weights are fixed. After every 1000 requests, the weights of the training network are copied to the inference network, which removes the training of the inference network from the critical path. We set the number of requests to 1000 based on our empirical evaluation of the experience buffer size (Figure 7-9). Each training step is composed of 8 batches of experiences from an experience buffer of 1000 experiences with a batch size of 128. We perform the training on the host CPU rather than on a dedicated hardware accelerator because (1) the network size is small and the weights perfectly fit in on-chip caches of the CPU in our evaluated system, and (2) to avoid continuous weight transfer overhead between the host CPU and the accelerator over the external interface.

Hyper-parameter tuning. We improve Sibyl’s accuracy by tuning its hyper-parameters. Hyper-parameters are sets of RL algorithm variables that can be tuned to optimize the accuracy of the RL agent [358, 437]. For hyper-parameter tuning, we perform cross-validation [29] using different hyper-parameter values. During cross-validation, we randomly select one workload for hyper-parameter tuning and use the other thirteen workloads for validation. On the selected workload, we use different hyper-parameter configurations that we choose using the *design of experiments* (DoE) [321]. DoE allows us to minimize the number of experiments needed to find the best hyper-parameter values without sacrificing the quality of the information gathered by the experiments. Unlike traditional supervised learning methods, we do *not* train Sibyl *offline* using a training dataset before deploying it for data placement. All training happens online in Sibyl. For every evaluated workload, Sibyl starts with no prior knowledge and gradually learns to make data placement decisions online by interacting with the hybrid storage system. Sibyl needs only one-time offline hyper-parameter tuning.

Table 7.2 shows the hyper-parameters considered in Sibyl’s design as well as their

⁷The inference network is identical in shape to the training network.

chosen values after the tuning process. The discount factor (γ) determines the balance between the immediate and future rewards. At $\gamma=0$ ($\gamma=1$), Sibyl gives importance only to the immediate (long-term) reward. The learning rate (α) determines the rate at which neural network weights are updated. A lower α makes small updates to the neural network weights, which could take more training iterations to converge to an optimal policy. While a higher α results in large updates to the neural network weights, which could cause the model to converge too quickly to a suboptimal solution. The exploration rate (ϵ) balances exploration and exploitation for Sibyl. We also explore different batch sizes (i.e., the number of samples processed in each training iteration) and experience buffer sizes to train our training network.

Table 7.2: Hyper-parameters considered for tuning

Hyper-parameter	Design Space	Chosen Value
Discount factor (γ)	0-1	0.9
Learning rate (α)	$1e^{-5} - 1e^0$	$1e^{-4}$
Exploration rate (ϵ)	0-1	0.001
Batch size	64-256	128
Experience buffer size (e_{EB})	10-10000	1000

7.7 Evaluation Methodology

Evaluation setup. We evaluate Sibyl using real systems with various HSS configurations. The HSS devices appear as a single flat block device that exposes one contiguous logical block address space to the OS, as depicted in Figure 7-1. We implement a lightweight custom block driver interface that manages the I/O requests to storage devices. Table 7.3 provides our system details, including the characteristics of the three storage devices we use. To analyze the sensitivity of our approach to different device characteristics, we evaluate two different hybrid storage configurations (1) *performance-oriented HSS: high-end device (H) [190] and middle-end device (M) [192], and (2) cost-oriented HSS: high-end device (H) [190] and low-end device (L) [412]*. We also evaluate two tri-hybrid HSS configurations consisting of (1) *H&M&L* and (2) *H&M&LSSD* devices. We run the Linux Mint 20.1 operating system [276] with the Ext3 file system [469]. We use the TF-Agents API [161] to develop Sibyl. We evaluate Sibyl using two different metrics: (1) *average request latency*, i.e., average of the latencies of all storage read/write requests in a workload, and (2) *request throughput (IOPS)*, i.e., throughput of all storage requests in a workload in terms of completed I/O operations per second.

Baselines. We compare Sibyl against two state-of-the-art heuristic-based HSS

Table 7.3: Host system and storage devices used in hybrid storage configurations

Host System	AMD Ryzen 7 2700G [22], 8-cores@3.5 GHz, 8×64/32 KiB L1-I/D, 4 MiB L2, 8 MiB L3, 16 GiB RDIMM DDR4 2666 MHz	
Storage Devices	Characteristics	
H: Intel Optane SSD P4800X [190]	375 GB, PCIe 3.0 NVMe, SLC, R/W: 2.4/2 GB/s, random R/W: 550000/500000 IOPS	
M: Intel SSD D3-S4510 [192]	1.92 TB, SATA TLC (3D), R/W: 550/510 MB/s, random R/W: 895000/21000 IOPS	
L: Seagate HDD ST1000DM010 [412]	1 TB, SATA 6Gb/s 7200 RPM Max. Sustained Transfer Rate: 210 MB/s	
L _{SSD} : ADATA SU630 SSD [2]	960 GB, SATA 6 Gb/s, TLC, Max R/W: 520/450 MB/s	
HSS Configurations	Fast Device	Slow Device
H&M (Performance-oriented)	high-end (H)	middle-end (M)
H&L (Cost-oriented)	high-end (H)	low-end (L)

data placement techniques, (1) cold data eviction (CDE) [303] and (2) history-based page selection (HPS) [310], (3) a state-of-the-art supervised learning-based technique (Archivist) [398], and (4) a recurrent neural network (RNN)-based data placement technique (RNN-HSS), adapted from Kleio [117], a data placement technique for hybrid memory systems. RNN-HSS provides a state-of-the-art ML-based data placement baseline. We compare the above policies with three extreme baselines: (1) **Slow-Only**, where all data resides in the slow storage (i.e., there is no fast storage), (2) **Fast-Only**, where all data resides in the fast storage, and (3) **Oracle** [310], which exploits complete knowledge of future I/O-access patterns to perform data placement and to select victim data blocks for eviction from the fast device.

Workloads. We use fourteen different block-I/O traces from the MSRC benchmark suite [324] that are collected from real enterprise server workloads. We carefully select the fourteen traces to have distinct I/O-access patterns, as shown in Table 7.4, in order to study a diverse set of workloads with different randomness and hotness properties (see Figure 7-3). We quantify a workload’s randomness using the average request size of the workload; the higher (lower) the average request size, the more sequential (random) the workload. The average access count provides the average of the access counts of all pages in a workload; the higher (lower) the average access count, the hotter (colder) the workload. Table 7.4 also shows the number of unique requests in a workload. To demonstrate Sibyl’s ability to generalize and provide performance gains across *unseen traces*, i.e., traces that are *not* used to tune the hyper-parameters of Sibyl, we evaluate Sibyl using four additional workloads from FileBench [455].

Table 7.4: Characteristics of 14 evaluated workloads

Workload	Write %	Read %	Avg. request size	Avg. access count	No. of unique requests
<i>hm_1</i>	4.7%	95.3%	15.2	44.5	6265
<i>mids_0</i>	88.1%	11.9%	9.6	3.5	31933
<i>prn_1</i>	24.7%	75.3%	20.0	2.6	6891
<i>proj_0</i>	87.5%	12.5%	38.0	48.3	1381
<i>proj_2</i>	12.4%	87.6%	42.4	2.9	27967
<i>proj_3</i>	5.2%	94.8%	9.6	3.6	19397
<i>prxy_0</i>	96.9%	3.1%	7.2	95.7	525
<i>prxy_1</i>	34.5%	65.5%	12.8	150.1	6845
<i>rsrch_0</i>	90.7%	9.3%	9.2	34.7	5504
<i>src1_0</i>	43.6%	56.4%	43.2	12.7	13640
<i>stg_1</i>	36.3%	63.7%	40.8	1.1	3787
<i>usr_0</i>	59.6%	40.4%	22.8	19.7	2138
<i>wdev_2</i>	99.9%	0.1%	8.0	17.7	4270
<i>web_1</i>	45.9%	54.1%	29.6	1.2	6095

7.8 Results

7.8.1 Performance Analysis

Figure 7-10 compares the average request latency of Sibyl against the baseline policies for *H&M* (Figure 7-10(a)) and *H&L* (Figure 7-10(b)) HSS configurations. All values are normalized to **Fast-Only**. We make five major observations. First, Sibyl consistently outperforms all the baselines for all the workloads in *H&L* and all but two workloads in *H&M*. In the **H&M** HSS configuration (Figure 7-10(a)), where the latency difference between two devices is relatively smaller than **H&L**, Sibyl improves average performance by 28.1%, 23.2%, 36.1%, and 21.6% over **CDE**, **HPS**, **Archivist**, and **RNN-HSS**, respectively. In the **H&L** HSS configuration (Figure 7-10(b)), where there is a large difference between the latencies of the two storage devices, Sibyl improves performance by 19.9%, 45.9%, 68.8%, and 34.1% over **CDE**, **HPS**, **Archivist** and **RNN-HSS**, respectively. We observe that the larger the latency gap between HSS devices, the higher the expected benefits of avoiding the eviction penalty by placing only performance-critical pages in the fast storage. Second, in the **H&M** HSS configuration, **CDE** and **HPS** are ineffective for certain workloads (*hm_1*, *prn_1*, *proj_2*, *proj_3*, and *src1_0*) even when compared to **Slow-Only**. In contrast, Sibyl consistently and significantly outperforms **Slow-Only** for all workloads because it can learn the small latency difference between the two storage devices in **H&M** and dynamically adapts its data placement decisions, which is difficult for **CDE** and **HPS** due to their inability to holistically take into account the underlying device characteristics. Third, Sibyl provides slightly lower performance than other baselines in only two workloads: **Slow-Only**, **HPS**, **Archivist**, and **RNN-HSS** for *hm_1* and **CDE** and **HPS** for *prxy_0* in the *H&M* HSS configuration. We observe that such workloads are write-intensive and have many random requests (in terms of both access pattern and request size). Therefore, such workloads would benefit from more frequent retraining of Sibyl’s

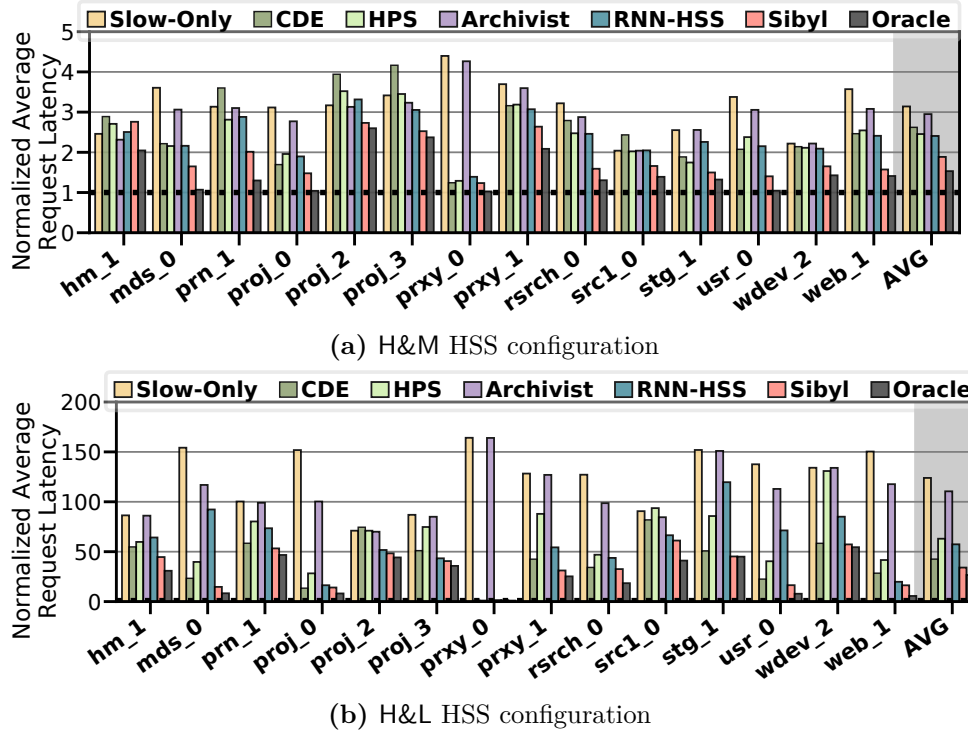
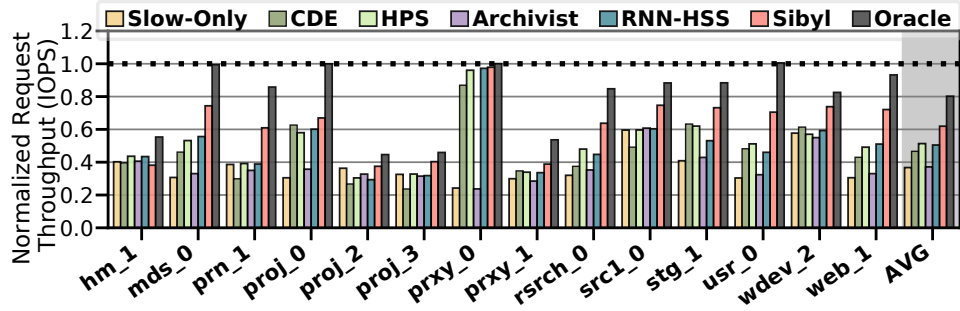


Figure 7-10: Average request latency under two different hybrid storage configurations (normalized to Fast-Only)

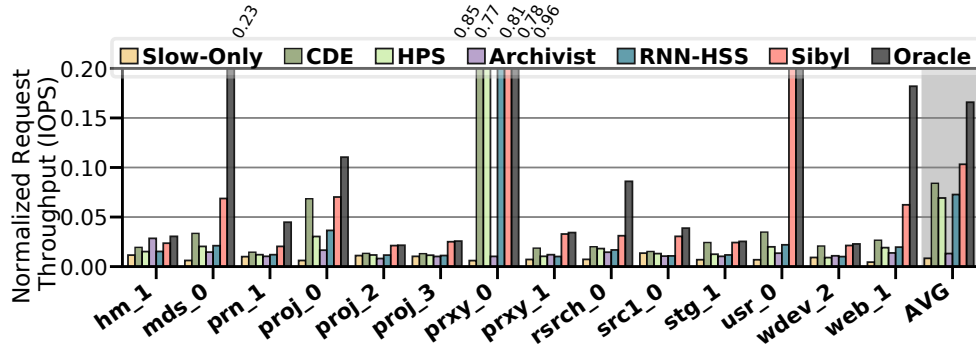
training network. We experimentally show in Section 7.8.3 that using a lower learning rate during the training of the training network helps to improve Sibyl’s performance for such workloads. Fourth, Sibyl achieves, on average, 80% of the performance of the Oracle, which has complete knowledge of future access patterns, across *H&M* and *H&L*. Fifth, RNN-HSS provides higher performance than heuristic-based policies (2.1% and 8.9% than CDE and HPS, respectively, in *H&M* and 9.8% than HPS in *H&L*), but Sibyl outperforms it by 27.9%. Unlike Sibyl, the two machine learning-based policies, Archivist and RNN-HSS, do *not* consider any system-level feedback, which leads to their suboptimal performance.

Figure 7-11 compares the request throughput (IOPS) of Sibyl against other baseline policies. We make two observations. First, in the *H&M* (*H&L*) HSS configuration (Figure 7-11), Sibyl improves throughput by 32.6% (22.8%), 21.9% (49.1%), 54.2% (86.9%), and 22.7% (41.9%) over CDE, HPS, Archivist, and RNN-HSS, respectively. Second, Sibyl provides slightly lower performance than Slow-Only, CDE, HPS, Archivist, and RNN-HSS for only *hm_1* in *H&M* HSS configuration. We draw similar observations for throughput results as we did for latency results (Figure 7-10) because as Sibyl considers the request size in state features and request latency in the reward, it also indirectly captures throughput (size/latency).

We conclude that Sibyl consistently provides higher performance than all five baselines and significantly improves both average request latency and request throughput.



(a) H&M HSS configuration



(b) H&L HSS configuration

Figure 7-11: Request throughput (IOPS) under two different hybrid storage configurations (normalized to Fast-Only)

7.8.2 Performance on Unseen Workloads

To demonstrate Sibyl’s ability to generalize and provide performance gains across *unseen* workloads that are *not* used to tune the hyper-parameters of the data placement policy of Sibyl, we evaluate Sibyl using four additional workloads from FileBench [455]. No data placement policy we evaluate, including Sibyl, is tuned on these workloads.

Figure 7-12 shows the performance of these unseen workloads. We observe the following observations. First, in H&M (H&L) HSS configuration, Sibyl outperforms RNN-HSS and Archivist by 46.1% (54.6%) and 8.5% (44.1%), respectively. Second, Sibyl may misplace some pages during the online adaptation period, but it provides significant performance benefits over existing ML-based data placement techniques. We conclude that Sibyl provides high performance benefits on unseen workloads for which it has not been tuned.

7.8.3 Performance on Mixed Workloads

We evaluate mixing two or more workloads at the same time while randomly varying their relative start times. Table 7.5 describes the characteristics of these mixed workloads. These workloads are truly independent of each other, potentially creating more evictions from the fast storage device than a single workload. Such a scenario

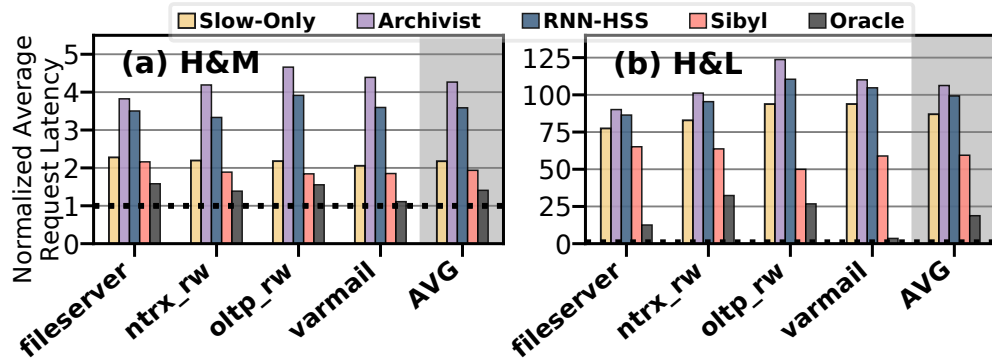


Figure 7-12: Average request latency on unseen workloads (normalized to Fast-Only) under two HSS configurations

(1) leads to unpredictable execution where requests arrive at different, unpredictable timesteps, (2) mimics distributed workloads, and (3) further tests the ability of Sibyl to dynamically adapt its decision-making policy.

Figure 7-13 shows average request latency for mixed workloads. We use two different settings for Sibyl: (a) $Sibyl_{Def}$, where we use our default hyper-parameters (Section 7.6.2), and (b) $Sibyl_{Opt}$, where we optimize the hyper-parameters for these mixed workloads and use a lower learning rate (α) of $1e^{-5}$. A lower learning rate performs smaller updates to the training network’s weights in each training iteration, thus requiring more training to converge to an optimal solution.

Table 7.5: Characteristics of mixed workloads

Mix	Workloads	Description
mix1	<i>prxy_0</i> [324] and <i>ntrx_rw</i> [455]	Both <i>prxy_0</i> and <i>ntrx_rw</i> are write-intensive
mix2	<i>rsrch_0</i> [324] and <i>oltp_rw</i> [455]	<i>rsrch_0</i> is write-intensive and <i>oltp_rw</i> is read-intensive
mix3	<i>proj_3</i> [324] and <i>YCSB_C</i> [96]	Both <i>proj_3</i> and <i>YCSB_C</i> are read-intensive
mix4	<i>src1_0</i> [324] and <i>fileserver</i> [455]	Both <i>src1_0</i> and <i>fileserver</i> have nearly equal numbers of reads and writes
mix5	<i>prxy_0</i> [324], <i>oltp_rw</i> [455] and <i>fileserver</i> [455]	<i>prxy_0</i> is write-intensive, <i>oltp_rw</i> is read-intensive, and <i>fileserver</i> has nearly equal numbers of reads and writes
mix6	<i>src1_0</i> [324], <i>YCSB_C</i> [96] and <i>fileserver</i> [455]	<i>src1_0</i> and <i>fileserver</i> have nearly equal numbers of reads and writes while <i>YCSB_C</i> is read-intensive

We make two observations. First, $Sibyl_{Def}$ consistently outperforms CDE, HPS, Archivist, and RNN-HSS by 27.9%, 12.2%, 12.1%, and 12.9%, respectively, in the H&M HSS configuration and 9.4%, 21.3%, 19.4%, and 17.1%, respectively, in H&L HSS configuration. Second, with a lower learning rate and optimized hyper-parameters,

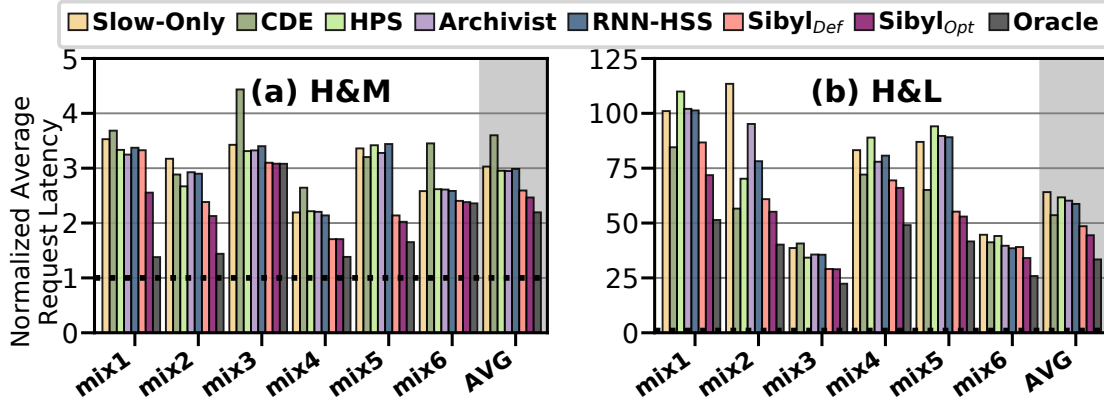


Figure 7-13: Average request latency on mixed workloads (normalized to Fast-Only) and two HSS configurations

$Sibyl_{Opt}$ provides 5.2% (9.3%) higher average performance for H&M (H&L) HSS configuration than $Sibyl_{Def}$. Third, for *mix_1*, HPS provides comparable performance to $Sibyl_{Def}$ in H&M, and CDE provides slightly better performance in H&L. As discussed in Section 7.8.1, *prxy_0* is write-intensive and has random requests (with an average request size of 7.2) within every 1000 requests, which is the experience buffer size to train the training network. Such a workload requires more frequent retraining of Sibyl’s training network to achieve higher performance. We conclude that Sibyl can effectively adapt its data placement policy online to highly dynamic workloads.

7.8.4 Performance with Different Features

Figure 7-14 compares the use of some of the most useful features for the *state* of Sibyl in our H&L HSS configuration. All represents using all the six features in Table 7.1. Sibyl autonomously decides which features are important to maximize the performance of the running workload.

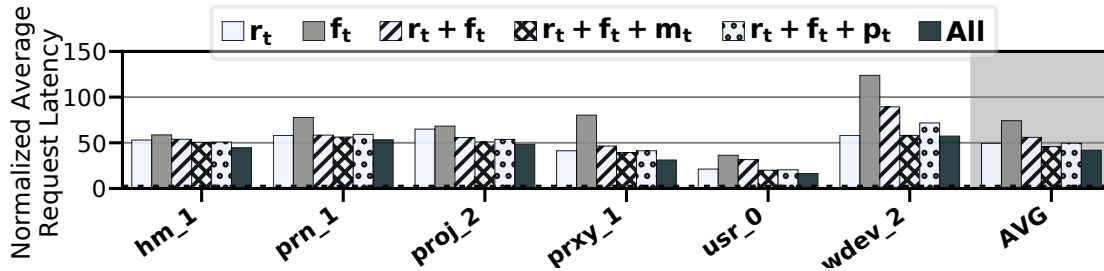


Figure 7-14: Average request latency when using different features (see Table 7.1) for the state space of Sibyl in the H&L HSS configuration (normalized to Fast-Only)

We make two key observations from Figure 7-14. First, Sibyl consistently achieves

the lowest latency (up to 43.6% lower) by using all the features mentioned in Table 7.1 (All in Figure 7-14). Second, by using the same features as in baseline heuristic-based policies, Sibyl is able to perform better data placement decisions. For example, r_t and f_t configurations of Sibyl (in Figure 7-14) use only one feature, just like CDE and HPS do. These two Sibyl configurations outperform CDE and HPS policies by 4.9% and 5.5%, respectively (*ref.* Figure 7-10(b)). Using the same features as a heuristic-based policy, Sibyl autonomously finds a higher-performance dynamic policy that can maximize the reward function, which heuristic-based policies cannot possibly do. We conclude that Sibyl uses a richer set of features that can capture multiple aspects of a storage request to make better data placement decisions than a heuristic-based policy. RL reduces the design burden on system architects, as Sibyl autonomously learns to use the provided features to achieve the highest cumulative reward. In contrast, traditional heuristic-based policies use features to make rigid data placement decisions without any system-level feedback, and thus they underperform compared to Sibyl.

7.8.5 Performance with Different Hyper-Parameters

Figures 7-15(a), 7-15(b), and 7-15(c) show the effect of three critical hyper-parameters (discount factor, learning rate, and exploration rate) on Sibyl’s throughput in *H&M* HSS configuration. Figure 7-15(a) shows that Sibyl’s throughput drops sharply at $\gamma = 0$. At $\gamma = 0$, Sibyl gives importance only to the immediate reward and not at all to the long-term reward, leading to lower performance. We use $\gamma = 0.9$, where Sibyl is more forward-looking, giving enough weight to long-term rewards. Figure 7-15(b) shows that at a learning rate of $\alpha = 1e^{-4}$, Sibyl provides the best performance. The learning rate determines the rate at which training network weights are updated. Both too slow and too fast updates are detrimental for adaptive learning and stable exploitation of a learned policy, respectively. Third, Figure 7-15(c) shows that the performance of Sibyl drops sharply if it performs exploration too frequently (i.e., $\epsilon = 1e^{-1}$) and thus does not sufficiently exploit its learned policy. Sibyl achieves the highest performance improvements for $1e^{-5} \leq \epsilon \leq 1e^{-2}$.

7.8.6 Sensitivity to Fast Storage Capacity

Figure 7-16 shows the average request latency of Sibyl and baseline policies as we vary the available capacity in the fast storage. The x-axis denotes a range of fast storage device sizes available for data placement and represented in terms of percentages of the entire fast storage device capacity, where 100% represents the size where all pages of a workload can fit in the fast storage.

We make two observations. First, for all fast storage sizes, Sibyl performs better than the baseline heuristic- and supervised learning-based policies for both *H&M* and

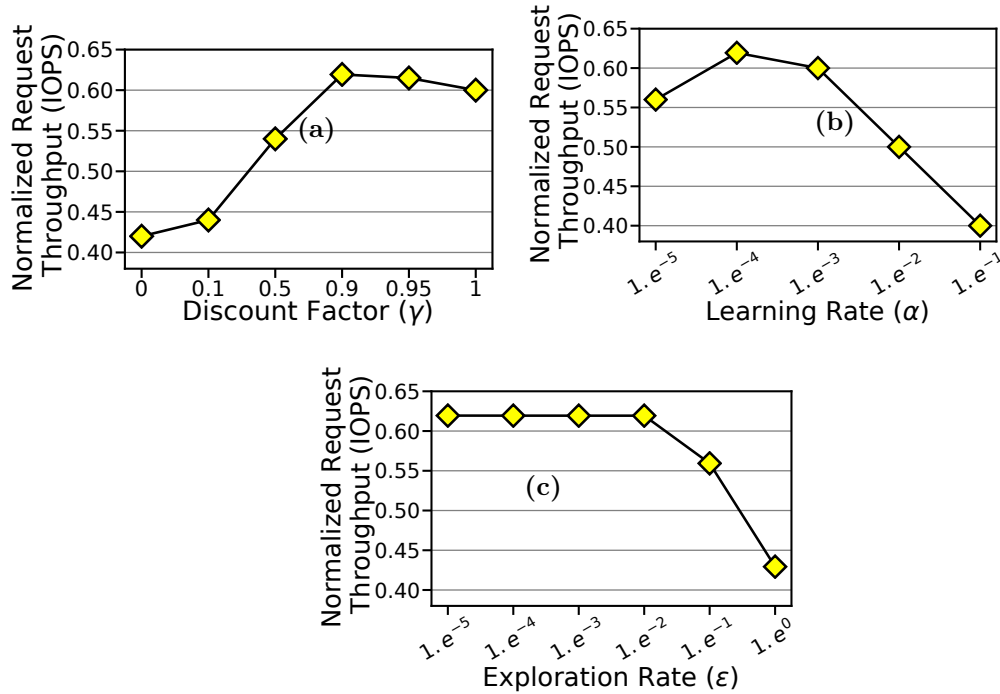


Figure 7-15: Sensitivity of Sibyl throughput to: (a) the discount factor (γ), (b) the learning rate (α), (c) the exploration rate (ϵ), averaged across 14 workloads (normalized to Fast-Only)

H&L HSS configurations. Even when the fast storage size is as small as 1%, Sibyl outperforms CDE, HPS, Archivist, RNN-HSS by 47.2% (11.5%), 17.3% (58.9%), 12.3% (110.1%), 21.7% (50.2%), respectively, in $H\&M$ ($H\&L$). Second, at a larger (smaller) fast storage device size, the performance approaches that of the Fast-Only (Slow-Only) policy, except for Archivist. Archivist classifies pages as hot or cold at the beginning of an epoch and does not change its placement decision throughout the execution of that epoch. It does not perform any promotion or eviction of data. We observe that Archivist often mispredicts the target device for a request and classifies the same number of requests for the fast and slow storage device under different fast storage sizes.

As we vary the size of the fast storage device, a dynamically adaptable data placement policy is required, which considers features from both the running workload and the underlying storage system. We conclude that Sibyl can provide scalability by dynamically and effectively adapting its policy to the available storage size to achieve high performance.

7.8.7 Tri-Hybrid Storage Systems

We evaluate two different tri-HSS configurations, $H\&M\&L$ and $H\&M\&L_{SSD}$ (Table 7.3), implemented as a single flat block device. The $H\&M\&L_{SSD}$ configuration

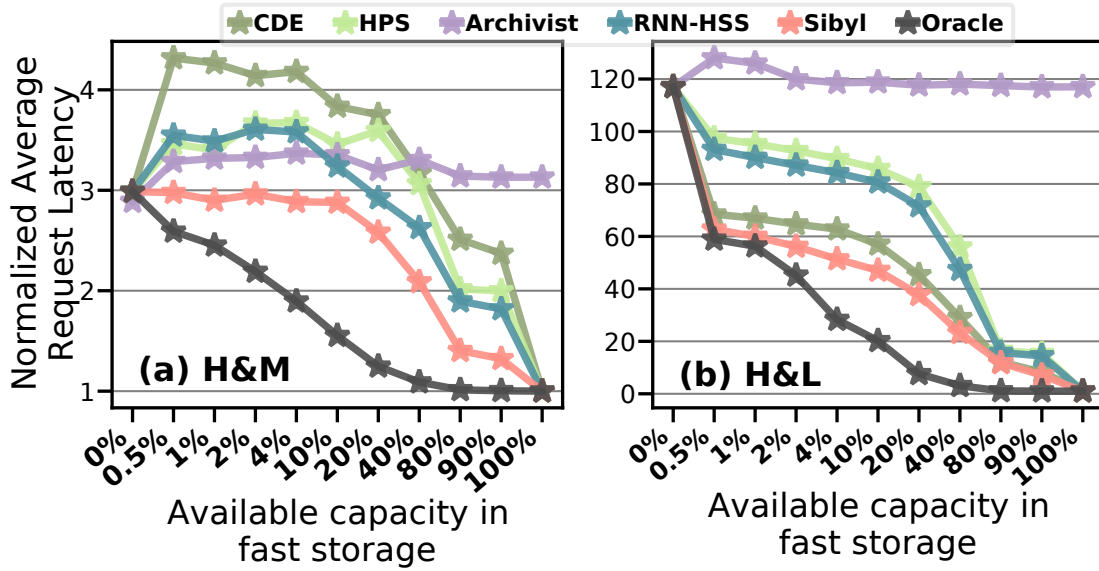


Figure 7-16: Average request latency for various fast storage device sizes (normalized to **Fast-Only**)

has a low-end SSD (L_{SSD}), whose performance is lower than the H and M devices but higher than the L device. We restrict the available capacity of H and M to 5% and 10%, respectively, of the working set size of a given workload. This ensures data eviction from H and M devices once they are full. We compare the performance of Sibyl on a tri-hybrid system with a state-of-the-art heuristic-based policy [303, 304] that divides data into *hot*, *cold*, and *frozen* and places them respectively into H, M, and L devices.⁸ Figure 7-17 shows the performance of the heuristic-based and Sibyl data placement policies.

We observe that Sibyl outperforms the heuristic-based policy by, on average, 43.5% (48.2%) and 23.9% (25.2%) for $H&M&L$ ($H&M&L_{SSD}$). This is because Sibyl is much more dynamic and adaptive to the storage system configuration due to its RL-based decision-making than the baseline heuristic-based policy, which is rigid in its decision-making. To extend Sibyl for three storage devices, we had to only (1) add a new action in Sibyl’s action space, and (2) add the remaining capacity in the M device as a state feature. We conclude that Sibyl provides ease of extensibility to new storage system configurations, which reduces the system architect’s burden in designing sophisticated data placement mechanisms.

⁸CDE, HPS, Archivist, and RNN-HSS do *not* consider more than two devices and are not easily adaptable to a tri-hybrid HSS.

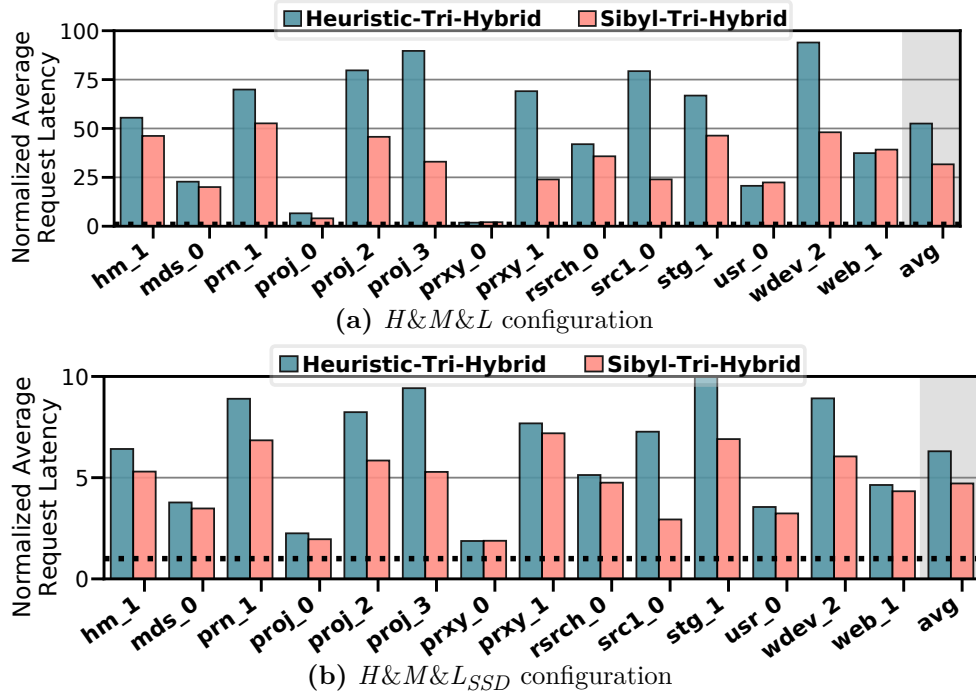


Figure 7-17: Average request latency for the tri-hybrid HSS (normalized to Fast-Only)

7.9 Explainability Analysis

We perform an explainability analysis to understand our results further and explain Sibyl’s decisions. We extract Sibyl’s actions for different workloads under $H\&M$ and $H\&L$ HSS configurations and analyze the page placements for each workload. Figure 7-18 shows Sibyl’s preference for the fast storage device over the slow storage device, measured as the ratio of the number of fast storage placements to the sum of the number of placements in both fast and slow storage devices (i.e., $\text{Preference} = \frac{\# \text{fast placements}}{\# \text{fast} + \# \text{slow placements}}$).

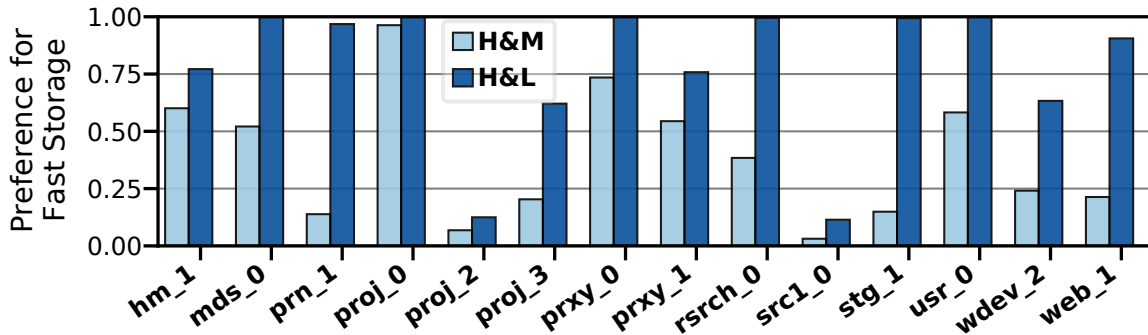
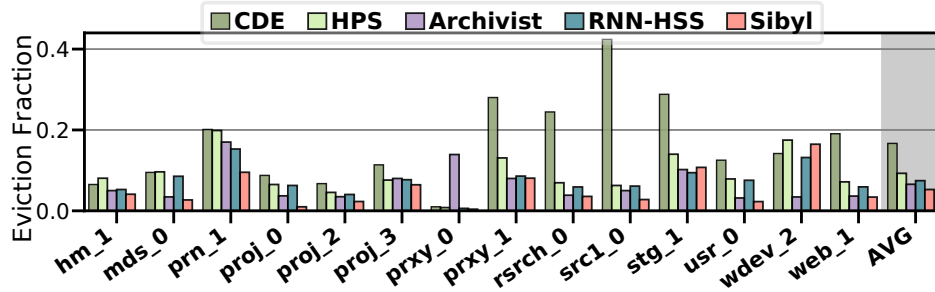
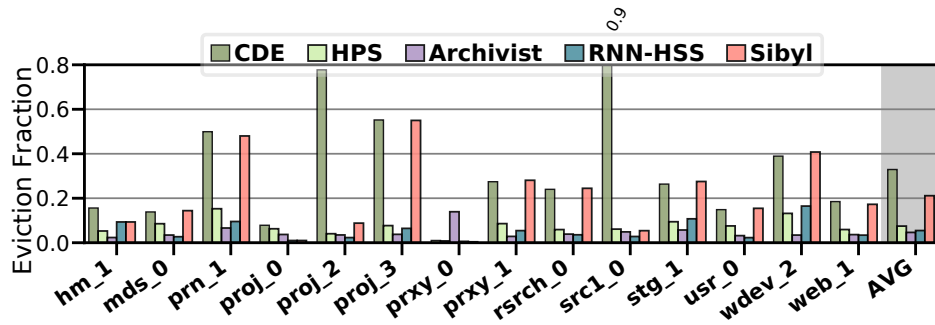


Figure 7-18: Sibyl’s preference for the fast storage device under different HSS configurations



(a) H&M HSS configuration



(b) H&L HSS configuration

Figure 7-19: Comparison of evictions from the fast storage to the slow storage (normalized to the total number of storage requests)

We make the following four observations. First, in the H&L configuration, where the latency difference is large between the two storage devices, Sibyl prefers to place more data in the fast storage device. Sibyl learns that despite the eviction penalty, the benefit of serving more requests from the fast storage device is significant. On the other hand, in the H&M device configuration, where the latency difference between two devices is smaller compared to H&L, Sibyl places only performance-critical pages in the faster storage device to avoid the eviction penalty.

Second, in the H&M configuration, Sibyl shows less preference to place pages from `mds_0`, `prn_1`, `proj_2`, `proj_3`, `src1_0`, `stg_1`, and `web_1` in the fast storage device. These workloads are cold and sequential (Table 7.4) and thus are less suitable for the fast storage device. Therefore, for such workloads, Sibyl shows more preference for the slow storage device. In contrast, for hot and random workloads (`prxy_0` and `prxy_1`), Sibyl shows more preference to place pages in the fast storage device.

Third, for `rsrch_0`, `wdev_2`, and `web_1`, Sibyl places $\leq 40\%$ of pages in the fast storage device. Such requests have random access patterns, while pages with cold and sequential accesses are placed in the slow storage.

Fourth, in the H&L setting, Sibyl shows more preference to place requests in the fast storage device, except for `proj_2` and `src1_0` workloads. We observe that these two workloads are highly random with a low average access count (Table 7.4). Therefore,

aggressive placement in the fast storage is not beneficial for long-term performance.

We also measure the number of evictions (as a fraction of all storage requests) that occur while using Sibyl and other baseline policies, as shown in Figure 7-19. We make two observations. First, in the *H&M* HSS configuration, Sibyl leads to 68.4%, 43.2%, 19.7%, and 29.3% fewer evictions from the fast storage than CDE, HPS, and RNN-HSS, respectively. Second, CDE places more data in the fast storage, which leads to a large number of evictions in both HSS configurations. However, if the latency difference between the two devices is large (e.g., *H&L* configuration), CDE provides higher performance than other baseline policies (see Figure 7-10(b)). Therefore, in the *H&L* HSS configuration, we observe that Sibyl follows a similar policy, leading to more evictions compared to other baselines.

7.10 Overhead Analysis

7.10.1 Inference and Training Latencies

The input layer of the training and inference networks consists of six neurons, equal to the number of features listed in Table 7.1. Each feature is normalized to transform the value range of different features to a common scale. The size of one state entry is 40 bits (32 bits for state features and 8 bits for the counter used for tracking the remaining capacity in the fast storage device). We make use of two hidden layers with 20 and 30 neurons each. The final output layer has neurons equivalent to our action space, i.e., two for dual-HSS configurations and three for the tri-HSS configurations.

Inference latency. Our inference network has 52 inference neurons ($20+30+2$) with 780 weights ($6\times 20+20\times 30+30\times 2$). As a result, Sibyl requires 780 MAC operations per inference ($1\times 6\times 20+1\times 20\times 30+1\times 30\times 2$). On our evaluated CPU, we can perform these operations in ~ 10 ns, which is several orders of magnitude smaller than the I/O read latency of even a high-end SSD (~ 10 us) [190, 404]. Sibyl’s inference computation can also be performed in the SSD controller.

Training latency. For each training step, Sibyl needs to compute 1,597,440 MAC operations, where each batch requires $128\times 6\times 20+128\times 20\times 30+128\times 30\times 2$ MAC operations. This computation takes ~ 2 us on our evaluated CPU. This training latency does not affect the benefits of Sibyl because (1) training occurs asynchronously with inference, and (2) training latency is $\sim 5\times$ smaller than the I/O read latency of even a high-end SSD.

We conclude that Sibyl’s performance benefits come at small latency overheads that are easily realizable in existing CPUs.

7.10.2 Area Overhead

Storage cost. We use a half-precision floating-point format for the weights of the training and the inference networks. With 780 16-bit weights, each neural network requires 12.2 KiB of memory. Since we use the same network architecture for the two networks, we need 24.4 KiB of memory. In total, with an experience buffer of 100 KiB (Section 7.6.2), Sibyl requires 124.4 KiB of DRAM overhead, which is negligible compared to the memory size of modern computing systems.

Metadata cost. HSSs need to maintain the address mapping information for the underlying storage devices [467]. Sibyl requires 40 bits to store state information (i.e., the per-page state features; see Table 7.1). This overhead is $\sim 0.1\%$ of the total storage capacity when using a 4-KiB data placement granularity (5-byte per 4-KiB data). We conclude that Sibyl has a very modest cost in terms of storage capacity overhead in main memory (DRAM).

7.11 Discussion

Cost of generality. We identify two main limitations of using RL for data placement. First, currently, RL is largely a *black-box policy*. Our explainability analysis (Section 7.9) tries to provide intuition into Sibyl’s internal mechanism. However, providing rigorous explainability to reinforcement learning-based mechanisms is an active field of research [214, 279, 296, 383, 414, 477], a problem that is beyond the scope of this paper. Perfectly finding worst-case workloads against an RL policy is, therefore, very difficult, in fact, impossible, given the state-of-the-art in reinforcement learning. There are many dynamic decisions that the agent performs, which cannot be easily explained or modeled in human-understandable terms. Second, Sibyl requires *engineering effort* to (1) thoroughly tune the RL hyper-parameters, and (2) implement and integrate Sibyl components into the host OS’s storage management layer. This second limitation is not specific to Sibyl and applies to any ML-based storage management technique. As quantified in Section 7.10, Sibyl’s storage and latency overheads are small.

Sibyl’s implications. Sibyl (1) provides performance improvements on a wide variety of workloads and system configurations (our evaluations in Section 7.8 show that Sibyl outperforms all evaluated state-of-the-art data placement policies under all system configurations), (2) provides extensibility by reducing the designer burden when extending data placement policies to multiple devices and different storage configurations, and (3) enables reducing the fast storage device size by taking better advantage of the fast-yet-small storage device and large-yet-slow storage device to deliver high storage capacity at low latency.

Adding more features and optimization objectives. An RL-based approach simplifies adding new features (such as bandwidth utilization) in the RL state and

optimization objectives (such as endurance) using the RL reward function. This flexibility allows an RL-based mechanism to self-optimize and adapt its decision-making policy to achieve an objective without the designer explicitly defining *how* to achieve it. We demonstrate and evaluate example implementations of Sibyl using a reward scheme that is a function of request latency and eviction latency. We find that request latency in the reward structure best encapsulates system conditions since latency could vary for each storage request based on complex system conditions. To optimize for a different device-level objective, one needs to define a new reward function with appropriate state features, e.g., to optimize for endurance, one might use the number of writes to an endurance-critical device in the reward function. Another interesting research direction would be to perform multi-objective optimization, e.g., optimizing for both performance and energy. We leave the study of different objectives and features to future work.

Necessity of the reward. RL training is highly dependent upon the quality of the reward function and state features. Using an incorrect reward or improper state features could lead to severe performance degradation. Creating the right reward is a human-driven effort that could benefit from design insights. We tried two other reward structures to achieve our objective to improve system performance:

- **Hit rate of the fast storage device:** Maximizing the hit rate of the fast storage device is another potentially plausible objective. However, if we use the hit rate as a reward, Sibyl (1) tries to aggressively place data in the fast storage device, which leads to unnecessary evictions, and (2) cannot capture the asymmetry in the latencies present in modern storage devices (e.g., due to read/write latencies, latency of garbage collection, queuing delays, error handling latencies, and write buffer state).
- **High negative reward for eviction:** We also tried a negative reward for eviction and a zero reward in other cases. We observe that such a reward structure provides suboptimal performance because Sibyl places more pages in the slow device to avoid evictions. Thus, with such a reward structure, Sibyl is not able to effectively utilize the fast storage.

We conclude that our chosen reward structure works well for a wide variety of workloads Section 7.8, as reinforced by our generality studies using unseen workloads in Section 7.8.2.

Managing hybrid main memory using RL. The key idea of Sibyl can be adapted for managing hybrid main memory architectures. However, managing data placement at different levels of the memory hierarchy has its own set of challenges [9, 10, 152, 171, 266, 272, 299, 311, 312, 366, 373, 388, 397, 524] that Sibyl would need to adapt to, such as the low latency decision-making and control requirements in main memory. Even with the use of hybrid main memories, many systems continue to benefit from using

hybrid storage devices due to much lower cost-per-bit of storage, which accommodates increasingly larger datasets. Therefore, we focus on hybrid storage systems and leave it to future work to study RL to manage hybrid main memories.

7.12 Related Work

To our knowledge, this is the first work to propose a reinforcement learning-based data placement technique for hybrid storage systems. Sibyl can continuously learn from and adapt to the running application and the storage configuration and device characteristics. We briefly discuss closely-related prior works that propose data management techniques for hybrid memory/storage systems and RL-based system optimizations.

Heuristic-based data placement. Many prior works [9, 10, 62, 80, 93, 118, 122, 131, 162, 171, 189, 236, 244, 266, 268, 274, 282, 292, 293, 294, 303, 304, 312, 366, 391, 403, 446, 453, 476, 488, 492, 508, 519, 528] propose heuristic-based techniques to perform data placement. These techniques rely on statically-chosen design features that usually favor certain workloads and/or device characteristics, leading to relatively rigid policies. In Section 7.3 and Section 7.8, we show that Sibyl outperforms two state-of-the-art works, CDE [303] and HPS [310].

ML-based data placement. Several works [83, 117, 398, 413, 422] propose ML-based techniques for data placement in hybrid memory/storage systems. These works 1) are based on supervised learning techniques that require frequent and very costly retraining to adapt to changing workload and device characteristics, and 2) have not been evaluated on a real system. We evaluate RNN-HSS, which is inspired by the state-of-the-art data placement technique in hybrid main memory [117]. It uses sophisticated recurrent neural networks (RNNs) for data placement and shows promising results compared to heuristic-based techniques. However, it has two major limitations that make it impractical or difficult to implement: it (1) trains an RNN for each page, which leads to large computation, storage, and training time overheads, and (2) requires offline application profiling. Our evaluation (ref. Section 7.8.1) shows that Sibyl outperforms two state-of-the-art ML-based data placement techniques, RNN-HSS [117] and Archivist [398], across a wide variety of workloads.

RL-based techniques in storage systems. Recent works (e.g., [217, 218, 281, 491, 523]) propose the use of RL-based approaches for managing different aspects of storage systems. These works cater to use cases and objectives that are very different from Sibyl’s. Specifically, Liu *et al.* [281] (1) propose data placement in cloud systems and *not* hybrid storage systems, (2) consider devices with unlimited capacity, sidestepping the capacity limitations, (3) *emulate* a data center network rather than use a real system for design and evaluation, and (4) focus only on data-analytics workloads.

Yoo *et al.* [523] do *not* focus on data placement; they instead deal with dynamic storage resizing based on workload characteristics using a trace-based simulator. Wang *et al.* [491] (1) focus on cloud systems to predict the data storage consumption, and (2) do *not* consider hybrid storage systems. Sibyl is the first RL-based mechanism for data placement in hybrid storage systems.

RL-based system optimizations. Past works [50, 133, 197, 201, 275, 278, 302, 318, 325, 328, 368, 370, 521, 534] propose RL-based methods for various system optimizations, such as memory scheduling [197, 325], data prefetching [50, 370], cache replacement [278], and network-on-chip arbitration [275, 521]. Along with Sibyl, designed for efficient data placement in hybrid storage systems, this body of work demonstrates that RL is a promising approach to designing high-performance, and highly-adaptive self-optimizing computing systems.

7.13 Conclusion

We introduce Sibyl, the first reinforcement learning-based mechanism for data placement in hybrid storage systems. Our extensive real-system evaluation demonstrates that Sibyl provides adaptivity and extensibility by continuously learning from and autonomously adapting to the workload characteristics, storage configuration and device characteristics, and system-level feedback to maximize the overall long-term performance of a hybrid storage system. We interpret Sibyl’s policy through our explainability analysis and conclude that Sibyl provides an effective and robust approach to data placement in current and future hybrid storage systems. We hope that Sibyl and our open-sourced implementation of it [95] inspire future work and ideas in self-optimizing storage and memory systems.

Chapter 8

Conclusions and Future Directions

In this dissertation, the goal was twofold. First, overcome the data movement bottleneck by following a data-centric approach of bringing processing close to the memory and ensure that system components are not overwhelmed by data; thus, enabling high-performance in an energy-efficient way. Second, leverage the enormous amount of data to devise computer architecture mechanisms that can assist us in architectural decisions or optimizations. To this end, the dissertation presented five contributions to effectively handle and leverage the vast amount of data for future computing systems. Table 8.1 shows nine architectural methods that we use across our five contributions.

A data-centric architecture: In **Chapter 3**, we designed NERO, a data-centric accelerator for a real-world weather prediction application. NERO overcomes the memory bottleneck of weather prediction stencil kernels by exploiting near-memory computation capability on specialized field-programmable gate array (FPGA) accelerators with high-bandwidth memory (HBM) that are attached to the host CPU. Our experimental results showed that NERO outperforms a 16 core POWER9 system by $4.2\times$ and $8.3\times$ when running two different compound stencil kernels. NERO reduces the energy consumption by $22\times$ and $29\times$ for the same two kernels over the POWER9 system with an energy efficiency of 1.5 GFLOPS/Watt and 17.3 GFLOPS/Watt. We concluded that employing near-memory acceleration solutions for weather prediction modeling is promising as a means to achieve both high performance and high energy efficiency.

Precision tolerance and alternate number system: In **Chapter 4**, we explored the applicability of different number formats and searched for the appropriate bit-width for complex stencil kernels, which are one of the most widely used scientific kernels. Further, we leveraged the arbitrary fixed-point precision capabilities of an FPGA to

Table 8.1: We highlight across five contributions nine different methods (concepts) used in this dissertation to achieve the thesis statement of handling data well. We make use of two guiding principles: (1) *data-centric* (DC) is bringing processing closer to where data resides and ensuring that data does not overwhelm system components; (2) *data-driven* (DD) is leveraging data to perform architectural decisions or predictions.

METHODS	CONTRIBUTIONS				
	NERO [434]	Low Precision [436]	NAPEL [437]	LEAPER [433]	Sibyl [438]
Specialization (DC)	FPGA-based accelerator	Implementation on an FPGA for fixed-point and floating-point representation		FPGA-based accelerator	
Revisit memory hierarchy (DC)	Scratchpad-based hybrid memory				Tiered hybrid storage system
Reducing copies between host and accelerator (DC)	Shared memory space	Quantize data			
Dataflow architecture (DC)	Task pipelining				
Near-memory computing (DC)	Processing near-high-bandwidth memory		Processing near-3D stacked memory		
Reducing memory footprint (DC)	Single and half floating-point precision	Different number representations—posit, fixed-point, and floating-point			
Static ML (DD)			Learns application performance and energy consumption	Learns resource utilization and performance models	
Speed up design space exploration (DD)	Auto-tuning for data transfer window size		Supervised ML, Design of experiment	Few-shot learning	Design of experiment
Dynamic ML (DD)					Reinforcement Learning
Goal	Overcome memory bottleneck of weather prediction application	Investigate computationally cheaper number representations	Quick performance and energy estimates of new applications	Quick area and performance estimates on new high-end FPGA-based platforms	Efficient and high performance data placement mechanism

demonstrate these kernels’ achievable performance on state-of-the-art hardware that includes IBM POWER9 CPU with an FPGA board connected via CAPI interface. Thus, this chapter filled the gap between current hardware capabilities and future systems for stencil-based scientific applications.

Data-driven alternative to system simulation: In **Chapter 5**, we proposed NAPEL, a machine learning-based application performance and energy prediction framework for data-centric architectures. NAPEL uses ensemble learning to build a model that, once trained for a fraction of programs on a number of architecture configurations, can predict the performance and energy consumption of different applications. Our inexpensive performance model can provide, on average, an additional 10× reduction in performance evaluation time with an error rate lower than 15% compared to a computationally-intensive state-of-the-art NMC simulator.

Data-driven modeling of FPGA-based systems: In **Chapter 6**, we presented LEAPER, the first use of *few-shot learning* to transfer FPGA-based computing models across different hardware platforms and applications. Experimental results showed that

our approach delivers, on average, 85% accuracy when we use our transferred model for prediction in a cloud environment with *5-shot learning* and reduces design-space exploration time by $10\times$, from days to only a few hours. These machine learning-based mechanisms follow *data-driven* techniques by using the vast amount of data to provide fast and accurate performance prediction results.

Data-driven mechanism for data-placement in hybrid storage systems: In **Chapter 7**, we proposed Sibyl, a reinforcement learning (RL)-based data-placement technique for a hybrid storage system (HSS). Sibyl observes different features of the running workload as well as the storage devices to make system-aware data placement decisions. For every decision it makes, Sibyl receives a reward from the system that it uses to evaluate the long-term performance impact of its decision and continuously optimizes its data placement policy online. Our real system evaluation results show that Sibyl provides 21.6%/19.9% performance improvement in a performance-oriented/cost-oriented HSS configuration compared to the best previous data placement technique. Our evaluation using an HSS configuration with three different storage devices shows that Sibyl outperforms the state-of-the-art data placement policy by 23.9%-48.2%, while significantly reducing the system architect’s burden in designing a data placement mechanism that can simultaneously incorporate three storage devices. We show that Sibyl achieves 80% of the performance of an oracle policy that has complete knowledge of future access patterns while incurring a very modest storage overhead of only 124.4 KiB.

We conclude that the mechanisms proposed by this dissertation provide promising solutions to handle data well by following a *data-centric* approach and further demonstrates the importance of leveraging data to devise *data-driven* policies.

8.1 Outlook and Future Directions

Throughout this dissertation, we considered data as a paramount resource and provided various mechanisms to effectively handle and leverage the vast amount of data. We identify topics for future research both in data-centric computing and data-driven optimization techniques.

8.1.1 Data-Centric Computing

In data-centric computing, we ensure that our computing systems are not overwhelmed by data. There are two different approaches to enable data-centric computing. First, near-memory computing (NMC) [11, 12, 68, 132, 145, 155, 182, 183, 225, 334, 434] adds processing capabilities close to the existing memory architectures. Second, computation-in memory (CIM) [7, 77, 144, 264, 265, 399, 416, 417, 419] exploits the

memory architecture and intrinsic properties of emerging technologies to perform operations using memory itself. We identify the following key topics for future research that we regard as essential to unlock the full potential of data-centric computing.

Architecture: It is unclear which emerging memory technology best supports data-centric computing; for example, much research is going into new 3D stacked DRAM and non-volatile memories such as PCM and ReRAM. The future of these new technologies relies heavily on advancements in endurance, reliability, cost, and density. Moreover, these memories have different memory attributes, such as latency, bandwidth, cost, and energy consumption. We believe a hybrid approach of complementing two different technologies, as we show in Chapter 7, can revolutionize our current systems. Huang *et al.* [386] evaluate one such architecture that tightly integrates CPU, DRAM, and a flash-based NVM to meet the memory needs of big data applications, i.e., larger capacity, smaller delay, and wider bandwidth. Processing near-heterogeneous memories is a new research topic with high potential (could provide the best of both worlds), and in the future, we expect much interest in this direction. Further, we see a trend towards processing near caches [7, 120], and we expect more works in this direction. The right level of cache where to place the processing unit would be an interesting future direction.

The interplay of NMC units with the emerging interconnects standards like CXL [421], CCIX [23], and CAPI [444] could be vital in improving the performance and energy efficiency of big data workloads running on NMC enabled servers. More quantitative exploration is required for interconnecting networks between the near-memory compute units and between the host and near-memory compute systems. Besides the design of the near-memory computing device itself, the integration of such architectures into the overall computing system and how multiple near-memory computing devices can work together to scale to larger data volumes are critical challenges to solve.

Software: Most of the evaluated architectures focus on the compute aspect. Few architectures focus on providing coherency and virtual memory support. As highlighted in Section 2.3, lack of coherency and virtual memory support makes programming difficult and obstructs the adoption of the NMC paradigm. At the application level, algorithms need to provide code and data co-location for efficient processing. For example, in NMC, algorithms should prevent excessive movement of data between vaults (as in 3D stacked memory, see Figure 2-1) and across different memory modules. Whenever it is not possible to avoid an inter-vault data transfer, we should provide light-weight data migration mechanisms.

Tool support and benchmarks: The field requires a generic set of open-source tools and techniques for these novel systems. Often researchers have to spend a significant amount of time and effort in building the needed simulation environment.

Application characterization tools should add support for static and dynamic decision support for offloading processing and data to near-memory systems. NMC-specific metrics are required to assist in the offloading decision to assess whether an application is suitable for these architectures. These tools could provide region-of-interest (or hotspots) in an application that should be offloaded to an NMC system. Besides, a standard benchmark set is missing to gauge different architectural proposals in this domain.

8.1.2 Data-Driven System Optimization

We are seeing an enormous amount of data being generated in different applications domains. Rather than discarding the available data, our machines should leverage this data to understand inherent characteristics or patterns to make better architectural decisions or predictions. To this end, machine learning-based approaches provide an attractive tool that can assist our computer architecture in various aspects. In this dissertation, we use this tool for performance and energy prediction to reduce the time for simulation overhead (Chapter 5), resource and application performance prediction to overcome the disadvantages of the slow FPGA downstream mapping process (Chapter 6), effective data-placement (Chapter 7), and perform design space exploration for the fixed-point precision (Appendix B). These mechanisms are likely just the beginning of a paradigm shift in computer architecture design and use. Below we highlight some aspects of computer architecture where data-driven mechanisms can greatly assist us.

Architecture: Past works have demonstrated the applicability of using supervised learning-based techniques in hardware such as prefetching [271], branch prediction [208], and cache replacement [424]. However, hardware feasibility is one of the fundamental challenges in the adoption of these techniques. In the future, we need to make these approaches hardware friendly with low cost and area overhead by using techniques such as pruning, quantization, model compression, etc.

Software: The operating system is a ripe place to use ML-based approaches as software-based mechanisms can tolerate higher latency and implementation overhead than latency-critical aspects of computer architecture such as prefetching and cache-replacement. We can apply modern ML techniques, such as deep reinforcement learning and natural language processing, on problems like software caching, task scheduling, power management, virtual memory management, etc.

Explainability: Explainability is providing an explanation of the internal mechanisms of a machine learning model that led the model to a certain prediction or decision. The machine learning community has started to look into the explainability to understand these models' inner workings. However, we still use these tools as mere black-box models in the computer architecture community without making them as

white-box models. Explainability can lead to certain insights that have been unknown to our current community, and learn from it to develop better human-driven policies. Since implementing ML algorithms in the hardware can be costly, leveraging insights from ML algorithms can help us better optimize our computing systems.

We hope that the ideas, analyses, methods, and techniques presented in this dissertation will enable the development of energy-efficient data-intensive computing systems and drive the exploration of new mechanisms to improve the performance and energy efficiency of future computing systems.

Appendix A

Review of Near-Memory Data-Centric Architectures

In the past, many near-memory computing (NMC) architectures have been proposed and/or designed. This appendix summarizes a large selection of NMC architectures that are either targeting main memory (Appendix A.1) or storage class memory (Appendix A.2). We couple different memory technologies with three broad classes of processing units: programmable unit, fixed-functional unit, and reconfigurable unit. The classification and evaluation metrics are detailed in Section 2.2.

A.1 Processing Near-Main Memory

Processing near-main memory can allow us to reduce the data movement bottleneck by circumventing memory-package pin-count limitations. We describe some of the notable architectures that process close to main memory. All solutions discussed in this section are summarized in Table 2.2.

A.1.1 Programmable Unit

NDC (2014) Pugsley *et al.* [382] focus on Map-Reduce workloads, characterized by localized memory accesses and embarrassing parallelism. The architecture consists of a central multi-core processor connected in a daisy-chain configuration with multiple 3D-stacked memories. Each memory houses many ARM cores that can perform efficient memory operations without hitting the memory wall. However, they were not able to fully exploit the high internal bandwidth provided by HMC. The NMC processing units need careful redesigning to saturate the available bandwidth.

TOP-PIM (2014) Zhang *et al.* [527] propose an architecture that consists of an accelerated processing unit (APU) coupled with 3D-stacked memory. Each APU

consists of a GPU and a CPU on the same silicon die. The authors focus on providing code portability with ease-of-programmability. The kernels analyzed span from graph processing to fluid and structural dynamics. However, the authors use traditional coherence mechanisms based on restricted memory regions that restrict data placement restriction.

AMC (2015) Nair *et al.* [334] develop an architecture called active memory cube (AMC), which is built upon the HMC-based memory. They add several processing elements to the vault of HMC, which they refer to it as *lanes*. Each lane has a computational unit, a dedicated register file, and a load/store unit that performs read and write operations to a dedicated part of AMC memory. The host processor coordinates the communication between AMCs. However, such an approach requires low communication overhead to avoid performance degradation and undoing benefits of processing near-memory.

PIM-enabled (2015) Ahn *et al.* [12] leverage an existing programming model so that the conventional architectures can exploit the NMC concept without changing the programming interface. They add compute-capable commands and specialized instructions to trigger the NMC computation. NMC processing units are composed of computation logic (e.g., adders) and an SRAM operand buffer. The authors place these processing units in the logic layer of an HMC-based memory. Offloading at the instruction level, however, could lead to significant overhead. In addition, the proposed solution requires substantial changes on the application side, hence reducing application readiness and can be a hurdle for wide adoption.

TESSERACT (2015) Ahn *et al.* [11] focus on graph processing applications. Their architecture consists of a host processor connected to an HMC-based memory. Each HMC vault has an out-of-order processor mapped to it. These cores can see only their local data partition, but they can communicate with each other using a message-passing protocol. The host processor has access to the entire address space of the HMC. The authors also use prefetching of data to exploit the high available memory bandwidth in their systems. However, the performance benefits largely depend upon the efficient distribution of graphs to the vaults in HMC-based memory, which the authors do not consider in this work.

TOM (2016) Hsieh *et al.* [182] propose an NMC architecture consisting of a host GPU interconnected to multiple 3D-stacked memories with small, light-weight GPU cores. They develop a compiler framework that automatically identifies possible offloading candidates. Code blocks are marked as beneficial to be offloaded by the compiler if the saving in memory bandwidth during the offloading execution is higher than the cost to initiate and complete the offload. A runtime system takes the final decision as to where to execute a block. Furthermore, the framework uses a mapping scheme that ensures data and code co-location. The cost function proposed for code

offloading makes use of static analysis to estimate the bandwidth saving. However, static analysis may fail on code with indirect memory accesses.

Pattnaik¹ (2016) Pattnaik *et al.* [365], similar to [182], develop an NMC-assisted GPU architecture. An affinity prediction model decides where to execute a kernel while a scheduling mechanism tries to minimize the application execution time. The scheduling mechanism can overrule the decision made by the affinity prediction model. The author proposes to invalidate the L2 cache of the host GPU after each kernel execution to keep memory consistency between the host GPU and the near-memory cores. However, their affinity prediction model is trained for a specific set of applications and architecture that would have low prediction performance for a new, unknown application or architecture.

MONDRIAN (2017) Drumond *et al.* [105] demonstrate that a hardware/software co-design approach is required to achieve efficiency and performance for NMC systems. In particular, they show that the current optimization of data-analytic algorithms heavily relies on random memory accesses while the NMC system prefers sequential memory accesses to saturate the huge bandwidth available. Based on this observation, the authors propose an architecture that consists of a mesh of HMC with tightly connected ARM cores in the logic layer.

MCN (2018) Alian *et al.* [15] use a light-weight near-memory processing unit in the buffered DRAM DIMM. The memory channel network (MCN) processor runs an OS with network software layers essential for running a distributed computing framework. The most striking feature of MCN is that the authors demonstrate unified near-data processing across various nodes using ConTutto FPGA [445] with IBM POWER8. However, supporting the entire TCP/IP stack on the near-memory accelerator requires a complex accelerator design. Current trends in the industry, however, are pushing for a simplified accelerator design shifting the complexity on the host core's side [444]).

DNN-PIM (2018) Liu *et al.* [280] propose heterogeneous NMC architecture for the training of deep neural network (NN) models. The logic layer of 3D-stacked memory comprises programmable ARM cores and large fixed-function units (adders and multipliers). They extend the OpenCL programming model to accommodate the NMC heterogeneity. Both fixed-function NMC and programmable NMC appear as distinct compute devices. A runtime system dynamically maps and schedules NN kernels on a heterogeneous NMC system based on online profiling of NN kernels.

Boroumand¹ (2018) Boroumand *et al.* [57] evaluate NMC architectures for Google workloads. They observe that: (1) many Google workloads spend a considerable amount of energy on data movement; (2) simple functions are responsible for a significant fraction of data movement. Based on their observations, they propose two

¹Architecture has no name, first author's name is shown.

NMC architectures, one with a general-purpose processing core and the other with a fixed-function accelerator coupled with HBM-based memory. While accelerating the Google workloads, the authors take into account the low area and power budget in consumer devices. They evaluate the benefits of the proposed NMC architectures.

FIMDRAM (2021) Kwon *et al.* [247] make the following two observations. First, ML has become a driving factor in the advancement of various technologies. Second, the improvements in DRAM bandwidth could only be delivered with a significant increase in power consumption. Based on the above observations, the authors’ goal is to develop an energy-efficient DRAM architecture for ML-based workloads that can deliver high bandwidth with low power consumption. To this end, the authors design an NMC architecture with 16-way floating-point16 (FP16) programmable compute units with an access granularity as the host processor, which simplifies various system-level aspects such as address mapping and interleaving. The experimental results demonstrate that FIMDRAM can provide $2\times$ performance and 70% less energy consumption than a GPU+HBM implementation for DeepSpeech2 workload. FIMDRAM shows promising results for ML-based workloads, however, the efficacy for other data-intensive workloads such as weather prediction, genomics, and databases is still an open question.

A.1.2 Fixed-Function Unit

JAFAR (2015) Xi *et al.* [510] embed an accelerator in a DRAM module to implement database select operations. The key idea is to use the near-memory accelerator to scan and filter data directly in the memory while only the relevant data will be moved to the host CPU. Thus, having a significant reduction in data movement. The authors suggest using memory-mapped registers to read and write via application program interface (API) function calls to control the accelerator. Even though JAFAR shows promising potential in database applications, its evaluation is quite limited as it can handle only filtering operations. More complex operations fundamental for the database domain such as sorting, indexing and compression are not considered.

IMPICA (2016) Hsieh *et al.* [183] accelerate pointer chasing operations, ubiquitous in data structures. They propose adding specialized units that decouple address generation from memory accesses in the logic layer of 3D-stacked memory. These units traverse through the linked data structure in memory and return only the final node found to the host CPU. They also propose to completely decouple the page table of IMPICA from the host CPU to avoid virtual memory-related issues. The memory coherence is assured by demarking different memory zones for the accelerators and the host CPU. This design provides a state-of-the-art technique for address translation in NMC for pointer chasing.

Vermij¹ (2017) Vermij *et al.* [478] propose a system for sorting algorithms where phases having high temporal locality are executed on the host CPU, while algorithm phases with poor temporal locality are executed on an NMC device. The architecture proposed consists of a memory technology-agnostic controller located at the host CPU side and a memory-specific controller tightly coupled with the NMC system. The NMC accelerators are placed in the memory-specific controllers and are assisted by an NMC manager. The NMC manager also supports cache coherency, virtual memory management, and communications with the host processor.

GraphPIM (2017) Nai *et al.* [332] map graph workloads in the HMC by exploiting its inherent atomic² functionality. As they focus on atomics, they can offload at instruction granularity. Notably, they do not introduce new instructions for NMC and use the host instruction set to map to NMC atomics through an uncacheable memory region. Similar to [12], offloading at instruction granularity can have significant overhead. Besides, the mapping to NMC atomics instruction requires the graph framework to allocate data on particular memory regions via custom *malloc*. This custom allocation requires changes on the application side, reducing the application readiness.

GRIM-Filter (2018) Kim *et al.* [234] develop a seed location filter for the read mapping stage of the genomics pipeline that exploits the high memory bandwidth and near-memory processing capabilities of 3D-stacked DRAM to improve the performance of DNA read mappers. The authors demonstrate a $5.6 \times -6.4 \times$ lower false-negative rate with end-to-end performance improvement of $1.8 \times -3.7 \times$ over a state-of-the-art DNA read mapper. GRIM-Filter targets only the short reads (i.e., segments on the order of several hundred base pairs long), while accelerating long reads is an important problem [377].

RecNMP (2020) Ke *et al.* [225] overcome the memory bottleneck of personalized recommendation systems. A personalized recommendation is a fundamental part of services like a search engine, social network, etc. After characterizing production-recommendation models, the authors observe that the recommendation model's sparse embedding step leads to a memory bottleneck. To this end, the authors propose RecNMC, which uses light-weight processing cores to accelerate embedding operations in the DIMM of existing standard DRAM. RecNMP accelerates the shows $9.8 \times$ memory latency speedup and 45.9% memory energy savings.

GenASM (2020) Cali *et al.* [68] accelerate the *approximate string matching* (ASM) step of genome analysis. ASM is a computationally-expensive step as it usually uses dynamic programming (DP)-based algorithms. The authors modify the underlying ASM algorithm to increase its parallelism and reduce its memory footprint

²An atomic instruction such as compare-and-set is an indivisible instruction where the CPU is not interrupted when performing such operations.

significantly. Their accelerator design follows a systolic-array-based architecture that they place in the logic layer of HMC-based memory. The authors demonstrate the flexibility of their accelerator design in accelerating multiple steps of genome analysis.

NATSA (2020) Fernandez *et al.* [132] design a near-memory accelerator for time series analysis. Specifically, the authors implement a matrix profile algorithm that has a low arithmetic intensity and operates on a large amount of data. As a result, this algorithm is memory-bound and performs poorly on multi-core systems. NATSA’s processing element consists of floating-point arithmetic units that they place next to HBM-based 3D stacked memory. NATSA improves performance by $9.9\times$ on average and reduces energy by $19.4\times$ on average over a multi-core implementation. However, it considers HBM as a stand-alone unit without a host-system. Such a scenario leads to practical concerns such as processing orchestration and data-mapping.

A.1.3 Reconfigurable Unit

Gokhale¹ (2015) Gokhale *et al.* [154] propose to place a data rearrangement engine (DRE) in the logic layer of the HMC to accelerate data accesses while still performing the computation on the host CPU. The authors target cache unfriendly applications with high memory latency due to irregular access patterns, e.g., sparse matrix multiplication. Each of the DRE engines consists of a scratchpad, a simple controller processor, and a data mover. To make use of the DRE units, the authors develop an API that supports several operations. Each operation is issued by the main application running on the host and served by a control program loaded by the OS on each DRE engine. Similar to [365], the authors propose to invalidate the CPU caches after each fill and drain operation to keep memory consistency between the near-memory processors and the main CPU. This approach can introduce a significant overhead. Furthermore, the synchronization mechanism between the CPU and the near-memory processors is based on polling. Therefore, the CPU wastes clock cycles waiting for the near-memory accelerator to complete its operations. On the other hand, a light-weight synchronization mechanism based on interrupts could be a more efficient alternative.

HRL (2015) Gao *et al.* [145] propose a reconfigurable logic architecture called heterogeneous reconfigurable logic (HRL) that consists of three main blocks: fine-grained configurable logic blocks (CLBs) for control unit, coarse-grained functional units (FUs) for basic arithmetic and logic operations, and output multiplexer blocks (OMBs) for branch support. Each memory module follows HMC like technology and houses multiple HRL devices in the logic layer. The central host processor is responsible for data partition and synchronization between NMC units. As in the case of [527], to avoid consistency issues and virtual-to-physical translation, the authors propose a memory-mapped non-cacheable memory region that puts restrictions on

data placement.

NDA (2015) Farmahini *et al.* [129] propose three different NMC architectures using coarse-grained reconfigurable arrays (CGRA) on commodity DRAM modules. This proposal requires minimal change to the DRAM architecture. However, programmers should identify which code would run close to memory. This dependence leads to increased programmer effort for demarking compute-intensive code for execution. Also, it does not support direct communication between NMC stacks.

A.2 Processing Near-Storage Class Memory

NAND flash-based non-volatile memories (NVM) are trying to fill the latency gap between DRAMs and disks are termed as storage-class memories (SCM) [333]. SCM, like NVRAM, is even touted as a future replacement for DRAM [392]. Moving computation in SCM has some of the similar benefits to DRAM concerning savings in bandwidth, power, latency, and energy but also because of the higher density it allows to work on much larger data-sets as compared to DRAM [387].

A.2.1 Programmable Unit

XSD (2013) Cho *et al.* [88] propose a solid-state drive (SSD)-based architecture that integrates graphics processing unit (GPU) close to the memory. They provide an API based on the MapReduce framework that allows users to express parallelism in their application and exploit the parallelism provided by the embedded GPU. They develop a performance model to tune the SSD design. The experimental results show that the proposed XSD is approximately $25\times$ faster than an SSD model incorporating a high-performance embedded CPU. However, the host CPU instruction set architecture (ISA) needs to be modified to launch the computation on the GPU embedded inside the SSD.

WILLOW (2014) Seshadri *et al.* [415] propose a system that has programmable processing units referred to as storage processor units (SPUs). Each SPU runs a small operating system (OS) that maintains and enforces security. On the host-side, the Willow driver creates and manages a set of objects that allow the OS and applications to communicate with SPUs. The programmable functionality is provided in the form of *SSD Apps*. Willow enables programmers to augment and extend SSD semantics with application-specific features without compromising file system protection. The programming model based on remote procedure call (RPC) supports the concurrent execution of multiple SSD Apps and trusted code execution. However, it neither supports dynamic memory allocation nor allows users to load their tasks to run on the SSD dynamically.

SUMMARIZER (2017) Koo *et al.* [241] design APIs that can be used by the host application to offload filtering tasks to the inherent ARM-based cores inside an SSD processor. This approach reduces the amount of data transferred to the host and allows the host processor to work on the filtered result. They evaluate static and dynamic strategies for dividing the work between the host and SSD processor. However, sharing the SSD controller processor for user applications and SSD firmware can lead to performance degradation due to interference between I/O tasks and in-storage compute tasks.

CompStor (2018) Torabzadehkashi *et al.* [463] propose an architecture that consists of NVMe over PCIe SSD and FPGA-based SSD controller coupled with in-storage processing subsystem (ISPS) based on the quad-core ARM A53 processor. They modify the SSD controller hardware and software to provide high bandwidth and low latency data path between ISPS and the flash media interface. Fully isolated control and data paths ensure concurrent data processing and storage functionality without degradation in either one's performance. The architecture supports porting a Linux operating system. However, homogeneous processing cores in the SSD are not sufficient to meet the requirement of complex modern applications [464].

A.2.2 Fixed-Function Unit

Smart SSD (2013) Kang *et al.* [219] implement the Smart SSD features in the firmware of a Samsung SSD and modify the Hadoop core and MapReduce framework to use task-lets as a map or a reduce function. To evaluate the prototype, they used a micro-benchmark and log analysis application on both the device and the host. Their SmartSSD is able to outperform host-side processing drastically by utilizing internal application parallelism. Likewise, Do *et al.* [363] extend Microsoft SQL Server to offload database operations onto a Samsung Smart SSD. The selection and aggregation operators are compiled into the firmware of the SSD. Quero *et al.* [387] modify the Flash Translation Layer (FTL) abstraction and implement an indexing algorithm based on the B++tree data structure to support sorting directly in the SSD. The approach of modifying the SSD firmware to support the processing of certain functions is fairly limited and can not support the wide variety of workloads [464].

ProPRAM (2015) Wang *et al.* [494] observe that NVM is often supporting built-in logic like for data comparison, write or flip-n-write module. Therefore, the authors propose to exploit the existing resources inside NVM-based memory chips to accelerate the simple non-compute intensive functions in emerging big data applications. They expose the peripheral logic to the application stack through ISA extension. Like [219, 363, 387], this approach cannot support the diverse workload requirements.

BISCUIT (2016) Gu *et al.* [160] present a near-memory computing framework that allows programmers to write a data-intensive application to run in a distributed

manner on the host and the NMC-capable storage system. The storage hardware incorporates a pattern matcher IP designed for NMC. The authors evaluate their approach by accelerating MySQL-based application. However, the NMC system acts as a slave to the host CPU, and all data is controlled by the host CPU. Therefore, this architecture needs to manage communications messages from the host effectively.

A.2.3 Reconfigurable Unit

BlueDBM (2015) Jun *et al.* [212] present a flash-based platform, called BlueDBM, built of flash storage devices augmented with an application-specific FPGA-based in-storage processor. The data-sets are stored in the flash array and are read by the FPGA accelerators. Each accelerator implements a variety of application-specific distance comparators used in the high-dimensional nearest-neighbor search algorithms. They also use the same architecture exploration platform for graph analytics. However, the platform does not support dynamic task loading, similar to [415], and has limited OS-level flexibility.

CARIBOU (2017) Zsolt *et al.* [199] enable key-value store interface over TCP/IP socket to the storage node comprising of an FPGA connected to DRAM/NVRAM. They implement selection operators in the FPGA, which are parameterizable at runtime, both for structured and unstructured data, to reduce data movement and avoid the negative impact of near-data processing on the data retrieval rate. Like [212], Caribou does not have OS-level flexibility, e.g., the file-system is not supported transparently.

Appendix B

PreciseFPGA: Low Precision Accelerator Search for FPGA

In Chapter 4, we demonstrate the benefits of using lower precision datatypes on an FPGA. However, determining the optimal fixed-point precision in terms of accuracy and power on an FPGA is challenging because of the following two reasons: (1) the design space of choices makes it infeasible to perform an exhaustive manual-tuning; and (2) FPGAs have a slow downstream mapping process. To this end, this appendix presents PreciseFPGA, our preliminary work on building an automated solution for fixed-point precision evaluation for FPGA-based devices, which overcomes the aforementioned issues.

B.1 Introduction

Fixed-point data types have been used for energy-efficient computing in various applications [111, 164, 166]. For a fixed-point configuration, the impact on accuracy, throughput, power, and resource utilization depends largely on its chosen configuration. A random selection of a fixed-point configuration can have a detrimental effect on the accuracy without significant gains in terms of area and power. Therefore, application-aware fixed-point configuration selection is critical to obtain an optimal solution in terms of resource/power consumption without compromising the accuracy.

An FPGA allows us to implement any arbitrary precision fixed-point configuration. However, the number of precision options leads to a very large design space that is infeasible to explore exhaustively on an FPGA because of its time-consuming design cycle. Recently, FPGA designers have started to adopt high-level synthesis (HLS) [481] to increase productivity with reduced time-to-market. HLS converts a C/C++ program into register-transfer logic (RTL) that is further synthesized and mapped to a target FPGA. This complete downstream process can take several hours

for a single design point [101]. Hence, it is impossible to enumerate all possible fixed-point precision choices and exhaustively search for the optimal design that offers low resource consumption while considering the hardware mapping constraints.

Our key idea is to develop an automated framework to obtain an application-aware optimal fixed-point configuration without exhaustively searching the entire design space while taking into account the mapping constraints of an FPGA. To this end, we propose PreciseFPGA - a resource and power estimation framework for arbitrary fixed-point data precision. PreciseFPGA requires HLS C-Synthesis results from only two fixed-point configurations (see Section B.3.3) to provide a Pareto-optimal post-implementation solution with respect to power and error. PreciseFPGA uses these two C-Synthesis utilization reports to obtain the relation between the operation-width of FPGA components and the fixed-point configuration. The extracted relation is extrapolated to obtain operation-width for all possible configurations. Compared to previous works [91, 221, 297, 346, 535], PreciseFPGA provides the following key capability. PreciseFPGA is aware of the effect of FPGA-resource saturation, e.g., in case if we saturate digital signal processing (DSP) units then our framework would map operands to a lookup table (LUT), which makes our approach more practical. We demonstrate our approach by quantizing weights of a neural network (NN)-based accelerator.

B.2 Motivation

In fixed-point representation (see Section 4.3), the feasible fixed-point configuration $\langle x, y \rangle$ for bit-width $\leq N$ can be represented by Equation B.1, where x is the total bitwidth including y integer bits. In general, the total number of fixed-point configurations can be given by Equation B.2.

$$x \leq N \quad \forall x \in [2, N] \quad \forall y \in [1, x - 1] \quad (\text{B.1})$$

$$S = \frac{N(N - 1)}{2} \quad (\text{B.2})$$

As we are interested in reduced precision fixed-point configurations, we restrict the maximum bitwidth to the default bitwidth of our baseline single-precision floating-point representation, i.e., 32-bit. An exhaustive search to obtain an optimal fixed-point configuration requires post-implementation resource and power estimates for all possible configurations. Therefore, with a bitwidth of 32, we would need 496 FPGA downstream mapping runs (using Equation B.2) to complete an exhaustive search. We have discussed different number systems, which include fixed-point, floating-point, and posit, in Chapter 4.

To motivate the need for PreciseFPGA, we perform three experiments to study

the behavior of an NN model with different fixed-point precision configurations.

B.2.1 Effect on Power Consumption

Figure B-1 shows the power consumption of the LeNet-5 [250, 339] convolutional neural network (CNN) model using different bitwidth. We analyze the impact on the post-implementation power consumption using all possible fixed-point configurations (●). We use Equation B.1 to enumerate all possible fixed-point configuration options. We draw two conclusions from Figure B-1. First, the power consumption increases with increasing bitwidth. Second, the maximum power consumption is given by floating-point (■) with a bitwidth of 32.

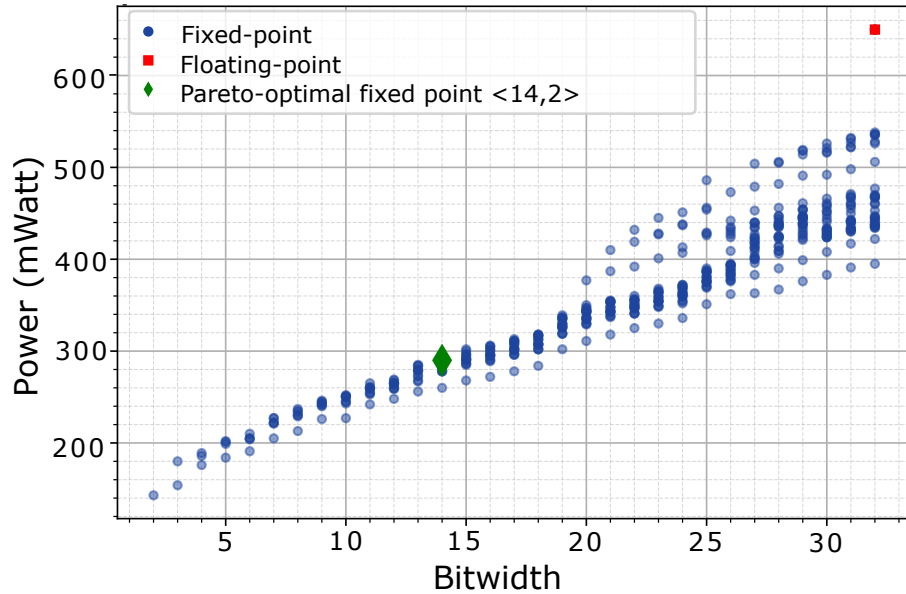


Figure B-1: Power consumption with change in bitwidth for LeNet-5 [250, 339].

B.2.2 Effect on Inference Accuracy

We also studied the impact of different fixed-point configurations on inference accuracy compared to our baseline 32-bit floating-point by following the approach in Section 4.3. We use the percentage accuracy drop of a fixed-point configuration with respect to floating-point implementation as an error metric. We calculated the error for all possible 496 fixed-point configurations using the C-simulation results. We plot the maximum (◆) and the minimum (●) error (%) of the fixed-point configurations with respect to bitwidth in Figure B-2. We draw two conclusions from Figure B-2. First, increasing the bitwidth only does not reduce the error. To find the right bitwidth, we need to find both the appropriate `integer` and the `fractional` part. Second,

increasing the bitwidth beyond a certain point does not significantly improve accuracy but drastically increases the power consumption. For LeNet-5, we found the optimum bitwidth, in terms of power consumption and accuracy, at $\langle 14, 2 \rangle$.

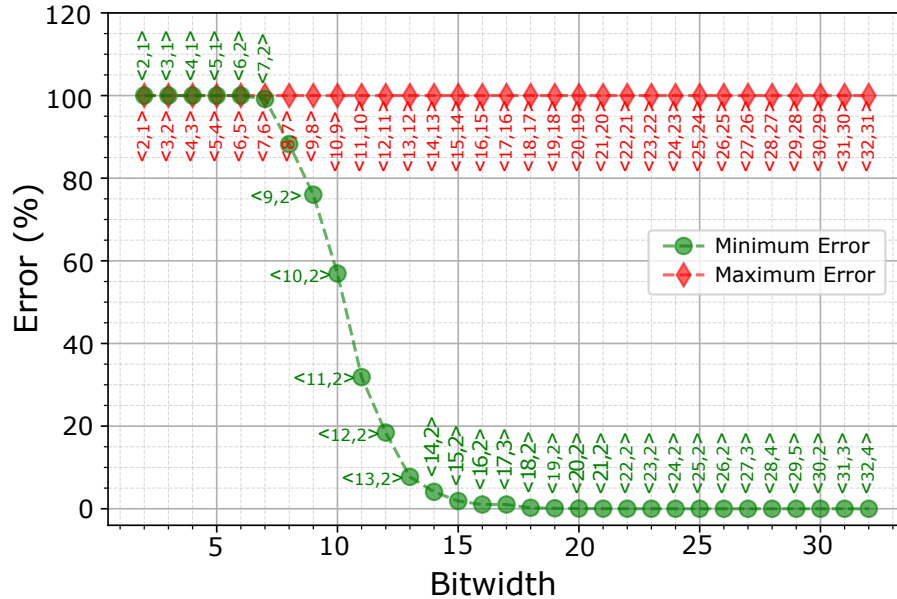


Figure B-2: Error in the inference accuracy of LeNet-5 [250, 339]. To find the optimum bitwidth that minimizes the error without a drastic increase in power consumption, we need to determine both the integer and the fractional part of a fixed-point configuration.

B.2.3 Design Space Exploration Time

While designing an efficient FPGA-based implementation, our goal is to find a Pareto-optimal configuration with respect to power and accuracy. The Pareto-Optimal configuration can vary according to the power budgets and accuracy requirements of a model. In Figure B-1, we observe that the optimal configuration is obtained at $\langle 14, 2 \rangle$ (\blacklozenge), and using a bitwidth beyond 14 does not add much to the accuracy (see Figure B-2) but increases the power consumption linearly. This Pareto-optimal point enables $\sim 55\%$ savings in terms of power with only a 4% loss in accuracy compared to a full-precision floating-point implementation.

However, to achieve this Pareto-optimal design point, we have to perform an exhaustive search for all design options. In the case of LeNet-5 architecture, it took us nearly five days to get the post-implementation results for all possible 496 configurations. This runtime is impractical, and it prohibits us from an effective design-space exploration. Therefore, we require a fast and accurate framework to explore the optimum fixed-point configuration that does not require post-implementation results for all possible configurations. This motivated us to create PreciseFPGA, which

can predict the post-implementation resource and power consumption for fixed-point configurations using only C-Synthesis results of two fixed-point configurations.

B.3 PreciseFPGA

PreciseFPGA is a resource and power estimation framework for fixed-point precision arithmetic targeting Xilinx HLS [481] designs. PreciseFPGA uses two realistic assumptions. First, the change in precision does not affect the control path, which means the number of operations in the application is not varied with the change in precision. Second, the operand-width associated with the precision arithmetic changes linearly with the change in the fixed-point configuration. In this section, we describe the main components of PreciseFPGA. First, we give an overview (Section B.3.1) of our framework. Second, we mention the HLS-based features that vary with change in fixed-point configuration (Section B.3.2). Third, we describe the two most important blocks of PreciseFPGA: (1) function detector and feature predictor (Section B.3.3) and (2) resource and power predictor (Section B.3.4).

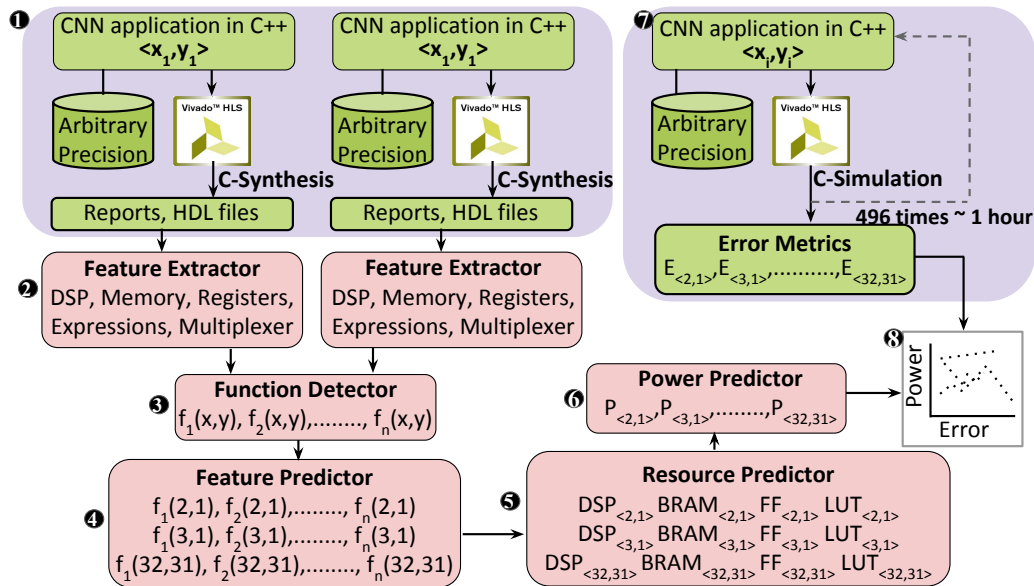


Figure B-3: Overview of PreciseFPGA.

B.3.1 Overview

The C-Synthesis results of a C++ application obtained for two fixed-point precision configurations (❶ in Figure B-3) are fed through a *feature extractor* block (❷ in Figure B-3). We extract all resource and timing-based features from the synthesis and the implementation reports. The *function detector* (❸ in Figure B-3) uses the features extracted from the feature extractor to calculate offsets $\hat{\mathbf{x}}$, $\hat{\mathbf{y}}$, and $\hat{\mathbf{x}} - \hat{\mathbf{y}}$ of each instance ¹

¹Instance refers to the functions or operators in a design.

for each of the two fixed-point configurations. We compare the calculated offsets of the two configurations to find a common offset function. This common function represents the relation of bitwidth with an instance.

The *feature predictor* block (④ in Figure B-3) uses the identified common functions to generate the feature values for all instances of all possible fixed-point configurations $\langle x_i, y_i \rangle$. The resource predictor block (⑤ in Figure B-3) uses the features generated from the feature predictor to predict the post-implementation resource utilization for all possible fixed-point configurations. The *power predictor* block (⑥ in Figure B-3) uses the resource estimates obtained from the resource predictor to obtain the post-implementation power prediction using a regression model called the Support Vector Regression (SVR)[448]. The power predictor output along with the C-Simulation (⑦ in Figure B-3) is used to obtain a Pareto-optimal fixed-point configuration (⑧ in Figure B-3) with respect to power and error in an inference task. We further explain the above steps in the following sections.

B.3.2 HLS-based Features

The Xilinx HLS tool transforms a C/C++ specification into a register transfer level (RTL) implementation using a C-Synthesis step. Our framework uses the reports and the RTL source code (generated in the C-Synthesis step of the FPGA design cycle) to predict the post-implementation resource and power consumption.

We mention the important components of the HLS report in Table-B.1. A C-Synthesis report captures the variables mapped to FPGA resources under five main categories (“Comp”). First, **Memory** represents instances mapped to block RAM (BRAM) or slice logic (i.e., FF and LUT) and is reported along with its three features, i.e., depth or words, width or bits, and banks. The bank depends on the memory ports. Second, **Expression (Expr)** represents the variables responsible for logical and arithmetic operations and lists their operand widths and operation type. Third, **Multiplexer (MUX)** includes the selector instances with the number of inputs and input bitwidth. Fourth, **DSP** describes multiply-accumulate (MAC) and multiplication (MUL) operation instances above a certain operand-width that are mapped to DSP slices. The operand-width of a DSP instance is extracted from the respective RTL source code generated from the C-Synthesis step. Fifth, **Register (Reg)** is implemented using flip-flop and stores the results of a look-up table.

Precision dependent features: The features expected to change with change in precision type are marked with ✓ and others with ✗ in the *Status* column of Table-B.1. For example, as mentioned above, for the Memory component, HLS reports define memory in terms of depth, width, and banks. A change in the fixed-point precision would affect the memory width only because the depth depends on the array size and banks depend on the access type (i.e., a single-port or a double-port). Thus, the

Table B.1: Components and their features extracted from the C-Synthesis report.

Comp	Feature1	Feature2	Feature3	Status	FF	LUT	BRAM	DSP
Memory	depth	width	bank	✗, ✓, ✗	✓	✓	✓	✗
Expr	op1 width	op2 width	op type	✓, ✓, ✗	✗	✓	✗	✓
MUX	ip size	bits	total bits	✗, ✓, ✓	✗	✓	✗	✗
DSP	op1 width	op2 width	op3 width	✓, ✓, ✓	✓	✓	✗	✓
Reg	variable bits	const bits	N/A	✓, ✗, ✗	✓	✗	✗	✗

Status has ✗ for depth and bank, and ✓ for width. In FPGA, we can use BRAM or LUT and FF to implement the memory component. Thus, these components have a ✓ while DSP is marked with ✗ as we cannot use DSP to implement a memory.

B.3.3 Function Detector and Feature Predictor

We require C-Synthesis reports of only two fixed-point configurations (for example $\langle x_1, y_1 \rangle$ and $\langle x_2, y_2 \rangle$) to determine if a feature is fixed or varies with a change in precision. As mentioned before, an instance that is a part of the control-flow, such as loop count, is expected to remain constant, whereas an instance involving fixed-point operands would change with a change in data width precision.

The features extracted for an application with precision configurations $\langle x_1, y_1 \rangle$ and $\langle x_2, y_2 \rangle$ are given as an input to the function detector block (③ in Figure B-3). The function detector uses two steps. In the first step, the offset between the feature *value*² and *bitwidth*, *integer*, and *fraction* part of a fixed-point representation for both $\langle x_1, y_1 \rangle$ and $\langle x_2, y_2 \rangle$ configurations is calculated separately. This offset captures the relation between feature value and different components of the number representation, i.e., *bitwidth*, *integer*, and *fraction*. The calculated offsets are mentioned under columns $\hat{\mathbf{x}}$, $\hat{\mathbf{y}}$, and $\hat{\mathbf{x}} - \hat{\mathbf{y}}$ for each of the two configurations. We obtain these offsets by subtracting *bitwidth*, *integer*, and *fraction* part of a fixed-point representation from the obtained *Value* of an instance’s feature, respectively.

To understand the relationship between an instance of an application and the *bitwidth*, *integer*, and *fraction* part of a fixed-point representation, we need to ensure that the two chosen fixed-point configurations follow the conditions given by Equation B.3

$$x_1 \neq x_2 \quad \text{and} \quad y_1 \neq y_2 \quad \text{and} \quad (x_1 - y_1) \neq (x_2 - y_2) \quad (\text{B.3})$$

In the second step, the offsets obtained in the first step for two different fixed-point precision configurations are compared to find a common matching offset function, which we refer to it as *function detected*. In the case of a match, the *function detected*

²Value refers to HLS reported output of an instance’s feature, which belongs to a specific component (see Table B.1) i.e, memory, expression, multiplexer, DSP, or register.

is replaced by the common offset function plus the offset’s calculated value. In case there is no match, the *function detected* is replaced with 1, which implies that an instance’s feature is independent of the chosen data-width and, therefore, remains constant for all the fixed-point configurations.

Example: In Table B.2 we explain the above step using the instances captured from the HLS C-Synthesis report for $\langle 17, 8 \rangle$ and $\langle 16, 10 \rangle$ fixed-point configurations for LeNet-5. We report the values achieved by HLS for different features under the *Value* column for each precision. In the case of the *Expression* component with instance name *out_V_d0*, we have two features, op1-width and op2-width. First, we calculate the offsets for each feature of the *Expression* component. For each fixed-point precision configuration, we mention the calculated offsets under \hat{x} , \hat{y} , and $\hat{x} - \hat{y}$. Second, we compare the offsets obtained for the two fixed-point precision configurations to find a common function. In the case of *op1-width*, the offsets obtained for $\langle x_1, y_1 \rangle$ are different than the offsets obtained for $\langle x_2, y_2 \rangle$. However, for *op2-width*, \hat{x} with a value of -1 is common between the offsets of the two precision configurations. Thus, the function detected for op1-width and op2-width features are 1 and $\hat{x} - 1$, respectively.

Table B.2: Example of an HLS C-Synthesis report with outputs from function-detector and feature-predictor.

Comp	Instance Name	Feature Name	$\langle x=17, y=8 \rangle$				$\langle x=16, y=10 \rangle$				Function Detected	Feature Predicted					
			Value	\hat{x}	\hat{y}	$\hat{x} - \hat{y}$	Value	\hat{x}	\hat{y}	$\hat{x} - \hat{y}$		$\langle 2,1 \rangle$	$\langle 3,1 \rangle$	$\langle 3,2 \rangle$	$\langle 4,1 \rangle$	$\langle 4,2 \rangle$	$\langle 4,3 \rangle$
Memory	C2_weights_V_0_U	width	9	-8	+1	0	6	-10	-4	0	$\hat{x} - \hat{y}$	1	2	1	3	2	1
Exr	out_V_d0	op1 width	1	-16	-7	-8	1	-15	-9	-5	1	1	1	1	1	1	1
		op2 width	16	-1	+8	+7	15	-1	+5	+9	$\hat{x}-1$	1	2	2	3	3	3
MUX	p_Val2_40_reg	bits	17	0	+9	+8	16	0	+6	+10	\hat{x}	2	3	3	4	4	4
DSP	mnet_mac_mmladd	op1 width	16	-1	+8	+7	15	-1	+5	+9	$\hat{x}-1$	1	2	2	3	3	3
		op2 width	10	-7	+2	+1	7	-9	-3	+1	$\hat{x} - \hat{y} + 1$	2	3	2	4	3	2
Reg	C2_weights_V_0_reg	bits	9	-8	+1	0	6	-10	-4	0	$\hat{x} - \hat{y}$	1	2	1	3	2	1

In the *feature prediction* phase, we use the *function detected* to find the value of an instance’s feature for all possible fixed-point precision configurations. In Table B.2, we demonstrate the feature prediction for six different fixed-point configurations ($\langle 2,1 \rangle$, $\langle 3,1 \rangle$, $\langle 3,2 \rangle$, $\langle 4,1 \rangle$, $\langle 4,2 \rangle$, and $\langle 4,3 \rangle$). For each of these configurations, to obtain the feature value of an instance, we replace $\langle x,y \rangle$ values of a configuration into the *function detected*.

B.3.4 Resource and Power Predictor

The resource predictor step uses the feature values generated from the feature predictor (4 in Figure B-3) to predict the post-implementation DSP, BRAM, FF, and LUT resource utilization for all possible fixed-point configurations. For each FPGA resource type, we employ a different estimation technique based on the feature complexity.

BRAM: Our target Xilinx FPGA board [440] has block RAM resources that store up to 36-Kbits of data and can be configured as either two independent 18-Kbits RAM or one 36-Kbit RAM. Each 18-Kb block RAM can be configured as a 16K x 1, 8K x 2, 4K x 4, 2K x 9, 1K x 18 or 512 x 36 in dual-port mode. For a given memory instance with width, depth, and banks, our BRAM resource predictor finds the possible BRAM utilization for all possible combinations of the configuration. The BRAM configuration requiring the lowest cascade depth and the lowest BRAM utilization is selected. This process is repeated for all the BRAM instances for the particular fixed-point configuration. Total BRAM count is obtained as the sum over all the BRAM instances.

FF and LUT: FF and LUT estimates vary non-linearly with the feature values. Therefore, for the prediction of the FF and LUT, we use SVR (Support Vector Machine) [448], which is a simple non-linear machine learning algorithm, to map HLS estimates to post-implementation FF and LUT count. We use the calculated FF, and LUT estimates from the feature predictor step as features to train our SVM model.

DSP: As discussed in Section B.3.2, MAC and MUL operations above a certain threshold are mapped to the dedicated DSP slices on an FPGA. This threshold value is extracted from the RTL generated in the C-Synthesis step of the HLS design cycle. There is a linear mapping between the number DSP slices a particular MAC, or MUL operation requires and the operand-width. Therefore, we use operand-width to estimate post-implementation DSP utilization.

Power Prediction: The power prediction step (6 in Figure B-3) uses the resource estimates obtained from the resource predictor to obtain the post-implementation power prediction for a certain fixed-point configuration. We again use a simple SVM [448] model for power prediction because of the non-linearity between the resource utilization and power consumption. We train a separate SVM-based model for each FPGA resource type, i.e., BRAM, FF, LUT, and DSP.

B.4 Evaluation

We evaluate our proposed method with LeNet-5 [250, 339]-based CNN architecture. A CNN model consists of a combination of convolution layers, activation layers, fully-connected layers, and pooling layers [14]. We vary the number of layers and dimensions of each layer of a CNN model to obtain 8 different NN architectures that have an impact on all the FPGA resource types, i.e., FF, LUT, BRAM, and DSP. Table-B.3 shows the number of parameters of each CNN model used in our evaluation. We use the Xilinx Vivado HLS 2019.1 [481] tool to implement CNN designs targeted for the Zynq-7z020 [440] edge FPGA-based device. To predict the post-implementation resources and power utilization of a particular model, we use that specific model as

the test set and exclude that model from the training and validation set. From the remaining set of 7 models, we randomly choose 6 models for training and 1 model for validation.

B.4.1 Resource and Power Prediction

For each model, we obtain C-Synthesis results for only two fixed-point configurations. We feed these results to our PreciseFPGA framework and obtain power prediction results for all the possible configurations of a model.

In Table B.3, we mention the total runtime and error results. The time taken to predict power and resource utilization for all possible fixed-point configurations using PreciseFPGA and Xilinx HLS [481] are mentioned under the columns *Total Runtime (PreciseFPGA)* and *Total Runtime (HLS)*, respectively. Total time taken by PreciseFPGA consists of the prediction time of making predictions for all possible fixed-point configurations (496 configurations) and runtime for C-Synthesis [483] for two distinct precision configurations. We calculate the *speedup* in time obtained using PreciseFPGA instead of the exhaustive search (using the HLS tool) in the column *Total Runtime (Speedup)*. We also mention the average prediction error for resources (FF, BRAM, LUT, and DSP) and power estimates. We calculate the prediction error by averaging the relative error with respect to HLS post-implementation estimates.

We achieve an average prediction error of 4.40%, 4.30%, 4.04%, and 4.21% for FF, LUT, BRAM, and DSP, respectively. We observe PreciseFPGA is, on average, 674× faster than an exhaustive search using HLS. For power prediction, we achieve an error of less than 4% for all the considered models.

Table B.3: Model runtime and resource prediction results.

Model	# Parameters	Total Runtime (hrs)			Average Relative Prediction Error (%)				
		HLS	PreciseFPGA	Speedup	FF	LUT	BRAM	DSP	Power
1	16278	223	0.205	1087	3.93	4.93	3.18	4.73	2.71
2	42704	107	0.213	502	4.26	3.96	2.83	4.99	3.07
3	14758	103	0.204	505	4.65	4.24	5.44	2.89	2.63
4	14822	115	0.219	525	4.42	3.80	5.91	3.25	2.42
5	9222	111	0.221	502	3.54	4.19	6.53	3.43	2.64
6	36004	132	0.227	581	4.04	4.19	2.84	4.95	3.41
7	24114	119	0.232	512	6.07	4.14	2.75	4.52	3.68
8	16498	239	0.203	1177	4.24	4.92	2.89	4.92	3.72
Average				673.8	4.40	4.30	4.04	4.21	3.03

B.4.2 Pareto Curve Generation

We use the MNIST [459] dataset to obtain the error in a CNN model’s inference task under test while using 32-bit floating-point baseline and 496 possible fixed-point

configurations. Figure B-4 shows the plot for the predicted power using PreciseFPGA and the relative error for each model. For the prediction error, we calculate the change in relative accuracy of fixed-point implementation compared to the baseline floating-point implementation. The power consumption estimated by PreciseFPGA and HLS tool is shown as *Predicted* and *Actual*, respectively. We also show the performance of baseline 32-bit floating-point (*Float*) as well as 16-bit floating point (*Half*) in the plot. The figure also highlights the entire search space (496 configurations) using the points labeled as *All*.

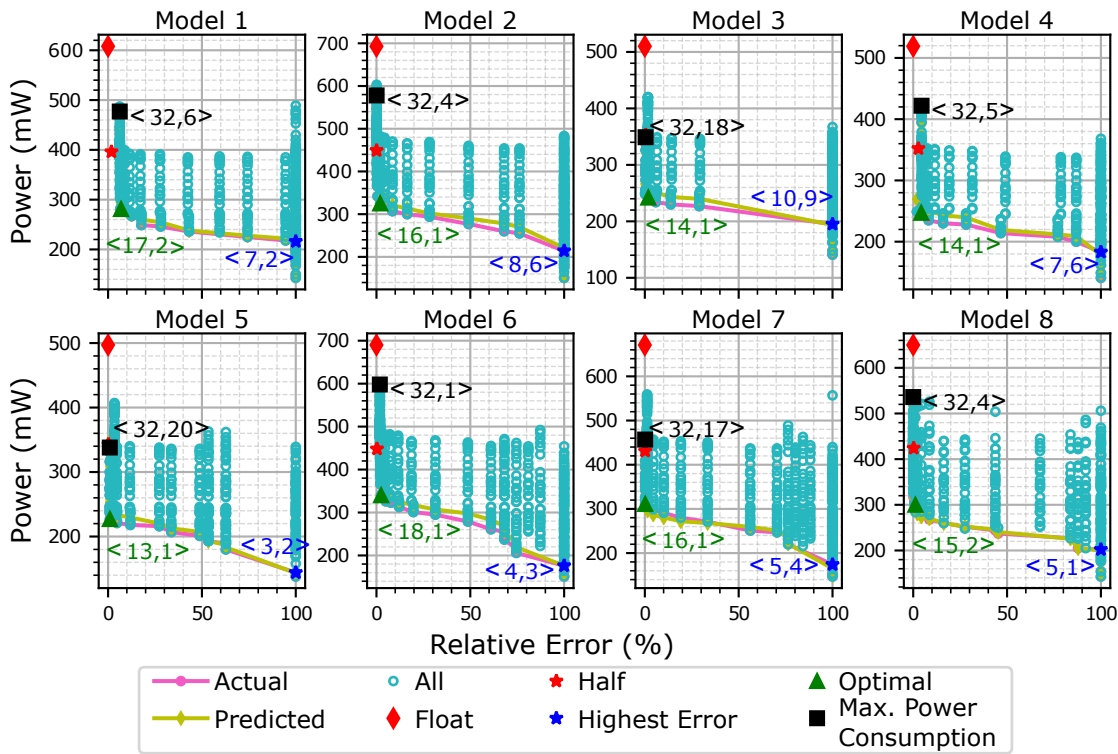


Figure B-4: Pareto-Optimal plot of power vs relative error for 8 different architectures of LeNet-5-based [250, 339] CNN model.

From the Pareto curve, we make three observations. First, the *Predicted* Power faithfully follows the trend of the *Actual* Power. Second, after attaining optimal configuration, in terms of power consumption and error, an increase in bitwidth does not improve the error but drastically increases the power consumption. Third, the optimal configuration enables greater saving in power consumption than the floating-point implementation and higher bitwidth fixed-point configurations.

B.5 Related Work

In this section, we discuss related work that makes use of prediction and analytic-based techniques to overcome the productivity issue with FPGAs.

ML-based. HLSPredict [346] estimates pre-implementation resource utilization using program-counters (PC) available in off-the-shelf CPU-based processors. As the PC of a processor is used, arbitrary precision cannot be evaluated using this method. Additionally, pre-implementation resource estimation deviates dramatically compared to post-implementation results [101]. Works such as [101], Pyramid[297], and Minerva [128] predict post-implementation resource utilization using an ML framework. However, these frameworks require C-Synthesis [483] run results for all possible fixed-point configurations, which is a time-consuming process.

Analytic-based. Frameworks such as Lin-Analyzer [535] and HLSCOPE+ [91] predict performance metrics for applications using an analytic-based approach. These works do not take into the effect of different fixed-point precision configurations. FINN [135] targets quantized NNs to generate dataflow style architectures for the network. However, these frameworks do not predict post-implementation resource utilization or power prediction for all possible fixed-point configurations.

ApproxFPGAs [380] is an ML framework that analyzes ASIC-based approximate circuits (ACs) to determine a set of Pareto-optimal FPGA-based designs with respect to power and performance. This framework is specialized only for ASIC-based ACs. Hence, it cannot be generalized for other applications. Additionally, this framework does not predict post-implementation DSP, BRAM, LUT, and FF utilization.

Compared to PreciseFPGA, none of the above frameworks incorporates the resource bound of a particular FPGA device. For example, if BRAM or DSP is exhausted, how can it be mapped to the slice logic is a question not answered by those frameworks. Hence, to our knowledge, PreciseFPGA is the only framework that: (1) predicts post-implementation power and resource utilization for all fixed-point configurations with only two C-Synthesis [483] run results, and (2) PreciseFPGA takes into account the heterogeneity of FPGA by mapping the logic to other possible components when any of the components is exhausted.

B.6 Conclusion

In this appendix, we propose PreciseFPGA, a resource and power prediction framework for the exploration of fixed-point representation on an FPGA. PreciseFPGA uses high-level synthesis results for only two fixed-point configurations to predict the post-implementation power and resource utilization for all possible fixed-point configurations. While predicting the post-implementation results,

PreciseFPGA takes into account the effect of resource saturation and provides a Pareto-optimal configuration in terms of power consumption and error. We show that PreciseFPGA can provide accurate estimates of resource utilization and power consumption with up to three orders of magnitude reduction in design space exploration time. In the future, we aim to extend PreciseFPGA to quantize the activations of a neural network and further examine our approach for other application domains.

Appendix C

Other Works of the Author

In addition to the works presented in this thesis, I have also contributed to several other research works done in collaboration with students and researchers at ETH, IBM, CMU, and TUE. In this section, I briefly overview these works.

In a recent work [430], we demonstrate the capability of a data-centric near-HBM FPGA-based accelerator for pre-alignment filtering step in genome analysis. Compared to our previous work on weather prediction, we see that genome analysis is even more memory-bounded and can significantly benefit from near-memory acceleration. We map the pre-alignment filtering algorithm to an HBM-based FPGA architecture and create a heterogeneous memory hierarchy using on-chip URAM, BRAM, and on-package HBM. We perform in-depth scalability analysis for both HBM and DDR4-based FPGA boards and show the memory bottleneck of the pre-alignment phase of genome analysis on a state-of-the-art IBM POWER9 system. Our analysis shows that our HBM-based pre-alignment filtering design provides a $20.1\times$ higher speedup and $115\times$ higher energy efficiency than a 16 cores IBM POWER9 system.

Casper [110] designs a *near-cache* accelerator that improves the performance and energy efficiency of stencil computations by eliminating the need to transfer data to the processor for computation while minimizing the unnecessary data movement within the cache hierarchy as well. To this end, we propose Casper, a novel hardware/software codesign approach specifically targeted at stencil computations. We minimize data movement by placing a set of stencil processing units (SPUs) near the last-level cache (LLC) of a traditional CPU architecture and provide novel mechanisms to introduce data mapping changes and support unaligned loads needed for high-performance stencil computations. Computation is mapped to SPU so that each SPU operates on the data that is located in the closest LLC slice. Thus, we can reduce the overall data access latency and energy consumption while matching the compute performance to the peak bandwidth of the LLC.

In our work [394], we propose a highly efficient and flexible interconnect network

capable of running the entire COSMO model on a CGRA-based accelerator. The central part of the COSMO model (called dynamical core or *dycore*) performs ~ 80 compound stencil computations. Our algorithm is able to route the connections in the weather stencil kernels while reducing the delay of the longest wire segment. Further, we propose a post routing optimization to improve the placement of the weather stencil kernels' operations in the COSMO CGRA-based accelerator to improve the routing results with minimum time complexity. Our evaluation shows that the proposed techniques achieve 50% lower delay and 12% lower power than a baseline CGRA switch box-interconnect network.

TDO-CIM [473] proposes a compiler for computation-in memory (CIM). Computation in-memory is a promising non-von Neumann approach aiming at completely diminishing the data transfer to and from the memory subsystem. In recent years, several CIM-based architectures have been proposed. However, the compiler support for such architectures is still lagging. In this work, we close this gap by proposing an end-to-end compilation flow for CIM based on the LLVM compiler infrastructure. Our compiler automatically and transparently invokes a CIM accelerator without any user intervention. Therefore, enabling legacy code to exploit CIM-based acceleration. We develop a light-weight run-time library for data allocation, transfer, and execution of computational tasks on a CIM device. We evaluate our approach using an open-source simulation environment based on the Gem5-simulator, where we model a host CPU connected to a CIM accelerator.

Agile auto-tuning [114] explores the possibility of automatically guiding the auto-tuning of an overlay architecture for different transprecision settings by leveraging knowledge from hardware experience. By adopting the concept of agile development, we built a pipeline of engineering tasks that support the auto-tuning process. Instead of eliminating the overlay hardware design space with pruning techniques, we propose a technique that builds a prediction model to quantify the impact of a hardware design choice towards an optimization goal. We show that the features with the highest impact differ for different precisions.

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Curriculum Vitae

Gagandeep was born in Chandigarh, India, in 1992. He received a joint M.Sc. degree with distinction in Integrated Circuit Design from Technische Universität München (TUM), Germany, and Nanyang Technological University (NTU), Singapore in 2017. He joined Eindhoven University of Technology, Netherlands, in 2017 to pursue a Ph.D. degree as a part of the Marie Skłodowska-Curie EID (Ph.D.) Program under the supervision of Prof. Henk Corporaal. From June 2018 to January 2020, he was a Predoctoral Researcher at IBM Research Zurich, Switzerland, in the group of Dr. Christoph Hagleitner. Since January 2020, he has been an Academic Guest in Prof. Onur Mutlu's group at ETH Zurich, Switzerland. He is passionate about FPGA design, computer architecture, and applied machine learning with skills in both hardware and software design.