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FPGA-Based Implementation and Synchronization Design of a New Five-Dimensional Hyperchaotic System

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Abstract: Considering the security of a communication system, designing a high-dimensional complex chaotic system suitable for chaotic synchronization has become a key problem in chaotic secure communication. In this paper, a new 5-D hyperchaotic system with high order nonlinear terms was constructed and proved to be hyperchaotic by dynamical characterization characteristics, the maximum Lyapunov exponent was close to 2, and there was a better permutation entropy index, while a valid chaotic sequence could be generated in three cycles in the FPGA (Field Programmable Gate Array)-based implementation. A multivariable nonlinear feedback synchronous controller based on FPGA was proposed to design and implement synchronization of high order complex hyperchaotic systems. The results show that the error signal converged to 0 rapidly under the effect of the non-linear feedback synchronous controller. This lays the foundation for the synchronization of high order complex chaotic systems.

Keywords: complex chaotic system; nonlinear feedback control; chaotic synchronization; FPGA; secure communication

1. Introduction

With the increasing demand for information security, secure communication technology research has become particularly important, and the application of chaos theory in secure communication has attracted increasing attention. Chaotic synchronization is a significant part of chaotic secure communication research. The transceiver system for chaotic secure communication has been extended from a low-dimensional chaotic system to a high-dimensional chaotic system. Creating high-dimensional complex chaotic systems and achieving chaotic synchronization have become the key in the research of chaotic secure communication.

In 1963, the American meteorologist E. N. Lorenz observed chaos in his atmospheric studies, opening the way for future exploration of chaos [1]. Chaos has favorable randomness and it is widely used in various fields such as secure communication [2], medical image processing [3–5], biomedical science [6,7], and finance [8–10]. In 1979, Otto Rössler proposed the first hyperchaotic system with two or more attractors and positive Lyapunov exponents, its phase orbitals can be separated in multiple directions, and the algebraic structure and dynamical behavior are more complex, confidential, and impenetrable than ordinary low-dimensional chaotic systems, with greater potential for research and development.

In [11], Chengqun zhou et al. constructed a four-dimensional hyperchaotic system based on the Lorenz system with the properties of stability, periodicity, multiple coexisting attractors, multiplicative period, and Hopf bifurcation, the maximum Lyapunov exponent being 0.4934. Li et al. proposed a new four-dimensional hyperchaotic system with exponential terms, the basic dynamical properties and chaotic behavior of the new attractor were analyzed. The results showed that the new hyperchaotic system has an

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equilibrium point or a single equilibrium point. The maximum Lyapunov exponent of the hyper-chaotic system is 0.1782 [12]. Sundarapandian et al. proposed a new multi-stable four-dimensional hyperchaotic system and confirmed the special properties of the new system such as multi-stability of coexisting attractors by bifurcation diagram, phase diagram, and dynamics analysis [13]. Bouteghrine et al. proposed a new multidimensional chaotic system with multiple parameters and nonlinear terms, and a two-phase algorithm was proposed to study the chaotic behavior using bifurcation and Lyapunov exponential theory [14].

Currently, there is little research on high-dimensional chaotic systems with high order terms. Meanwhile, the maximum Lyapunov exponent of most hyperchaotic systems does not exceed 1. For hyperchaotic systems, the larger the Lyapunov exponent, the better the performance of the system. Thus, it is necessary to investigate high-dimensional, high order hyperchaotic systems with larger Lyapunov exponents.

Compared with traditional programmable devices, FPGA (Field Programmable Gate Array) is of great interest to engineers because of the excellent properties such as design flexibility, high integration, and high-speed parallel processing, and is gradually occupying an increasing share in today's digital information market. Yuan et al. implemented a chaotic circuit for a new Chen-like system by introducing the product and square terms of variable coefficients and using 32-bit fixed-point operations with the help of the Quartus II 13.0 platform from ALTERA [15]. Sun et al. similarly used the Lorenz system as the object and completed the chaotic system with a modular design approach in the form of data processing by floating-point operations through a hardware description language [16]. Xue et al. completed a synchronization and corresponding confidential video communication system based on the hyperchaotic system using FPGA [17]. Liu designed and implemented the computing architecture of the Qi hyperchaotic system based on FPGA technology, which required 27 clock cycles to generate a new valid chaotic iteration value [18]. Tang et al. designed and implemented the computing architecture of the Chen hyperchaotic system based on FPGA technology, which required five clock cycles to generate a new valid chaotic iteration value [19]. In the investigation of FPGA-based implementation of chaotic systems, numerous clock cycles to generate a valid chaotic sequence, in the application to the field of secure communication, reduce the efficiency of the operation of encryption and decryption of plaintext data, thus reducing the overall efficiency.

Chaotic systems are widely used in the field of secure communication because of their high initial value sensitivity and unpredictability, but they have also been considered unsynchronizable for a long time. It was not until 1990 that T.L. Pecora and L.M. Carroll first proposed drive-response synchronization and observed synchronization in circuits, opening the door for the study of chaotic synchronization methods and their applications [20].

Several chaotic synchronization methods have been proposed, including adaptive synchronization control [21], backstepping control [22], nonlinear feedback control [23], and drive-response synchronization control [24]. Moon Sungju et al. investigated the selfsynchronization problem of high-dimensional Lorenz systems and showed that satisfactory synchronization results could not be obtained when the dimensions of the drive and response systems were different [25]. In [26], Dan Li et al. used a drive-response synchronization control method to achieve two 6-vortex chaotic attractor synchronizations based on the recent multi-vortex chaotic attractor synchronization theory. Liu Yangzheng et al. constructed a new four-dimensional hyperchaotic Liu system based on the three-dimensional Liu system. The chaotic synchronization of this hyperchaotic system was achieved by using a nonlinear feedback control method. Based on the stability theory of the system, the structure of the nonlinear feedback controller and the range of values of the feedback control gain when the system reaches chaotic synchronization were obtained [27]. Compared with other synchronization methods, the nonlinear feedback synchronization control does not need to decompose the system and is more suitable for complex high-dimensional chaotic systems.

In this paper, a five-dimensional chaotic system with cubic nonlinear terms is proposed and implemented by FPGA. The Lyapunov exponential spectrum, bifurcation diagram, permutation entropy, and heterogeneity of the new chaotic system are analyzed and the resulting sequences are tested with the NIST SP800-2 standard. A new five-dimensional hyperchaotic system based on FPGA is designed and implemented. In conjunction with the Lyapunov stability theory, a multivariate non-linear feedback synchronous controller is designed and analyzed. Finally, the FPGA hardware design is completed and validated at the board level using the Vivado development platform and the ARTIX-7 development board.

The subsequent sections of this paper are organized as follows: Section 2 describes the new 5-D hyperchaotic system used in this paper. The proposed non-linear feedback synchronous control by FPGA is described in Section 3. Section 4 presents the simulation results. Conclusions are drawn in Section 5.

2. New 5-Dimensional Hyperchaotic System and Its Dynamical Properties

2.1. Theory of Hyperchaotic System

In 1963, in his work on the effects of atmospheric convection on climate, the American meteorologist Lorenz used Newtonian mechanics to establish a set of nonlinear differential equations, which can be expressed as follows:

$$\dot{\mathbf{x}} = \alpha(\mathbf{y} - \mathbf{x})$$

$$\dot{\mathbf{y}} = \gamma \mathbf{x} - \mathbf{y} - \mathbf{x}z$$

$$\dot{\mathbf{z}} = \mathbf{x}\mathbf{y} - \beta z$$
(1)

In 2005, Qi et al. proposed the Qi hyperchaotic system, which contains three subsystems, Lorenz hyperchaotic, Chen hyperchaotic and Lü hyperchaotic, which can produce more complex dynamical properties with attractors showing biplanarity and a larger trajectory traversal range in phase space [24]. Qi hyperchaotic can be expressed as:

$$\dot{\mathbf{x}} = \alpha(\mathbf{y} - \mathbf{x}) + \mathbf{y}\mathbf{z}\mathbf{w}$$
$$\dot{\mathbf{y}} = \beta(\mathbf{x} + \mathbf{y}) - \mathbf{x}\mathbf{z}\mathbf{w}$$
$$\dot{\mathbf{z}} = -\gamma \mathbf{z} + \eta \mathbf{x}\mathbf{y}\mathbf{w}$$
$$\dot{\mathbf{w}} = -\sigma \mathbf{w} + \mathbf{x}\mathbf{y}\mathbf{z}$$
(2)

where x, y, z, w are state vectors. When $\alpha = 50$, $\beta = 4$, $\gamma = 13$, $\sigma = 20$, $\eta = 4$, there exists two positive Lyapunov exponents and the system exhibits a hyperchaotic state.

By simultaneously adding dimensionality and nonlinear terms to this system, this paper proposes a new 5-D chaotic system with cubic nonlinear terms, which can be defined as:

$$\dot{x} = ay - bx + cyz + yzw$$

$$\dot{y} = dx + ly - xz - fv - xzw$$

$$\dot{z} = -hz + y^{2} + xyw$$
 (3)

$$\dot{w} = -jyz - pw + xyz$$

$$\dot{y} = k(x + y)$$

where x, y, z, w, v represent state vectors and a, b, c, d, l, f, h, j, p, k represent constant parameters.

2.2. Dynamical Properties Analysis

2.2.1. Dissipativity

In relation to system (3) it is known that:

$$\nabla V = \frac{\partial \dot{x}}{\partial x} + \frac{\partial \dot{y}}{\partial y} + \frac{\partial \dot{z}}{\partial z} + \frac{\partial \dot{w}}{\partial w} + \frac{\partial \dot{v}}{\partial v} = -b + l - h - p + k$$
(4)

When $\nabla V = -b + 1 - h - p + k < 0$, the chaotic system is dissipative and converges exponentially, the rate of phase space convergence can be calculated to be:

$$\frac{dv}{dt} = -(b-l+h+p-k)V$$

$$V = e^{-(b-l+h+p-k)}\frac{dv}{dt}$$
(5)

Namely, this chaotic system converges to a volume V_0 at moment t to $e^{-(b-1+h+p-k)}$. When time t tends to infinity, all the orbits of the system converge to a subset of zero measure, i.e., generating chaotic attractors.

2.2.2. Lyapunov Exponents and Bifurcation Diagram

Taking the parameters as a = 14, b = 0.5, c = 2, d = 2, l = 6, f = 4.5, h = 3, j = 0.5, p = 15, k = 0.423, for the initial value of the chaotic system $(x_0, y_0, z_0, w_0, v_0) = (1, 0.25, 2, -1, 1.5)$, the Lyapunov exponents of the system can be obtained as $LE_1 = 1.9380$, $LE_2 = 0.1391$, $LE_3 = -0.0084$, $LE_4 = -2.3637$, $LE_5 = -11.1328$, indicating the chaotic system is a hyper-chaotic system. The partial phase diagrams of this hyperchaotic system are shown in Figure 1.

The Poincaré cross section converts the trajectory of a dynamical system to its intersection with the cross section to be studied. The continuous trajectory of the phase space is presented as some discrete points in the cross-section, the changes of the system morphology can be judged by these discrete points: the quasi-periodic motion is presented as a closed curve; the periodic motion is presented as a small number of discrete points; the chaotic motion is presented as aggregated and dense points. Figure 2 shows the x-y cross section selection at z = 5. It can be observed that the points are clustered and dense, indicating that the system is in a hyperchaotic state.





Figure 1. Phase diagrams of a hyperchaotic system. (a) Phase diagram of the x-y plane. (b) Phase diagram of the x-z plane. (c) Phase diagram of the x-w plane. (d) Phase diagram of the x-v plane. (e) Phase diagram of the y-z plane. (f) Phase diagram of the y-w plane. (g) Phase diagram of the z-v plane. (h) Phase diagram of the z-w plane.





Such that a = 14, b = 0.5, c = 2, d = 2, l = 6, f = 4.5, h = 3, j = 0.5, p = 15, $0.2 \le k \le 1$, for the initial value $(x_0, y_0, z_0, w_0, v_0) = (1, 0.25, 2, -1, 1.5)$, Figures 3 and 4 depict the variation of the Lyapunov exponent with the parameter k and the corresponding bifurcation diagram respectively. With the increase of k, the attractor exhibits a different form. For k = -0.095, one Lyapunov exponent is equal to zero, and the rest of the Lyapunov exponent is negative, representing that the attractor is in the form of a periodic attractor. For k = 0.055, there is a positive Lyapunov exponent and there exists a Lyapunov exponent equal to zero, indicating that the system is chaotic. For k = 0.423, there are two positive Lyapunov exponents at this point, suggesting that the system is hyperchaotic. The bifurcation diagram also shows the system switching between the periodic, chaotic, and hyperchaotic state with the change of k. The specific values are shown in Table 1. The corresponding three-dimensional phase diagrams of the system are shown in Figure 5.



Figure 3. Spectrum of Lyapunov exponents.



Figure 4. Bifurcation diagram of x with k.

 Table 1. Lyapunov exponents and the corresponding attractor morphology.

k	LE1	LE ₂	LE3	LE ₄	LE5	Attractor Morphology
-0.095	0.0137	-0.0810	-0.9829	-5.0398	-5.0774	Periodic attractor
0.055	0.4044	0.0064	-0.1136	-1.4236	-10.9422	Chaotic attractor
0.423	1.9380	0.1391	-0.0084	-2.3637	-11.1328	Hyperchaotic attractor



5

5

0

0

y

y



Figure 5. Phase diagrams of various attractor morphologies (**a**) x-y-z plane phase diagram of periodic attractor, (**b**) y-v-w plane phase diagram of periodic attractor, (**c**) x-y-z plane phase diagram of chaotic attractor, (**d**) y-v-w plane phase diagram of chaotic attractor, (**e**) x-y-z plane phase diagram of hyperchaotic attractor.

Table 2 shows the comparison of the maximum Lyapunov exponent of the hyperchaotic system proposed in this paper with several hyperchaotic systems in the literature. As can be seen from Table 2, the maximum Lyapunov exponent of the five-dimensional hyperchaotic system proposed in this paper is 1.9380, which is much higher than the maximum Lyapunov exponent of other hyperchaotic systems, indicating that the system proposed in this paper has a superior performance compared with other systems.

Proposal	The Maximum Lyapunov Exponent
ours	1.9380
Ref. [25]	1.0461
Ref. [26]	0.7362
Ref. [27]	1.0100
Ref. [28]	0.0044
Ref. [29]	1.0241

Table 2. Comparison of the maximum Lyapunov exponent.

2.2.3. Randomness and Initial Value Sensitivity

The NIST system test standard was proposed by the National Institute of Standardized Technology (NIST) and is widely used in sequential randomized testing. The output sequence is tested with the NIST-SP800-2 test suite and the data length is 1×10^6 bits. The significance level was determined to be 0.01. When *p*-value > 0.01, the test is qualified, and the results are shown in Table 3. It could be found that the output sequence of the new chaotic system passed the 16 NIST tests, and the results showed that the obtained sequence had good randomness.

Table 3. NIST test of proposed 5-D hyperchaotic system.

Testing Item	<i>p</i> -Value(x)	Result
Approximate Entropy	0.210398	pass
Block Frequency	0.180283	pass
Cumulative Sum	0.582341	pass
FFT	0.596701	pass
Frequency	0.645639	pass
Linear Complexity	0.151631	pass
Longest Run	0.408543	pass
NonOverlapping template	0.601890	pass
Overlapping template	0.851142	pass

Random Excursion	0.621039	pass
Random Excursions Variant	0.602752	pass
Rank	0.298427	pass
Runs	0.054103	pass
Serial1	0.200412	pass
Serial2	0.145922	pass
Universal	0.304519	pass

Initial value sensitivity is one of the characteristics of a non-linear dynamical system and a criterion for measuring the stochasticity of the system. According to the established dynamical equations, changing the initial value of the system will change the dynamical behavior dramatically. When the difference between the two initial conditions is small, the dynamic behavior will initially remain the same or behave similarly, and with the increase of time, the dynamic behavior will be significantly different.

V(t) for example, the output sequence, is shown in Figure 6a for the initial value $(x_0, y_0, z_0, w_0, v_0) = (1, 0.1, 0, 0, 0)$ and in Figure 6b for $(x_0, y_0, z_0, w_0, v_0) = (1, 0.1, 0, 0, 0.0001)$. Observing the two figures, it is clear that even if the initial value is only modified by 0.0001, the output trajectory remains similar only at the beginning, and the trajectory is completely distinct as the time and number of iterations increase. This indicates that the system has favorable initial value sensitivity.



Figure 6. Time-series diagram comparison of v(t) (**a**) $(x_0, y_0, z_0, w_0, v_0) = (1, 0.1, 0, 0, 0)$ sequence; (**b**) $(x_0, y_0, z_0, w_0, v_0) = (1, 0.1, 0, 0, 0.0001)$ sequence.

2.2.4. Permutation Entropy

The complexity of a chaotic system refers to the degree to which a chaotic sequence is close to a pseudo-random sequence using a correlation algorithm. The larger the complexity value, the closer the sequence is to a random sequence, and the higher the corresponding security. The permutation entropy algorithm belongs to one of the algorithms for calculating the complexity of a chaotic system, and the permutation entropy algorithm can be expressed as follows:

- (a) There exists a time series of length N $_{x(1),x(2),x(3),...,x(N)}$, embedding dimension m with time delay t for phase space reconstruction.
- (b) The reconstructed subsequence can be expressed as $x_{(i)}$, where $X_{(i)} = x_{(i),x_{(i+1),\dots,x_{(i+(m-1)t)}}$, and the reconstructed matrix Y is obtained, which can be expressed as:

$$Y = \begin{vmatrix} x(1) & x(1+t) & L & x(1+(m-1)t) \\ x(2) & x(2+t) & L & x(2+(m-1)t) \\ x(j) & x(j+t) & L & x(j+(m-1)t) \\ M & M & L & M \\ x(i) & x(i+t) & L & x(i+(m-1)t) \end{vmatrix}$$
(6)

where i = N - (m - 1)t, each row of the matrix Y is a reconstructed component, and there are i reconstructed components. By reordering each reconstructed component X(i) in ascending order, the column indices of the positions of the elements in the vector are obtained to form a set of symbolic sequences $S(1) = \{j_1, j_2, ..., j_m\}, l=1,2,...,i$, and $i \le m!$, thus are mapped to $\{j_1, j_2, ..., j_m\}$.

- (c) Calculating the number of occurrences of each symbol sequence divided by the total number of occurrences of m! different symbol sequences as the probability of the occurrence of that symbol sequence, it can be expressed as ${P_1, P_2, ..., P_i}$.
- (d) The entropy of the permutation of the time series can be expressed as:

$$H(m) = -\sum_{j=1}^{i} P_{j} ln(P_{j})$$
(7)

(e) where $P_i = 1/m!$, that is, each symbol has an equal probability, at this point the complexity of the time series is the highest, the permutation entropy is the largest, the permutation entropy is ln(m!), and for the convenience of representation, H(m) is normalized and expressed as follows:

$$0 \le \frac{H(m)}{\ln(m!)} \le 1 \tag{8}$$

Taking the x(t) series as an example, the proposed system time series in this paper was compared with other literature, and the results are shown in Table 4.

Hyperchaotic System	m	t	PE
Ours	3	1	0.7024
Ref. [28]	3	1	0.6841
Ref. [29]	3	1	0.5714
Ref. [30]	3	1	0.6201

Table 4. Comparison of permutation entropy value.

As can be seen from Table 4, it can be concluded that the chaotic system proposed in this paper produces a higher entropy of sequence permutation, i.e., a higher complexity of the sequence, which can be effectively applied to improve security performance in areas such as secure communication.

In summary, a five-dimensional hyperchaotic system containing three nonlinear terms is proposed. The analysis of dynamics characteristics shows that the maximum Lyapunov exponent of the system can reach 1.9380, and from the analysis of permutation entropy it can be concluded that the new hyperchaotic system has a better permutation entropy exponent of 0.7042, which indicates that its complexity is higher and the corresponding security is higher; The proposed hyperchaotic system contains five signal variables and ten system parameters, multiple signal variables and system parameters make the key space larger, and its application to the field of confidential communication and image encryption can greatly enhance the security of the system and improve the confidentiality of communication.

3. FPGA-Based Hyperchaotic Synchronization Design

3.1. Hyperhaotic Synchronization Algorithm Design

Since FPGA can only process discrete digital signals, 5-D hyperchaotic systems need to discretize. Currently, the main discretization methods comprise the Runge–Kutta and Euler discretization. The Runge–Kutta method offers higher accuracy, while the hardware implementation is more difficult and consumes more hardware resources. In contrast, the Euler discretization method provides a relatively well-balanced compromise between hardware resource consumption and accuracy. Considering the large hardware overheads associated with longer data formats, this paper adopts a 24-bit fixed-point format, of which the higher 6 bits are the integer parts, where the highest bit is the sign bit and the lower 18 bits are the fractional parts.

The Euler discrete master system can be formulated as:

$$\begin{aligned} x(n+1) &= [ay(n) - bx(n) + cy(n)z(n) + y(n)z(n)w(n)] \times T + x(n) \\ y(n+1) &= [dx(n) + ly(n) - x(n)z(n) - fv(n) - x(n)z(n)w(n)] \times T + y(n) \\ z(n+1) &= [-hz(n) + y(n)^2 + x(n)y(n)w(n)] \times T + z(n) \\ w(n+1) &= [-jy(n)z(n) - pw(n) + x(n)y(n)z(n)] \times T + w(n) \\ v(n+1) &= [k(x(n) + v(n))] \times T + v(n) \end{aligned}$$
(9)

similarly, the Euler discrete slave system can be formulated as:

$$\begin{aligned} x_{1}(n+1) &= [ay_{1}(n) - bx_{1}(n) + cy_{1}(n)z_{1}(n) + y_{1}(n)z_{1}(n)w_{1}(n)] \times T + x_{1}(n) + u_{1} \\ y_{1}(n+1) &= [dx_{1}(n) + ly_{1}(n) - x_{1}(n)z_{1}(n) - fv_{1}(n) - x_{1}(n)z_{1}(n)w_{1}(n)] \times T + y_{1}(n) + u_{2} \\ z_{1}(n+1) &= [-hz_{1}(n) + y_{1}(n)^{2} + x_{1}(n)y_{1}(n)w_{1}(n)] \times T + z_{1}(n) + u_{3} \\ w_{1}(n+1) &= [-jy_{1}(n)z_{1}(n) - pw_{1}(n) + x_{1}(n)y_{1}(n)_{1}z_{1}(n)] \times T + w_{1}(n) + u_{4} \\ v_{1}(n+1) &= [k(x_{1}(n) + v_{1}(n))] \times T + v_{1}(n) + u_{5} \end{aligned}$$
(10)

where T is the sampling period and $T = 2 \times 10^8$, x(n), y(n), z(n), w(n), v(n) represent state dynamics for the master system, and $x_1(n), y_1(n), z_1(n), w_1(n), v_1(n)$ represent state dynamics for the slave system, a, b, c, d, l, f, h, j, p, k are the parameters. The error dynamic system is obtained as:

$$\Delta e_{x} = T \times [ae_{y} - be_{x} + c(y_{1}(n)z_{1}(n) - y(n)z(n)) + y_{1}(n)z_{1}(n)w_{1}(n) - y(n)z(n)w(n)] + u_{1}$$

$$\Delta e_{y} = T \times [de_{x} + le_{y} - (x_{1}(n)z_{1}(n) - x(n)z(n)) - fe_{v} - x_{1}(n)z_{1}(n)w_{1}(n) + x(n)z(n)w(n)] + u_{2}$$

$$\Delta e_{z} = T \times [-he_{z} + (y_{1}(n) + y(n))e_{y} + x_{1}(n)y_{1}(n)w_{1}(n) - x(n)y(n)w(n)] + u_{3}$$

$$\Delta e_{w} = T \times [-j(y_{1}(n)z_{1}(n) - y(n)z(n)) - pe_{w} + x_{1}(n)y_{1}(n)z_{1}(n) - x(n)y(n)z(n)] + u_{4}$$

$$\Delta e_{v} = T \times [k(e_{x} + e_{v})] + u_{5}$$

$$(11)$$

where $e_x = x_1(n) - x(n)$, $e_y = y_1(n) - y(n)$, $e_z = z_1(n) - z(n)$, $e_w = w_1(n) - w(n)$, $e_y = v_1(n) - v(n)$, $u_i(i=1,2,3,4,5)$ is the synchronous controller. The target is to design a controller for master and slave systems such that the global synchronization holds. It means that the synchronization error converges to zero and stays in its vicinity:

$$\lim_{t \to \infty} \left\| \mathbf{e}(t) \right\| = 0 \tag{12}$$

Theorem 1. *The master system (9) and the slave system (10) can be globally synchronized by the following controller:*

$$u_{1}=x(n) - x_{1}(n) - T \times [ae_{y}+cy_{1}(n)z_{1}(n) - cy(n)z(n)+y_{1}(n)z_{1}(n)w_{1}(n) - y(n)z(n)w(n)]$$

$$u_{2}=y(n) - y_{1}(n) - T \times [de_{x}+2le_{y} - x(n)z(n)+x_{1}(n)z_{1}(n) - fe_{y}+x(n)z(n)w(n) - x_{1}(n)z_{1}(n)w_{1}(n)]$$

$$u_{3}=z(n) - z_{1}(n) - T \times [e_{y}(y_{1}(n)+y(n))+x_{1}(n)y_{1}(n)z_{1}(n) - x(n)y(n)z(n)]$$

$$u_{4}=w(n) - w_{1}(n) - T \times [j(y(n)z(n) - y_{1}(n)z_{1}(n))+x_{1}(n)y_{1}(n)z_{1}(n) - x(n)y(n)z(n)]$$

$$u_{5}=v(n) - v_{1}(n) - T \times [2ke_{y}+ke_{x}]$$
(13)

Proof of Theorem 1. Considering the Lyapunov function as:

$$V(e) = \frac{1}{2} (e_x^2 + e_y^2 + e_z^2 + e_w^2 + e_v^2) \ge 0$$
(14)

derivative of (14) can be represented as:

$$\begin{aligned} \frac{\Delta V(e)}{T} &= e_x \frac{\Delta e_x}{T} + e_y \frac{\Delta e_y}{T} + e_z \frac{\Delta e_z}{T} + e_w \frac{\Delta e_w}{T} + e_v \frac{\Delta e_v}{T} \\ &= e_x [ae_y - be_x + c(y_1(n)z_1(n) - y(n)z(n)) + y_1(n)z_1(n)w_1(n) - y(n)z(n)w(n) + \frac{u_1}{T}] \\ &+ e_y [de_x + le_y - (x_1(n)z_1(n) - x(n)z(n)) - fe_v - x_1(n)z_1(n)w_1(n) + x(n)z(n)w(n) + \frac{u_2}{T}] \\ &+ e_z [-he_z + (y_1(n) + y(n))e_y + x_1(n)y_1(n)w_1(n) - x(n)y(n)w(n) + \frac{u_3}{T}] \\ &+ e_w [-j(y_1(n)z_1(n) - y(n)z(n)) - pe_w + x_1(n)y_1(n)z_1(n) - x(n)y(n)z(n) + \frac{u_4}{T}] \\ &+ e_v [k(e_x + e_v) + \frac{u_5}{T}] \end{aligned}$$
(15)

by substituting Equation (13) into Equation (15), $\frac{\Delta V(e)}{T}$ can be obtained as:

$$\frac{\Delta V(e)}{T} = e_x \left(-be_x - \frac{e_x}{T}\right) + e_y \left(-le_y - \frac{e_y}{T}\right) + e_z \left(-he_z - \frac{e_z}{T}\right) + e_w \left(-pe_w - \frac{e_w}{T}\right) + e_v \left(-ke_v - \frac{e_v}{T}\right) = \left(-b - \frac{1}{T}\right)e_x^2 + \left(-l - \frac{1}{T}\right)e_y^2 + \left(-h - \frac{1}{T}\right)e_z^2 + \left(-p - \frac{1}{T}\right)e_w^2 + \left(-k - \frac{1}{T}\right)e_v^2 < 0$$
(16)

Since $_{\Delta V(e)/T}$ is negative definite, the error dynamics system is globally asymptotically stable according to the Lyapunov stability theorem, and the master system and slave system errors will eventually converge to zero to reach full synchronization, regardless of the initial value. \Box

3.2. FPGA-Based Hyperchaotic Synchronization Design

Figure 7 provides the top-level architecture for the hyperchaotic synchronization system. To begin with, different 120-bit keys are input for the master and the slave system, and the intermediate signals, chaos_x [23:0], chaos_y [23:0], chaos_z [23:0], chaos_v [23:0], chaos_v [23:0], are generated by the hyper_chaos_generate module. All these are transmitted to the syn_hyper_chaos module, and the synchronized sequence and error signal are output under the operation of the non-linear feedback synchronization controller in the syn_hyper_chaos module, with the system reaching full synchronization when the error signal value is 0. The individual signal definition in Figure 7 is described in Table 5.

Figure 7. Top-level architecture of the hyperchaotic synchronization system.

Table 5. Signal definition.

clk

Signal	Signal Definition
clk	The system clock
rst_n	The reset signal
key_tx [119:0]	Initial key on the transmitter
tx_valid	Transmit initial key valid signal
key_rx [119:0]	Initial key on the receiver
rx_valid	Receive initial key valid signal
syn_x/syn_y/syn_z/ syn_w/syn_ v [23:0]	The synchronised sequence
error_x/error_y/error_z/ error_w/error_v [23:0]	Sequence error

In order to prevent the multiplication result from overflowing, saturation truncation and rounding operations are required. In addition, the sign bit is also expanded to prevent data overflow when adding two data. In the hardware implementation, the multiplier consumes much more resource than the adder and subtractor. In order to reduce the number of multipliers, the parameters of the hyperchaotic system are obtained by shifting in this paper; the algorithm flow diagrams of the master system and the slave system are shown in Figures 8 and 9, where ">>" indicates a right shift operation, "+" indicates an addition operation, and " – " indicates a subtraction operation, "×" for multiplication, "round" for rounding, "saturation cut off" means saturation cut-off.

The hyper_chaos module and the syn_hyper_chaos module use the Verilog HDL to develop a state machine to implement the above operations. The workflow of the hyper_chaos module state machine is shown below.

- (1) The state machine is asynchronous reset, when the reset signal is valid, all signals are initialized, and the state converts to S0.
- (2) S0: The initial key key_tx [119:0] is assigned to chaos_x [119:96], chaos_y [95:72], chaos_z [71:48], chaos_w [47:24], chaos_v [23:0], while the output valid signal is pulled up, indicating that the output is valid at the time, the state converts to S1.
- (3) S1: Complete the shift operation and pull down the output valid signal, then the state converts to S2.
- (4) S2: When the state converts to S2, the result of S1 is added and subtracted, and the result of the operation needs to be extended by one sign bit in order to prevent the overflow of the sum. This paper completes polynomial multiplication and fractional bit processing operations in the outside of the always block; first, the characteristics of the sign bit and the truncated part to determine the need of a carry bit—if the

number is positive, the highest bit of the truncated part is 1—then it is necessary to generate a carry bit. If the number is negative, it is necessary to determine whether the highest bit of the truncated part and the other bits in addition to the highest bit have 1, if that situation exists it is not necessary to generate a carry bit. After calculating the carry bit, it is added to the number after the truncated decimal bit to complete the rounding operation, and at the same time, to prevent overflow when adding the carry bit, it is necessary to carry out a sign bit expansion, and then the state converts to S3.

(5) S3: In S2 we have completed the processing of fractional bits, in S3 we mainly deal with integer bits. We need to truncate the extra integer bits: if the part to be truncated and the highest bit after truncation is the same, that is, all 0 or all 1, then the part to be truncated is the extension of the sign bit, directly truncated; if different, the sign bit is judged, if positive, it will be changed to the maximum value that can be stored in the required format data, if negative, it will be changed to the minimum value that can be stored in the required format data. The final result is assigned to chaos_x, chaos_y, chaos_z, chaos_w, chaos_v, and then the valid signal of output is pulled up, the state converts to S1, the data is transferred to the syn_hyper_chaos system, and the set of data generation is completed.

The state machine workflow of the syn_hyper_chaos module is similar to that of the hyper_chaos and is shown below.

- (1) The state machine is asynchronous reset, when the reset signal is valid, all signals are initialized and then the state converts to S0.
- (2) S0: The initial key key_rx [119:0] is assigned to syn_x [119:96], syn_y [95:72], syn_z [71:48], syn_w [47:24], syn_v [23:0], the first output sequence is the initial key, in the second iteration, the output of the hyper_chaos module will be input to the syn_hyper_chaos module to participate in circular iteration, and then the output valid signal is pulled up, indicating that the output is valid at this time, and the state converts to S1.
- (3) S1: To complete the shift operation and pull down the output valid signal, in the syn_hyper_chaos module, the output needs to add error signals, the value of the error signal is the difference between the syn signal and the chaos signal, at this point the valid signal of error is pulled up and then the state converts to S2.
- (4) S2: When the state converts to S2, the result of S1 is added and subtracted, and the result of the operation needs to be extended by one sign bit in order to prevent the overflow of the sum. The same as the hyper_chaos module, the syn_hyper_chaos module completes polynomial multiplication and fractional bit processing operations in the outside of the always block. The valid signal of error is pulled down and the state converts to S3.
- (5) S3: In S2 we have completed the processing of fractional bits, in S3 we deal mainly with integer bits. We need to truncate the extra integer bits and assign the final result to syn_x, syn_y, syn_z, syn_w, syn_v, the valid signal of output is pulled up, and then the state converts to S1, the set of data generation is finished.

Figure 8. Algorithm flow diagram of the Master System.

Figure 9. Algorithm flow diagram of the Slave System.

4. Simulation Results

The chip model chosen for this paper is Xilinx Airtex-7 series xc7a100tfgg484-2, as shown in Figure 10. The development board model used is the Xilinx Artix-7 series AX7103 development board. Simulation is completed by vivado2019.1 and modelsim2017.4. The simulation results of the new 5-dimensional hyperchaotic system based on FPGA are shown in Figure 11. The initial key is set as 120'h040000_010000_080000_FCFFFF_060000. Compared with MATLAB simulation data, both results are consistent. It indicates that the result of the digital design of the FPGA-based chaotic system is accurate. Furthermore, it takes three clock cycles to generate a valid data which greatly improves the efficiency of the system compared with the contents of the references. Meanwhile, the modelsim simulation data were exported and the corresponding NIST tests performed, and the results are shown in Table 6. The test results show that the chaotic sequences generated by the digitized hyperchaotic system still have high randomness. The RTL view of the chaotic synchronous top-level design is shown in Figure 12.

Figure 10. Xilinx Artix-7 Series AX7103 Development Board.

🔷 clk	0	mn	กกก	ாா	ուու	ாா	ாா	ուու	ուու	ուու	nnn
🔷 rst_n	1	-									
	0400000100	04000001000	10080000fc	:ffff060000							
🔷 start	1										
⊞ 🔷 x	045c62	000000	040000	040e80	041c10	0428a1	043427	043e95	0447dd	044ff5	0456d0
⊞ 🔷 у	0061b2	000000	010000	00f100	00e15b	00d110	00c020	00ae8a	009c4e	00896c	0075e3
. 🕁 z	072f0e	000000	080000	07e780	07cf55	07b77f	079ffc	0788ca	0771e7	075b52	07450a
	fe474e	000000	fcffff	fd2dff	fd5942	fd81ef	fda82c	fdcc1c	fdeddf	fe0d95	fe2b5b
	0616fc	000000	060000	060280	060503	06078b	060a16	060ca5	060f37	0611cb	061462
♦ hcg_valid	St1		<u> </u>								<u>л </u>

Figure 11. x, y, z, w, v time-series diagram for modelsim simulation.

Testing Item	<i>p</i> -Value(x)	Result
Approximate Entropy	0.352142	pass
Block Frequency	0.199847	pass
Cumulative Sum	0.421255	pass
FFT	0.751245	pass
Frequency	0.604212	pass
Linear Complexity	0.320412	pass
Longest Run	0.201485	pass
Non-Overlapping template	0.581245	pass
Overlapping template	0.782121	pass
Random Excursion	0.604712	pass

Random E	xcursions Variant		0.580073		pass	3	
	0.300047	pass					
	Runs		0.067581		pass		
	Serial1		0.200412		pass		
	Serial2		0.102476		pass	3	
U	niversal		0.294578		pase	3	
			_	SHC			
	HCG			+]		
	•				err_valid	- err_valid	
L	clk	v[23:0]	chaos_v[23:0]		error_v[23:0]	- error_v[23:0]	
tx_key[119:0]	key_in[119:0]	w[23:0]	chaos_w[23:0]		error_w[23:0]	- error_w[23:0]	
rst_n	rst_n	x[23:0]	chaos_x[23:0]		error_x[23:0]	- error_x[23:0]	
tx_valid	start	y[23:0]	chaos_y[23:0]		error_y[23:0]	error_y[23:0]	
_		z[23:0]	chaos_z[23:0]		error_z[23:0]	error_z[23:0]	
	hyper_chaos_	generate	clk	L _	shcg_valid	syn valid	
			rst_n		v[23:0]	syn v[23:0]	
rx valid			start		w[23:0]	- svn w[23:0]	
rx kev[119:0]			syn_key_in[119:0]	L _	x[23:0]	syn_x[23:0]	
				_	y[23:0]	syn_y[23:0]	
					z[23:0]	Syn 7[23:0]	
			s	n_hyper_cha	Jos		

Figure 12. Chaotic synchronization RTL view.

By observing Figure 12, it can be seen that Figure 12 corresponds to the top-level design in Section 3. Table 7 shows the resource consumption and the result of the FPGA-based synchronization design of the hyperchaotic system is shown in Figure 13, Figure 14 provides a partial view of the simulation results. It can be determined that the output time of the first synchronization sequence is 0.00066 ms under the 50 MHz clock condition, and when 0.00096 ms, error_x [23:0], error_y [23:0], error_z [23:0], error_w [23:0], and error_v [23:0] are all zero, achieving complete synchronization of two hyperchaotic systems with the same structure and different initial values, with a very minimal establishment time, and thus demonstrating the superior performance of hardware implementation of hyper-chaotic synchronization.

Table 7.	Table o	f resource	consumption.
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Resource	Utilization	Available	Utilization%
LUT	2477	41,000	6.04
LUTRAM	26	13,400	0.19
FF	1963	82,000	2.39
DSP	40	240	16.67

🔷 clk	0			ممر				บาป	
🔷 rst_n	1								
🗄 🔷 tx_key	0800001000000c000	080000100000c0000	040000080000						
🗄 🔷 rx_key	0c000008000004000	0c0000080000040000	100000100000						
🗄 🌧 chaos_x	15b66d	000000	080000	096c00	0add37	0c5452	0dd1f8	0f56b	d 10e3
🗄 🌧 chaos_y	0f4838	000000	100000	101c00	10313f	103e42	10411a	10375	1 101c
🗄 🌧 chaos_z	0f60ed	000000	0c0000	0c3c00	0c7e91	0cc872	0d1aa3	0d765	c Oddo
🗄 🌧 chaos_w	071b26	000000	040000	040c00	042ab8	045c4c	04a0f0	04f8d	c 0564
🗄 🌧 chaos_v	08c7ef	000000	080000	081000	08217c	08347a	084902	085f1	c 0876
💠 hcg_valid	0								
🗄 🔷 syn_x	15b66d	000000	0c0000	096a00	0add38	0c5452	0dd1f8	Of56b	d 10e3
	0f4838	000000	080000	104c00	10301f	103e48	104119	10375	1 1010
± 🔷 syn_z	0f60ed	000000	040000	0c5400	0c7e49	0cc873	0d1aa3	0d765	c Oddo
	071b26	000000	100000	035800	043544	045bae	04a0f9	04f8d	c 0564
± 🔷 syn_v	08c7ef	000000	100000	080800	082184	08347a	084902	085f1	c 0876
💠 shcg_valid	0								
	000000	000000	040000	fffe00	000001	000000			
• + error_y	000000	000000	f80000	003000	fffee0	000006	Internet		000000
± 🔷 error_z	000000	000000	f80000	001800	ffffb8	000001	000000		
🗉 🔶 error_w	000000	000000	0c0000	ff4c00	000a8c	ffff62	000009		000000
± 🔷 error v	000000	000000	080000	fff800	000008	000000			
				-98-		W			
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🔒 🎤 😄 Cursor	4 0.00096 ms	5						0.000	96 ms

Figure 13. RTL view of chaotic synchronization.

🗉 🔷 erro	r_x	000000	000000	040000	fffe00	000001	000000		
🗉 🔷 erro	r_y	000000	000000	f80000	003000	fffee0	000006	ffffff	000000
🗉 🔷 erro	r_z	000000	000000	f80000	001800	ffffb8	000001	000000	
🗉 🔷 erro	r_w	000000	000000	0c0000	ff4c00	000a8c	ffff62	000009	000000
🖽 🔷 erro	r_v	000000	000000	080000	fff800	000008	000000		
	Now Cursor 1 Cursor 2 Cursor 3	0.02032 ms 0.00066 ms 0.00084 ms 0.0009 ms)006 ms	0.00066 ms	i a a	0.0008 ms	084 ms	009 ms	0.001 m
<mark>⊕</mark> /*≎	Cursor 4	0.00096 ms						0.00	096 ms

Figure 14. Partial view of chaotic synchronization results simulated with modelsim.

To show the design results more clearly, in this paper, the modelsim simulation data of the chaotic synchronous system are exported to generate .dat files and input into MATLAB R2018 to generate the final error result graph as shown in Figure 15.

Figure 15. Error result of MATLAB simulation. (**a**) Diagram of errorx simulation result, (**b**) diagram of errory simulation result, (**c**) diagram of errorz simulation result, (**d**) diagram of errorw simulation result, (**e**) diagram of errory simulation result.

It can be concluded form Figure 15 that the error of each output sequence soon reaches 0, indicating that the above design is correct. Compared with the software implementation of chaos synchronization, the hardware implementation has high stability and does not show significant fluctuations in the error convergence process. Due to the high-speed performance of the hardware itself, the FPGA-based chaotic synchronization time is much shorter than the software-based chaotic synchronization time. Compared with the content of the same field, the overall convergence speed of the synchronous controller designed in this paper is rapid, indicating that at the same clock rate, the synchronous controller only needs a few iterations to achieve full synchronization, which demonstrates the excellent performance of the FPGA-based chaotic synchronous design.

5. Conclusions

In this paper, a new five-dimensional chaotic system suitable for synchronization was constructed and its phase diagrams observed by MATLAB simulation. The analysis of the Lyapunov exponent spectrum and bifurcation diagram shows that the chaotic system has hyperchaotic characteristics, and the maximum Lyapunov exponent is 1.9380 with a favorable permutation entropy index. A new five-dimensional hyperchaotic system based on FPGA was designed and implemented. Simulation results show that the FPGA-based hyperchaotic system designed in this paper can generate a chaotic sequence in three clock cycles. In addition, the synchronization of the hyperchaotic system was also investigated. A multivariate nonlinear feedback synchronization controller was proposed, and the synchronization control of the high-dimensional hyperchaotic system with higher order terms was designed and implemented based on FPGA. The simulation result shows that two hyperchaotic systems with the same structure and different initial values can be

synchronized quickly under the effect of the controller, which proves the validity of the designed controller.

Author Contributions: Y.W. (Yanan Wu) was responsible for conceiving and writing, hardware design, and implementation; X.L. (Xinyu Li) and X.L. (Xiaodong Li) were in charge of software; Y.G. provided guidance for the paper structure; Y.W. (Ya Wang), data curation. Project administration and supervision were carried out by Q.D. All authors have read and agreed to the published version of the manuscript.

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