# **The Sparse Abstract Machine**

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## **Abstract**

We propose the Sparse Abstract Machine (SAM), an intermediate representation and abstract machine model for targeting sparse tensor algebra to reconfigurable and fixed-function spatial dataflow accelerators. SAM defines a streaming abstraction with sparse primitives that encompass a large space of scheduled tensor algebra expressions. SAM dataflow graphs naturally separate tensor formats from algorithms and is expressive enough to incorporate many sparse-iteration and hardware-specific optimizations. We show an automatic compilation technique from a high-level language to SAM and a set of hardware primitives which implement it. We evaluate the generality and extensibility of our sparse abstract machine, explore the performance space of sparse tensor algebra optimizations using SAM, and provide an example implementation of our SAM architecture.

## 1. Introduction

Specialized hardware dataflow accelerators, leveraging parallelism, pipelining, and locality, are becoming increasingly popular as efficient alternatives to CPUs/G-PUs. This efficiency comes at the cost of programmability: all have some limits to their application domain, and most have limited and/or difficult programming interfaces. As a result, users often access these accelerators through library calls that are created by expert programmers [56, 57]. These point solutions, either from the hardware or software or both, are justified for a few extremely common operations, like dense matrix multiplication for deep neural networks, but many important applications depend on a class of operations instead of just one. This class of computation leaves a large gap between these accelerators and CPU or GPU solutions. Recent research has proposed closing this gap by creating reconfigurable dataflow architectures/coarse-grained reconfigurable arrays [43, 39, 13, 38, 8], including compilation tools to map a class of user applications to these arrays [62, 31, 36, 44].

Given these trends, it is not surprising that interest in general accelerators for sparse tensor algebra is increasing. It has applications across many fields, including science, engineering, data and graph analytics, and machine learning [15, 7, 32, 27, 1, 41]. Sparse tensor algebra, expressed with tensor index notation, is an important language with a long history, starting as a mathematical notation [46]. It has recently gained traction as a computational language [3] that subsumes linear algebra. We use the qualifier "sparse" to indicate that we mean a tensor algebra language where the tensors can be stored in either dense arrays or compressed data structures that omit zeros. To accelerate these computations, many papers have been published on point solutions for single-expression hardware, which is often sparse matrix multiplication [40, 45, 21, 63, 61, 52, 51].

Since these accelerators are fixed function, arbitrary sparse tensor contractions must be reduced to sparse matrix multiplications through algebraic factorization [21]. Factorization requires using transpositions, tensor-to-matrix and matrix-to-tensor conversions, and temporaries to break up large expressions. However, compared to dense tensor algebra, factorization is significantly more expensive for sparse tensor algebra.

More importantly, the lack of sparse expression fusion can, and often does, lead to higher asymptotic complexity: a sequence of matrix multiplications is usually orders of magnitude slower compared to fused implementations.

To address this issue, we define an abstract machine model called the Sparse Abstract Machine (or SAM). SAM consists of dataflow blocks that lend themselves to VLSI implementations and can be composed to:

- implement any sparse tensor algebra expression;
- implement many algorithms for each expression, including fused algorithms with pipelining, unfused algorithms with temporaries, tiled algorithms, and parallelized and vectorized algorithms; and
- implement algorithms that operate on both dense tensors stored in arrays and sparse tensors stored in compressed data structures.

Thus, SAM can be used to analyze point solutions, serve as the architecture of a programmable dataflow sparse tensor accelerator, and be the intermediate representation of its requisite compiler.

SAM is to dataflow accelerators as an ISA is to a conventional processor. It provides an interface between the hardware and compiler, allowing the end-to-end system to continue to function while both sides are optimized

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independently. The next two sections describe SAM, introducing the essential elements in Section 2 and then the extensions needed to express optimizations in Section 3. With that background, Section 4 shows how SAM can be used to describe related architectures in the literature, and Section 5 describes a scheme to compile any sparse tensor algebra expression to SAM dataflow graphs that are then mapped to a cycle-accurate simulator and a VLSI implementation in Section 6.

Our technical contributions are:

- an abstract machine model that represents the space of sparse tensor algebra as spatial streaming dataflows,
- 2. an analysis of existing optimized sparse tensor algebra dataflow accelerators using our abstract machine, and
- 3. a compilation strategy from a high-level tensor index notation to our abstract machine model and an example hardware implementation of the abstract machine.

## 2. The Core of the Sparse Abstract Machine

To serve as an ISA-like interface for sparse tensor algebra accelerators, SAM needs to not only have a clean method to define (Section 2.1) and transport (Section 2.2) arbitrary tensors but also express all tensor algebra operations. These operations are provided by seven types of dataflow blocks that can be composed to execute sparse tensor algebra expressions.

Level scanner blocks (Section 2.3) fetch a tensor's nonzero coordinates and send them as streams to intersection, union, and replication blocks that combine coordinates from different tensors (Section 2.5). Add, multiply, and reduction blocks (Section 2.6) compute tensor operations. And, finally, unnecessary result coordinates are filtered and level writer blocks write the resulting sparse tensor to memory (Section 2.7).

SAM lets programs use as many blocks as needed. Of course any physical implementation will be constrained to a finite set of resources. Our compiler can be used to transform an unconstrained graph to a specific physical backend by breaking up the computation in time through data movement into temporary memories and block reuse.

#### 2.1. Tensor Data Model

The abstract data model of the Sparse Abstract Machine views each tensor as a coordinate tree where each tree level represents the coordinates of a different tensor dimension (often called a mode). This coordinate tree abstraction was first introduced as part of the sparse iteration model [30] of the TACO system [29, 11] and further abstracted and formalized as fibertrees [53, 59]. Fibertrees are trie data structures where each coordinate at one level is linked to a fiber (or segment)—a list of child coordinates—at the next level. Crucially, only those children whose sub-trees have nonzeros are stored, which compresses out zeros. Figure 1a depicts a sparse matrix

and Figure 1b its corresponding fibertree. The matrix is stored in row-major order, so the i coordinates, shown as orange circles, are stored at the top fibertree level. Coordinate 2 of level i is not stored since its sub-tree (the third row) has only zeros. The middle level stores one j coordinate for every nonzero component and, finally, the last level stores the tensor's explicit values. Fibertrees are a useful abstraction that lets us reason about tensors level-by-level without regard of the exact representations in storage.

Tensor fibertrees can be stored in memory and transmitted via streams. When in memory, we store each tree level separately and assign to each level a storage type that specifies its data representation. A level's data representation (or format) can be as simple as an uncompressed level that stores a single number encoding the fiber size or it may be multiple compressed data structures that stores only those coordinates with nonempty sub-trees. Many other data representations are also possible with this abstraction [11, 53, 59]. Figure 1c depicts one of many possible in-memory data structures for the fibertree in Figure 1b, in which both levels are stored in compressed data structures. This specific storage format is often called doubly-compressed sparse row (DCSR) or compressed sparse fiber (CSF).

#### 2.2. Tensor Streams

Streams in the Sparse Abstract Machine are an abstraction of physical wires that transmit data between processing blocks and hence connect blocks to implement dataflow algorithms. Each SAM stream is a sequence of tokens that transmits one level of fibertree data, along with stop tokens  $(S_n)$  denoting the hierarchical fiber boundaries within a level, and a done token (D) to mark the end of a stream. There are three types of SAM streams: coordinate streams that transmit coordinate levels, value streams that transmit last-level tensor values, and reference streams that transmit references to the location of each coordinate's child fiber in memory. Figure 1d shows the fibertree in Figure 1b as two coordinate streams and one value stream. Streams can also be interpreted as variable-length nested lists where each stop token level represents a parenthesis. Thus, the value stream in Figure 1d,

$$D, S_1, 5, 4, S_0, 3, 2, S_0, 1$$

represents the nested value level

## 2.3. Tensor Iteration

SAM sparse dataflow algorithms start with level scanners that load tensors from memory and turn them into streams. In other words, they convert tensor fibertrees from space (see Figure 1c) to time (see Figure 1d).

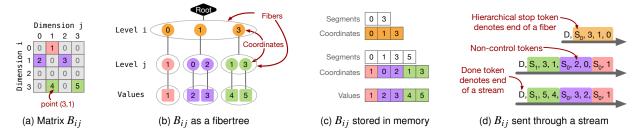


Figure 1: The data model of the SAM models sparse tensors (Figure 1a) as a coordinate fibertree, (Figure 1b) that can be stored in memory (Figure 1c), or sent through streams (Figure 1d) where time increases from right to left.

**Definition 2.1 (Level Scanner).** The level scanner takes in a reference stream and outputs two streams: one coordinate and one reference. It produces a single level of a tensor on its output coordinate stream, fiber by fiber. Each non-control token on the input stream is a reference to a single fiber location for a given level in memory. The level scanner uses it to generate all coordinates in that fiber, along with their corresponding references, and then adds an additional stop token to denote the end of that fiber.

SAM level scanners only generate fibers for one dimension. Therefore, multiple scanners compose to iterate over the memory representation of an entire multi-dimensional tensor. The composition uses the references emitted from each successive level scanner to locate the fibers of the next level scanner. The key to this composition is that level scanners communicate information by embedding both fiber location and coordinate hierarchy—needed by all downstream level scanners—into the reference streams. Each level scanner adds a level to the hierarchy by either adding an  $S_0$  stop token at the end of each scan or by incrementing all input stop tokens by one. Thus, they chain together to load an entire tensor and to convert it to per-level streams. Figure 2 shows two level scanners that together iterate over the compressed matrix in Figure 1c. The reference stream emitted by the final-level scanner is sent to blocks that load values from memory, as described in Section 2.6. Note that each level scanner usually also connects to a memory array (defined in Definition 2.5) which stores the fiber and coordinate information for the level. These arrays are not shown in the figure to reduce clutter.

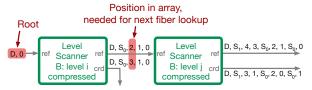


Figure 2: Composition of level scanner blocks.

We designed the SAM level scanners to support it-

erating over tensors stored in various in-memory level formats presented in [11], which purposely decouples an algorithm from the tensor formats. Thus, the interfaces of the level scanner are format agnostic. Figure 3 demonstrates how the level scanner interfaces remain unchanged as the level-format implementation varies.

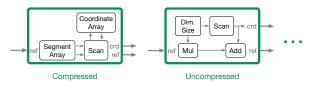


Figure 3: Specific implementations of level scanners demonstrating how the interface is format agnostic. Black blocks denote physical hardware and are not SAM blocks.

## 2.4. Illustrative Example

We will use the linear combination of rows algorithm (sometimes referred to as Gustavson's algorithm [17]) for sparse-matrix sparse-matrix multiplication (SpM\*SpM) to illustrate the operation of SAM blocks, and to demonstrate how their composition defines different algorithms. The Einstein summation notation for this algorithm is  $X_{ij} = \sum_k B_{ik} * C_{kj}$ , where the matrix multiplication is accomplished by using an index order of  $i \rightarrow k \rightarrow j$  [61].

Figure 4 shows the algorithm as a SAM dataflow graph. Starting at the left of the figure, the coordinates of the two tensors are first loaded from a DCSR data structure in memory by level scanners. The coordinates are then transformed into a three-dimensional iteration space by chaining together the  $i \rightarrow k$  coordinates of the B matrix with the  $k \rightarrow j$  coordinates of the C matrix. Generating this space sometimes requires duplicating data to fill in missing dimensions. In this example each matrix is broadcast over the other index variable of the other matrix (B over j and C over i). How this operation is handled and how these multiple streams are merged is described next.

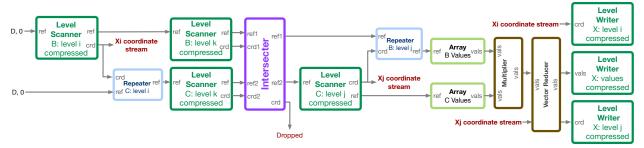


Figure 4: The SAM dataflow graph for sparse matrix multiplication  $X_{ij} = \sum_k B_{ik} C_{kj}$ , on doubly compressed sparse row (DCSR) matrices with linear combination of rows, ik j-order.

## 2.5. Stream Merging

Once the operand coordinate streams have been generated, the next task is to merge them. The index variables of a tensor index notation expression creates an iteration space that we must cover, optimally taking advantage of both the sparsity of the tensors and the mathematical properties of the operations to avoid unnecessary computation. Our design covers this sparse iteration space hierarchically by merging the coordinates of one dimension at a time, with the surviving coordinates from one dimension dictating what fibertree fibers need to be merged in the next dimension. The hierarchical merging is implemented with per-level merging blocks (intersection and union) and replication machinery to handle the case where a tensor is broadcast [25, 19] across the dimension of another tensor, as required in our example application in Section 2.4.

The key merging operation combines m streams, that represent the same coordinate level of all operand tensors, fiber by fiber. Coordinate merging is inherently a set operation: specifically, intersection (since a\*0=0) and union (since a+0=a) suffice for tensor algebra.

**Definition 2.2 (Joiner: Intersecter).** The intersecter has *m* pairs of coordinate and reference streams go in and one coordinate stream and *m* reference streams come out. This block outputs coordinates, and their corresponding input references, only when all input coordinates are equivalent.

**Definition 2.3 (Joiner: Unioner).** The unioner has the same input/output interface as the intersecter. This block outputs coordinates and their associated input references whenever there exists at least one coordinate from any input. If the coordinate exists only on p inputs where p < m, the union block outputs an empty (N) token on the the other m - p output reference streams.

Figure 5 shows an example of a binary unioner: it takes as input two coordinate streams and their corresponding reference streams. It produces a coordinate stream that is the union of the input streams, along with the the references from each input reference stream whose coordinates survived the union. Finally, both emitted reference streams are augmented with empty tokens to have the same shape as the emitted coordinate stream.

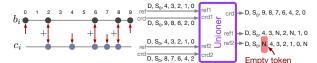


Figure 5: Example of union coiteration for  $b_i + c_i$ 

As we saw in Figure 4, it is common for expressions to replicate one tensor across a dimension of another, which is often called array broadcasting. Figure 6 shows a simple vector scaling example. It demonstrates how the repeater block replicates a provided reference stream over every coordinate of the provided coordinate stream.

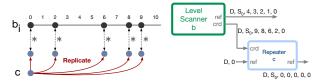


Figure 6: Repeating a scalar with a repeater block.

**Definition 2.4 (Repeater).** Repeaters have one input coordinate stream, one input reference stream, and one output reference stream. Each non-control token in the input reference stream is repeated m number of times, where m is the number of non-control tokens from the input coordinate stream before a stop token is seen.

Hierarchical repeating and stream merging compose to express algorithms for multi-dimensional tensor contractions. Lets reconsider the linear combination of rows SpM\*SpM algorithm from Figure 4. The i coordinates of B are first loaded. Their references are then not only used to load B's k coordinates, but also fed to a repeater that broadcasts all of C's k coordinates over each i. The advantage of this iteration order is that k coordinates are first intersected, and only if there is an intersection is the j level of C requested and sent to the computation units.

#### 2.6. Computation

After coordinate merging, the remaining coordinates are those points of the coordinate space that contribute to the result. Their corresponding reference streams are passed to array blocks that load their values.

**Definition 2.5 (Array).** An array block is a contiguous section of memory. It has two interface modes—load, which given one input reference stream fetches data to produce one output stream of any type, and store, which given one input reference stream and one input data stream of any type has a side effect that stores the data to its corresponding reference location in memory.

In SAM, Arrays are used to store values, coordinates, and references. In the computation pipeline, they store values, and the resulting value streams of each operand, all with the same coordinates, are combined using streaming arithmetic-logic units (ALUs). In Figure 4 this is the multiply unit.

**Definition 2.6 (ALU).** An ALU block consumes two value streams and produces one value stream. The block combines the two inputs by applying an arithmetic operator (add, subtract, or multiply) while treating empty tokens as zeros.

In addition to combining elements at the same coordinate, often the algorithm needs to accumulate a tensor. In our multiply example from Figure 4, this occurs at the end, where we remove the k dimension of the iteration space. This reduction is performed by summing over the tensor dimension (multiple dimensions can be summed over by chaining reduction blocks) being eliminated. Reductions in tensor algebra may occur over any tensor dimension, independent of the order in which we choose to merge coordinates. Thus, summation reductions may occur over the coordinate level that is merged last (requiring a scalar to accumulate the result), over the coordinate-level merged second to last (requiring a vector to accumulate the results), or over coordinates merged earlier (requiring a higher-dimensional tensor to accumulate the results). SAM provides one block for reductions that must be configured for any dimension of accumulation.

**Definition 2.7 (Reducer).** A reducer is configured by n, the dimension of the memory needed in the reduction. It inputs and outputs n coordinate streams and one value stream. The block is sent entire n-dimensional (sub) tensor with repeated points and values and outputs streams that represent that tensor with unique coordinates and summed values. Specific reducers include: scalar where n = 0, vector where n = 1, and matrix where n = 2.

The reducer internally adds together values for equivalent coordinate points and stores the results in an internal storage, which may be a dense or a sparse data structure. Finally, when an *n*-level reduction is completed, for example when a whole row has been processed for the Gustavson's algorithm in Figure 4, the reducer emits the resulting tensor as streams with deduplicated coordinates. Like with level scanners, various implementations of the reducer are possible underneath the abstraction, including k-way merging, dense arrays, compressed data structures, and bitmaps. Figure 7 shows an example of a row reducer.

$$x_{j} = \sum\nolimits_{i}^{\text{D, }} \underbrace{S_{\text{1}}, 3, 1, S_{\text{0}}, 2, 0, S_{\text{0}}, 1}_{\text{D, }} \underbrace{\text{crd j}}_{\text{val}} \underbrace{\sum\nolimits_{i}^{\text{D, }} \underbrace{S_{\text{0}}, 3, 2, 1, 0}_{\text{D}}}_{\text{val}} \underbrace{\sum\nolimits_{i}^{\text{D, }} \underbrace{S_{\text{0}}, 3, 2, 1, 0}_{\text{D}}}_{\text{D}} \underbrace{\sum\nolimits_{i}^{\text{D, }} \underbrace{S_{\text$$

Figure 7: Example using the row reducer, where n=1, to accumulate the columns of the matrix from Figure 1a.

#### 2.7. Tensor Construction

Following computation, the final step of a SAM algorithm is to store the resulting tensor streams back to memory. Specifically, the coordinate streams that were used to index the left-hand side of the tensor index notation (that survived), as well as the computed values, need to be stored back into per-level tensor memory representations.

**Definition 2.8 (Level writer).** Level writers take in either one value stream or one coordinate stream, and store its contents to memory, internally generating reference information and auxiliary level format data structures. As a result, the block is a wrapper around the store mode of the coordinate array block (and its metadata) or value array block in Definition 2.5. The level writer's internally generated references store the data tokens from the input stream in order.

In cases with at least two or more adjoining intersection levels, the result coordinate streams need to be cleaned before the level writer can store them back into memory. The coordinate cleanup needs to remove any outer-level result coordinates that have ineffectual inner-level intersections (either empty intersections or zero values) as shown in Figure 8. We introduce the coordinate dropper block to handle these cases.



Figure 8: Dropping outer coordinate 2 using the same example matrix from Figure 1a.

**Definition 2.9 (Coordinate Dropper).** The coordinate dropper takes in one outer-level coordinate stream and one inner-level coordinate or value stream. Given the outer-level coordinate stream and the nested inner-level

stream (coordinate or value) for the same tensor, the block will remove both the outer and inner tokens that came from ineffectual merging or computation (empty fibers or zeros) at the inner level.

## 3. Optimization Extensions

The core SAM blocks that we described in Section 2 are complete in the sense that they can be composed to express every tensor algebra expression. More subtly, they suffice to express all coordinate processing orders (or dataflow orderings), which is the primary tool to construct algorithms with better asymptotic complexity [2]. To allow SAM to express graphs that either further optimize performance, or deal with finite hardware, we need to add a few additional blocks. These blocks allow the graph to express parallelism, tiling, and new ways to represent tensor information either in-memory or as streams.

## 3.1. Tensor Locating

We can sometimes improve intersection efficiency over using an intersecter block, especially if one tensor has far fewer elements than the other. Rather than waiting for the larger tensor to stream all its level coordinates, it can be more efficient to ask the larger tensor if it contains any of the coordinates from the smaller tensor. This operation is possible with a new type of SAM block that uses a coordinate instead of a reference to index an array.

**Definition 3.1 (Locater).** A locater takes in one coordinate and reference stream with an associated array, and outputs one coordinate and two reference streams. For each coordinate, the block finds its associated reference within the array block, if it exists, and outputs that reference and the input coordinate and reference. Otherwise, it will drop an empty fiber on all streams.

With the locater block we can reorganize SAM graphs to avoid intersection units altogether. This optimization is also called iterate-and-locate or leader-follower. A prominent example that benefits from this optimization is the inner product sparse matrix-vector multiplication, where the vector is dense. By streaming through the coordinates of a row of the matrix and locating into the vector, we avoid loading the values of the vector whose corresponding matrix value is zero. Locate blocks can also be used to scatter into a result that supports random insert, such as a dense left-hand-side tensor. Thus, algorithms like the linear combination of rows matrix-vector multiplication can avoid a vector reducer.

Locate blocks can also speed up intersection when used in conjunction with intersecters that communicate information back to level scanners about coordinate ranges that are no longer needed. This optimization, called coordinate skipping or galloping, is common in software and has also been proposed in hardware [21]. In coordinate

skipping, the intersection block sends a signal back to the trailing stream producer block, informing it of the minimum coordinate that is needed next. The level scanner, in conjunction with a locater block, can then skip ahead to this coordinate and avoid sending useless coordinates between its current coordinate and the coordinate sent by the intersection unit.

## 3.2. Splitting and Flattening

The split block turns a tensor stream into two nested tensor streams and the flatten block turns two nested tensor streams into a combined stream, analogous to stripmining and flattening imperative loops. Split and flatten have several uses. By using two split blocks on two coordinate input streams, the resulting streams can be hierarchically intersected, which may be more efficient. Combined with SAM graph restructuring, a split block can tile a tensor stream, which improves temporal locality. By splitting with respect to the number of nonzeros in a stream, the stream will be more load balanced [48]. And by combining flattening with splitting on nonzeros, multi-dimensional tensor streams can also be load-balanced.

**Definition 3.2 (Splitter).** A splitter converts an input coordinate stream, denoted by stream $_{in}$ , into two coordinate streams representing nested levels. There are two splitter modes, coordinate and position, that each take a split factor s. In coordinate mode, for each coordinate c in stream $_{in}$ , the block outputs an outer-level coordinate  $c_{outer} = \lfloor c/s \rfloor$  and an inner-level coordinate  $c_{inner} = c \mod s$ . In position mode, assume that  $c_w$  is the w-th coordinate on the input stream. The position mode split emits  $c_{outer} = \{c_0, c_s, \dots, c_{(m-1)*s}\}$  where  $m = \lceil \operatorname{len}(\operatorname{stream}_{in})/s \rceil$  and  $c_{inner} = c_w - c_{outer}|_{w/s} \rceil$ .

**Definition 3.3 (Flattener).** The flattener block combines two input coordinate streams into one single-level output coordinate stream, and like the Splitter, has coordinate and position modes. The output coordinate c is computed by the formula  $c = s * c_{outer} + c_{inner}$  for coordinate mode and  $c = c_{outer} + c_{inner}$  for position mode, for split factor s.

## 3.3. Parallelization

The last extension to SAM enables parallelism via vectorization and graph duplication. Conceptually the simplest extension is to vectorize reference and coordinate streams as wire busses and to update the blocks to enable them to handle the increased data rates. Furthermore, using bitvectors to compress coordinate information before vectorization can increase efficiency. In some hardware, bitvectors may be the only coordinate protocol that is used, as in Capstan [47] and SIGMA [45], or it may be offered in addition to compressed coordinates, with blocks that convert between the stream protocols.

**Definition 3.4 (Bitvector Converter).** Bitvector converters transform b coordinates from the input coordinate stream into a single bitvector token of width b-bits on the bitvector stream output. Each bit indicates whether it has children or whether its sub-tree is empty

To enable coarse-grained parallelism, SAM dataflow graphs can fork streams with a parallelizer and join streams with a serializer. The parallelizer block takes in a sequential tensor stream and parcels out different elements to multiple output streams concurrently. The serializer block works inversely and joins parallel streams into a sequential stream by interleaving their coordinates.

**Definition 3.5** (Parallelizer). The parallelizer block takes in m tokens from one stream of any type and forwards one token to the head of each of the m streams on the output.

**Definition 3.6 (Serializer).** The serializer takes m tokens from m ordered input streams of any type and emits those tokens interleaved sequentially onto one stream of any type at the output.

#### 4. SAM Case Studies

By construction, we designed SAM to be able to represent many dataflow algorithms for every sparse tensor algebra expression, which includes varied data formats, dataflows, and optimizations. To demonstrate its expressive power, we identified and analyzed prior SpM\*SpM hardware accelerators and reconfigurable dataflow backends including Gamma [61], SIGMA [45], Extensor [21], Capstan [47], and OuterSPACE [40] and represented them as SAM dataflows. For example, Gamma's dataflow is similar to Figure 4. The main difference is that Gamma adds a parallelize block after the intersection unit, and then uses a multi-input vector reducer to rejoin the threads.

For space reasons, we will only describe OuterSPACE, which leverages an outer-product dataflow  $(k \to i \to j)$ . We chose OuterSPACE because it factorizes SpM\*SpM into two stages: a multiply phase  $(Y_{ikj} = B_{ik}C_{kj})$  and a merge phase  $(X_{ij} = Y_{ikj})$ , thus showing how SAM supports factorization. For efficiency,  $B_{ik}$  and  $C_{kj}$  are respectively stored in column-major and row-major order.

The first phase computes outer products between all columns of B and all rows of C and stores the partial result into a 3-dimensional tensor  $Y_{ikj}$ , as shown in Figure 9. To efficiently merge in the next phase, the intermediate result Y is stored in ikj-order, which is discordant with the dataflow kij. To efficiently support a discordant write of the tensor streams, OuterSPACE utilizes a linked-list representation as the level-format for k. Because our level writer is not restricted to a specific representation, SAM supports this dataflow.

The merge phase (not shown) then accumulates the partial product  $Y_{ikj}$  from the previous phase into a final result  $X_{ij}$ . This dataflow consists of three cascaded level scanners to generate the values  $Y_{ikj}$  that need to be summed, a vector reducer to sum the k dimension, and three level writers to store the  $X_{ij}$  results.

## 5. Compiler

We present the Compiler for Unified Sparse Tensor Algebra Reconfigurable Dataflows (Custard), our compiler to the SAM intermediate representation. Custard compiles tensor algebra expressions with associated in-memory data structure specifications [11] and schedules [48] to SAM dataflow graphs (see Figure 10). Custard builds on the TACO system [29] and goes through TACO's concrete index notation (CIN) [28] stage before the code generation path diverges. Although Custard generates dataflow graphs, the binding to specific hardware backends from prior work in Section 4 is left as future work.

Figure 10 illustrates a partial compilation to the SAM dataflow graph for the ik j-order sparse matrix-matrix multiplication example from Section 2.4. Custard converts the concrete index notation—tensor index notation with additional abstract loop and scheduling information—to a graph that represents each tensor's path through the index variables (shown as colored arrows with tensor labels in Figure 10). Custard then builds the following three sections in order: tensor iteration and merging, computation, and tensor construction assignment. It builds the tensor iteration and merging by visiting the Cartesian product of index variables and input tensors, which in our example is  $\{i,k,j\}$  by  $\{B,C\}$ . For every index variable in a tensor's path, Custard places and connects a level scanner, which is colored corresponding to its associated tensor paths in Figure 10. For every index variable absent from a tensor's path, Custard inserts a repeat block. Finally, if multiple tensor paths exist for an index variable, then Custard inserts an intersecter (for multiplication) or unioner (for

Next, the output reference streams from the first part are connected to the compute tree, which consists of point operations and reductions, (directly extracted from the CIN abstract syntax tree). Finally, the output values from the computation section and each index variable's final coordinate stream is connected to the output construction blocks (denoted by the orange in Figure 10) with coordinate drop blocks inserted if necessary.

## 6. Evaluation

SAM provides us an opportunity for an apples-to-apples comparison of spatial and temporal optimization techniques for sparse tensor algebra. Its versatility and flexibility lets us simulate various algorithms, giving us in-

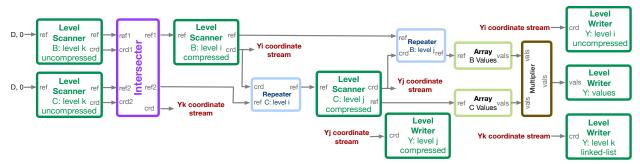


Figure 9: The SAM dataflow graph for SpM\*SpM that represents the OuterSPACE multiply phase, which is followed by the OuterSPACE merge phase. Compare this outer product graph to the linear combination graph in Figure 4.

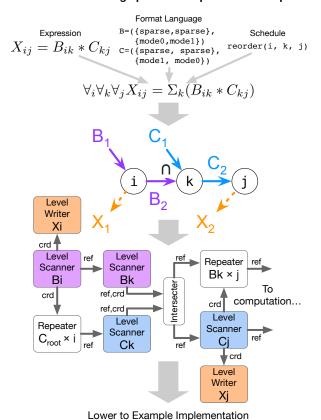


Figure 10: Custard's steps for compiling SAM tensor iteration, merging, and construction for Gustavson's (Section 2.4) SpM\*SpM example. From top down, Custard concretizes tensor index notation, creates the index-variable paths for each tensor, and constructs the partial SAM graph (where the color of each block corresponds to a tensor path—purple for B, blue for C, and orange for X).

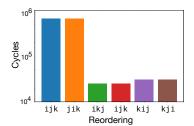
sight into their performance on accelerators. Since for this study we are interested in evaluating Custard as well as both the performance and area that is needed to implement our SAM hardware blocks, we use a cycle accurate simulator which models all pipelined computation and assumes that all data fits on chip, and provide area estimates of our SAM primitives.

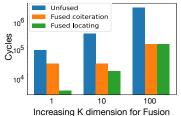
## **6.1. Effectiveness of Optimizations**

We first explore the performance attributed to: dataflow ordering, fusion, and tensor locating and acceleration via bitvectors, coordinate-skipping, or iteration-space splitting. While ordering and fusion fundamentally change the dataflow of the computation, the other optimizations presented are orthogonal and, being only concerned with a single tensor level, they can be used in conjunction with any dataflow.

**Reordering** Index variable reordering is an optimization that not only allows avoiding different data-dependent asymptotic behaviors [23, 60], but also allows for generality in the execution of a particular dataflow algorithm. We simulate all six ordering permutations of ijk for the SpM\*SpM expression using two distinct 95% sparse (5% nonzeros) uniformly random (urandom) matrices with different dimensions of sizes I = 250, K = 100, and J = 250. Figure 11 shows the inner-product algorithms, *i jk* and *jik*, perform the worst for matrix multiply. The linear combination of rows ik i and iki and outer product ki i and k ii algorithms perform a least an order of magnitude better. The performance is dictated by the order of k since coordinates are filtered out (intersected) at k earlier in the dataflow before repeating along the other dimensions iand j. These algorithms do, in fact, differ in their asymptotic complexity [30, 2], so the performance difference would increase as the sparsity increases. However, the inner product algorithm may be more efficient for low sparsity and uses asymptotically less memory for the reduction (a scalar instead of a row), so the choice is a tradeoff. For efficiency, therefore, sparse hardware must support many processing orders.

**Fusion** We demonstrate the algorithmic performance advantage of fusion using a common expression from machine learning, the ijk-ordered sampled dense-dense matrix multiplication (SDDMM)  $X_{ij} = \sum_k B_{ij}C_{ik}D_{jk}$  [16, 4]. We generate a 95% sparse (5% nonzeros) uniformly random matrix along with two dense matrices of dimension sizes I = 250, J = 250, and a sweep of  $K = \{1, 10, 100\}$ . Figure 12 shows that the unfused implementation performs far worse, since calculating and storing the en-





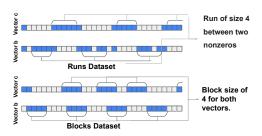


Figure 11: Simulated performance of differently ordered SpM\*SpM algorithms

Figure 12: Simulated performance of fused and unfused SD-DMM algorithms

Figure 13: Sample runs and blocks vectors

tire dense matrix multiplication is costly and mostly wasted work. Given the number of nonzeros in B as  $nnz_B$ , the unfused computation complexity is proportional to  $max(nnz_B*K,locate(nnz_B))$  while the cost of factorization becomes  $I*J*K+locate(nnz_B)$ . The only case where we would want to factorize this expression is when both the matrix B is almost dense and we have very efficient dense matrix multiplication hardware. But for a sufficiently sparse matrix, a fused expression will perform far better. Efficient sparse hardware must support fused expressions; a library of efficient binary operators will never be good enough.

Performance can be further enhanced by using locater blocks (Section 3.1) to find the sampled i, j values, which is trivial in a dense array. Interestingly, Figure 12 shows that this advantage becomes negligible as K increases: the cost of iterating through the dense inner-product dimension k starts to dominate the computation time, hiding the benefits of locating during intersection. But locating provides significant performance gains when the amount of computation is modest, which is often true in sparse computations.

Accelerator Structures We next explore different iteration acceleration techniques by comparing various configurations of coordinate-skipping (Section 3.1), bitvector iteration (Section 3.3), and iteration-splitting (Section 3.2). Figure 14 compares the performance when both vectors are in the following formats: one uncompressed level (Dense), one compressed coordinate level (Crd), one compressed coordinate level with coordinate-skipping (Crd w/ skip), two compressed coordinate levels (Crd w/ split), one pseudo-sparse bitvector level (BV), and two bitvector levels (BV w/split), which is also known as a bittree. For this set of experiments, we assume the coordinates were already split before this operation and use the vectorvector element-wise multiply expression  $x_i = b_i * c_i$  with both b and c as single dimensional vectors of size 2000. We use three types of synthetic vectors, namely *urandom*, runs, and blocks; runs and blocks are shown in Figure 13. Vectors with runs are pairs of vectors where one vec-

| Name        | Expression                                     | Name      | Expression                                 |
|-------------|--|-----------|--|
| SpMV        | $x_i = \sum_j B_{ij} c_j$                      | Residual  | $x_i = b_i - \sum_j C_{ij} d_j$            |
| SpM*SpM     | $X_i = \sum_j B_{ij} C_{jk}$                   | TTV       | $X_{ij} = \sum_{k} B_{ijk} c_k$            |
| MMAdd       | $X_{ij} = B_{ij} + C_{ij}$                     | TTM       | $X_{ijk} = \sum_{l} B_{ijl} C_{kl}$        |
| Plus3       | $X_{ij} = B_{ij} + C_{ij} + D_{ij}$            | MTTKRP    | $X_{ij} = \sum_{kl} B_{ikl} C_{jk} D_{jl}$ |
| SDDMM       | $X_{ij} = \sum_{k} B_{ij} C_{ik} D_{jk}$       | InnerProd | $\chi = \sum_{ijk} B_{ijk} C_{ijk}$        |
| MatTransMul | $x_i = \sum_j \alpha B_{ji}^T c_j + \beta d_i$ | Plus2     | $X_{ijk} = B_{ijk} + C_{ijk}$              |

Table 1: The expressions used to evaluate this work. All tensors are represented in CSF with the exception of C,D in SDDMM which are dense.

tor will have longer stretches of nonzeros between the nonzeros of the other vector. Similarly, *blocks* are vectors which have dense blocks of nonzeros placed throughout the vector. For both these vectors, the number of nonzeros is 400 (20%) with the index indicating the size of the runs/blocks in each vector.

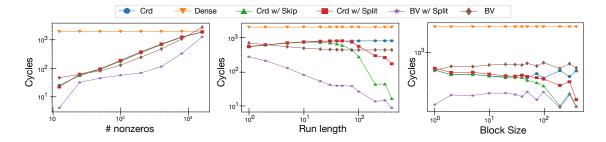
Figure 14a shows the performance as a function of sparsity for *urandom* data with b, s = 64 where applicable, and shows the limitations of a single level bitvector. As the sparsity increases, we see that the compressed coordinate format becomes better than bitvector, since bitvector is still a dense representation. The coordinate-skipping behaves exactly the same as the compressed coordinate format since *urandom* tensors on average have small run lengths (about 1.5 on average).

Figure 14b showcases the utility of coordinate skipping and splitting. As the run length increases, there are more opportunities to coordinate skip invalid input coordinates or avoid computation at the outer-level intersection. The bitvector remains relatively constant since the number of nonzeros remains about the same for various run lengths. This advantage of skipping and spliting remains in the *blocks* case, without the dependence on block size, since now intersections can be dense too. Overall these results show the advantage of the implicit parallelism that bitvectors provide, but show that for robust performance they need to be organized hierarchically.

#### 6.2. Simulated Hardware Performance

We demonstrate that Custard can automatically lower a breadth of expressions by providing the modeled perfor-

<sup>&</sup>lt;sup>1</sup>The splitting operation requires a full scan through the data structure, which for this example is as expensive as the operation itself.



- (a) Performance vs. sparsity of uniformly random synthetic vectors on a log-log scale
- (b) Performance vs. run length of synthetic vectors with runs on a log-log scale
- (c) Performance vs. block size of blocked synthetic vectors on a log-log scale

Figure 14: Simulated performance of various optimization techniques (compression, splitting, skipping, and bitvectors) for sparse vector sparse vector element-wise multiplication.

mance numbers for the SAM graphs in Table 1. The expressions are from real-world applications and prior work [47, 29] using only CSF representations (with the exception of SDDMM) [50]. We chose CSF since it allows for the largest compression of zeros. To approximate execution time, we use simulated cycle count assuming a 1GHz clock speed. The runtimes are shown in Figure 15 with some expressions omitted to conserve space. To provide some context on these numbers, we also show runtimes of CPU codes generated by the TACO compiler [29].<sup>2</sup> We show TACO because it is the only system that can compute our entire space of expressions and data formats.

We run each expression in Table 1 on a large subset of real and integer SuiteSparse [14] matrices, the Facebook [58] tensor, and FROSTT [49] tensors.<sup>3</sup> For the other tensor operands, we used the following tensor depending on the shape: the original tensor was either shifted by one (or two for three input operands) in its last mode as in [23, 60], the shifted tensor was transposed similar to in [51, 40], or a 0.1% nonzero *urandom* tensor

## 6.3. Example RTL Implementation

Custard automatically binds the generated SAM graphs to example implementations in RTL with an assumed data path width of 16-bits [8]. Our implementation of SAM supports the following specific level formats: uncompressed/dense, compressed/sparse, and singleton as defined in [11]. Of course, in any physical implementation, there are many other considerations that the SAM model abstracts away but that our compiler must handle. Blocks with N-ary inputs (like the intersection) are rewritten and physically bound to binary trees to avoid a large

| Block         | Area ( $\mu m^2$ ) | Block                | Area (µm²) |
|---------------|--------------------|----------------------|------------|
| Level scanner | 2550               | Merger + Crd Dropper | 4608       |
| Repeater      | 1518               | Array                | 9749       |
| ALU           | 1417               | Scalar Reducer       | 852        |
| Level writer  | 1788               |                      |            |

Table 2: The area of each elementary SAM block as synthesized in a 16 nm commercial technology.

number of distinct blocks. To further reduce the number of blocks required, Custard also maps matrix and vector reduction to existing blocks. A matrix reduction requires three arrays, three level scanners and level writers, two unioners, and an ALU to accumulate into a temporary tensor.

The input FIFO depth selection of most blocks is informed by the pipeline depth of each expression to avoid live-locking. Our example implementation also includes mechanisms for n-buffering [42] directly within the array blocks. The instances in our hardware implementation include: the intersecter/unioner/coordinate dropper, ALU, scalar reducer, level scanner, level writer and array. All these units can handle one token per cycle, though the level scanner has a startup latency (of 6 cycles) that is not in the SAM model. This additional delay can cause up to a  $6\times$  slowdown for tensor datasets with a single element in each fiber.

Table 2 shows the resulting area for each primitive using a 16 nm commercial technology. These implementations assume a FIFO depth of 8 and 4 KB of scratchpad memory per Array block. A FIFO depth of 8 ended up hitting a good trade-off between performance and area in RTL simulation. We find that the control logic in each block is rather small with most of the area dominated by FIFOs. We then determined from Section 6.2 that the maximum number of blocks of any given type used is 10. Thus, conservatively assuming our hardware contains 10 of each block in Table 2 along with 10 composed reducers, yields a modest total area of 2.32 mm<sup>2</sup>.

<sup>&</sup>lt;sup>2</sup>We use a 12 core dual-socket Intel Xeon E5-2680v3 CPU at 2.50 GHz with 30 MB L3 cache and 132 GB of memory. TACO uses GCC 7.5.0. We limit our evaluation to sequential performance as neither compiler supports parallel sparse loops, which we leave as future work.

<sup>&</sup>lt;sup>3</sup>For the CPU, we completed all datasets that fit in memory. However, due to limitations we only completed the following datasets SAM: all of SuiteSparse for SpM\*SpM and SpMV and about 130–550 for the other expressions and Facebook for the tensor expressions.

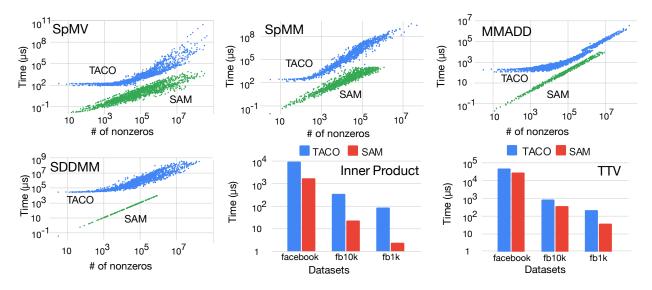


Figure 15: The performance of some expressions from Table 1 simulated in SAM along with the CPU performance compiled using TACO. For 3-tensor expressions fb10k and fb1k are 1k and 10k sub-tensors of the Facebook [58] tensor.

## 7. Related Work

The Sparse Abstract Machine is an abstract machine model for sparse tensor algebra execution that is designed both to express efficient implementations of many sparse dataflow algorithms and to be a good compilation target from high-level sparse tensor algebra languages. We discuss related work on sparse tensor algebra accelerators, on other programming models for sparse accelerators, and on other compilers for sparse tensor algebra.

#### 7.1. Streaming Dataflow Abstractions and IRs

There has been a long history of stream and dataflow processing. SAM blocks and streams are similar to Kahn processing networks (KPNs) [26], but our model (or implementations) may test for the existence of inputs. Synchronous Dataflow (SDF) is a restricted subset of KPNs with known input and output token rate [35, 34], while SAM provides support for sparse streaming computation. The StreamIt [54] language and Spidle [12] provide languages and compilers that capture streaming behaviour, however, SAM is designed for sparse irregular streams and Custard is exposes a high-level tensor algebra application language to the user and only compiles to a streaming abstraction. More recently, [39] proposed stream-dataflow acceleration as a pipelined, stream-based architectural abstraction. Although SAM's design follows some of the properties of stream-dataflow acceleration (like low control overhead and stream engines), there is no instruction control or dispatching since SAM directly compiles to graphs from a high-level language, unlike [39] which leverages a modified general-purpose compiler and ISA.

## 7.2. Sparse Dataflow Accelerators

Many dataflow accelerators have been proposed for accelerating sparse matrix multiplication kernels with a fixed dataflow [51, 61, 45, 63, 40]. Additionally, many sparse neural network accelerators have been proposed that compute some variant of sparse matrix-vector or matrix-matrix multiplication [22, 41, 18, 20, 10]. Tensaurus [52] and Extensor [21] support general tensor expressions, but they rely on factorization of a common computation pattern, which is expressible using SAM but not a limitation of the abstraction.

Capstan [47] and SPU [13] aim to leverage novel dataflow paradigms for efficient integration into general purpose, reconfigurable dataflow arrays. These are most comparable to SAM as they layer a dataflow graph with control codes over a reconfigurable array of primitives. As a result, both Capstan and SPU support different tensor algebra algorithms. SAM, however, is an abstract machine model general enough to describe these architectures, but can also describe additional algorithms. For instance, Capstan uses (dense) bitvectors to optimize for neural network workloads. The lack of general coordinate processing facilities prevents it from handling high degrees of sparsity. The SPU combines stream joins (akin to our intersections and unions) with a general von Neumann processor which breaks fused pipelines for larger expressions, while the SAM is a pure dataflow machine that supports arbitrarily deep fusion.

Specific hardware implementations of SAM primitives exist in several of the accelerators described above. However, these hardware blocks are hardened implementations of the Sparse Abstract Machine with fixed design decisions. For example, the ExTensor [21] intersection unit implements the specification defined by the SAM intersecter in Definition 2.2. Because SAM abstracts over concrete implementation choices made in prior work, we are able to bind to various hardware backends in a unified manner. We demonstrate one such binding in Section 4 and leave automatic binding from SAM to multiple hardware backends as future work. In this way, SAM functions as an ISA for sparse tensor algebra dataflow backends.

## 7.3. Sparse Tensor Algebra Compilers

Several compilers have been developed that compile to a subset of sparse linear algebra [5, 33] or the entirety of dense tensor algebra [24, 9, 55]. The TACO system [29] was the first to compile general sparse linear and tensor algebra expressions to CPUs, with abstraction over different data structures [11] and a scheduling language to generate different algorithms and target GPUs [28, 48]. Other systems for compiling sparse tensor algebra include COMET [37] and the MLIR SparseTensor dialect [6]. Unlike the Custard compiler, which emits a dataflow graph for accelerators, these compilers generate imperative loopbased code that runs on von Neumann machines. We also leave compilation of sparse array programs to dataflow architectures, as in the work of Henry and Hsu et al. [23] for CPUs, as future work.

## 8. Conclusion

We introduced the Sparse Abstract Machine, an abstract machine model for both reconfigurable and fixed-function spatial dataflow accelerators. Our Custard compiler demonstrates SAM's utility as a compiler target. The design of SAM lead to a small set of physical blocks that Custard can compile to. In addition, the flexibility and generality of SAM let us fairly evaluate optimization and dataflow alternatives for accelerating sparse tensor algebra algorithms. We hope that the Sparse Abstract Machine model will enable the microarchitectural design of future accelerators and inform the design decisions of architects. We also hope that compiler designs like Custard, targeting an abstract machine for portability, will improve the programmability and usability of this space.

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